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3025 Digital RF Signal Generator PXI Module



Operating Manual

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About this manual

This manual applies when the instrument is used with the supplied software.

It explains how to set up and configure an Aeroflex 3025 digital RF signal generator PXI module. Where necessary, it refers you to the appropriate installation documents that are supplied with the module.

This manual provides information about how to configure the module as a stand-alone device. However, one of the advantages of Aeroflex 3000 Series PXI modules is their ability to form versatile test instruments, when used with other such modules and running 3000 Series application software.

Getting Started with afSigGen (supplied on the CD-ROM that accompanies each module (see Associated documentation)) explains how to set up and configure a 3020 Series RF signal generator with a 3010 Series RF synthesizer module. Using the signal generator soft front panel and/or dll or COM object supplied, the modules form an instrument that provides the functionality and performance of an integrated, highly-specified signal generator, but with the adaptability to satisfy a diverse range of test or measurement requirements.

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Intended audience

Users who need accurately-generated signals in the VHF and UHF spectrum.

This manual is intended for first-time users, to provide familiarity with basic operation. Programming is not covered in this document but is documented fully in the help files that accompany the drivers and associated software on the CD-ROM.

Driver version

To maintain optimum performance, all 3000 Series PXI modules should be used either with the software driver version with which they were supplied (on the Aeroflex 3000 Series PXI Modules CD-ROM part no. 46886/028), or the latest driver, which you can download from the Aeroflex website.

Aeroflex endeavours to ensure modules remain backwards compatible with earlier driver version releases.

However, continual improvement means that from software version **6.2.0** onwards there are exceptions, which are explained below.

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Checking the software compatibility of a PXI module

- Modules that are compatible with all driver versions display on their front panel a serial number label consisting of black lettering on a **white** background.
- Modules that are only compatible with software driver installation version 6.2.0 and higher have a serial number label consisting of black lettering on a **yellow** background.

White background to label
use all driver s/w versions

Yellow background to label
use v. 6.2.0 s/w or higher

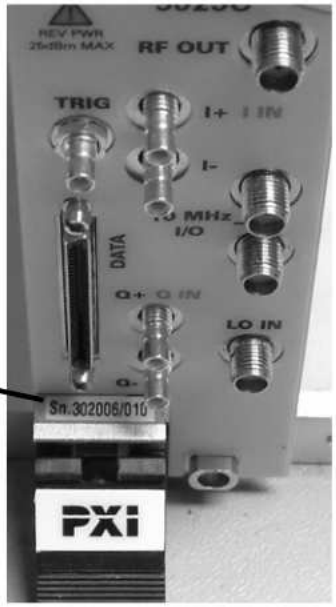


Fig. 1 Location of serial no. label (example)

Please ensure that you install the correct version of software for your module.

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Associated documentation

The following documentation covers specific aspects of this equipment:

PXI Modules CD-ROM	Part no. 46886/028	Compilation containing soft front panels, drivers, application software, data sheets, getting started and operating manuals for this and other modules in the 3000 Series.
3000 Series PXI Modules Common Installation Guide	Part no. 46882/663	Detailed information on installing modules into a rack, external connections, powering up and installing drivers.
3000 Series PXI Modules Installation Guide for Chassis	Part no. 46882/667	Explains how to set up a populated chassis ready for use.
PXI Studio User Guide	Part no: 46892/809	Setting up and using the universal PXI application for system configuration and operation.
Getting Started with afSigGen	Part no. 46892/678	Setting up and using the signal generator application for 3010 Series and 3020 Series modules.

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Preface

The PXI concept

VXI and GPIB systems meet the specific needs of instrumentation users but are often too large and expensive for mainstream applications. PC-based instrumentation may cost less but cannot meet the environmental and operational requirements of many systems.

PXI (PCI Extensions for Instrumentation) is based on CompactPCI, itself based on the PCI standard. PCI was designed for desktop machines but CompactPCI was designed for industrial applications, and features a rugged Eurocard format with easy insertion and removal. PXI adds to the CompactPCI specification by defining system-level specifications for timing, synchronization, cooling, environmental testing, and software. While PXI extends CompactPCI, it also maintains complete interoperability so that you can use any CompactPCI-compliant product in a PXI system and vice versa. PXI also makes use of Windows software, VXI timing and triggering, and VXIplug&play instrument drivers to provide powerful and affordable systems.

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PXI™ is a registered trademark of the PXI Systems Alliance
Windows™, Windows XP™ and Windows NT™ are trademarks of Microsoft Corporation

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Abbreviations/acronyms

ACP(R)	Adjacent Channel Power (Ratio)
ADC	Analog-to-Digital Converter
ALC	Automatic Level Control
AM	Amplitude Modulation
ARB	Arbitrary Waveform Generator
ATE	Automatic Test Equipment
CW	Continuous Wave
DAC	Digital-to-Analog Converter
dB	Decibels
dBc	Decibels relative to the carrier level
dBm	Decibels relative to 1 mW
EVM	Error Vector Magnitude
FM	Frequency Modulation
FPGA	Field Programmable Gate Array
GND	Ground
IQ	In-phase/Quadrature
ISP	In-System Programming
LO	Local Oscillator
LSTB	List Strobe
LVDS	Low-Voltage Differential Signaling
PCI	Peripheral Component Interconnect

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Pk-Pk	Peak-to-Peak
PXI	PCI eXtensions for Instrumentation
RF	Radio Frequency
RMS	Root Mean Square
SDRAM	Synchronous Dynamic RAM
SFP	Soft Front Panel
SMA	SubMiniature version A (connector)
SMB	SubMiniature version B (connector)
TDMA	Time Division Multiple Access
TRIG	Trigger
TTL	Transistor-Transistor Logic
UUT	Unit Under Test
VCO	Voltage-Controlled Oscillator
VHDCI	Very High Density Connector Interface
VSWR	Voltage Standing-Wave Ratio
VXI	VMEbus Extension for Instrumentation

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Chapter 1 GENERAL INFORMATION



Introduction

Welcome to the operating manual for the 3025 Digital RF Signal Generator.

The 3025 Digital RF Signal Generator operates over a frequency range of 100 MHz to 6 GHz and a level range of +5 dBm to −120 dBm (0 dBm to −120 dBm above 3 GHz). The RF output may be continuous wave (CW) or modulated. Modulation can be internal analog AM/FM, internal and external digital IQ, or external vector (when Option 01 is fitted).

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Internal digital IQ modulation is supported by a built-in dual-channel arbitrary waveform generator (ARB). This ARB is compatible with waveforms designed or packaged using the ***IQCreator*** ® software application. Differential baseband I and Q outputs from the ARB are available as an option. External digital IQ modulation is supported via an LVDS data interface. An external synthesizer provides a local oscillator input signal: the 3010 Series RF Synthesizer is recommended. The two modules together occupy only three slots in a 3U PXI chassis.

Applications

The 3025 is ideal for generating complex modulated waveforms for digital radio communications test and measurement applications, satellite and terrestrial TV broadcasting, military communications and WLAN. When the 3025 is used with other Aeroflex PXI RF modules, complete RF test systems can be implemented. High RF accuracy, stability and repeatability ensure consistent measurement results, helping to improve manufacturing yield.

Wide frequency coverage

The 3025's frequency range makes it ideal for multi-purpose applications in UHF radio communications, especially important when testing multi-mode cellular terminals.

Low noise and frequency-agile

When used with a 3010 Series synthesizer, the 3025 provides the low noise and high switching speed necessary for high-productivity RFIC testing or the stimulus to frequency-hopping radios.

RF level accuracy and bursting

The 3025 maintains accurate RF output levels to typically ±0.3 dB, and can generate modulated RF bursts to simulate TDMA signal characteristics.

IQ digital modulation

The 3025 provides high-quality digital modulation suitable for all common radio communications applications, either from the internal ARB or from an external source via the LVDS data connector.

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Analog I &Q inputs and outputs (optional)

The 3025 can provide baseband I and Q output and CW RF output simultaneously. Differential analog I and Q outputs from the ARB are provided, with control of differential output level, DC bias and offset voltage.

IQ vector modulation

Analog I and Q inputs can be used to generate wideband vector modulation from external analog I and Q sources such as test instruments and device outputs.

Arbitrary waveform generator (ARB)

The ARB can store 32 MSamples, either as a single long waveform or any number of smaller waveforms up to the capacity limit of the sample memory. Waveforms transfer quickly between the PXI controller and the ARB because of the wide bandwidth of the PCI backplane. Playback times of more than 30 minutes are possible, longer if ARB sequencing is used.

ARB sequencing

ARB sequencing provides a method for extending the effective ARB sample memory as well as providing a flexible way to compile test sequences. You can define up to 128 sequence steps, each of which defines an ARB file from a selection of 64, and plays it a chosen number of times before continuing on to the next file in the ARB sequence.

Triggering and synchronization

The 3025 provides flexible, configurable triggering facilities from inputs on the front panel or the PXI backplane. Triggers can be used for addressed selection or stepped incrementing of list mode. Triggers can generate power bursts and can be programmed into ARB waveforms to provide trigger outputs for other instruments.

A configurable routing matrix provides flexibility in how you interconnect signals on the PXI backplane, the LVDS and TTL front-panel inputs, and the module's internal functions. Predefined routing scenarios can be loaded, or new scenarios created to meet particular requirements.

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List mode

List mode enables very fast settling times for new signal configurations. In list mode, up to 128 internal hardware settings are pre-calculated and stored, providing fast switching of frequency and level whilst maintaining RF output accuracy. List addresses are sourced externally or from an internal counter driven by the test application controlling the 3025.

Software

The 3025 is supplied with a VXI PNP driver and soft front panel for use as a standalone module. It is also supplied with an instrument-level signal generator soft front panel, a dll and a COM object, for use with a 3010 Series RF synthesizer.

Refer to the guide *Getting Started with afSigGen* (part no. 46882/678), also available on the PXI Modules CD-ROM part no. 46886/028.

IQCreator ® allows you to design your own, or system-specific, complex modulation files for use with the 3025's ARB.

PXI Studio, also supplied with the module, configures your PXI modules as logical instruments using an intuitive and powerful graphical interface. Currently, PXI Studio provides comprehensive signal generator, digitizer and spectrum analyzer applications and further development will provide analysis plugins to suit any modulation scheme.

RF Investigator, also supplied with the module, is an application that provides combined operation of all Aeroflex 3000 Series modules from a single user interface, especially useful for acceptance testing.

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Deliverable items

- 3025 RF Signal Generator PXI module
- PXI Modules CD-ROM (part no. 46886/028), containing soft front panels, drivers, application software, data sheets, getting started and operating manuals for this and other modules in the 3000 Series
- *3000 Series PXI Modules Common Installation Guide*, part no. 46882/663
- *3000 Series PXI Modules Installation Guide for Chassis*, part no. 46882/667
- SMA connector cable, part no. 43139/590

Cleaning

Before commencing any cleaning, switch off the chassis and disconnect it from the supply. You can wipe the front panel of the module using a soft cloth moistened in water, taking care not to wet the connectors. Do not use aerosol or liquid solvent cleaners.

Putting into storage

If you put the module into storage, ensure that the following conditions are not exceeded:

Temperature range:	–20 to +70°C (–4 to +158°F)
Humidity:	5 to 93%, non-condensing

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Chapter 2 INSTALLATION

WARNING

Initial visual inspection

Refer to the 3000 Series Common Installation Guide 46882/663.

CAUTION

Handling precautions

Refer to the 3000 Series Common Installation Guide 46882/663.

Hardware installation

Installing the module into the PXI chassis

Refer to the 3000 Series Common Installation Guide 46882/663 and Installation Guide for Chassis 46882/667.

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Connector care and maintenance

How to connect and torque an SMA connector

1 First, ensure that the mating halves of the connector are correctly aligned.

2 Next, engage the threads of the nut and tighten it by hand, ensuring that the mating halves do not move relative to each other.

3 Then use a torque spanner to tighten the connector, in order to ensure consistent matching and to avoid mechanical stress.

Torque settings for connectors are:

0.56 Nm test torque (development use, semi-permanent installations)

1 Nm final torque (permanent installations)

Never use pliers to tighten connectors.

Maintenance

SMA

Clean connectors regularly, using a cotton bud dipped in isopropyl alcohol. Wipe within the connector cavity, then use a dry cotton bud to finish off. Check for any deposits.

Do not use other cleaners, as they can cause damage to the plastic insulators within the connectors.

Cap unused connectors.

PCI

Protect PCI connector pins by keeping modules in their original packing when not fitted in the rack.

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Chapter 3 OPERATION

Front-panel connectors

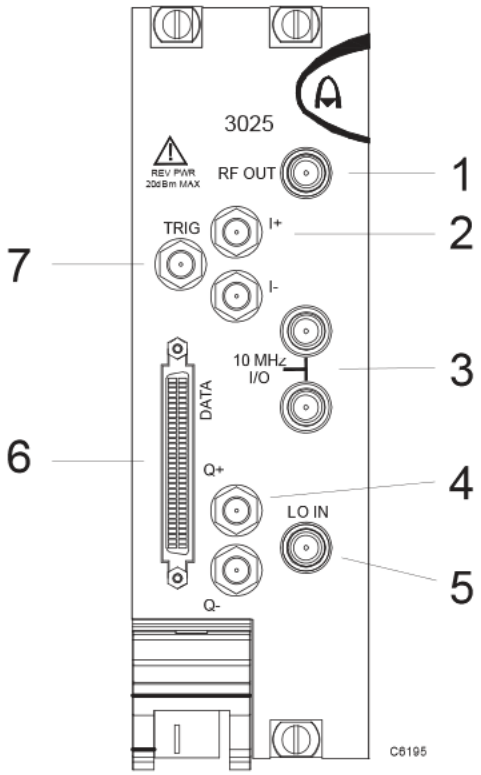


Fig. 3-1 3025 front panel

1	RF OUT	RF output, −120 to +5 dBm, 100 MHz to 6 GHz. SMA socket, 50 □.
2	I+ , I− Option 01 only	Analog I output (I+ and I−), 50□ single-ended, 100 □ differential. SMB sockets. Analog Q input, selectable 50□/100 k□.
3	10 MHz I/O	Two SMA I/O sockets in parallel. **Input** External frequency standard input for sampling clock. 0.4 to 4 V pk-pk into 50 □. **Output** Link-through from input.
4	Q+ , Q− Option 01 only.	Analog Q output (Q+ and Q−), 50□ single-ended, 100 □ differential. SMB sockets, 50 □. Analog I input, selectable 50□/100 k□.
5	LO IN	1.5 to 3 GHz, nominally 0 dBm. SMA socket, 50 □.
6	DATA	68-way VHDCI connector for LVDS data I/O, 14-bit IQ digital data input. See Appendix B for details.
7	TRIG	TTL +ve or –ve edge. SMB socket, 50 □.

CAUTION

Maximum safe power

Reverse power handling: not to exceed **+20 dBm**

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Soft front panel (af3020_sfp)

The soft front panel provides a graphical interface for operating the module. It is intended for testing and diagnosing, for demonstration and training, and for basic operation of the module. It represents most of the functions available in the instrument driver. It is not however a comprehensive application suitable for measurements; for this, use the afSigGen DLL, the afcomSigGen COM object, or PXI Studio.

Installation

The soft front panel is installed during the driver installation process (refer to the 3000 Series PXI Modules Common Installation Guide, part no. 46882/663).

Open the *AF3020_sfp.exe* file: this is in the *C:\VXIPNP\WinNT\af3020* directory on a Windows NT machine, for example. It is also accessible from the Windows Start menu under *Programs\Aeroflex\PXI Module Front Panels\AF3020 Front Panel*. The soft front panel, similar to that in Fig. 3-2, is displayed.

Detailed help information

Soft front panel controls are all available as driver export functions unless noted otherwise, and are documented in the help files. This operating manual provides an overview of the facilities that the module provides and summarizes its operation; however, refer to the help files for detailed descriptions of functions, together with their parameter lists and return values.

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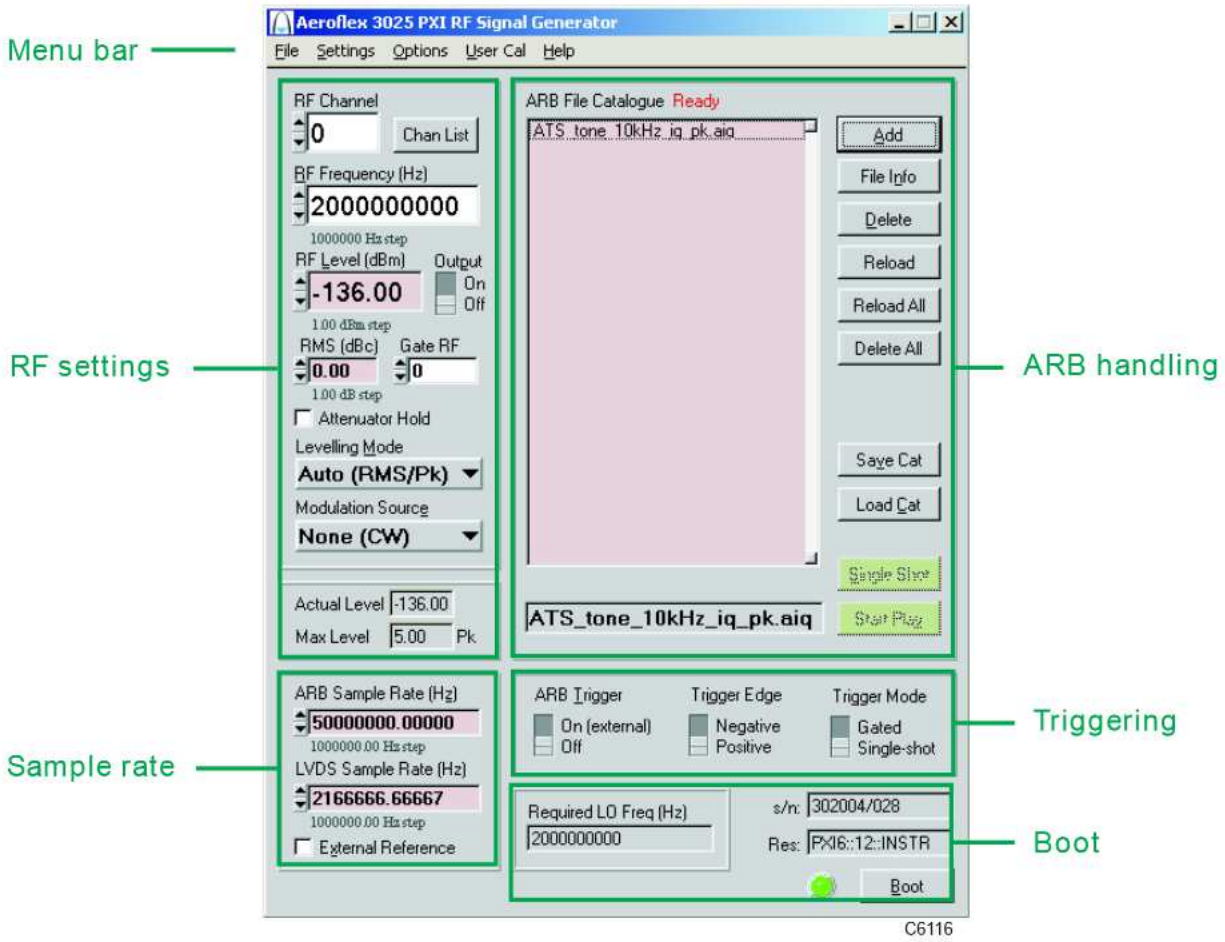


Fig. 3-2 3025 soft front panel

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Soft front panel controls

Menu bar

File

Click **Exit** to close the application.

Settings

Load and **Save** allow you to load and save soft front panel configurations from and to your preferred locations. If you did not change the default location when installing the software, it is *C:\VXIPNP\WinNT\af3020\settings*, and configurations are saved as *.ini* files.

> You can edit, copy and paste settings files as required; for example, you may want to save only a new routing setup without changing other parameters. Edit the saved *.ini* file using a text editor (for example, Notepad) to remove unwanted parameters. Ensure only that you do not delete the General (VendorID, DeviceID) and Version (Major/Minor) parameters. Save the changed file. When the settings file is next loaded, the configuration of the soft front panel changes to match the parameters remaining in the settings file, leaving all other settings unchanged.

Directories lets you choose the locations for your front-panel configuration settings, ARB files and catalogs, synthesizer plugin DLLs and calibration files.

Synthesizer plugins must support a VXIPNP (VISA) RF synthesizer resource capable of 1.5 GHz to 3 GHz. Certain exported functions are also required: refer to online help for details.

LVDS: select the Data Size (14-bit or padded to 16-bit) and Sign (unsigned/signed) to match different data types.

IQ Bandwidth Correction…: not used on this module.

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Routing Scenarios allows you to select a predefined routing matrix connection. A tick against the scenario's title shows that it is selected.

If you select a scenario, and then a second, any connected or enabled outputs common to both scenarios are overwritten by the second. Enabled outputs in the first scenario that do not appear in the second also remain active. If the second scenario changes any outputs that were used by the first, the first scenario is invalidated. This process extends to further scenarios.

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Routing Matrix displays a matrix that provides interconnection between input and output signals on the PXI backplane bus, the DATA connector, the TRIG connector and the module's internal circuitry, as shown diagrammatically in Fig. 3-3. This provides great flexibility in how you route signals between modules.

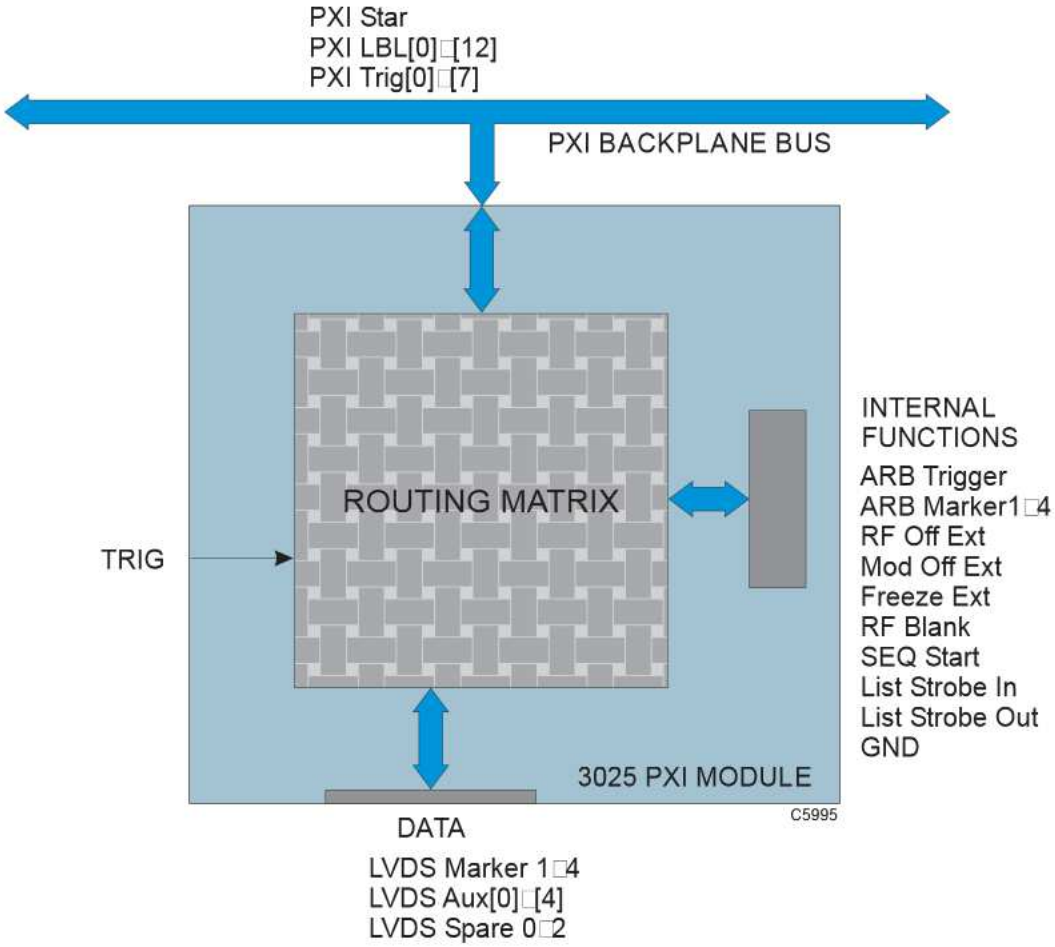


Fig. 3-3 Routing matrix in 3025

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Use the routing matrix (Fig. 3-4) to interconnect signals. Output signals form the body of the matrix. Select appropriate input signals from the drop-down menus under each down-arrow to create the interconnections.

Check the boxes to enable the outputs. **Reset** sets all input signals to GND, which is the default state.

When operating the module in default signal generator mode (routing matrix reset), all necessary input, output and trigger signals are available on front-panel DATA, SMA or SMB connectors and there is no need to configure the matrix. If you need to set up particular signal routings, you can define these using the drop-down menus on the matrix and save them using the **Load** and **Save** commands in **Settings**, or use **Routing Scenarios** to access pre-set alternative routings, or contact Aeroflex if you need assistance in defining particular routing requirements.

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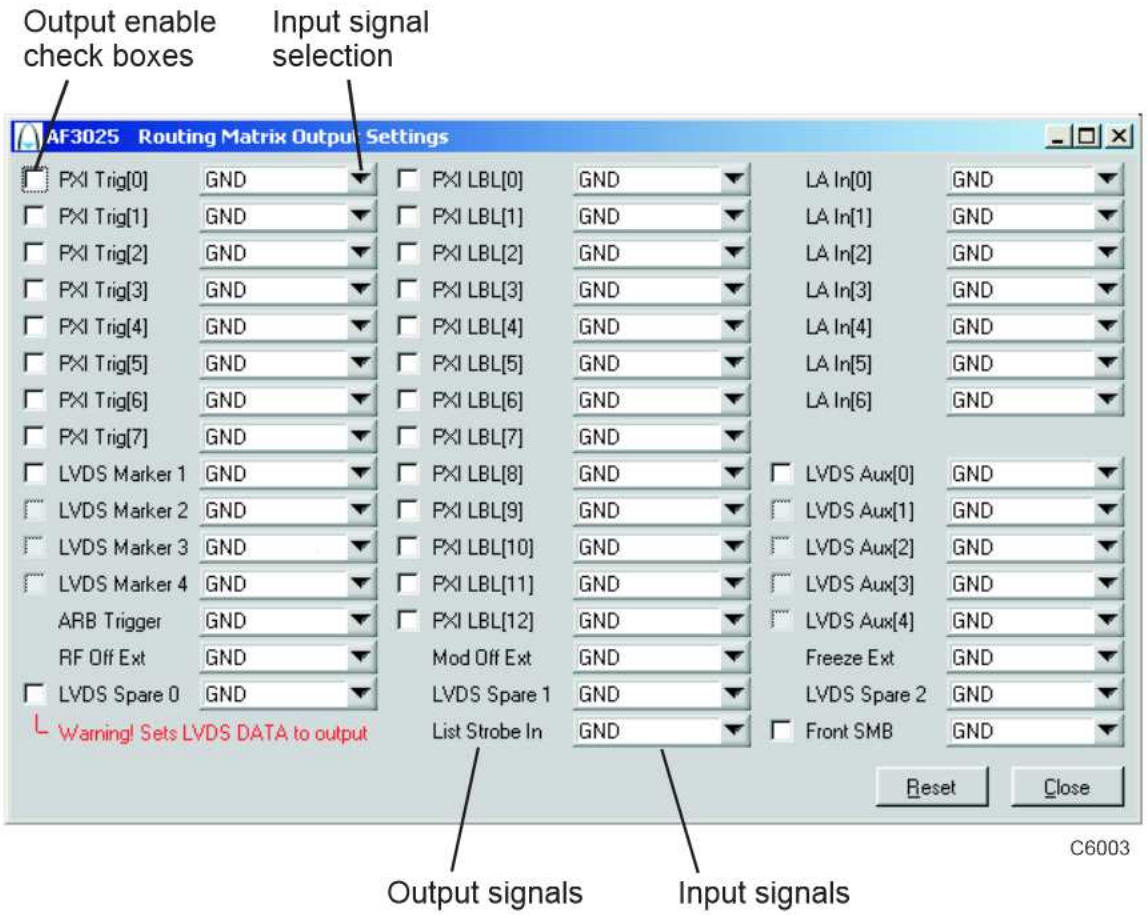


Fig. 3-4 Routing matrix inputs and outputs

Differential IQ

This menu item appears only when Option 01 'Analog I & Q Inputs and I & Q Outputs' is fitted.

See **Available Options**.

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Analog Modulation displays the screen for setting up internal AM and FM modulation (Fig. 3-5). Analog modulation is enabled when **Modulation Source** is set to Internal AM or Internal FM.

The modulation source for internal AM/FM analog modulation is a sinusoid with user-settable frequency (modulation rate).

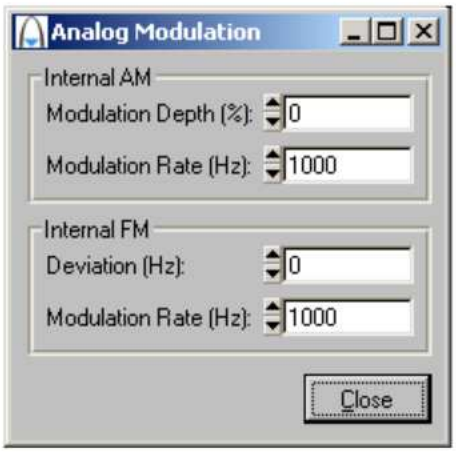


Fig. 3-5 Analog modulation setup screen

Analog Modulation

Modulation Depth (%) sets AM modulation depth, in %.

Modulation Rate (Hz) sets AM modulation rate, in Hz.

Deviation (Hz) sets FM deviation, in Hz.

Modulation Rate (Hz) sets FM modulation rate, in Hz.

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Options

Allows you to enable or disable additional instrument options if you have the appropriate password (available from the Aeroflex sales desk). Click **Edit** to display the options screen (Fig. 3-6).

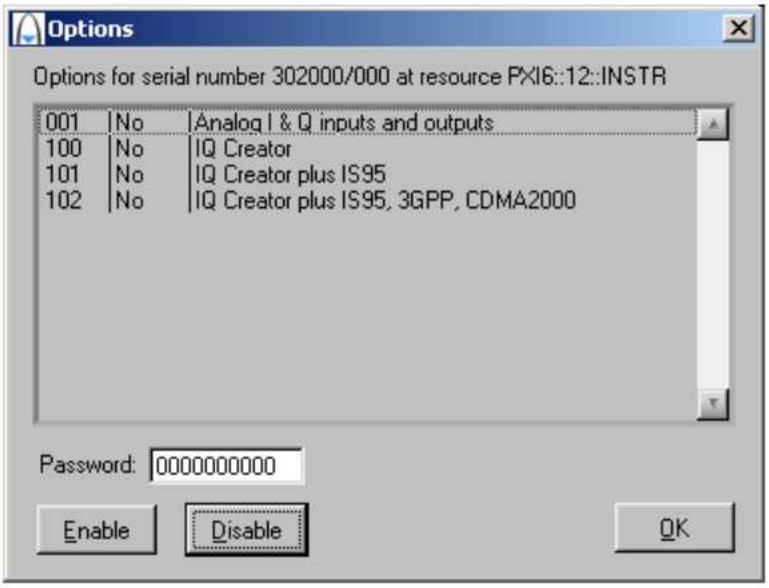


Fig. 3-6 Options screen

Disabled options are shown grayed out. To enable an option, enter the appropriate password. Click **Enable**. The enabled option is shown highlighted in green. Click **OK**.

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User Cal

Calibration is needed to ensure that some specifications — such as carrier leak — are met, and are guaranteed only if a user calibration has been performed. The module calibrates at the current frequency, or at a range of frequencies, and stores the results so that if you change frequency and return again, the calibration still applies.

In some cases, an LO signal is required; the user calibration screen prompts for the LO Plugin Filename. You can browse for this and boot the selected device from the User Calibration screen.

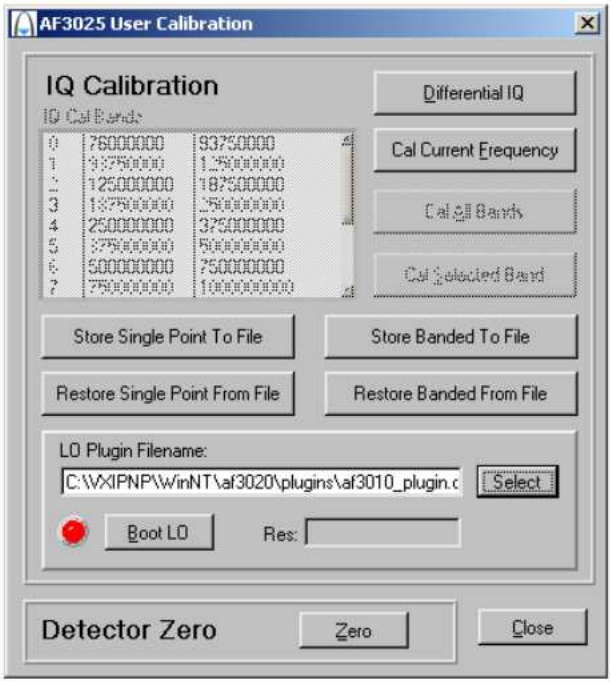


Fig. 3-7 User calibration screen

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IQ Calibration

Differential IQ: there are two differential IQ calibrations:

Cal Outputs is used to null out any DC offset on the differential outputs.

Cal Inputs is used to null out DC offsets on the analog IQ input path. If you apply no signal, this cal nulls DC offsets internal to the module's analog IQ input path. If you apply a nominal 0 V signal level, this cal nulls both the user and the internal module DC offsets.

See also **Differential IQ**.

Cal Current Frequency calibrates the IQ modulator at the current frequency. Calibration is valid for frequencies within ±1 MHz of the current frequency. The plugin is not used, but the LO signal must be present at the correct frequency.

Cal All Bands calibrates the IQ modulator over the entire frequency range of the module and returns the instrument to its current state. The plugin is required.

Cal Selected Band calibrates the IQ modulator over individual bands and returns the instrument to its current state. The plugin is required.

Store Single Point/Banded to File lets you save calibrations using the standard Windows browser. Calibrations are saved as *.ciq* files.

Restore Single Point/Banded from File lets you restore *.ciq* calibrations using the standard Windows browser.

Detector Zero

Zero sets the leveling detector to zero. This ensures that the module meets the level accuracy specified in the data sheet. No LO plugin or LO signal is needed.

Help

Instrument Information provides the module's PXI resource code and serial number, revision numbers for driver, FPGA and PCI, and its last calibration date.

About provides the version and date of the soft front panel.

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Boot

Click **Boot** to initialize the module and view the Boot Resource window. Resources available for initializing are shown in blue.

Select the 3025 you want to boot.

Boot default FPGA configuration box.
Check this. Do not change the configuration unless you are advised otherwise.

EEPROM caching box.
Check this, so that when you boot a particular module for the first time, calibration data is read from the module and placed in the local cache that you define in the EEPROM Cache Path. This initial boot time is of the order of 45 seconds. Then check the EEPROM caching box at subsequent power-ups of this module to provide considerably faster boot times. The EEPROM caching box is cleared at each power-down.

Click **OK**. While you select the boot resource, the indicator is amber. Once the module has initialized, the indicator changes to green in a few seconds.

If no calibration data is available, the driver returns a caution. If this happens, return the module for calibration.

s/n:

After the module initializes, this field displays its serial number.

Res:

After the module initializes, this field displays its VISA resource string.

Required LO Freq (Hz)

Shows the frequency that needs to be set on the 3010 Series synthesizer to give the chosen RF frequency at the 3025's output. Double-click in this field, copy the value, and paste into the RF Frequency (Hz) field on the 3010 Series module's soft front panel.

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RF settings

The controls available in this group allow you to configure up to 128 channels for frequency, level, leveling mode, and other parameters. These parameters are stored, and are recalled as each channel is selected. This selection can be manual (by clicking the up/down arrows of the RF Channel field) or by list mode operation.

RF Channel

Sets the currently active channel in a range of 0 to 127.

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Chan List

Click this to set up each of up to 128 channels. You can edit, copy and paste the settings to make setup quick and easy.

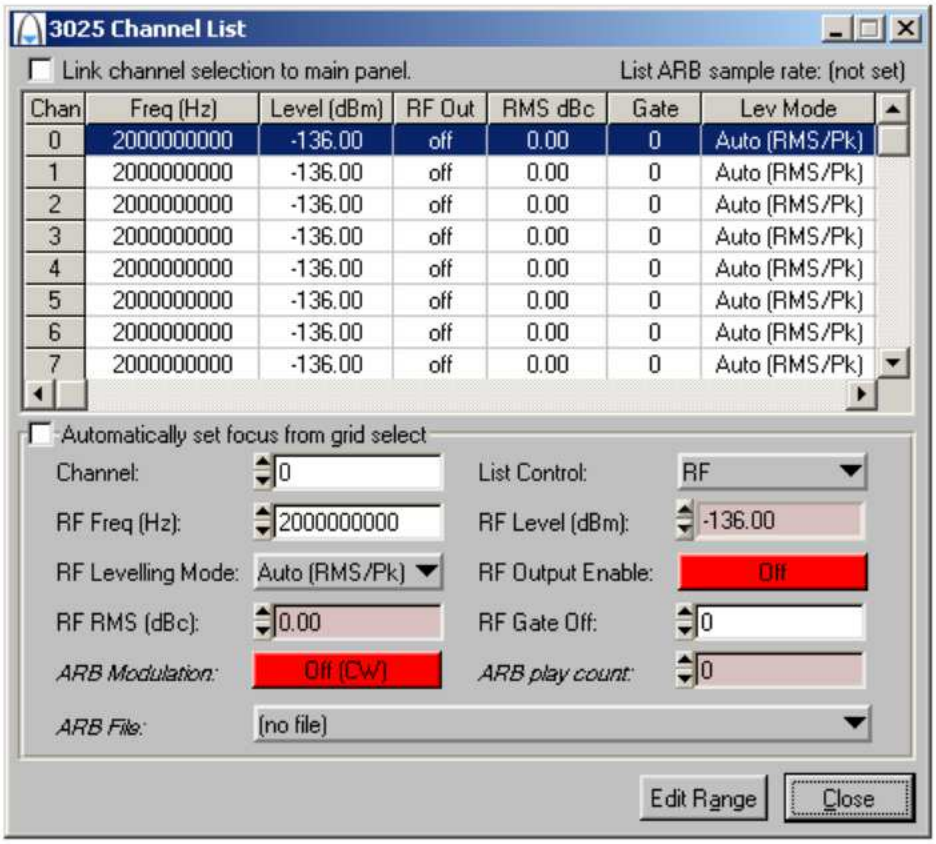


Fig. 3-8 Edit channel list settings

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Edit the grid in the upper part of the screen by means of the fields in the lower part. Most fields (Channel, RF Freq (Hz), etc) are similar to those on the soft front panel. Edit each channel individually or by range for:

- Channel
- RF Freq (Hz)
- RF Levelling Mode
- RF RMS (dBc)
- RF Level (dBm)
- RF Output Enable
- RF Gate Off
- ARB Modulation
- ARB Play Count
- ARB File

Click on the link for details.

Check the **Automatically set focus from grid select** box to make the associated field active when you click on a channel parameter in the grid.

If you check the **Link channel selection to main panel** box, changing the channel on this screen also changes the active channel (as shown on the soft front panel) and vice versa.

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Click **Edit Range** to display the Edit Channel Range screen (Fig. 3-9), which lets you apply changes to a set of channels simultaneously, speeding up channel setup.

Define start and finish values for address numbers in the **Chan range, from:** and **to:** fields.

Insert values and click **Set** for each field. You are asked to confirm each action. When finished, click **Close** to return to the Channel List screen.

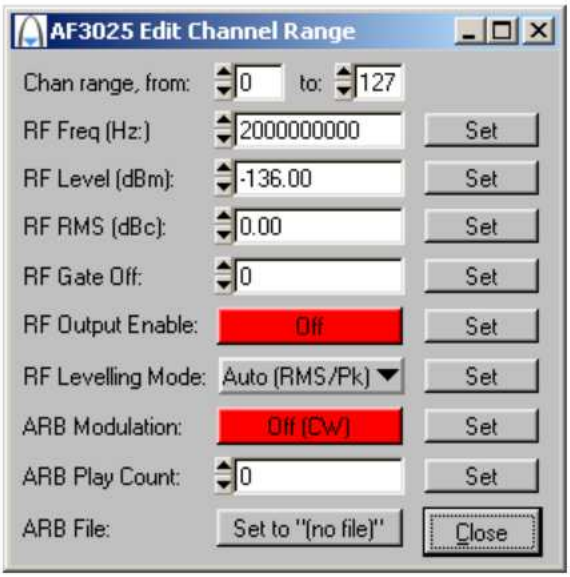


Fig. 3-9 Edit all channel settings

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RF Frequency (Hz)

Set the output frequency using the up/down arrows or by entering the frequency in Hz or scientific (e) notation, in the range 100 MHz to 6 GHz.

***Note**: the* Required LO Freq (Hz*) box shows the frequency that needs to be set on the 3010 Series synthesizer to give the chosen RF frequency at the 3025's output.*

Step size: double-click on the step value under the frequency field to set up the size of frequency step.

RF Level (dBm)

Set the output level using the up/down arrows or by entering the value in dBm in the range −120 to +5 dBm.

Step size: double-click on the step value under the RF level field to set up the size of level step.

Output

On/Off: enable or disable the RF output.

RMS (dBc)

□□□□□® files contain header information that indicates the RMS power level of the waveform. When using other sources of IQ, this information may not be present, in which case the RMS value needs to be entered in order to achieve the calibrated output level.

For files that do not contain RMS level header information, you can enter the RMS value of the signal here, and select **RMS** in the Levelling Mode field. The power output then matches that selected in the RF Level (dBm) field.

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Gate RF

If set to 1 (enabled), this turns the RF output for the active channel off when $\sqrt{(I^2 + Q^2)}$ is near to zero. This minimizes IQ leakage to a nominal –80 dBc during periods when the signal is 'off'.

ARB Modulation

Sets ARB modulation off or on. Effective only when List Control is set to RF & ARB. When set to Off (CW), the output becomes CW at the level specified.

ARB Play Count

Sets the number of ARB cycles to play, from 0 to 4095. 0 represents continuous play. Effective only when List Control is set to RF & ARB.

ARB File

Displays the standard file name in *.aiq* format. The file must already be loaded in the ARB File Catalog (page 3-24).

The first ARB file you select for entry defines the sample rate (shown top right in the Channel List screen). Any other ARB file selected must have the same sample rate.

The software automatically fills all succeeding channels in the list with the last-entered ARB file. These 'filler' files are shown with a +--> prefix to distinguish them from the file that you entered.

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Attenuator Hold

As the step attenuator changes range, small changes in VSWR can occur. Check the box to freeze the attenuator on its current range.

The maximum positive excursion is restricted to the 8 dB range of the attenuator pad, but you can reduce the RF level over a range of up to 40 dB. However, the level accuracy specification is invalid if you exceed the pad's range by more than a few dB.

With **attenuator hold disabled**, the RF level hardware is set for optimum level accuracy and spectral purity, and changes to the attenuator setting are possible.

Note that level accuracy and spectral purity cannot be guaranteed outside the normal level range.

The current active RF channel cannot be changed while attenuator hold is on.

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Levelling Mode

Leveling mode	Internal ARB	External Analogue IQ inputs (Opt. 01)
Auto (RMS/Pk)	Sets leveling automatically to RMS for ARB files that contain appropriate header information (□□□□□® files). The set level is RMS. If the RMS value is unavailable, or for inputs via the DATA connector, peak mode is selected automatically.	The set level is for $\sqrt{I^2+Q^2}=0.5V$. Headroom is left for the signals to peak at I=Q=0.5 V. Equivalent to using RMS mode with "RMS (dBc)" set to −3 dB.
Frozen	When frozen mode is selected, the leveling integrator is held at its current value and the system operates open-loop. To recalibrate for temperature changes, switch back to one of the other leveling modes, then back to frozen mode. This mode is advantageous for certain pulsed signals that cannot be easily leveled.	As for Auto mode. Note that the leveling system is always open-loop during external analog IQ operation. The leveling mode selects the reference power level. The system recalibrates to the internal reference voltage whenever the leveling mode, frequency or level is changed.
Peak	Causes the set RF Level to appear at the RF output if you apply full-scale I and Q sample values. As I and Q are decreased, the output decreases proportionally.	The set level is for I=Q=0.5 V Note that at no time should I or Q exceed 0.5 V in any mode, or clipping may occur. For example, do not use I=0, Q=0.707 V.
RMS	Causes the set RF Level to appear at the RF output if the RMS value of the applied IQ data stream equals the value set in the RMS (dBc) field. When you select this leveling mode, the RMS (dBc) field is set to a default value of 0. Note that the values are with respect to I=Q=Max.	You can enter the RMS level of your signal with respect to I=Q=0.5 V. The set level is then in RMS. For example if your signal is $\sqrt{I^2+Q^2}=0.25V$, you would set RMS (dBc) to –9 dB. If you then set -10 dBm, you should get nominally -10 dBm RMS.

***Note**: The maximum power specified on the datasheet is for I=Q=Max (I=Q=0.5 V for analog IQ inputs). This is the same in all modes, and the set level is clipped to avoid exceeding this limit. For example, if the relative RMS level is –3 dBc, the maximum set level in RMS mode is 3 dB below maximum. You are still able to reach the maximum level if you input I=Q=Max.*

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Modulation Source

Select between:

LVDS (external modulation via DATA connector on front panel)
ARB (internal modulation using the arbitrary waveform generator)
None (CW) (no modulation, carrier wave only). **None (CW)** sets I and Q to maximum level.
Internal AM
Internal FM
External Analog (allows use of IQ analog inputs when Option 001 is fitted)

Actual Level

Shows the current actual output level achieved by the module. A red indicator beside the RF Level (dBm) field shows either that attenuator hold is enabled or that the output level is not achieving the level requested.

Max Level

Shows the maximum possible output achievable by the module for the current settings and waveform selected.

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Sample rates

ARB Sample Rate (Hz)

Set the ARB's sample rate when Modulation Source is set to ARB. This is necessary only when the ARB file contains no header (files not generated using □□□□□®).

LVDS Sample Rate (Hz)

Sets the LVDS sample rate when Modulation Source is set to LVDS. The instrument calculates the interpolation automatically to place the interpolated frequency in the range 44 to 66 MHz.

External Reference

Checked: External 10 MHz reference via front-panel SMA connector
Unchecked: 10 MHz reference from PXI chassis.

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ARB handling

Introduction

The ARB is a dual-channel arbitrary waveform IQ baseband source generator. It is used to generate signals from samples stored in non-volatile memory. Four marker bits may be stored with the samples, and these are processed to maintain their time relationship to the output waveforms.

□□□□□® is a software package that allows you to create and package an arbitrary waveform file that can be loaded onto any 3020 Series digital RF signal generator. It is also possible to package and download files that have been created using other tools. Arbitrary waveforms that can be created by □□□□□® cover a wide range of digital modulation schemes.

□□□□□® is supplied on a CD-ROM together with a *Getting Started* manual (part no. 46882/599) that explains how to create, download and package waveforms to run on the ARB, and a *User Guide* (part no. 46882/627) that details the different modulation schemes supported. □□□□□® and its associated documentation are also available to download from the Aeroflex website http://www.aeroflex.com/iqcreator.

ARB File Catalogue

This field displays files currently loaded into the ARB's memory.

Add

Lets you add an ARB waveform to the ARB File Catalogue, using the standard Windows browser. The file must be in *.aiq* format (as generated by □□□□□®). Details of the format of ARB files and headers are given in Format of ARB Files.

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File Info

Provides information about the currently selected ARB file, such as file name and maximum output level.

Delete

Deletes the currently selected ARB file from the specified catalog.

Reload

Reloads an ARB file from hard disk to the specified catalog.

Reload All

Reloads all ARB files from hard disk. This may improve performance if the ARB memory has become fragmented.

Delete All

Deletes all ARB files from the specified catalog.

Save Cat

Saves a catalog of the currently loaded files into a new folder. This function is available only on the soft front panel.

Load Cat

Loads a previously saved catalog of files from a named folder.

Start Play

Plays the selected ARB file and displays its filename. This function automatically sets the IQ source to ARB, and the VCO frequency appropriate to the file being played.

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Triggering

Trigger setup for the external ARB trigger. ARB trigger sources are:

PXI backplane	Trigger bus
LVDS AUXiliary inputs	Front-panel DATA connector
TTL TRIG input on front panel	SMB
Star trigger	Star controller card in Slot 2.

Select trigger sources with the routing matrix.

ARB Trigger

On (external)	Dependent on Trigger Edge and Trigger Mode
Off	Internal software triggering

Trigger Edge

Selects the positive- or negative-going edge of a pulse to trigger the ARB.

Trigger Mode

Gated	Begins playing the ARB file continuously on receipt of the leading edge of a gate pulse. After the trailing edge of the gate, the ARB file continues playing until its end, then stops.
Single-shot	Plays the ARB file once through.

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Driver export functions

On-line help and functional documentation for driver export functions are available on the CD-ROM supplied with your module. They are installed onto your computer at the same time as the drivers.

Driver installation folder

Find help and functional documentation in the driver installation folder on your computer. This is typically:

C:\vxipnp\winnt\af3020

Help

Within the driver installation folder are help files that provide descriptions, parameter lists and return values. Help files are provided in three formats:

af3020.doc	3020 Series function documentation	Text file
af3020.hlp	3020 Series Visual BASIC function reference	Windows Help file format
af3020_C.hlp	3020 Series C language function reference	

We recommend that you use the C or Visual Basic formats, as these are easier to navigate.

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The file opens at the Contents page:

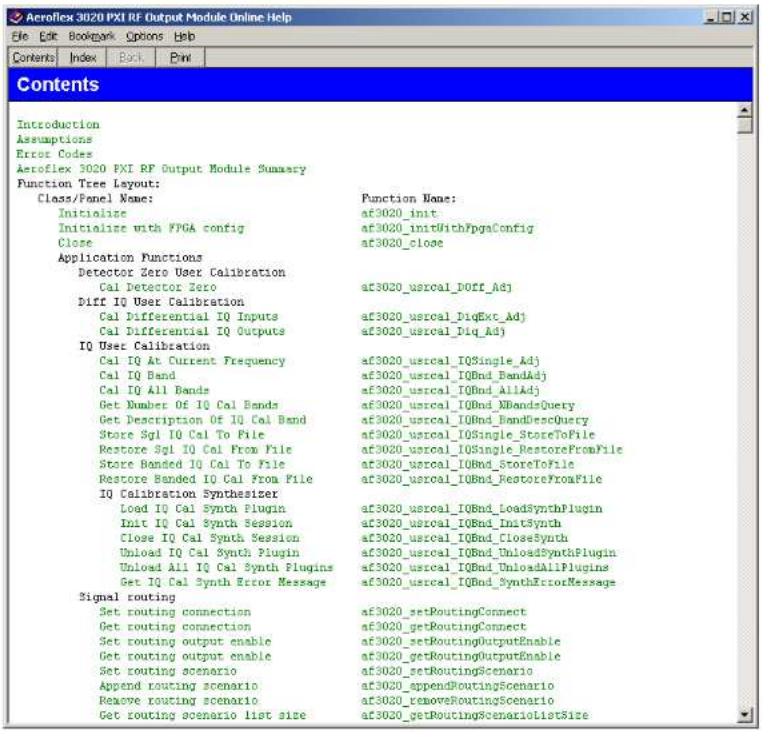


Fig. 3-10 Online help contents — example

Hyperlinks from here take you to

- Introduction
- Assumptions
- Error codes
- Functions listings.

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Functions listings

Functions are grouped by type. Click on the hyperlink for details of the function. Each function has a description of its purpose, and may have a list of parameters and return values.

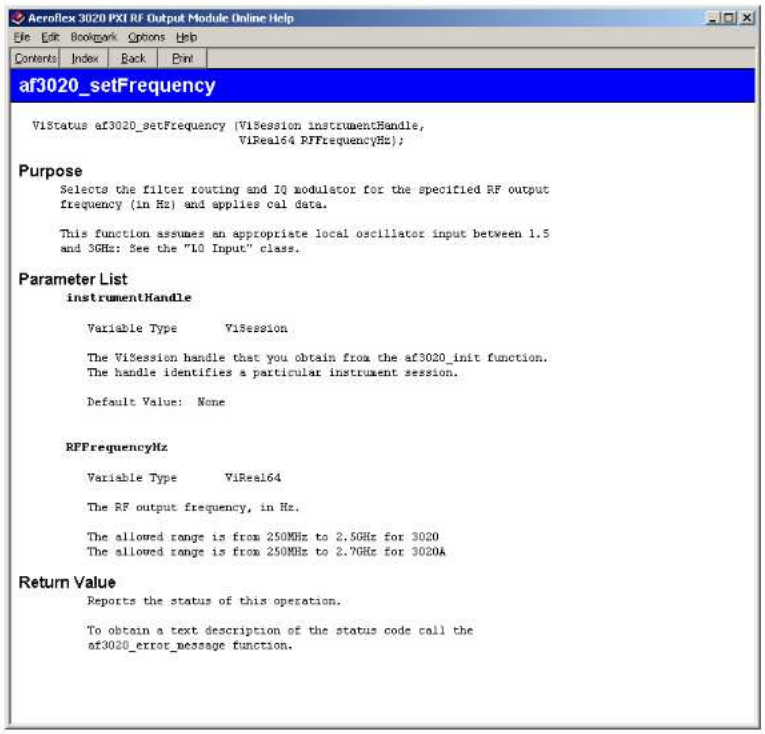


Fig. 3-11 Function description — example

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Available options

Option 01 Analog I & Q inputs and I & Q outputs

Differential IQ

When this option is fitted, **Differential IQ** displays the screen for setting up differential outputs (Fig. 3-12) and single-ended inputs.

The module provides balanced baseband I and Q **outputs** suitable for feeding devices with differential inputs. Signals that appear on I+ and I−, Q+ and Q−, are of equal magnitude but of opposite polarity. The positive or negative I and Q pairs can also be used as unbalanced single-ended outputs.

The module also accepts single-ended **inputs** into a switchable high or low impedance. Feed analog Q signals into the I+ connector, analog I signals into the Q+ connector.

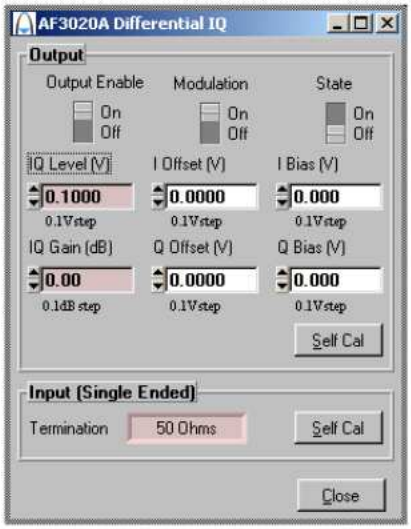


Fig. 3-12 Differential IQ setup screen

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Output Enable enables or disables the differential IQ outputs. When set Off, the output is high impedance. When set On, the ouput impedance is 50 □. **Modulation** enables or disables the bias and offset voltages. When set Off, it zeroes bias, offset and signal voltages.

State enables or disables the ARB signal component. When set Off, it disables the signal but bias and offset levels remain.

IQ Level (V) specifies the peak-peak amplitude of the output signal component (see Fig. 3-13) into 50 □ (single-ended) or 100 □ (differential).

IQ Gain (dB) specifies the relative amplitudes of the I and Q signals. Adding gain (+x dB) to the signal increases the magnitude of the I component by $\frac{x}{2}$dB whilst decreasing the magnitude of the Q component by the same factor. Similarly, removing gain (−x dB) from the signal increases the magnitude of the Q component by $\frac{x}{2}$dB whilst decreasing the magnitude of the I component by the same factor.

I Offset (V) specifies the differential voltage between I+ and I− (see Fig. 3-13).

Q Offset (V) specifies the differential voltage between Q+ and Q−.

I Bias (V) specifies the common-mode I voltage.

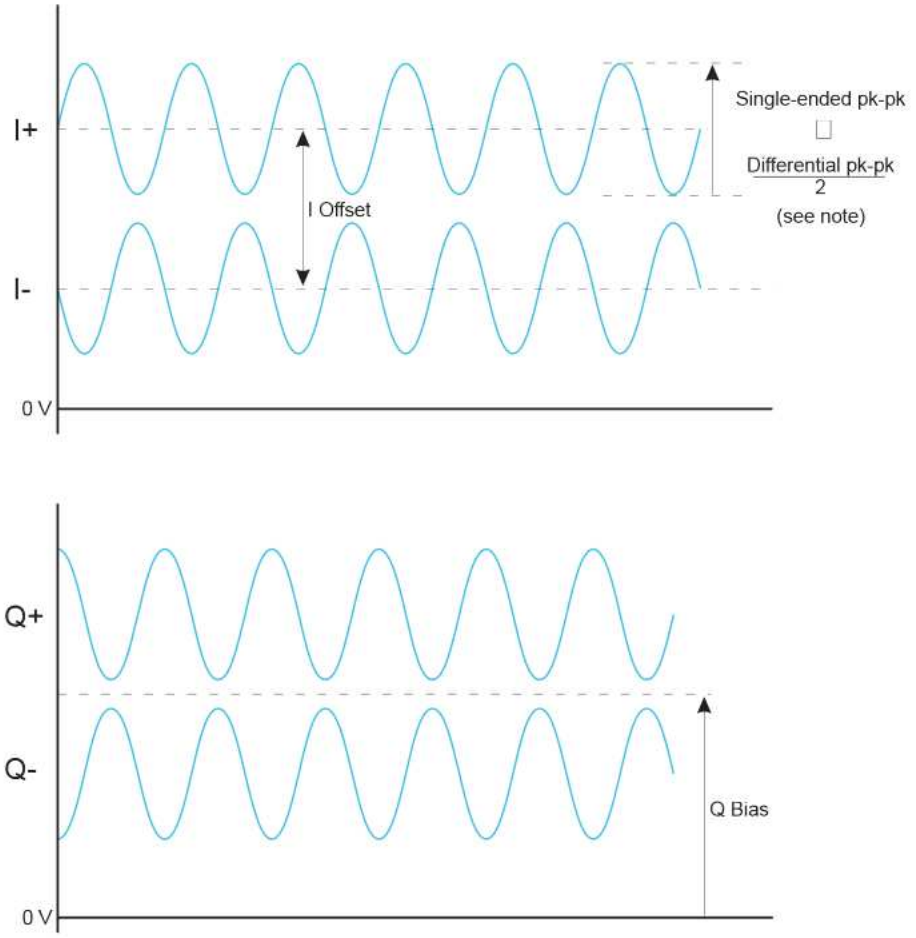
Q Bias (V) specifies the common-mode Q voltage (see Fig. 3-13).

Self Cal (output) calibrates the differential IQ by setting input or output levels to 0 V and recalibrating DACs.

Self Cal (input, single-ended) nulls out any DC offset present at the input.

Termination shows the value of input impedance selected. Inputs are enabled when Modulation Source is set to Ext Analog.

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Gain
Adding x dB increases I Level by x/2 and decreases Q Level by x/2.
Removing x dB increases Q Level by x/2 and decreases I Level by x/2.

This diagram represents a condition where the signal is output into a floating 100 Wload.

Note: the differential signal level is twice the single-ended signal level.

Fig. 3-13 Differential IQ parameters

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Digital RF signal generator using 3010/3011 and 3025

Refer to *3000 Series PXI Modules Installation Guide for Chassis* (document no. 46892/667), *Getting Started with afSigGen* (document no. 46892/678), and *PXI Studio User Guide* (document no. 46892/809), all supplied on the CD-ROM with the module, for detailed information on creating a fully functional digital signal generator using the 3025 and 3010/3011 together. The afSigGen soft front panel and afSigGen dll or afcomSigGen COM object combine the functions of the individual modules to provide a single interface with the appearance and functionality of an integrated instrument.

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Appendix A
Format of ARB files

General

The ARB stores digital representations of waveforms. Any number of waveforms can be stored, up to a total capacity of 32 Msamples. The memory used is volatile.

Each waveform consists of two components, I and Q. When the ARB is enabled and one of the waveforms selected, it is converted into a pair of analog signals that can be used to drive the I and Q channels of the RF modulator, or output as analog baseband IQ when Option 01 is fitted. Waveform data files are created externally and require packaging before they can be used by the ARB.

Each sample contains two 14-bit numbers, one each for I and Q. To minimize the required file size and reduce aliasing problems, the ARB includes an interpolator to increase the D-A converter sample rate by factors of between 2 and 3072 so that the D-A converter runs at between 44 and 66 M sample/s.

A waveform is looped continuously. The rate at which the sample plays is set during file creation and is coded in the header.

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An example showing data rates and sizes for an IS-95 waveform

IS-95 has a chip rate of 1.2288 Mchip/s. For our purposes we will consider a chip to be the significant symbol. Each symbol must be sampled at least four times. This would give a rate of 4.9152 Msample/s. There are 24 576 symbols per 20 ms frame. Four frames would have 98 304 symbols, which after oversampling gives 393 216 samples. As the oversample ratio increases, the file becomes larger.

When the above waveform is selected and played, it is read out of the memory at 4.9152 Msample/s. The ARB interpolates this data stream so that it has a data rate of 58.9824 Msample/s.

The data is written to the two 14-bit D-A converters at 58.9824 Msample/s. The analog outputs from the D-A converters are then filtered to remove switching and quantization noise and high-frequency images. The I and Q outputs are then routed to the RF modulator.

Markers

Markers are used to mark important events within the file; for example, the start of a TDMA slot or frame.

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Format for header of ARB IQ files (*.aiq)

	Comment	No. of bytes
[File]		
Date=	Date file was created (mm/dd/yyyy)	12
Time=	Time file was created (hh:mm:ss)	10
PackSWVers=nn.nn	SW version of Packager (files that are created using software other than □□□□□® must set nn.nn = 00.00)	5
Samples=	No. of IQ Samples as an ASCII number	8
Title=	Name of AIQ file without extension and without path	80
SampleRate=	In Hz, in steps of 100 Hz, converted from user entry in packager	8
Description=	Description field entered in packager	120
RMS=	RMS value of the stored waveform	9
RelRMS=	RMS relative to maximum (dB)	8
CrestFactor=	Crest factor of stored waveform	8
[Assign]		
Mkr1=	Marker 1 assignment (not used or general)	12
Mkr2=	Marker 2 assignment (not used or general)	12
Mkr3=	Marker 3 assignment (not used or general)	12
Mkr4=	Marker 4 assignment (not used or general)	12

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All headers are stored as ASCII strings, each line terminated with CR/LF.

The header is terminated by a ^Z. Data following the header is the IQ and marker data stored as IQIQIQ…

The format is:

bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	S	Q	Q	Q	Q	Q	Q	Q	Q	Q	Q	Q	Q	Q	M2	M1

bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	S	I	I	I	I	I	I	I	I	I	I	I	I	I	M4	M3

where Mn = marker number n, S = sign bit.

The last 32-bit value in the file is a checksum that is calculated as the running unsigned sum of the 32-bit numbers.

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Appendix B
DATA connector and timing

The DATA connector is a 68-way female VHDCI-type LVDS (low-voltage differential signaling) interface. It can be used to input data and associated control and timing signals.

The DATA connector is shown in Fig. B-1. LVDS data conforms to ANSI/TIA/EIA-644.



Fig. B-1 DATA connector (looking onto front panel)

The DATA interface provides:

- input for IQ data
- input/output for trigger and marker signals.

The electrical level is LVDS: V_{OH} typically 1.38 V, V_{OL} typically 1.03 V

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Table B-1 DATA pin-out

Contact	Function	Contact	Function
1	AUX0-	35	AUX0+
2	AUX1−	36	AUX1+
3	AUX2−	37	AUX2+
4	SPARE1−	38	SPARE1+
5	SPARE2−	39	SPARE2+
6	CLK_OUT−	40	CLK_OUT+
7	GND	41	GND
8	CLK_IN−	42	CLK_IN+
9	D0−	43	D0+
10	D1−	44	D1+
11	D2−	45	D2+
12	D3−	46	D3+
13	D4−	47	D4+
14	D5−	48	D5+
15	D6−	49	D6+
16	D7−	50	D7+
17	D8−	51	D8+
18	D9−	52	D9+
19	D10−	53	D10+
20	D11−	54	D11+
21	D12−	55	D12+
22	D13−	56	D13+
23	D14−	57	D14+
24	D15−	58	D15+
25	IQSELECT_IN−	59	I/QSELECT_IN+
26	IQSELECT_OUT−	60	IQSELECT_OUT+
27	SPARE0−	61	SPARE0+
28	GND	62	GND
29	MARKER1−	63	MARKER1+
30	MARKER2−	64	MARKER2+
31	MARKER3−	65	MARKER3+
32	MARKER4−	66	MARKER4+
33	AUX3−	67	AUX3+
34	AUX4−	68	AUX4+

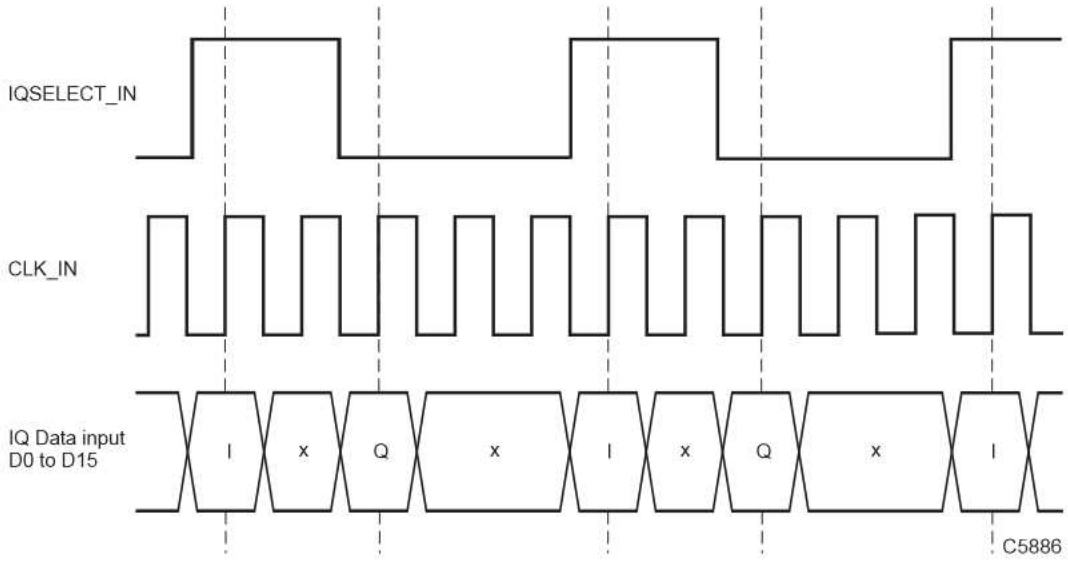
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LVDS data used as IQ input

Data is supplied to the LVDS interface using a 16-bit bus. The D/A converters are 14 bits and by default the module uses bits [15:2]; however, it is possible to select to use [13:0] instead. Similarly, data is signed two's complement by default, but it is possible to select unsigned instead. See **LVDS**.

IQ data pairs are clocked sequentially, with I always followed by Q. I data is clocked into the module on the first CLK_IN edge following IQSELECT_IN going high. Q data is clocked in on the first edge following IQSELECT_IN going low.

Multiple CLK_IN cycles can occur between IQSELECT_IN changing state, and CLK_IN can be any frequency up to 132 MHz. However, the resulting IQ sample pair rate must be the same as the sample rate set for the module. For this to occur, it is important to lock CLK_IN to the same 10 MHz reference that the module is using, otherwise frequency drift will cause periodic data errors.



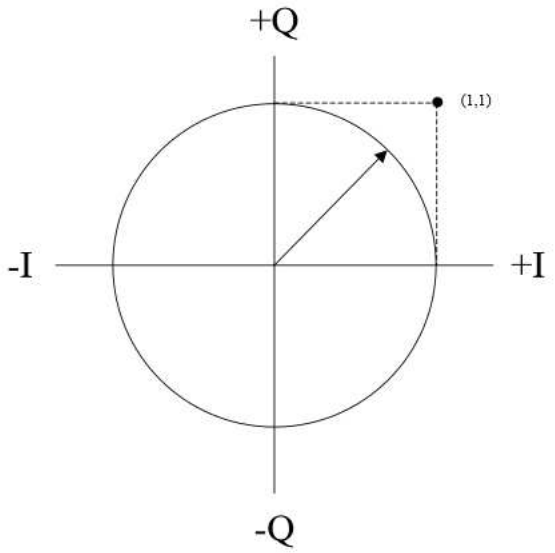
Data in is latched on the rising edge of CLK_IN.

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Output power level

The IQ leveling loop is referenced to maximum I and Q level (1,1 on the vector diagram), and the maximum RF power using IQ data is also referenced to this. Output level for a modulated signal with constant envelope (for example, GSM) is reduced by 3 dB on the maximum available CW level. This type of signal will fall on the unit circle.

For complex modulation schemes that include amplitude modulation, the maximum achievable mean power depends on the ratio of mean to peak signal levels; this value is provided in the header information (RelRMS) of files generated in □□□□□®.



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Markers

There are four marker inputs/outputs on the DATA connector. The markers can be used for triggering and addressing.

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Chapter 4 BRIEF TECHNICAL DESCRIPTION

Introduction

The 3025 is a digital RF signal generator PXI module. It contains IQ modulators, leveling control, step attenuators, and a dual-channel arbitrary waveform generator. An external source, preferably a 3010 Series RF synthesizer, provides the LO signal. The two modules together then form a digital RF signal generator.

The 3025 comprises three printed circuit boards. The logic and control board contains the PCI interface, baseband VCO, IQ ARB, leveling control and an external LVDS data interface. The RF board is housed in a full clamshell shield, containing RF dividers, IQ modulators, output amplifier and step attenuator. The differential IQ board contains a bias source for the IQ modulators and (when Option 001 is fitted) differential IQ processing.

Only the logic board connects to the PXI backplane, so power and control to the RF board is routed through the logic board. Ribbon cables interconnect the logic, RF and differential IQ boards, handling power to the RF board, differential analog IQ, analog leveling signals and various switched control signals.

A block schematic of the instrument is shown in Fig. 4-1.

Logic and control board

The PCI interface uses an FPGA, which boots up at power-on from a local ISP PROM. The interface provides all the required PCI-compliant handshaking and data transfer. A serial EEPROM is used for calibration data as well as all module information, such as serial number.

A baseband VCO generates a clock signal forthe IQ generation and processing. This is a fractional-N-based system, operating from 88 to 132 MHz and using either the PXI 10 MHz clock or an external 10 MHz signal as its reference.

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Analog IQ signals are generated by two DACs, their clocks supplied directly from the VCO at 88–132 MHz. The DACs interpolate at 2x, giving a data rate of 44–66 MHz. The DACs each produce differential signals that are fed through filters, two for each DAC. The data for the DACs may come from static registers for CW operation, the internal ARB, internal AM/FM generator, or the LVDS data interface.

The ARB consists of SDRAM devices configured as 64-bit-wide memory. An SDRAM controller handles bursted writing and reading from the memory. The ARB sample width is 32-bit: 14-bit I, 14-bit Q, and 4-bit markers. The memory is configured as 64-bit to provide capacity to set up bursts and perform the frequent auto-refreshes required of SDRAM.

The LVDS interface provides a digital input. A rate-matching FIFO is used to allow the data source to use an independent clock, but it must be assumed that it is locked to the same reference for correct operation.

Digital interpolation filters allow a range of data rates less than the 44 to 66 MHz clock range. The highest order of interpolation is 3072, which means the lowest sample rate is 14.323 kHz. These filters are used on both ARB and LVDS data. The module applies all corrections to IQ data in the digital domain. This includes DC offset, gain imbalance and phase skew between I and Q. Additional digital filters are used to correct for inaccuracy in the analog reconstruction filters and frequency response of the DACs.

A closed-loop leveling control drives leveling on the RF board via a 14-bit DAC. The signal from an RF detector after this stage is converted by an ADC.

The leveling loop derives its error signal by comparing the input to the comparator from the RF detector ADC, and the wanted IQ power. The IQ power is converted to detector volts in a look-up table. During bursted IQ data, the loop can be frozen while ramping IQ data up or down, and can also switch off the signal between bursts, improving on-off ratio.

A burst of data from the detector ADC can be stored and retrieved by the software driver, which is useful for operations such as offset-nulling the ADC and performing IQ calibration. During IQ calibration short test-signals are loaded to the ARB, and by synchronizing ADC data capture, the driver can make the necessary calculations and corrections to IQ offsets, gain and skew.

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RF board

LO input and RF output is via front-panel-mounted SMA connectors. The LO input is in the range 1.5 to 3 GHz at a nominal level of 0 dBm. Frequency division extends the available RF frequency range down to 250 MHz. The RF signal is generated using an IQ modulator, which accepts divided LO and IQ baseband signals.

The RF input signal drives a chain of three dividers. A signal at the required output frequency is routed from the appropriate divider to one of two IQ modulators via harmonic filtering.

One modulator covers frequencies from 100 MHz to 4 GHz; the other, frequencies from 4 GHz to 6 GHz. Filtering is repeated after the modulators. The appropriate signal is routed to the output section.

A PIN attenuator operates over a range of at least 20 dB. The drive to this level control incorporates a shaping network to approximate to logarithmic control. The leveling is entirely under software control and as such is completely flexible.

Level detection takes the form of voltage sensing behind a 50 □ resistor.

The switchable step attenuator operates in increments of 6 dB, from 0 dB up to 132 dB. The attenuator uses 50 □ resistive pads that are switched in and out of circuit. The incremental attenuation values are 6, 12, 24 and 30 dB.

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The detector output is amplified and buffered before being fed back to the logic board for A-D conversion. A temperature-sensing mode is provided, where the detector is disabled and the output replicates the voltage. This can be measured and used to periodically adjust calibration in accordance with temperature and stored data.

Differential IQ board

When Option 001 is fitted, this board provides baseband IQ modulation outputs, and external IQ inputs. Single-ended inputs and differential outputs share the same front-panel SMB connectors.

The board has three modes of operation:

Internal, where the SMB baseband IQ connectors are not used

External IQ input, where RF modulation is controlled by single-ended external inputs

External IQ output, where IQ baseband from the logic and control board is available as a differential output. The RF output provides an unmodulated CW signal, useful for RFIC testing.

The board multiplexes three sources of baseband modulation onto the RF board. When normal operation is selected, IQ modulation is routed from the logic and control board. When external inputs are selected, modulation from the external inputs is selected. When external outputs are selected, a DC level is applied to provide a CW signal at the RF output. Low-pass filters are switched onto the modulator drive to enhance isolation of spurious sidebands.

In single-ended input mode, I and Q inputs are buffered into 100 k□; alternatively, this input can be switched to 50 □ to ground. Input clamping protection is provided. Offset voltages are added to the IQ signals before they enter the multiplexer.

In differential output mode, I and Q outputs from the logic and control board are buffered and pass through variable attenuators that provide up to 22.5 dB attenuation in 1.5 dB steps. They are then amplified by switched gain power stages, formed of paralleled amplifiers in order to provide low noise. Offset voltages are summed at this stage. The outputs pass to the front panel SMB sockets via relays.

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Whether option 001 is fitted or not, the board puts a programmable bias onto the IQ signals for the modulators on the RF board. In addition, it provides a clean 5 V power supply for the RF board from the chassis 5 V supply.

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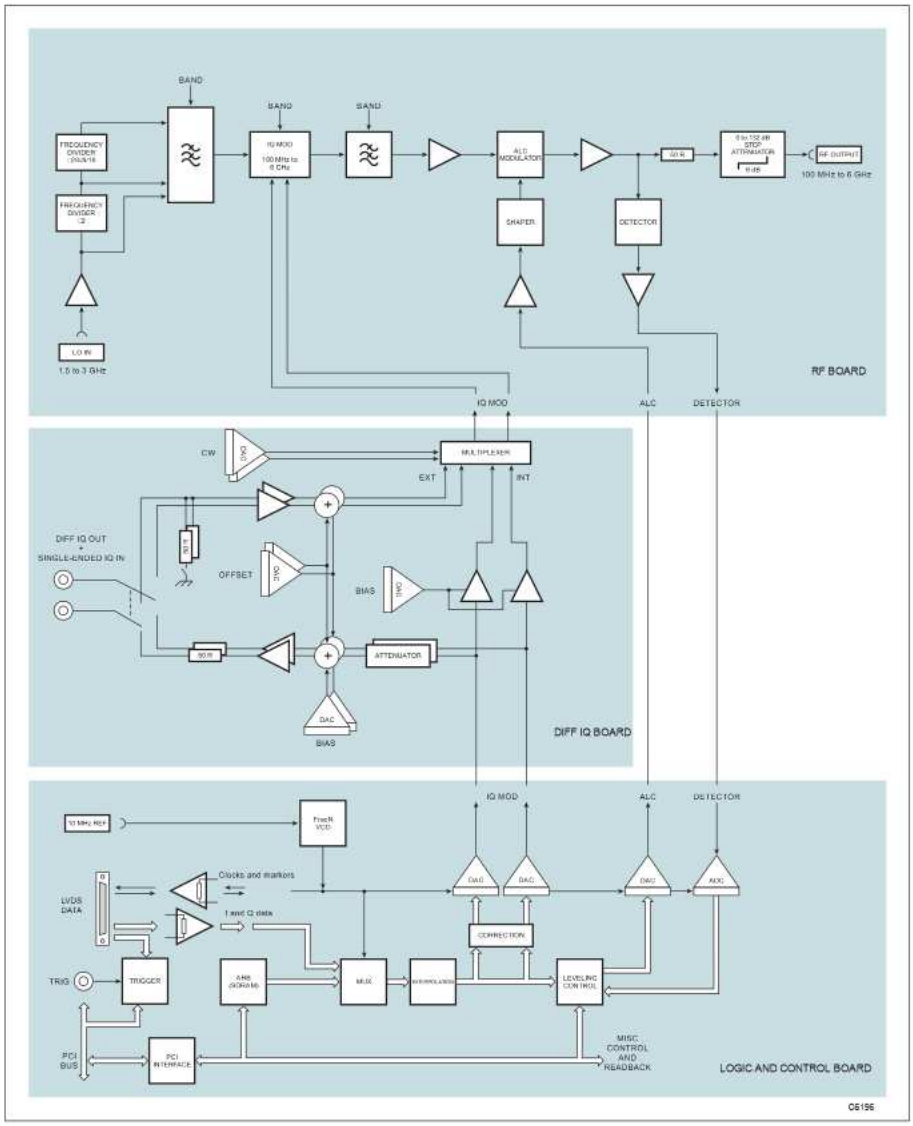


Fig. 4-1 3025 block schematic diagram

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