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53A-425 QUAD ARINC-429 TRANSMITTER CARD

OPERATING MANUAL

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53A-425 QUAD ARINC-429 TRANSMITTER CARD

OPERATING MANUAL

DESCRIPTION

The 53A-425 Quad ARINC-429 Transmitter Card is a printed circuit board assembly for use in a CDS 53/63 Series System. The card transmits data onto the Mark 33 Digital Information Transfer System (DITS) found on commercial aircraft. The 53A-425 Card has four independent transmitters, each with an associated buffer memory for storing up to 32,768 ARINC-429 words for transmission on the DITS bus.

The data stored in memory can be updated "on the fly", i.e., while the 53A-425 Card is transmitting. Transmission data in each memory is organized into "frames" consisting of a header word, for frame control, and one or more ARINC-429 data words. The header word controls the time interval between the start of one frame and the start of the next frame, and whether data in memory is to be transmitted once or continuously. To allow frame-by-frame testing of word-format protocol, the header word also controls parity (odd/even), word length (31, 32, or 33 bits), and the interword gap (two or four bit times) for the frame's ARINC-429 data words. The bit rate for each channel is programmable from 122 b/s to 125 kb/s, or an external clock can be used to set the bit rate.

The 53A-425 Card has Direct Memory Access (DMA) transfer capability to efficiently accept data from the system controller. Using a system controller with DMA capability, the card supports memory updating "on the fly" when all four buses are operating at 100-kHz bit rates. Either a programmable frame-by-frame interrupt, or a readback of the address of the last ARINC word transmitted, allows the user to synchronize updates to the card with the actual data transmission.

The differential data output voltage levels may be programmed independently on each channel to ±13 V, ±10 V, ±6.5 V, or ±2.5 V, line-to-line, to allow high-level, standard-level, low-level, and no-data-level receiver parametric electrical testing.

Extensive self test capabilities are provided, including a wraparound check of each channel, self test of the PROM and RAM memories, and testing of the bit-rate and frame-rate counter/timers on the card. Error reporting provides readback of any errors encountered during self test or during programming. Status LEDs at the front edge of the card provide a visual indication of programming errors and data transmission on each channel.

CONTROLS AND INDICATORS

The following controls and indicators are provided to select and display the functions of the 53A-425 Card's operating environment.

Address-Select Switch

The 53A-425 Card has a miniature, 10-position switch labeled "ADDRESS" that selects the 53A-425 Card's address (0-9) in the 53/63 Series System. The switch's cover opens to allow the address to be reselected. A screwdriver with a narrow, flat blade should be used to turn the cam-action wiper to the desired address position.

Power LED

The Power LED provides a valuable diagnostic tool by giving the system programmer a visual indication of the action which the system is currently taking. Whenever the 53A-425 Card is addressed by the system controller, the LED goes out. The LED remains out until another function card is addressed. Since only one function card can be addressed at a time, an unlit Power LED indicates the function card with which the system controller is currently communicating. The Power LED being lit not only indicates that the 53A-425 Card is unaddressed, but that all required dc power (5 V dc, ±15 V dc) is being supplied.

Fuses

The 5-volt dc and ±15-volt dc power buses each have a fuse that protects the system from overloads. If any fuse has blown, the Power LED will not light.

Function LEDS and Switches

LEDs

The following LEDs are provided at the top front edge of the 53A-425 Card to indicate the status of the card's operation:

Status LEDs

Five LEDs are located near the front-edge connector, arranged in the order listed below, which indicate the following:

Status LED	Definition
XMIT1	When lit, channel 1 is transmitting data over the Mark 33 DITS bus.
XMIT2	When lit, channel 2 is transmitting data over the Mark 33 DITS bus.
XMIT3	When lit, channel 3 is transmitting data over the Mark 33 DITS bus.
XMIT4	When lit, channel 4 is transmitting data over the Mark 33 DITS bus.

ERR

1. During self test, the ERR LED blinks on and off. If an error is encountered during self test, the ERR LED stays on continuously.

2. The ERR LED lights if a syntax error is encountered during programming. The LED will go out when the error is reported to the system controller.

Switches

The following switches are provided to select the proper functions for the 53A-425 Card's operating environment:

Halt Switch

This two-position slide switch is located near the card's backplane edge connector. It selects the state of the 53A-425 Card after an @XH (Halt) or STOP command is received by the 53/63 Series System.

a. If the Halt Switch is in the ON position, then the 53A-425 Card is reset to its power-up state, all parameters are reset to their default values, and the Power LED is lit.

b. If the Halt Switch is in the OFF position, then the 53A-425 Card becomes unaddressed, the Power LED is lit, and any programmed parameters of the card remain unchanged.

SPECIFICATIONS

Configuration:	Quad ARINC-429 Transmitter
Coupling:	Connects directly to Mark 33 DITS bus.
RAM:	32K x 32 RAM memory associated with each channel for data and control instructions.
Processor:	Intel 80186 (LCC).
Error Buffer:	16 errors, maximum.
Parity (programmable):	The 53A-425 Card can generate odd or even parity, programmable on a frame-by-frame basis for each channel.
DITS Word Format (programmable):	The transmitted DITS word can have 31, 32 or 33 bits, programmable on a frame-by-frame basis for each channel.
Interword Gap (programmable):	Between words: two or four bit times, programmable on a frame-by-frame basis for each channel.
Frame Interval (programmable):	Delay between the start of one frame and the start of the next frame: 5 ms to 4 s in 1-ms steps, programmable on a frame-by-frame basis for each channel. Delay accuracy: one bit-rate clock cycle ±150 us, one channel transmitting; one bit-rate clock cycle ±500 us, four channels operating.
Bit-Rate Period (programmable):	8 μs to 8.19 ms in 250-ns steps, programmable independently for each channel.
Data-Transfer Rate:	2 μs, maximum (time required by card to receive and store one byte of data into memory).
53A/63A System Interrupts (programmable):	Programmable on a frame-by-frame basis for each channel to indicate the start of a frame.
ARINC Output (each channel)	
Type Output:	Differential.
Programmable Voltage Levels (no load to full load):	Normal Levels

Logic High:
Line A to Ground - +5 ± 0.25 V.
Line A to B - +10 ± 0.50 V.
Line B to Ground - -5 ± 0.25 V.

Logic Low:
Line A to Ground - -5 ± 0.25 V.
Line A to B - -10 ± 0.50 V.
Line B to Ground - +5 ± 0.25 V.

Logic Null:
Line A to Ground - 0 ± 0.25 V.
Line A to B - 0 ± 0.50 V.
Line B to Ground - 0 ± 0.25 V.

Parametric High Levels

Logic High:
Line A to Ground - +6.5 ± 0.325 V.
Line A to B - +13.0 ± 0.650 V.
Line B to Ground - -6.5 ± 0.325 V.

Logic Low:
Line A to Ground - -6.5 ± 0.325 V.
Line A to B - -13.0 ± 0.650 V.
Line B to Ground - +6.5 ± 0.325 V.

Logic Null:
Line A to Ground - 0 ± 0.25 V.
Line A to B - 0 ± 0.50 V.
Line B to Ground - 0 ± 0.25 V.

Parametric Low Levels

Logic High:
Line A to Ground - +3.25 ± 0.163 V.
Line A to B - +6.50 ± 0.326 V.
Line B to Ground - -3.25 ± 0.163 V.

Logic Low:
Line A to Ground - -3.25 ± 0.163 V.
Line A to B - -6.50 ± 0.326 V.
Line B to Ground - +3.25 ± 0.163 V.

Logic Null:
Line A to Ground - 0 ± 0.25 V.
Line A to B - 0 ± 0.50 V.
Line B to Ground - 0 ± 0.25 V.

Parametric Null Levels

Logic High:
Line A to Ground - +1.25 ± 0.1 V.
Line A to B - +2.50 ± 0.2 V.
Line B to Ground - -1.25 ± 0.1 V.

Logic Low:
Line A to Ground - -1.25 ± 0.1 V.
Line A to B - -2.50 ± 0.2 V.
Line B to Ground - +1.25 ± 0.1 V.

Logic Null:
Line A to Ground - 0 ± 0.25 V.
Line A to B - 0 ± 0.50 V.
Line B to Ground - 0 ± 0.25 V.

Rise/Fall Time: 16 kb/s to 125 kb/s: 1.5 ± 0.5 μs.

0 b/s to 16 kb/s: 0 ± 5 μs.

Output Impedance: 75 ± 5 Ohm, balanced.

Drive Capability: 20 ARINC receivers (400-Ohm minimum load).

Auxiliary Inputs/Outputs (each channel)

Sync Out*:
Type output: TTL.
Drive: 6 standard TTL loads.
Sense: High while ARINC-429 word is being transmitted.

Frame Transmitting*:
Type output: TTL.
Drive: 6 standard TTL loads.
Sense: Low while frame is being transmitted.

Clock Out*:
Type output: TTL.
Drive: 6 standard TTL loads.
Sense: Free-running clock at ARINC-429 data-transmission bit rate.
Duty cycle: 50%.

NRZ Data Out*:
Type output: TTL.
Drive: 6 standard TTL loads.
Sense: ARINC-429 output data in NRZ, high-true format. Data is valid on the falling edge of Data Clock Out.
Transmission order: LSB of ARINC-429 word first.

Data Clock Out*:
Type output: TTL.
Drive: 6 standard TTL loads.
Sense: NRZ data is valid on the falling edge of Data Clock Out. One output pulse for each data bit transmitted.
Duty Cycle: 50%.
Rate: Equal to ARINC-429 bit rate.

External Clock Input:

Type input: TTL-compatible.
Loading: 0.8 standard TTL load.
Range: 0-Hz to 125-kHz square wave, 50% duty cycle.

*These signals are intended for use by the 53A-427 ARINC-429/561 Converter Card.

Power-Up:

The 53A-425 Card powers up to the following states:

- Interrupts disabled.
- 100-kb/s bit rate for all channels.
- Transmitter outputs in null state.
- Internal bit-rate clock selected.
- Channel 1 selected.
- Power LED lit.
- XMIT1 LED out.
- XMIT2 LED out.
- XMIT3 LED out.
- XMIT4 LED out.
- ERR LED out if no self-test errors are found.
- Channel-memory addresses at location 0.

Self Test Performed:

Memory, time-base, and output-data tests (data output wrapped around to one of the processor's input ports prior to differential drive amplifiers).

NOTE: During self test, test patterns are transmitted over DITS bus at parametric null voltage level (below user receiver threshold).

Power Requirements:

5V and ±15V dc power is provided by the internal Power Supply in the 53/63 Series Card Cage.

Voltage (5-volt Supply):

4.75 V dc to 5.25 V dc.

Current (5-volt Supply):

1.6 A, maximum quiescent.
1.7 A, peak.

Voltage (±15-volt Supplies):

+14.5 V dc to +15.5 V dc.
-14.5 V dc to -15.5 V dc.

Current (+15-volt Supply):

100 mA, maximum quiescent.
105 mA, peak.

Current (-15-volt Supply):

95 mA, maximum quiescent.
100 mA, peak.

Cooling:

Provided by fan in the 53/63 Card Cage.

Temperature:	-10 °C to +65 °C, operating (assumes ambient temperature of 55° and airflow to assure less than 10 °C temperature rise). -40 °C to +85 °C, storage.
Humidity:	Less than 95% R.H., noncondensing.
Dimensions:	197 mm high, 221 mm deep, 13 mm wide. (7.75 in x 8.69 in x 0.5 in).
Dimensions, Shipping:	When ordered with a 53/63 Card Cage, the card is installed in one of the card cage's function-card slots. When ordered alone, the shipping dimensions are: 254 mm x 254 mm x 127 mm. (10 in x 10 in x 5 in).
Weight:	0.64 kg. (1.4 lb).
Weight, Shipping:	When ordered with a 53/63 Card Cage, the card is installed in one of the card cage's function-card slots. When ordered alone, the shipping weight is: 1.00 kg. (2.2 lb).
Mounting Position:	Any orientation.
Mounting Location:	Installs in any function-card slot of the 53/63 Series Card Cage.
I/O Connection:	A 48-pin hooded connector (53A-780) connects to all front-edge signals.
Required Equipment (not supplied):	53A-780 Hooded Connector, or 53A-746 Analog Cable (contain Channel 1-4 Line A and Line B signals only).
Equipment Supplied:	1 - 53A-425 Quad ARINC-429 Transmitter Card. 1 - Spare fuse (Part #42202-52001). 1 - Spare fuse (Part #42202-52004). 1 - Operating Manual (Part #00000-14250). 1 - Service Manual (Part #00000-24250).

DATA-TRANSMISSION FORMAT

Data output to a channel on the 53A-425 Card is organized into frames. Each frame consists of a single header word followed by one or more ARINC data words. Each header word or ARINC data word is four bytes long. The most significant bit of the fourth byte of each word specifies whether the word is a header word or an ARINC data word. A bit value of 1 specifies a header word; a bit value of 0 specifies an ARINC data word. A channel can receive multiple frames, limited only by the channel's RAM size of 32K words.

In this manual, as in other 53/63 Series System manuals, "input" refers to data flow from the 53/63 Series System to the system controller (calculator or computer); "output" refers to data flow from the system controller to the 53/63 Series System.

Header Word

The header word, which is output to an individual channel's memory as four 8-bit bytes, contains the control information listed below:

- The delay between the start of the current frame and the start of the next frame.
- Output transmission parity (odd or even).
- Output data-word length (31, 32 or 33 bits).
- Interword-gap time between data words in the current frame (two or four bit times).
- Whether to stop transmitting after the preceding frame's data has been transmitted, or to wrap around and continue transmitting from the top of memory.

NOTE: A frame with a header word, but no ARINC data words, is treated as if the frame contains data words, i.e., the frame time is still used as a delay time. The first word in a channel's memory must be a header word; otherwise, an error is returned, and the channel will not start transmitting.

Figure 425-1 shows the format of a header word.

First output byte:

Bit Position	7	6	5	4	3	2	1	0
Data	T3	T2	T1	T0	X	X	X	X

Second output byte:

Bit Position	7	6	5	4	3	2	1	0
Data	T11	T10	T9	T8	T7	T6	T5	T4

Third output byte:

Bit Position	7	6	5	4	3	2	1	0
Data	STOP	TMWRP	INT	X	IWG	LEN33	LEN31	EVNPAR

Fourth output byte:

Bit Position	7	6	5	4	3	2	1	0
Data	1	0	0	0	0	0	0	0

X = Don't care.

A bit value of 1 means "high" or true.

A value of 1 in bit 7 of the fourth output byte means that this 4-byte word is a header word.

Figure 425-1: Header-Word Format for the 53A-425 Card

T0-T11

Bits T0 through T11 are the data for the frame's delay time. Each frame's delay time is the time between the start of that frame and the start of the next frame. Setting particular T bits true causes the sum of the delay times for those bits to become the frame's delay time.

T Bit	Delay Time (ms)
0	1
1	2
2	4
3	8
4	16
5	32
6	64
7	128
8	256
9	512
10	1024
11	2048

The maximum delay time which can be programmed (all T bits = 1) is 4.095 s; the minimum delay time is 5 ms. If a delay time of less than 5 ms is programmed for a frame, that frame's delay time automatically defaults to 5 ms.

NOTE: If the time required to transmit the ARINC data within a frame exceeds that frame's delay time, an error will be generated (error code Y6, Delay-time error), and transmission will cease on the affected channel.

STOP

If the STOP bit is set, the channel stops transmitting after the preceding frame has been transmitted. If the first header word in a channel's memory has the STOP bit set, the channel will not transmit, and interrupts will not be returned.

TMWRP

If the TMWRP (top-of-memory wrap) bit is set, the channel will continue transmitting from the top of memory. Data words following a header word whose TMWRP bit is set will be ignored.

INT

If the INT bit is set, then at the start of the current frame, a 53/63 Series System backplane interrupt is generated; this assumes that interrupts have been enabled previously with the I (Interrupt) command. For a discussion of 53/63 Series System backplane interrupts, see the @XS command in the 53A-171 Control Card Operating Manual. Depending on the type of communications card installed in the 53/63 Series System, a backplane interrupt will also generate an interrupt back to the system controller. In the case of a 53A-128 Communications Card, for example, a backplane interrupt generates an SRQ (service request) on the IEEE-488 bus.

IWG

IWG specifies the interword-gap time between the current frame's ARINC data words:

IWG = 0 specifies four bit times between words; this is the normal interword-gap time for an ARINC data word.

IWG = 1 specifies two bit times between words.

LEN33, LEN31

LEN33 and LEN31 specify the length of the current frame's ARINC data words:

LEN33	LEN31	
0	0	32-bit word selected. This is the length of a normal ARINC data word.
0	1	31-bit word selected.
1	0	33-bit word selected.
1	1	Illegal value.

NOTE: When a 33-bit word is selected, bit 32 will be output as a 0, and bit 33 will be the parity bit. When a 31-bit word is selected, bit 31 will be the parity bit.

EVNPAR

EVNPAR specifies the parity of the current frame's ARINC data words:

EVNPAR = 0 specifies odd parity; this is the normal ARINC parity.

EVNPAR = 1 specifies even parity.

ARINC Data Word

Each 32-bit ARINC data word is stored as four 8-bit bytes. The order in which each byte is transmitted and the ARINC data bits contained in each byte are shown in Figures 425-2a and 425-2b.

First output byte:

Bit Position	7	6	5	4	3	2	1	0
ARINC Data Bits	1	2	3	4	5	6	7	8
Label	Most significant bit to least significant bit							

Second output byte:

Bit Position	7	6	5	4	3	2	1	0
ARINC Data Bits	16	15	14	13	12	11	10	9
Least Sig. Data Byte	Most significant bit to least significant bit							

Figure 425-2a: Transmission Order for ARINC Data Words (Bytes 1 and 2)

Third output byte:

Bit Position	7	6	5	4	3	2	1	0
ARINC Data Bits	24	23	22	21	20	19	18	17
Mid Sig. Data Byte	Most significant bit to least significant bit							

Fourth output byte:

Bit Position	7	6	5	4	3	2	1	0
ARINC Data Bits	32	31	30	29	28	27	26	25
Most Sig. Data Byte	Value = 0	Most significant bit to least significant bit.						

Figure 425-2b: Transmission Order for ARINC Data Words (Bytes 3 and 4)

BITS 1 THROUGH 8

Bits 1 through 8 of an ARINC word are assigned as the word label by ARINC Specification 429.

BITS 31 THROUGH 9

Bits 31 through 9 of an ARINC word are assigned as data by ARINC Specification 429.

BIT 32

Bit 32 of an ARINC data word (bit 7 of the fourth output byte) must be set to 0 to indicate to the 53A-425 Card that this is an ARINC data word and not a header word. Bit 32 of the ARINC data word is assigned as the parity bit by ARINC Specification 429, but it is not necessary for the system controller to output a parity bit to the 53A-425 Card. The 53A-425 Card will generate the parity bit in the hardware; the generated parity bit is based on the parity defined in the frame's header word.

ARINC-429 Bus Data Transmission Order

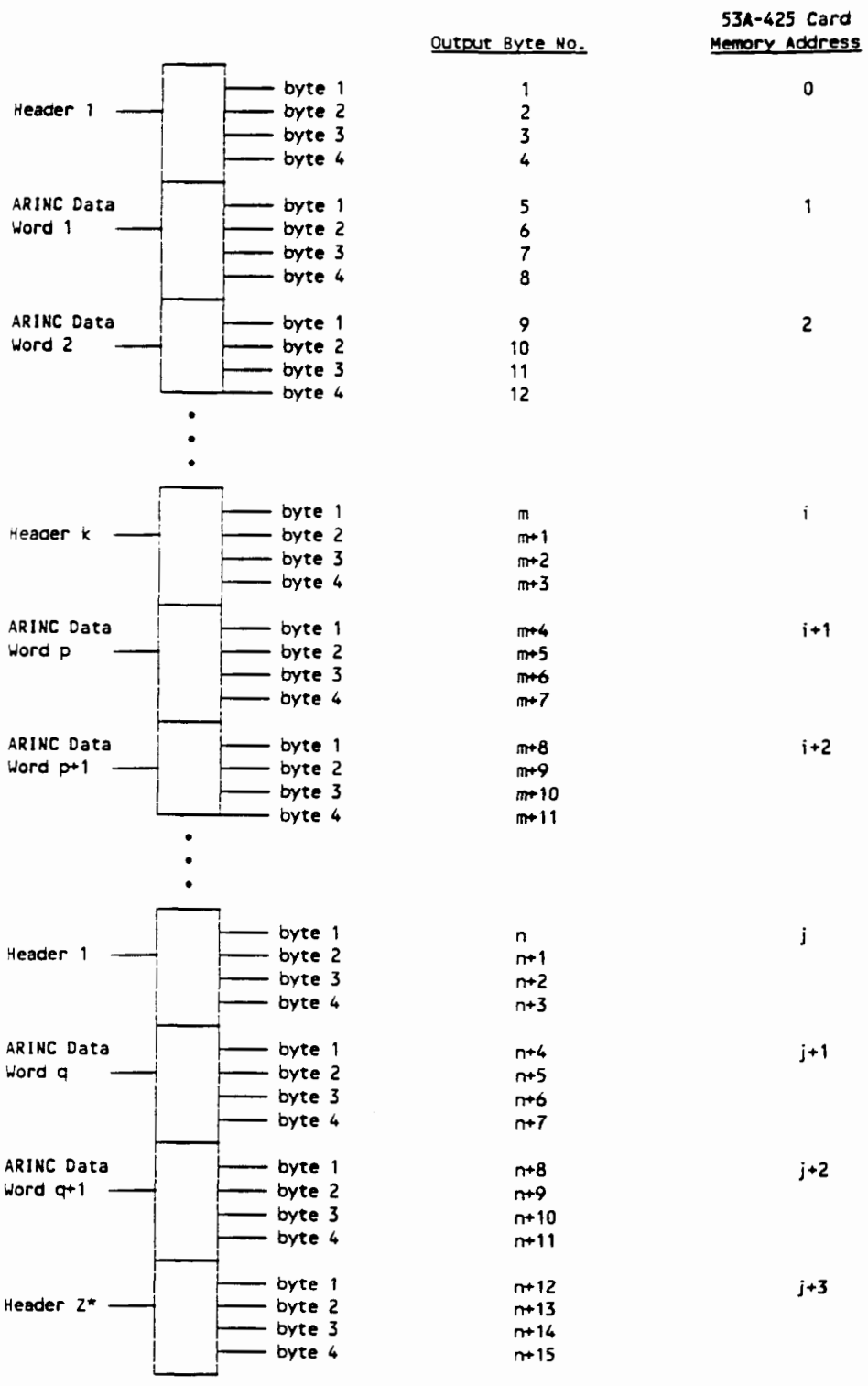
The order in which the system controller sends the ARINC data word's bytes to the 53A-425 Card and the order of the bits in each byte are based on the needs of the programmer and the requirements of ARINC Specification 429. The order in which data is transmitted on the ARINC-429 bus is ARINC data bit 1 first, bit 2 second, ..., and bit 32 last.

Looking at how the four output bytes are defined in Figures 425-2a and 425-2b above; bytes 1, 2, 3, and 4 are transmitted in that order. The most significant bit of byte 1, as output by the system controller, is transmitted first; the least significant bit of each of the other three bytes is transmitted first. This is because ARINC Specification 429 requires the order of transmission to be the label with the most significant bit first, followed by 24 bits of data with the least significant bit first.

The 53A-425 Card is designed to transmit the bits in the proper order, but to allow loading of the memory on the card with a label and data as they would be stored in the user's computer; i.e., the most significant bit of the label and of each data byte is the most significant bit as sent from the system controller to the card. This saves the programmer from having to write a routine to reverse the bit order of the label before it is sent to the 53A-425 Card.

System Controller-to-Card Data Transmission Order

Data is sent to the 53A-425 Card in four 8-bit bytes as either a header word or an ARINC data word. The order in which the bytes are sent to the 53A-425 Card is shown in Figure 425-3.



*Header Z must be present, and either the STOP bit or the TMWRP bit must be set true. If Header Z is not present, the resulting operation is undefined.

Figure 425-3: Order of Data Transmission from System Controller to Card

"On-the-fly" Updates

Internal to the 53A-425 Card, ARINC-429 data words are moved from the main memory in 8-ARINC-word blocks to a separate, high-speed, 16-ARINC-word, FIFO memory prior to transmission on the DITS data bus. The ARINC data words and frame headers contained in main memory can be updated "on the fly" (while the 53A-425 Card is transmitting); these updates are limited by the following considerations:

1. Updates to the frame header currently being transmitted are not effective until the next pass through the transmission list.

2. Updates to the first eight ARINC data words of a frame that is within 5 ms of being transmitted are not sent on the bus until the next pass through the transmission list.

3. Updates to the next eight ARINC data words of the frame currently being transmitted are not sent on the bus until the next pass through the transmission list.

4. The header word following a frame whose last data word has already been transmitted cannot be changed to an ARINC data word.

When updating a channel's memory "on the fly", there are two ways of determining where the channel is in its transmission sequence:

1. Requesting input from the 53A-425 Card automatically provides the next memory address to be accessed by the selected channel; the address is always five ASCII digits with leading 0's. This feature is available at all times except when an error-code return is requested (see OPERATION section, E command).

2. The INT bit in the header can generate an interrupt to the system controller at the start of any user-selected frame.

OPERATION

Overview

The 53A-425 Card is programmed by ASCII characters issued from the system controller to the 53/63 System's communications card. The 53A-425 Card is interfaced to the communications card through the 53 Series or 63 Series Card Cage's backplane.

To address a function card for the first time, the system command @XY must be issued. X is the card cage address (0-9) selected on the 53A-171 Control Card in the addressed card cage; Y is the 53A-425 Card's address (0-9) within the addressed card cage. The 53A-425 Card's address is selected using the card's Address-select switch. Once a function card is addressed, it remains addressed until the system receives another @ character. Appendix A fully discusses the @XY command and the other 53/63 Series System commands. After the 53A-425 Card is addressed, individual card commands may be issued until another function card is addressed.

Actual programming of the 53A-425 Card is organized as follows:

One of the four ARINC-429 channels is selected for programming using the S (Select) command. After the S command is issued, all subsequent commands apply to the selected channel until another channel is selected.

R (Rate) and V (Voltage) commands are issued next in order to set the ARINC-429 data rate and output signal's voltage level.

An A (Address) command is issued next in order to define the starting address in the selected channel where header and ARINC-429 data words will be loaded. Following the A command, an L (Length) command is issued to inform the 53A-425 Card how many header and ARINC-429 data words are to be loaded into memory.

Header and ARINC-429 data words are then sent to the card, followed by a B (Begin) command to start ARINC-429 data transmission.

Additional card commands are available to stop data transmission (K and Q commands), restart data transmission (C command), enable or disable 53/63 Series System interrupts (I command), read back error status (E command), or retrieve contents of the user-loaded, on-card memory (M command).

Appendix D provides a sample BASIC program for loading and transmitting ARINC-429 data.

Summary

An overview of the commands, listed alphabetically), is as follows:

A Address - sets an address in the selected channel's memory where the frame headers and ARINC data are to start being loaded, or the memory address from where the M (Memory) command is to start reading back message RAM.

B Begin - starts transmission on a single channel or on all four channels.

C Continue - continues transmission on a single channel after a STOP bit has been encountered in a header word.

E Error - prepares the 53A-425 Card to return programming or hardware error codes to the system controller on its next request for input from the card.

I Interrupt - enables or disables the generation of 53/63 Series System interrupts.

K Kill - stops transmitter operation, and returns the 53A-425 Card to its power-up state.

L Length - specifies the number of header or ARINC data words to be transferred to the selected channel's memory.

M Memory - used to retrieve data previously loaded into the selected channel's memory.

Q Quit - stops transmission on a single channel, or on all channels, after a maximum of 17 words is sent by each transmitter.

R Rate - specifies the period (in nanoseconds) of the bit-rate clock for the selected channel.

S Select - selects the active channel for future commands.

T Test - performs a functional self test of the complete 53A-425 Card.

V Voltage - specifies the output voltage level (normal, parametric high, parametric low, or parametric null) for the selected channel's transmitter.

Card Commands

Detailed descriptions of the 53A-425 Card's commands, in the same order as listed above, are as follows:

Command	Description
[addr]A	The A (Address) command sets an address in the selected channel's memory where the frame headers and ARINC data are to start being loaded, or the memory address from where the M (Memory) command is to start reading back message RAM. The selected channel is the last channel specified by an S (Select) command. The A command is required only at the beginning of a data transfer. The 53A-425 Card automatically increments the address after every word is transferred. [addr] is a 1- to 5-digit decimal integer, from 0 to 32767, that specifies the current memory address for the selected channel. If [addr] is omitted, the address is set to 0 (first word in memory). A 53A-425 Card memory location is 32 bits wide and contains one complete header word or ARINC data word. *NOTE:* The first header word loaded and its associated ARINC data words must start at memory address 0, and be contiguous. If they are loaded into noncontiguous memory locations, the random data in the nonprogrammed locations will be transmitted on the ARINC-429 bus. A word is defined as 32 bits or four bytes. Data loading always begins with byte 1 of a word. Examples: 1. 14000A programs the memory address of the selected channel to 14000. 2. For the example shown in Figure 425-3, the command 2A starts data loading with ARINC Data Word 2. Data following ARINC Data Word 2 are loaded into the next consecutive memory addresses.

Command	Description
[chan]B	The B (Begin) command starts transmission on a single channel or on all four channels.

[chan] is a 1-digit decimal integer that specifies the following:

[chan]	Begin Transmission on Channel(s)
0	1-4
1	1
2	2
3	3
4	4

If [chan] is omitted, transmission starts on all four channels. The B command has no effect on channels already transmitting.

Examples:

1. 4B starts transmission on channel 4.

2. 0B (or simply B) starts transmission on all four channels.

Command	Description
[chan]C	The C (Continue) command continues transmission on a single channel after a STOP bit has been encountered in a header word.

[chan] is a 1-digit decimal integer that specifies the following:

[chan]	Continue Transmission on Channel
1	1
2	2
3	3
4	4

If a C command is issued for a channel which has not encountered a STOP bit in a header word, the command has no effect on that channel.

Internal to the 53A-425 Card, data for each channel is moved from main memory in blocks of eight ARINC words to a separate, 16-ARINC-word, high-speed, First In/First Out (FIFO) memory which drives a given channel's DITS data bus. Once a channel has halted transmission due to encountering a header word's STOP bit, a C command should not be issued until the FIFO memory has emptied. To determine when to issue the C command, proceed as follows:

1. Select the desired channel using an S command, and request input from the card. The address of the current memory locations being processed will be returned.

2. When the returned current memory location is equal to the location of the header word containing the STOP bit, then wait for 576 times the programmed bit rate before issuing the C command.

Command	Description
E	The E (Error) command prepares the 53A-425 Card to return programming or hardware error codes to the system controller on its next request for input from the card. Each returned error code consists of two ASCII characters followed by <CR><LF>. After an E command is initiated, the 53A-425 Card continues to return error codes on each input request from the system controller until 99 (no additional errors to report) is returned. Additional requests for input, after error code 99 is returned, cause the address of the last transmitted word from the last selected channel to be returned. If an E command is issued and no errors are found, only error code 99 is returned. Because the error buffer can store a maximum of 16 errors, only the first 16 errors are returned; any additional errors are lost. Errors are returned in reverse order; i.e., the last error encountered is returned first, and the first error encountered is returned last. See Appendix C for a list of returned error codes and error-code formats.

Command	Description
[ena]*I*	The I (Interrupt) command enables or disables the generation of 53/63 Series System interrupts. The 53A-425 Card interrupts to indicate the start of transmission of a frame with the INT bit set in the frame's header word. After an interrupt occurs, it is latched by the 53A-425 Card, and will continue to generate a 53/63 Series System interrupt until the interrupt status of the 53/63 Series System is checked using the @XS command described in Appendix A.

[ena] is a 1-digit decimal integer that specifies the following:

[ena]	Action
0	Interrupts are disabled.
1	Interrupts are enabled.

Programming Caution:

When the applications program enters its interrupt handler and executes the @XS command, the handler should readdress the card cage immediately after receiving a colon (:). The following BASIC program illustrates one way to do this:

```
1000 REM INTERRUPT HANDLER
1010 PRINT "@1S"
1020 INPUT A$
1030 IF A$ = "1" GOTO 1100
1040 IF A$ <> ":" GOTO 1020
1050 PRINT "@1"
1060 RETURN
1100 REM 425 INTERRUPT HANDLER
      .
      .
      .
```

If the 53/63 Series System's card cage is not readdressed following the @XS command, subsequent interrupts from the 53A-425 Card may be lost.

Command	Description
K	The K (Kill) command stops transmitter operation, and returns the 53A-425 Card to its power-up state. The ARINC transmitters immediately stop, regardless of how far the transmissions have progressed or how much data is in each transmitter's First In/First Out (FIFO) memory. This command also resets any errors and clears the Error LED.

Command	Description
[len]L	The L (Length) command specifies the number of header or ARINC data words to be transferred to the selected channel's memory. The selected channel is the last channel specified by an S (Select) command.

[len] is a 1- to 5-digit decimal integer, from 1 to 32768, that specifies the number of header words and ARINC data words to be sent to the selected channel's message RAM.

After the L command is received, the 53A-425 Card sets the 53/63 Series System's backplane interface to the binary mode; all data output to the 53A-425 Card, after the L command, is treated as binary data and immediately stored in the selected channel's message RAM. Therefore, any <CR> and <LF> characters that might be sent by the system controller after the L command, as part of a "normal" output statement, must be suppressed; if they are not suppressed, they will be stored in message RAM as part of the channel's message data!

If an error is detected within the L command, the 53A-425 Card will purposely "hang up" the system controller. This is done to prevent binary data, following the L command, from being transmitted on the backplane and possibly being interpreted as ASCII data; e.g., binary 01000000 might be interpreted as the ASCII @ character, and cause another card to be addressed.

Example:

1000L sets the number of header and ARINC data words to be received by the selected channel to 1,000 words. Each of the 1,000 header or ARINC data words is sent by the system controller as four separate 8-bit bytes. The next character received, after the L character, is assumed to be a header or ARINC data word, and is stored in message RAM.

Command	Description
[len]M	The M (Memory) command is used to retrieve data previously loaded into the selected channel's memory. The selected channel is the last channel specified by an S (Select) command. The command specifies the number of 4-byte words to be transferred from the selected channel's memory to the system controller. After issuing the M command, the 53A-425 Card expects the system controller to request four bytes of input for each of the number of words specified in the M command. [len] is a 1- to 5-digit decimal integer, from 1 to 32768, that sets the number of 4-byte words to be transferred. After the M command is received, the 53A-425 Card sets the 53/63 Series System's backplane interface to binary mode on each occurance of an input request. Any data output to the 53A-425 Card, after the M command is issued, will cause the card to terminate the M command. Therefore, any terminating <CR> or <LF> characters sent by the system controller after the M command, as part of a "normal" output statement, must be suppressed; if they are not suppressed, the 53A-425 Card will terminate the M command, and returned data will be the current transmission address of the selected channel. If an error is detected within an M command, the 53A-425 Card will not complete the M command; the backplane will not go into binary mode, and all returned data will consist of the current transmission address of the selected channel. Following the last 4-byte data word returned to the system controller, terminating <CR> and <LF> characters will be sent to the system controller by the card.

Command	Description

[chan]Q

The Q (Quit) command stops transmission on a single channel, or on all channels, after a maximum of 17 words is sent by each transmitter. The Q command causes an asynchronous stopping of transmission at the end of a complete ARINC word, but in the middle of a frame. For a synchronous stopping of transmission at the end of a complete ARINC frame, the STOP bit should be set in a header word.

[chan] is a 1-digit decimal integer that specifies the following:

[chan]	Channel(s) Stopped
0	1-4
1	1
2	2
3	3
4	4

If [chan] is omitted, transmission stops on all four channels.

Internal to the 53A-425 Card, data for each channel is moved from main memory in blocks of eight ARINC words, to a separate, 16-ARINC-word, high-speed, FIFO memory which drives a given channel's DITS data bus. When a Q command is issued, the specified channel will not cease transmission until the FIFO memory associated with the channel has emptied. If a Q command is to be followed by a B command in order to restart transmission from the first word in memory, a time delay equal to 576 times the programmed bit rate should be placed between the issuance of the Q and B commands. Failure to do so will result in data transmission stopping in the middle of an ARINC word.

Examples:

1. 0Q stops transmission on all four channels.

2. 2Q stops transmission on channel 2.

Command	Description
[per]R	The R (Rate) command specifies the period (in nanoseconds) of the bit-rate clock for the selected channel. The selected channel is the last channel specified by an S (Select) command.

[per] is a 2- to 5-digit decimal integer, from 32 to 32767 (see Example 4 below for [per] = 00), that sets the bit-rate clock based on the following equation:

$$\text{bit-rate frequency (Hz)} = 1 / ([\text{per}] \cdot 10^{-9} \cdot 250)$$

The bit-rate clock for a given channel cannot be updated while the channel is transmitting; if this is attempted, no action is taken.

If there is an error in an R command and the selected channel is transmitting, no error is logged by the 53A-425 Card.

Examples:

1. 32R specifies a bit-rate frequency of 125 kHz (125 kb/s) for the selected channel.

2. 40R specifies a bit-rate frequency of 100 kHz (100 kb/s) for the selected channel.

3. 320R specifies a bit-rate frequency of 12.5 kHz (12.5 kb/s) for the selected channel.

4. The special case 00R (or simply R) sets the bit rate for the selected channel to the external bit-rate clock. Before issuing 00R, the transmitter's bit-rate clock should first be set to an internal bit rate that gives the proper rise and fall times according to the 53A-425 Card's specifications.

Command: F (Select Trigger Output)

Syntax: [chan][ftrg][VXItrg]F

Purpose: The F (Select Trigger Output) command specifies the front-panel and/or VXIbus TTL trigger line to be used as the output trigger line(s) for the specified channel(s).

Description:

[chan] a 1-digit decimal integer from 0 to 4 that specifies the channel(s) affected by the F command. Zero or no parameter specifies all channels.

[ftrg] a 1-digit decimal integer from 1 to 4 that specifies the front-panel trigger line to be used as the trigger output for the channel(s) defined by [chan].

[ftrg]	Trigger line Selected
1	Front-panel Trigger 1
2	Front-panel Trigger 2
3	Front-panel Trigger 3
4	Front-panel Trigger 4

If any other value other than those listed above are used for the [ftrg] parameter, the front-panel trigger lines will be disconnected from the channel(s) defined by [chan].

[VXItrg] a 1-digit decimal integer from zero to 6 that specifies the VXIbus TTL trigger line to be used as the trigger output for the channel(s) defined by [chan].

[VXItrg]	Trigger line Selected
0	VXIbus TTL Trigger 0
1	VXIbus TTL Trigger 1
2	VXIbus TTL Trigger 2
3	VXIbus TTL Trigger 3
4	VXIbus TTL Trigger 4
5	VXIbus TTL Trigger 5
6	VXIbus TTL Trigger 6
7	VXIbus TTL Trigger 7

If any other value other than those listed above are used for the [VXItrg] parameter, the VXIbus TTL trigger lines will be disconnected from the channel(s) defined by [chan].

Examples:

1. The command sequence 101F selects the VXIbus trigger line 1 as the output trigger line for channel 1 and disconnects all front panel trigger lines from channe 1.

2. The command sequence 011F (or 11F) selects the front-panel trigger line 1 and VXIbus TTL trigger line 1 as the output trigger lines for all channels.

Errors: A Syntax error will result if an out-of-range value is specified for [chan] or if the number of characters for the [chan], [ftrg], and [VXItrig] parameters exceed 3 characters.

If a Syntax error is generated when the command is received, the command will be ignored.

Command	Description
T	The T (Test) command performs a functional self test of the complete 53A-425 Card. For each channel, message RAM is fully tested, the output transmitters are looped back to a processor input port and checked prior to the final differential drive amplifiers, and the channel counter/timers are tested. After this test is performed, all data stored in message RAM is lost, and the card returns to its power-up state. The error code for any errors found during self test can be read back using the E (Error) command. This test takes approximately 45 seconds to perform. Any characters received by the 53A-425 Card, following the T command, will not be processed until self testing of the card is complete. To avoid appearing to "hang up" the system controller during the self test period, any terminating <CR> or <LF> characters "normally" output by the system controller, following the T command, should be suppressed.

Command	Description
[lev]V	The V (Voltage) command specifies the output voltage level (normal, parametric high, parametric low, or parametric null) for the selected channel's transmitter. The selected channel is the last channel specified by an S (Select) command.

[lev] is a 1-digit decimal integer, from 0 to 3, that specifies the following:

[lev]	Action
0	Normal ARINC-429 data levels
1	Parametric high
2	Parametric low
3	Parametric null

The output voltage level cannot be updated while the 53A-425 Card is transmitting ARINC-429 data.

Normal ARINC-429 data levels and parametric high, low, and null data levels are defined in the SPECIFICATIONS section of this manual.

INSTALLATION

The 53A-425 Card is a function card; therefore, it may be plugged into any blue card slot. Setting the Address Select switch defines the card's programming address. To avoid confusion, it is recommended that the slot number and the programming address be the same.

CAUTION:

To avoid plugging the card in backwards, observe the following:

a. Match the keyed slot on the card to the key in the backplane connector. The component side should be to the right for a 53 Series Chassis and to the top for a 63 Series Chassis.

b. There are two ejectors on the card. Make sure the ejector marked "53A-425" is at the top for a 53 Series Chassis and to the left for a 63 Series Chassis.

CAUTION:

The 53A-425 Card is a piece of electronic equipment and therefore has some susceptibility to electrostatic damage (ESD). ESD precautions must be taken whenever the module is handled.

APPENDIX A

53/63 SERIES SYSTEM COMMANDS

Command	Description
@XY	The @XY (Address) command addresses a function card in the 53/63 Series System. @ is a delimiter used by the 53/63 Series System. X is a card cage address (0-9) defined by the Address-select Switch on the 53A-171 Control Card in the addressed card cage. Y is a function-card address (0-9) defined by the Address-select Switch on the function card. Once a card cage/function-card combination is addressed, it remains addressed until the 53/63 Series System detects a new @ character.
@XS	The @XS (Status) command provides the interrupt status of all function cards within the mainframe defined by X. The mainframe backplane interrupt status of all function cards in the addressed mainframe is latched into the 53A-171 Control Card when the @XS command is issued. The 53A-425 Card has interrupt capability that indicates, under program control, the start of selected frames. All function cards in all mainframes become unaddressed after the @XS command. The 53A-171 Control Card Operating Manual describes the @XS command in detail.
@XH	The @XH (Halt) command halts all function cards within the card cage defined by X. The command does not affect function cards in other card cages. How a function card reacts to the @XH command depends on the card. In all cases, an addressed function card (Power LED out) becomes unaddressed (Power LED lit). On the 53A-425 Card, the position of the Halt Switch determines the @XH command's effect: 1. If the Halt Switch is in the ON position, the 53A-425 Card resets to its power-up state. 2. If the Halt Switch is in the OFF position, the 53A-425 Card is simply unaddressed.
STOP	The STOP command is not a string of ASCII characters. The command is hard-wired from the system controller (calculator or computer) to the 53/63 Series System communications card in each mainframe. When the system controller issues a STOP command, each function card, including the 53A-425 Card, reacts as if it received the @XH command described above. How the system controller executes the STOP command depends on the communications card used. With the 53A-128 IEEE-488 Card, for example, a STOP command is executed when the system controller asserts the IEEE-488 bus line IFC (Interface Clear) true.

APPENDIX B

FRONT-EDGE-CONNECTOR PIN ASSIGNMENTS

Pin No.	Function
1	CHANNEL 1 LINE A
2	CHANNEL 1 LINE B
4	CHANNEL 1 EXT CLK IN
5	CHANNEL 1 FRAME TRANSMITTING
7	CHANNEL 2 LINE A
8	CHANNEL 2 LINE B
10	CHANNEL 2 EXT CLK IN
11	CHANNEL 2 FRAME TRANSMITTING
13	CHANNEL 3 LINE A
14	CHANNEL 3 LINE B
16	CHANNEL 3 EXT CLK IN
17	CHANNEL 3 FRAME TRANSMITTING
19	CHANNEL 4 LINE A
20	CHANNEL 4 LINE B
22	CHANNEL 4 EXT CLK IN
23	CHANNEL 4 FRAME TRANSMITTING
24	GROUND
A	GROUND
B	CHANNEL 1 CLOCK OUT
C	CHANNEL 1 SYNC OUT
D	CHANNEL 1 NRZ DATA OUT
E	CHANNEL 1 DATA CLOCK OUT
F	GROUND
H	GROUND
J	CHANNEL 2 CLOCK OUT
K	CHANNEL 2 SYNC OUT
L	CHANNEL 2 NRZ DATA OUT
M	CHANNEL 2 DATA CLOCK OUT
N	GROUND
P	GROUND
R	CHANNEL 3 CLOCK OUT
S	CHANNEL 3 SYNC OUT
T	CHANNEL 3 NRZ DATA OUT
U	CHANNEL 3 DATA CLOCK OUT
V	GROUND
W	GROUND
X	CHANNEL 4 CLOCK OUT
Y	CHANNEL 4 SYNC OUT
Z	CHANNEL 4 NRZ DATA OUT
AA	CHANNEL 4 DATA CLOCK OUT
BB	GROUND

A description of each of the front-edge-connector signals is given below:

CHANNEL n LINE A (pins 1, 7, 13, 19)

These are the analog output signals for direct connection to the ARINC-429 bus, line A.

CHANNEL n LINE B (pins 2, 8, 14, 20)

These are the analog output signals for direct connection to the ARINC-429 bus, line B.

CHANNEL n EXT CLK IN (pins 4, 10, 16, 22)

These signals let the user vary the bit rate for channel n on the ARINC-429 bus by supplying an external, TTL, clock signal. The external clock's frequency may vary between 0 Hz and 125 kHz. The duty cycle of the clock input must be 50% ± 2.5%.

CHANNEL n FRAME TRANSMITTING (pins 5, 11, 17, 23)

These outputs are TTL-level signals that indicate when a channel frame is actually being transmitted over the ARINC-429 bus. These signals go low at the beginning of a frame's transmission, and return high at the end of the frame's transmission.

CHANNEL n CLOCK OUT (pins B, J, R, X)

These TTL-level signals are free-running clocks at the ARINC-429 data-transmission bit rate and are intended for use with the 53A-427 ARINC-429/561 Converter Card as the XMIT Data Clock Inputs to the 53A-427 Card.

CHANNEL n SYNC OUT (pins C, K, S, Y)

These TTL-level signals go high at the beginning of each ARINC-429 word transmission and return low when the last bit of the ARINC word is transmitted. They are intended for use with the 53A-427 ARINC-429/561 Converter Card as the Sync Signal Inputs to the 53A-427 Card.

CHANNEL n NRZ DATA OUT (pins D, L, T, Z)

These TTL-level signals provide the ARINC-429 output data in NRZ, high-true format. Data on these lines is valid on the falling edge of Channel n Data Clock Out. The signals are intended for use with the 53A-427 ARINC-429/561 Converter Card as the DITS Word Inputs to the 53A-427 Card.

CHANNEL n DATA CLOCK OUT (pins E, M, U, AA)

These TTL-level signals provide clocks for strobing Channel n NRZ Data Out. A single output pulse occurs for each NRZ data bit. These signals are intended for use with the 53A-427 ARINC-429/561 Converter Card as the Data Clock Inputs to the 53A-427 Card.

In the above signal names, "n" represents a channel number (1 through 4). The pins noted in parentheses, following each signal name, correspond to channels 1 through 4, respectively.

APPENDIX C

ERROR CODES

Each error code is returned as two ASCII characters followed by <CR> and <LF> characters.

Fatal Errors

Fatal errors cause the 53A-425 Card to disable the ARINC transmitter outputs. The 53A-425 Card will then accept commands from the system controller, but will not perform functions for any commands except the @XH command and the STOP command. Any input from the card will return only the error code for the fatal error.

Error Code		
Char 1	Char 2	Description
0	0	Message-RAM failure
0	1	Stack-RAM failure
0	2	Interrupt-controller failure
0	3	(Reserved)
0	4	General hardware failure

Nonfatal Errors

Nonfatal errors do not cause the 53A-425 Card to totally suspend its operations. However, a hardware error within a channel permanently disables transmission from that channel until the error is cleared.

Error Code		
Char 1	Char 2	Description
X	0	Unrecognized command
X	1	Invalid parameters (includes a value out of bounds)

X = Number of channel selected when error occurred.

Error Code		
Char 1	Char 2	Description
Y	2	Frame-header error
Y	3	ARINC-transmitter error (hardware error)
Y	4	Time-base error (hardware error)
Y	5	Reserved
Y	6	Delay-time error (Frame's delay-time is too short)
9	9	No additional errors to report.

Y = Number of channel in which error occurred

APPENDIX D

SAMPLE BASIC PROGRAM

FOR LOADING AND TRANSMITTING ARINC-429 DATA

The sample program below is written in Advanced BASIC (BASICA) for an IBM PC. The PC is connected to the CDS card cage using a 53A-903 I/O Card installed in the PC. The 53A-903 I/O Card provides an IEEE-488 interface between the PC and the CDS card cage. The 53A-425 Card has been set to address 9. The address of the 53/63 Series System card cage containing the 53A-425 Card is address 1.

The sample program loads two frames of data into the 53A-425 Card. Each frame contains two identical ARINC-429 words. Following the second frame of data, a third header word is loaded to cause the 53A-425 Card to "wrap" back to the beginning of memory and continue transmission.

Line numbers 1000 through 1070 define the ARINC-429 header and data words to be sent to the 53A-425 Card at line 1080. The CALL statements at lines 1080 and 1100 transfer the contents of the string variable WRT$ to the 53A-425 Card.

Sample BASIC Program

In this program listing, lines which are not preceded by a line number (except for the one following 1070) are not part of the BASIC program. They are inserted here as comments to explain what the program is doing at each numbered line.

```
.
.
.

1000 HEADER$ = CHR$(0) + CHR$(192) + CHR$(0) + CHR$(128)
     HEADER$ is a 4-byte string used to define the frame's header word.
          Bytes 1 and 2 set the frame's delay time to 3.096 seconds.
          Byte 3 defines the following:
               - Stop bit is not set.
               - Top-of-memory wrap is not set.
               - Interrupt bit is not set.
               - Interword gap is set to 4 bit times.
               - Word length is set to 32 bits.
               - Parity is set to odd.
          Byte 4 defines this word as a header word.

1010 WHEADER$ = CHR$(0) + CHR$(0) + CHR$(64) + CHR$(128)
     WHEADER$ is a 4-byte string which defines a wrap-to-top-of-memory header word.
          Bytes 1 and 2 are ignored; they are not used in a wrap header word.
          Byte 3 defines the following:
               - Stop bit is not set.
               - Top-of-memory wrap is set.
               - Interrupt bit is not set.
               - Interword gap is not set; it is unused in a wrap header word.
```

- Word length is not set; it is unused in a wrap header word.
- Parity is not set; it is unused in a wrap header word.

Byte 4 defines this word as a header word.

```
1020 LABEL1 = 8
1030 LABEL2 = 37
1040 ARINCD1$ = CHR$(LABEL1) + CHR$(16) + CHR$(212) + CHR$(9)
1050 ARINCD2$ = CHR$(LABEL2) + CHR$(192) + CHR$(20) + CHR$(5)
```

ARINCD1$ and ARINCD2$ are 4-byte strings defining the ARINC data:

Byte 1 is the ARINC label; LABEL1 (distance to go) is for string variable ARINCD1$, and LABEL2 (time to go) is for string variable ARINCD2$. Bytes 2, 3, and 4 are the ARINC data bytes. String variable ARINCD1$ contains a distance of 2750.4 nautical miles, and string variable ARINCD2$ contains a time of 145.3 minutes as taken from Attachment 6 of the ARINC-429 specification.

```
1060 C$ = "@191S40R0A7L"
```

C$ is a string used to define commands to be sent to the 53A-425 Card.

- @19 is the @XY address command.
- 1S sets the selected channel to 1.
- 40R sets the bit-rate frequency on the selected channel (channel 1) to 100 kHz (100 kb/s).
- 0A sets a 53A-425 Card memory address of 0 at which to start loading the header word and ARINC data words for the selected channel (channel 1).
- 7L sets the number of header and ARINC data words to be loaded to 7.

```
1070 WRT$ = C$ + HEADER$ + ARINCD1$ + ARINCD1$ + HEADER$ + ARINCD2$ +
     ARINCD2$ + WHEADER$
1080 CALL IBWRT(CDS%,WRT$)
```

Output the contents of string variable WRT$ to the 53A-425 Card.

```
1090 WRT$ = "1B"
```

Start transmission on channel 1.

```
1100 CALL IBWRT(CDS%,WRT$)
```

Output the contents of string variable WRT$ to the 53A-425 Card.

•
•
•

SERVICE MANUAL

53A-425

QUAD UNIVERSAL ARINC-429 TRANSMITTER CARD

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form without the written permission of Colorado Data Systems, Inc.

REFERENCE DESIGNATOR	CDS PART NUMBER	QTY.	PART DESCRIPTION	MFG. NUM.	MFG. PART NUMBER
	425SA1	1	BOTTOM BOARD FOR 53A-425	0026	425SA1
	425SA2	1	TOP BOARD FOR 53A-425	0026	425SA2

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REFERENCE DESIGNATOR	CDS PART NUMBER	QTY.	PART DESCRIPTION	MFG. NUM.	MFG. PART NUMBER
C03,04,07,1031,1041,1071,1151 1171,13,14,17,23,24,27,331,332 34,35,41,43,46,53,57,661,662,73 74,77,81,83,97	20128-10006	31	CAP FXD CER .1UF 20% 50VDCW	0058	C322C104M5U5CA
C061,062	21528-20002	2	CAP FXD MICA 20PF 5% 500VDCW	0025	CD6ED200J03
C1072,1172	22022-20008	2	CAP FXD TA 22UF 10-20% 20-25VDCW	0106	199D226X9025CA1
C64	21018-15009	1	CAP FXD ELECT 150UF 75% -10% 16VDCW	0025	NLW150-16
C771	21528-75002	1	CAP FXD MICA 75PF 5% 500VDCW	0012	DM10-750J-500VDCW
C87	22022-10008	1	CAP FXD TA 10UF 10-20% 25VDC	0106	199D106X9025CA1
CR87	32000-04148	1	DIODE SILICON 75V 1A 5%	0078	1N4148
DS01	32000-00103	1	DIODE LIGHT EMITTING RED 50MA	0039	550-0406
DS11,12,13,14,15	32000-02003	5	DIODE LIGHT EMITTING RED WITH RESISTOR 0	0039	547-2003
E1	40401-00425	1	STAMP 53A-425 STYLE B BLUE	0026	40401-00425
E2	40401-10031	1	STAMP XMIT STYLE D BLUE	0026	40401-10031
E3	45050-03301	1	DCL LED 5POS DRW 00000-00598	0026	45050-03301
E4	45050-03240	1	DCL LED 5POS BLK DRW 00000 -00470	0026	45050-03240
F07	42202-52004	1	FUSE SUB-MIN 4 AMP OR 5 AMP	0061	251004 OR 251005
F1071,1171	42202-52001	2	FUSE SUB-MIN 2AMP	0061	251002
P07,52	45002-72040	2	CONNECTOR PC BRD MNT 40 PIN BLOCK HEADER	0044	FCN-724P040-AU-W
PCB	41530-42500	1	P.C. BOARD VERSION 6L 9201	0026	41530-42500
Q021,12	51100-03646	2	TRANSISTOR NPN HIGH SPEED SWITCH	0074	MPS3646

425SA1 BOTTOM BOARD FOR 53A-425

REV 9201-03-B

REFERENCE DESIGNATOR	CDS PART NUMBER	QTY.	PART DESCRIPTION	MFG. NUM.	MFG. PART NUMBER
Q022	51100-03906	1	TRANSISTOR PNP SWITCHING	0107	2N3906
R021,121,37	10117-10004	3	1K RES COMP 1-4W 5%	0087	R25J-1K-5%
R022	10117-33005	1	33K RES COMP 1-4W 5%	0087	R25J-33K-5%
R1011,322,521,823	14024-10005	4	10K RES FILM 1-4W 1% 100PPM	0035	RN55D1002F
R1012,1022,21,22,31,321,91,923	14024-37402	8	37.4 OHM RES FILM 1-4W 1% 100PPM	0035	RN55D37R4F
R1021,323,522,824	14024-29405	4	29.4K RES FILM 1-4W 1% 100PPM	0035	RN55D2942F
R122,56,61,711,712,77,81,871,872	10117-10005	9	10K RES COMP 1-4W 5%	0087	R25J-10K-5%
R123,66	10117-33003	2	330 OHM RES COMP 1-4W 5%	0087	R25J-330-5%
R124	10117-33004	1	3.3K RES COMP 1-4W 5%	0087	R25J-3.3K-5%
R13,14,36,46	12008-33004	4	3.3K RES NETWORK SIP 5% 1.5W 9-PKG	0027	750-101-R3.3K
R27,55	12004-33004	2	3.3K RES NETWORK SIP 5% .9W 5-PKG	0027	750-61-R3.3K
R341	10117-62002	1	62 OHM RES COMP 1-4W 5%	0087	R25J-62-5%
R342,343	10117-10003	2	100 OHM RES COMP1-4W 5%	0087	R25J-100-5%
R344	12001-91002	1	100 OHM RES NETWORK 5% 1-4W 8-PKG	0037	MDP1603-101G
R421,423,821,921	14024-20005	4	20K RES FILM 1-4W 1% 100PPM	0035	RN55D2002F
R422,424,822,922	14024-19605	4	19.6K RES FILM 1-4W 1% 100PPM	0035	RN55D1962F
S27	42050-10101	1	SWITCH DIP 1POS SPST	0093	JS-8794-01
S97	42050-10010	1	SWITCH 10POS.	0101	C42315-A61-A11
U03,04	73309-74245	2	IC HCT OCTAL BUS TRANSCEIVER	0107	74HCT245
U05,15,25	73005-74573	3	IC HCT TRISTATE OCTAL D-TYPE LATCH	0107	74HCT573
U07	79814-00082	1	PAL PROGRAMMED EP310-2 REV C 53A-425	0026	79814-00082

425SA1 BOTTOM BOARD FOR 53A-425

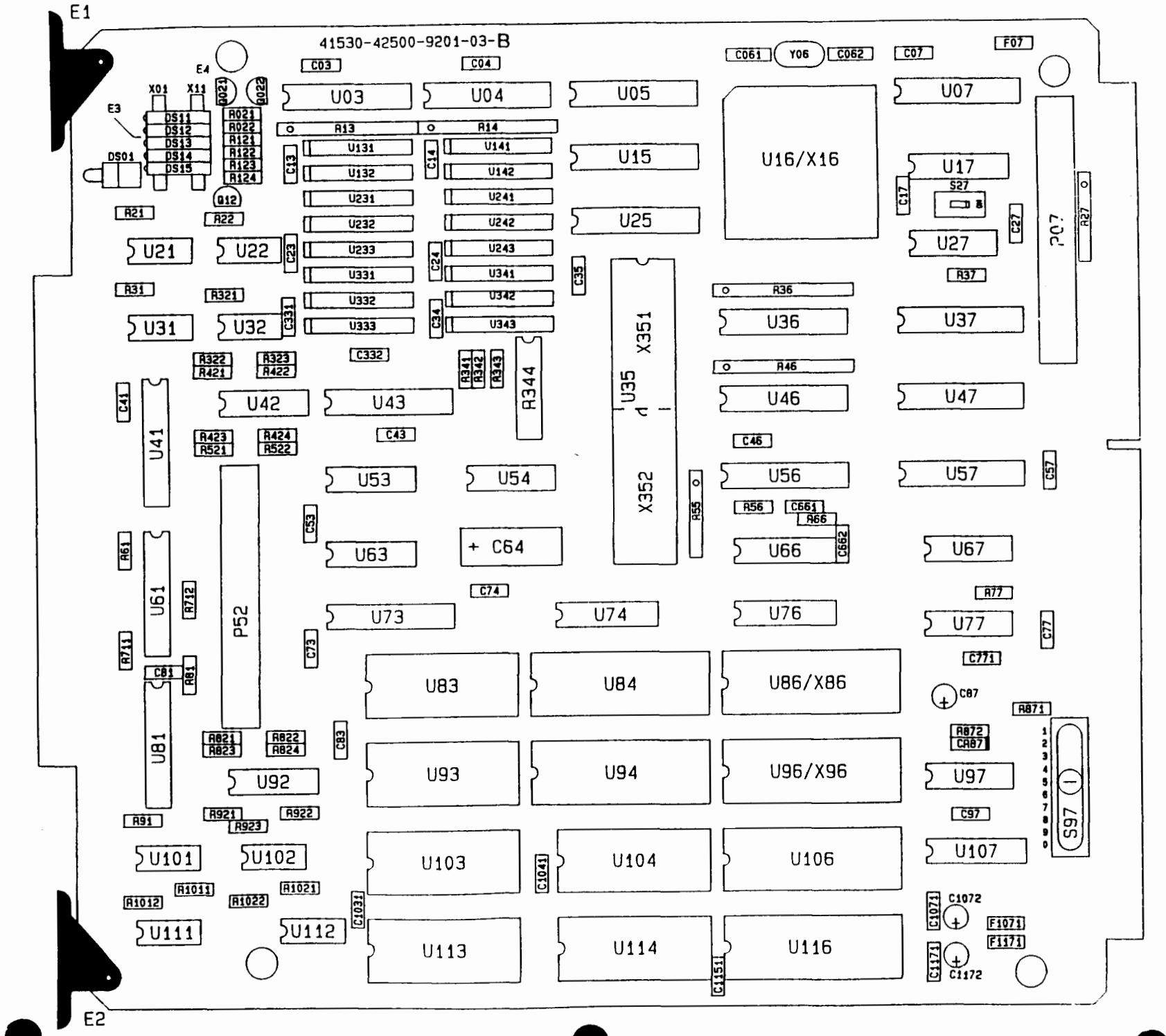
REV 9201-03-B

REFERENCE DESIGNATOR	CDS PART NUMBER	QTY.	PART DESCRIPTION	MFG. NUM.	MFG. PART NUMBER
U101,102,111,112,21,22,31,32	20102-00002	8	IC CURRENT AMPLIFIER	0078	LH0002CN
U103,104,113,114,83,93	79801-08254	6	IC CMOS PROGRAMMABLE INTERVAL TIMER	0051	CP82C54
U106,116	79805-06264	2	IC CMOS 8K X 8 SRAM 150NS	0401	HY6264P-15
U107,17	79008-74138	2	IC HCT 3-TO-8 LINE DECDR DEMULTIPLEXER	0107	74HCT138
U131,132,141,142,231,232,233,241 242,243,331,332,333,341,342,343	79805-50257	16	IC MOS 256K X 1 DRAM 150NS ZIP	0281	MT1259Z-15
U16	79801-80187	1	IC NMOS 80186 CPU LCC PLASTIC	0002	N80186
U27	73300-07406	1	IC TTL HEX INVERTER BUFFER-DRIVER	0107	7406
U35	79825-08208	1	IC CMOS DYN RAM CTL 10 MHZ	0118	82C08-10
U36,46	73308-74245	2	IC TTL ALS OCTAL BUS TRANSCEIVER	0107	74ALS245
U37	79814-00083	1	PAL PROGRAMMED EP310-2 REV B 53A-425	0026	79814-00083
U41	73310-74240	1	IC TTL LS OCTAL BUFFER	0107	74LS240
U42,92	61000-00347	2	OP AMP FET QUAD	0078	LF347
U43	79814-00123	1	PAL PROGRAMMED 16L8 REV A 53A-425	0026	79814-00123
U47	73005-74534	1	IC HCT OCTAL D-TYPE EDGE TRIG INVERT	0107	74HCT534
U53,63	73001-07474	2	IC TTL LS DUAL D-TYPE EDGE TRIG FLIP-FLOP	0107	74LS74A
U54	77200-07408	1	IC TTL QUAD 2-INPUT AND GATE	0107	7408
U56	76510-74804	1	IC TTL AS HEX 2-INPUT NAND DRIVER	0107	74AS804
U57	73003-74534	1	IC TTL ALS OCTAL D-TYPE EDGE INVERTING	0107	74ALS534
U61,81	73310-74241	2	IC TTL LS OCTAL BUFFER NON-INVERTING	0078	74LS241
U66	73004-74375	1	IC HCMOS 4-BIT BISTABLE LATCH	0107	74HC375

425SA1 BOTTOM BOARD FOR 53A-425

REV 9201-03-3

REFERENCE DESIGNATOR	CDS PART NUMBER	QTY.	PART DESCRIPTION	MFG. NUM.	MFG. PART NUMBER
U67	77825-07432	1	IC TTL ALS QUAD 2-INPUT OR GATE	0107	74ALS32
U73	79814-00084	1	PAL PROGRAMMED EP310-2 REV A 53A-425	0026	79814-00084
U74,76	73005-74174	2	IC HCT HEX D-TYPE FLIP-FLOP	0088	74HCT174
U77	73306-07404	1	IC TTL AS HEX INVERTER	0107	74AS04
U84,94	79801-08259	2	IC CMOS PROGRAMMABLE INTERRUPT CONTROLLER	0051	P82C59A
U86	79813-00014	1	PROGRAMMED PROM U86 53A-425	0026	79813-00014
U96	79813-00015	1	PROGRAMMED PROM U96 53A-425	0026	79813-00015
U97	78403-07414	1	IC HCT HEX SCHMITT INVERTING BUFFER	0088	74HCT14
X01,11	45010-07100	2	SOCKET SIP 7 PIN	0032	CAS07VSC-12B
X16	45010-80186	1	SOCKET 68 PIN PLCC	0243	QILE68P-410T
X351,352	45012-24128	2	SOCKET 24-PIN DIP NO SUB	0089	ICT-246-S-TG30
X86,96	45012-28100	2	SOCKET 28-PIN DIP LOW PRO	0089	ICO-286-S8A-TG
Y06	89500-16000	1	CRYSTAL 16.000MHZ 25PPM	0062	MP-1 16.0000


41530-42500-9201-03-B
E1
E2
E3
E4
X01
X11
DS01
DS11
DS12
DS13
DS14
DS15
Q021
Q022
Q12
R021
R022
R121
R122
R123
R124
R13
R14
R21
R22
R31
R321
R322
R323
R421
R422
R423
R424
R521
R522
R341
R342
R343
R344
R36
R46
R55
R56
R61
R712
R711
R81
R821
R822
R823
R824
R91
R921
R922
R923
R1011
R1012
R1021
R1022
R27
R37
R77
R871
R872
CR87
C03
C04
C061
C062
C07
C13
C14
C17
C23
C24
C27
C331
C332
C34
C35
C41
C43
C46
C53
C57
C661
C662
C73
C74
C77
C771
C81
C83
C87
C97
C1031
C1041
C1071
C1072
C1171
C1172
C11511
F07
F1071
F1171
Y06
S27
S97
P52
U03
U04
U05
U07
U131
U132
U141
U142
U15
U16/X16
U17
U231
U232
U241
U242
U25
U27
U21
U22
U233
U243
U331
U341
U332
U342
U333
U343
U31
U32
U35
X351
X352
U36
U37
U41
U42
U43
U46
U47
U53
U54
U56
U57
U61
+ C64
U63
U66
U67
U73
U74
U76
U77
U81
U83
U84
U86/X86
U92
U93
U94
U96/X96
U97
U101
U102
U103
U104
U106
U107
U111
U112
U113
U114
U116

425SA2 TOP BOARD FOR 53A-425

REV 9009-03-B

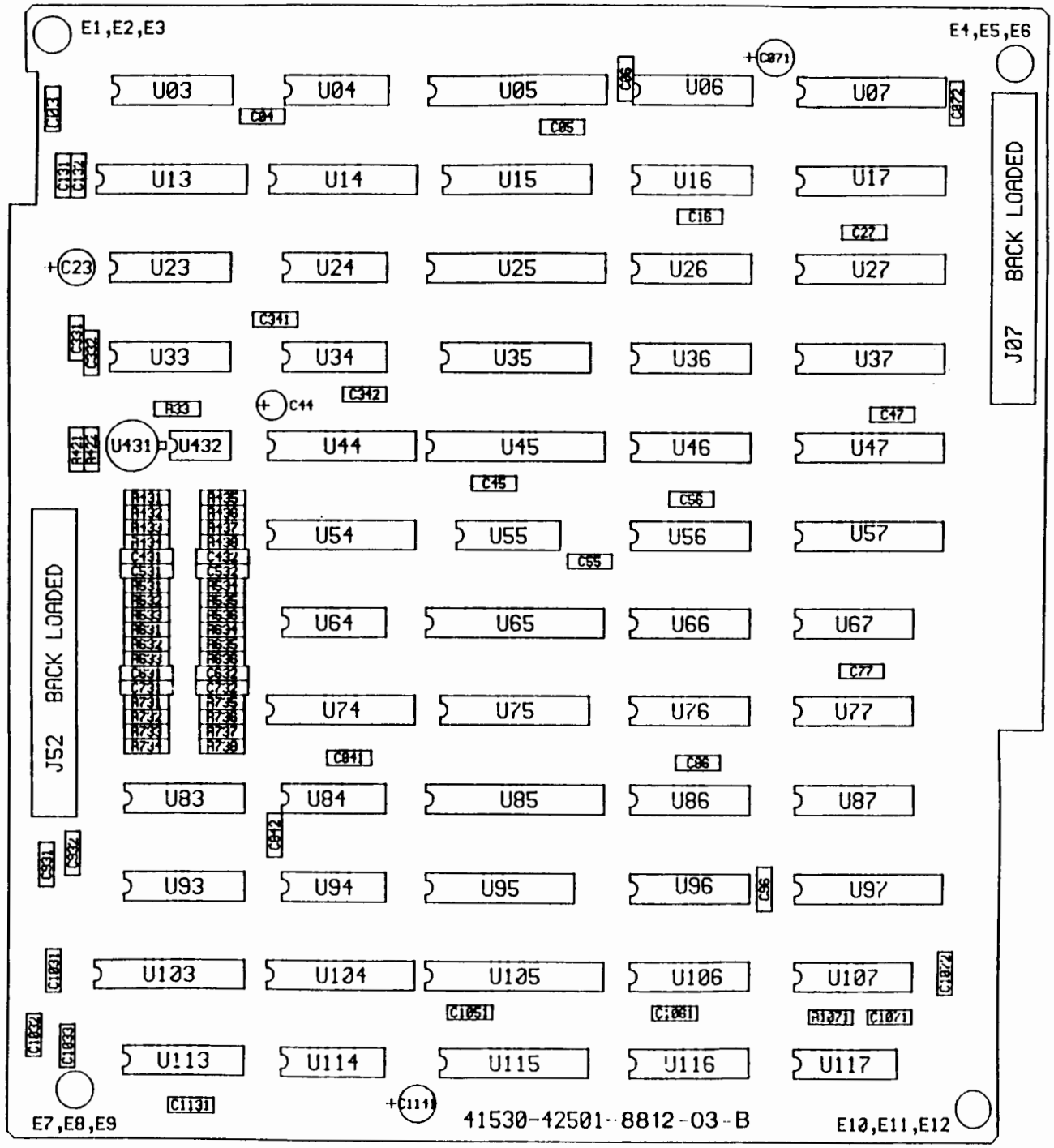
REFERENCE DESIGNATOR	CDS PART NUMBER	QTY.	PART DESCRIPTION	MFG. NUM.	MFG. PART NUMBER
C03,04,05,06,072,1031,1032,1033 1051,1061,1071,1072,1131,131,132 16,27,331,332,341,342,45,47,55 56,77,841,842,86,931,932,96	20128-10006	32	CAP FXD CER .1UF 20% 50VDCW	0058	C322C104M5U5CA
C071,1141,23,44	22022-20008	4	CAP FXD TA 22UF 10-20% 20-25VDCW	0106	199D226X9025CA1
C431,532,632,731	21528-20002	4	CAP FXD MICA 20PF 5% 500VDCW	0025	CD6ED200J03
C432,531,631,732	21528-47003	4	CAP FXD MICA 470PF 5% 100VDCW	0025	CD7FA471J03
E1,10,4,7	92301-00440	8	SCREW PHIL PNHD 4-40X5-16 BRITEZINC	0137	4-40X5-16 PHIL PNH
E11,13,14,15,16,2,5,8	92300-00440	12	WASHER SPLITRING 4-40 3-16 OD	0137	4R
E12,3,6,9	92201-00003	4	STAND-OFF 4-40 X 0.5 X 3-16 OD	0059	2027
J07,52	45002-70040	2	CONNECTOR PC BRD MNT 40 PIN DIP SOCKET	0044	FCN-704J040-AU-0
PCB	41530-42501	1	P.C. BOARD VERSION 4L 9106	0026	41530-42501
R1071	10117-10004	1	1K RES COMP 1-4W 5%	0087	R25J-1K-5%
R33,422,533,536,631,634	14024-10005	6	10K RES FILM 1-4W 1% 100PPM	0035	RN55D1002F
R421	14024-49904	1	4.99K RES FILM 1-4W 1% 100PPM	0035	RN55D4991F
R431,432,435,436,733,734,737,738	14024-30904	8	3.09K RES FILM 1-4W 1% 100PPM	0035	RN55D3091F
R433,434,437,438,731,732,735,736	14024-20005	8	20K RES FILM 1-4W 1% 100PPM	0035	RN55D2002F
R531,534,633,636	14024-22104	4	2.21K RES FILM 1-4W 1% 100PPM	0035	RN55D2211F
R532,535,632,635	14024-33205	4	33.2K RES FILM 1-4W 1% 100PPM	0035	RN55D3322F
U03,113,23,33,83,93	81001-00211	6	IC CMOS ANALOG SWITCH SPST QUAD	0102	DG211CJ
U04,114,34,84	78400-07410	4	IC HCMOS TRIPLE 3-INPUT NAND	0107	74HC10

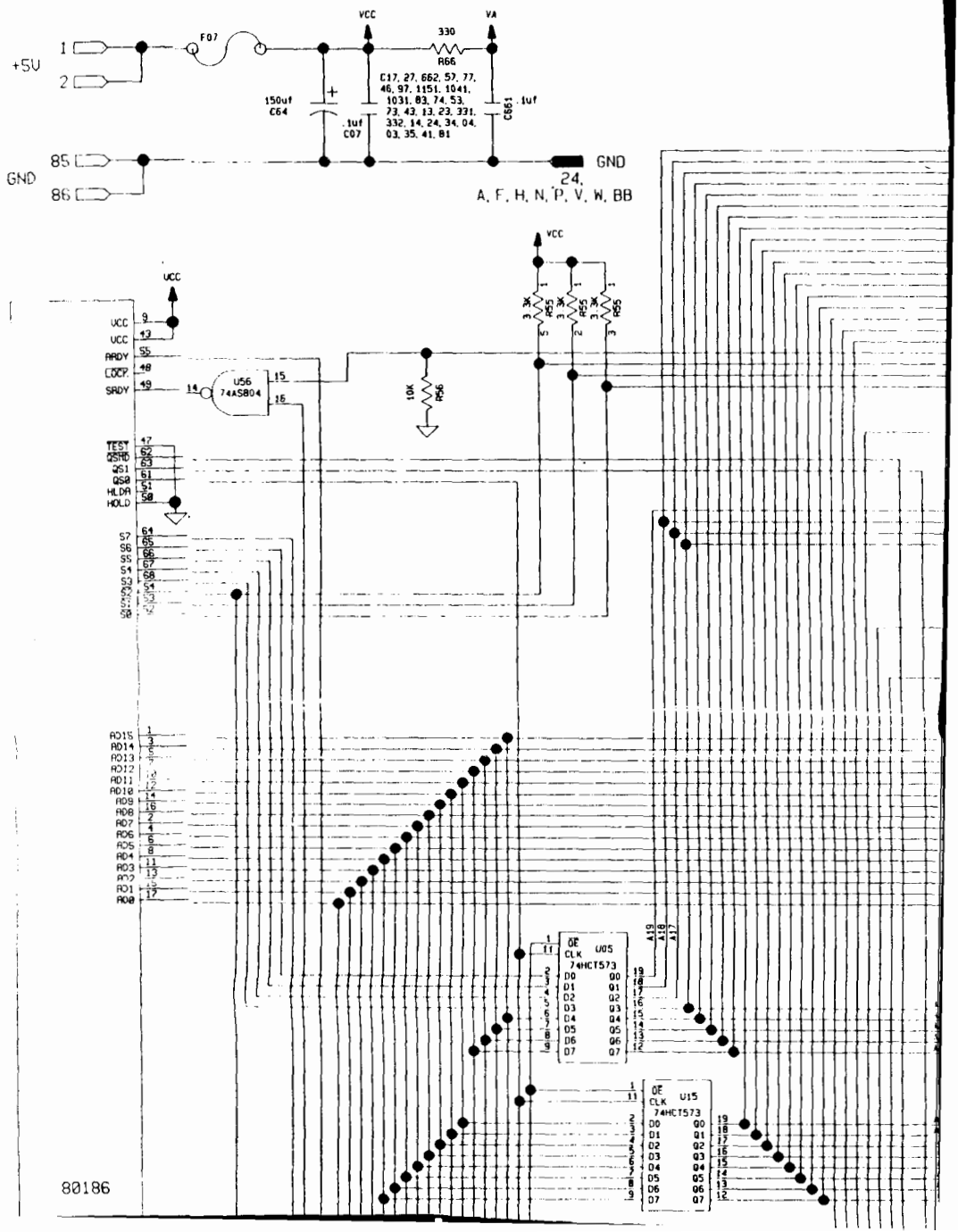
REFERENCE DESIGNATOR	CDS PART NUMBER	QTY.	PART DESCRIPTION	MFG. NUM.	MFG. PART NUMBER
U05,105,45,65	79814-00088	4	PAL PROGRAMMED EP600 REV B 53A-425	0026	79814-00088
U06,106,116,16,46,56,66,76	79800-67401	8	IC CMOS 64K X 4-BIT FIFO	0218	CY7C401-15PC
U07	73314-74241	1	IC HCT OCTAL BUFFER INVERTING	0107	74HCT241
U103,104,13,14,27,37,44,57,74	73005-74374	9	IC HCT OCTAL D-TYPE FLIP-FLOP	0107	74HCT374
U107	71201-74161	1	IC HCMOS SYNCH 4-BIT BINARY COUNTER	0107	74HC161N
U115	79814-00108	1	PAL PROGRAMMED EP310-2 REV A 53A-425	0026	79814-00108
U117	76603-07410	1	IC TTL AS 3-INPUT NAND GATE	0107	74AS10
U15,35,75,95	79814-00087	4	PAL PROGRAMMED EP310-2 REV A 53A-425	0026	79814-00087
U17	79814-00107	1	PAL PROGRAMMED EP310-2 REV A 53A-425	0026	79814-00107
U24,94	73303-07404	2	IC HCMOS HEX INVERTER	0107	74HC04
U25,85	73003-74873	2	IC TTL ALS DUAL 4-BIT D-TYPE LATCH	0107	74ALS873
U26,36,86,96	75404-74194	4	IC HCMOS 4-BIT BIDIRECTIONAL SHIFT REGISTER	0107	74HC194
U431	61000-00356	1	OP AMP JFET	0078	LF356BH
U432	52200-00001	1	REFERENCE 10V 20MA 0-25 PPM	0082	REF01CP
U47	79814-00085	1	PAL PROGRAMMED EP310 REV A 53A-425	0026	79814-00085
U54	73309-74240	1	IC HCT OCTAL BUFFER INVERTING	0088	74HCT240
U55	77203-07408	1	IC TTL ALS QUAD 2-INPUT AND GATE	0107	74ALS08
U64	61000-00347	1	OP AMP FET QUAD	0078	LF347
U67,77	79008-74138	2	IC HCT 3-TO-8 LINE DECDR DEMULTIPLEXER	0107	74HCT138
U87	79008-74137	1	IC HCT 3-TO-8 DECODER WITH LATCH	0107	74HCT137

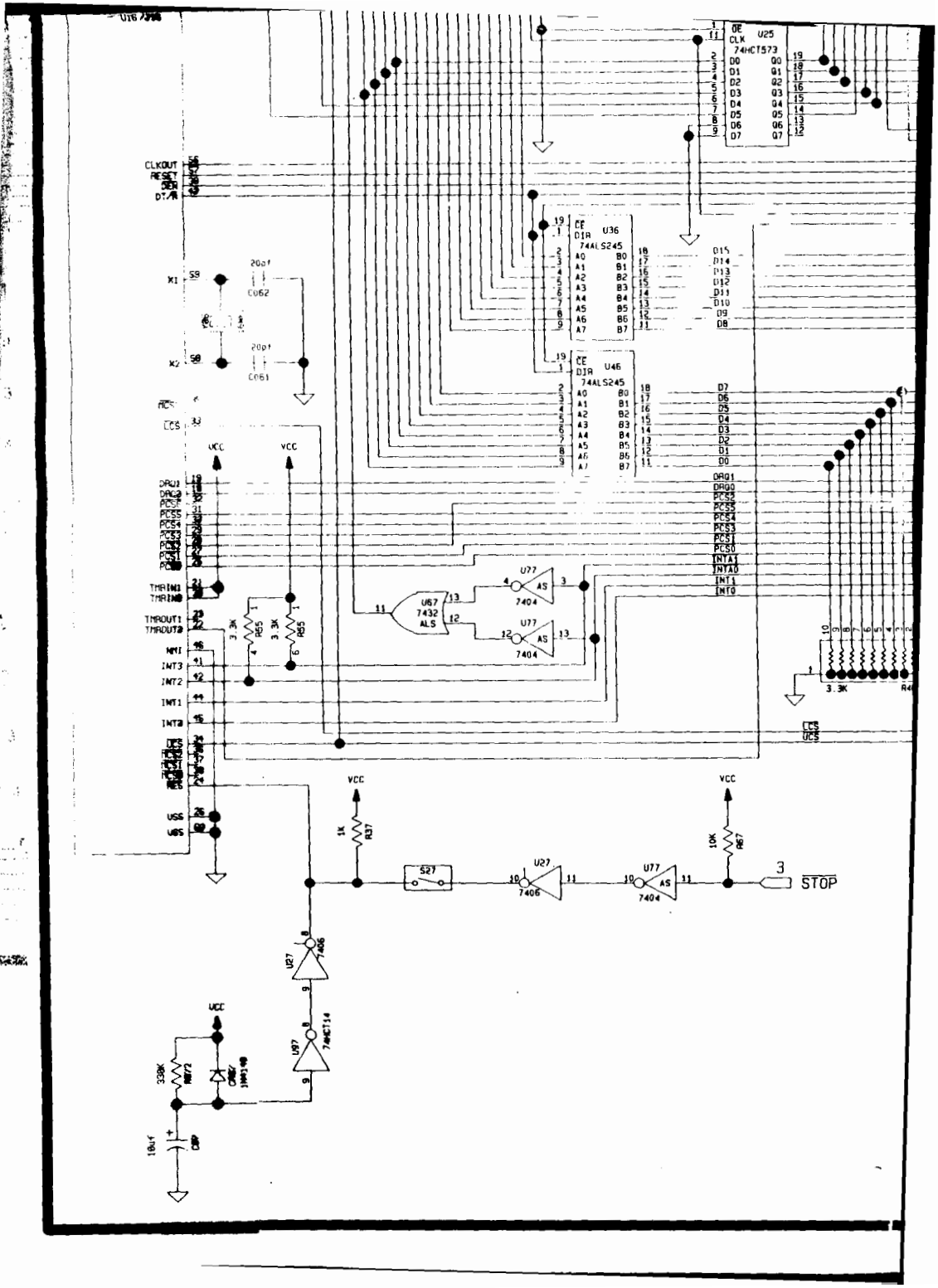
425SA2 TOP BOARD FOR 53A-425

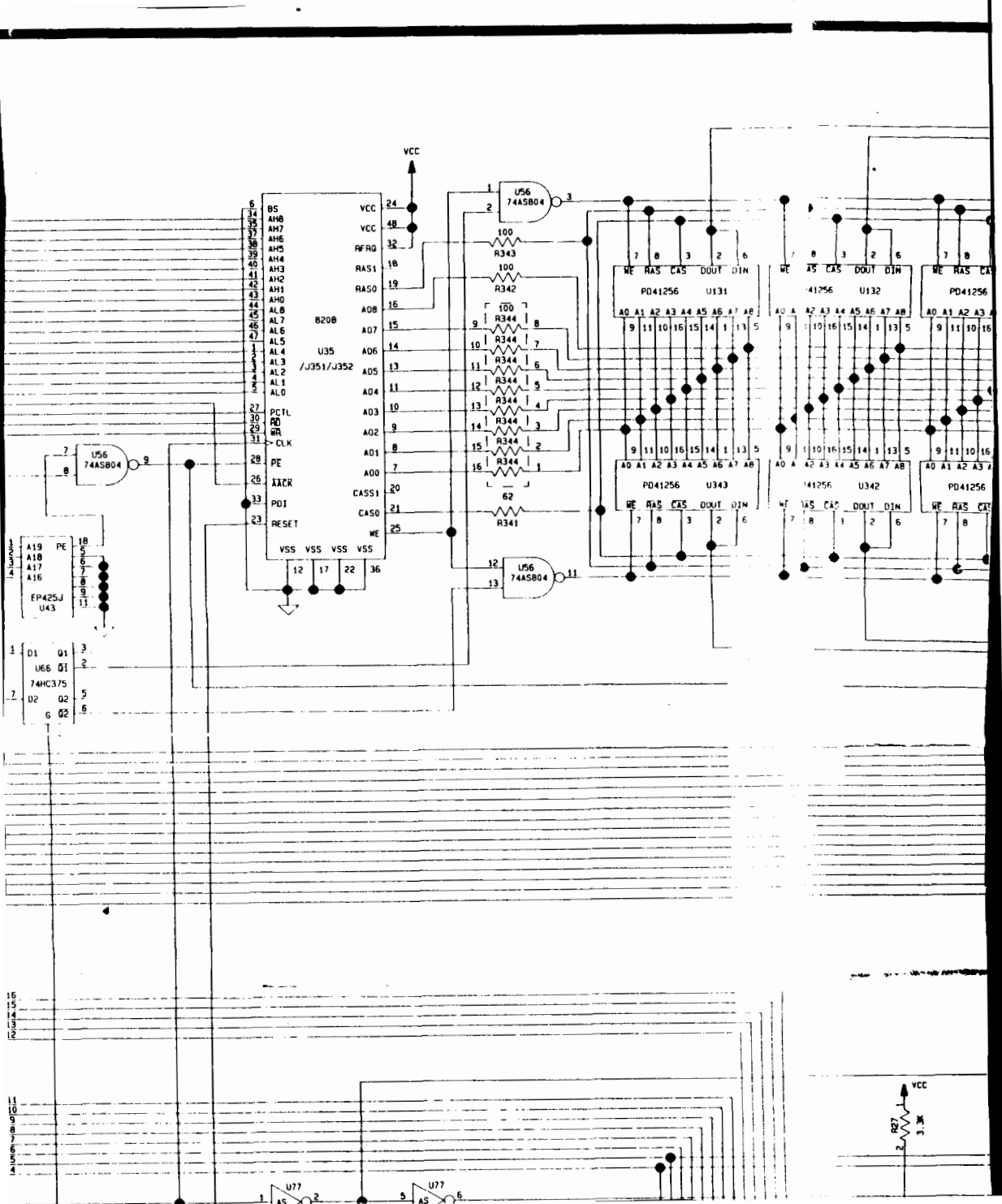
REV 9009-03-B

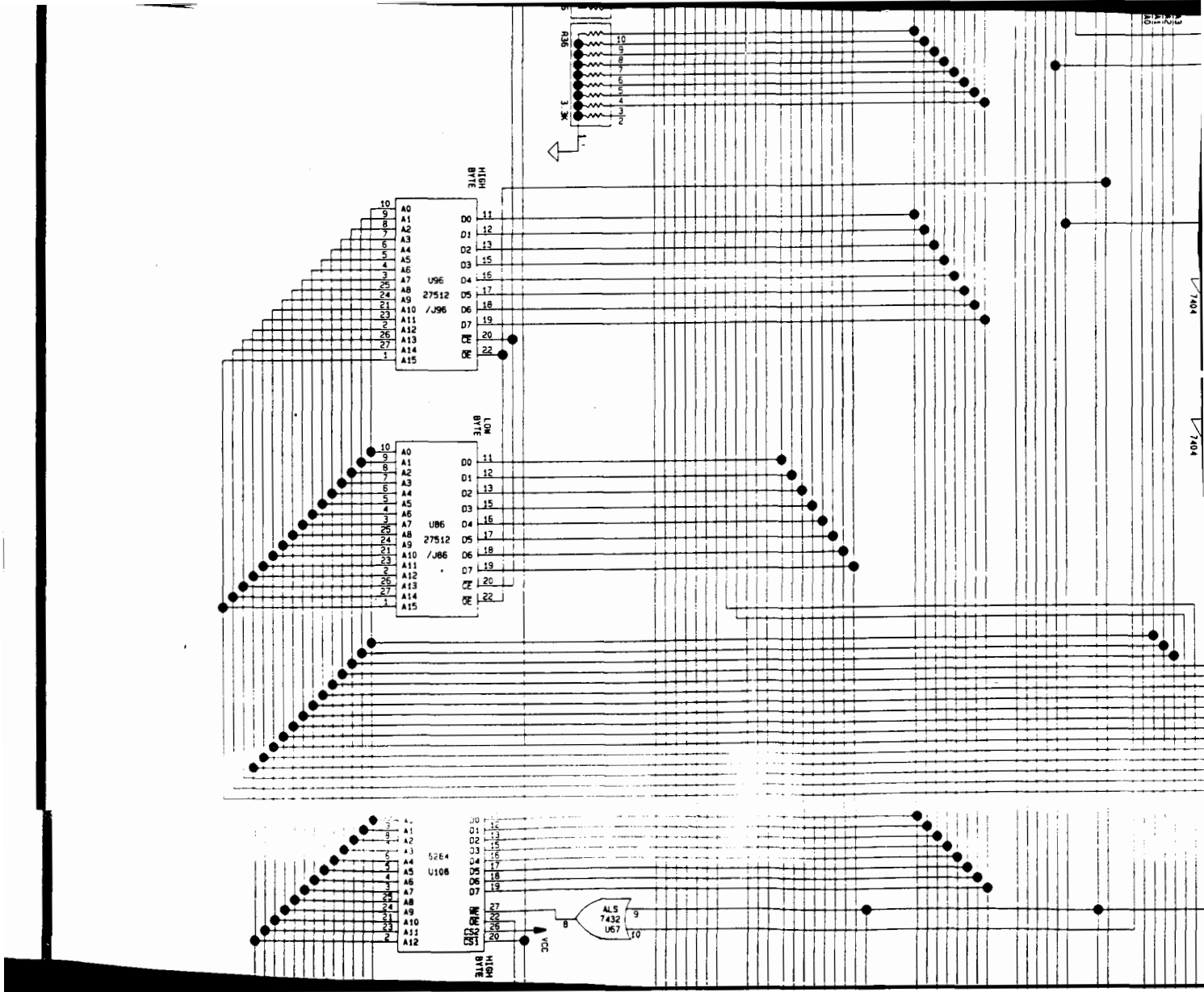
REFERENCE DESIGNATOR	CDS PART NUMBER	QTY.	PART DESCRIPTION	MFG. NUM.	MFG. PART NUMBER
U97	79814-00086	1	PAL PROGRAMMED EP310-2 REV A 53A-425	0026	79814-00086

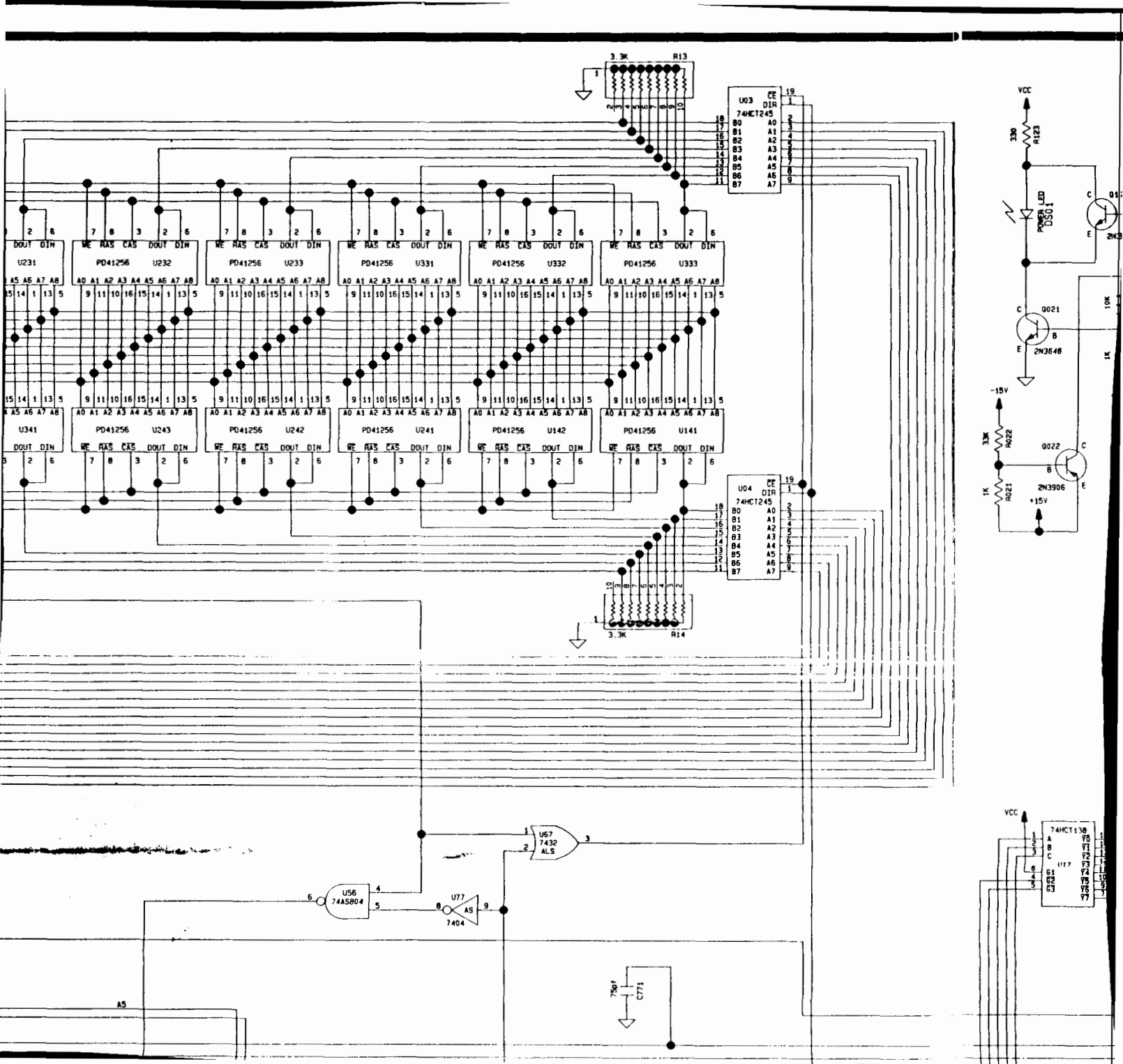

E1,E2,E3
E4,E5,E6
E7,E8,E9
E10,E11,E12
J52 BACK LOADED
J07 BACK LOADED
41530-42501--8812-03-B
U03
U04
U05
U06
U07
U13
U14
U15
U16
U17
U23
U24
U25
U26
U27
U33
U34
U35
U36
U37
U431
U432
U44
U45
U46
U47
U54
U55
U56
U57
U64
U65
U66
U67
U74
U75
U76
U77
U83
U84
U85
U86
U87
U93
U94
U95
U96
U97
U103
U104
U105
U106
U107
U113
U114
U115
U116
U117
C23
C44
C871
C16
C22
C341
C342
C45
C47
C56
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C86
C842
C96
C1051
C1061
C1131
C1111
R33
R1071

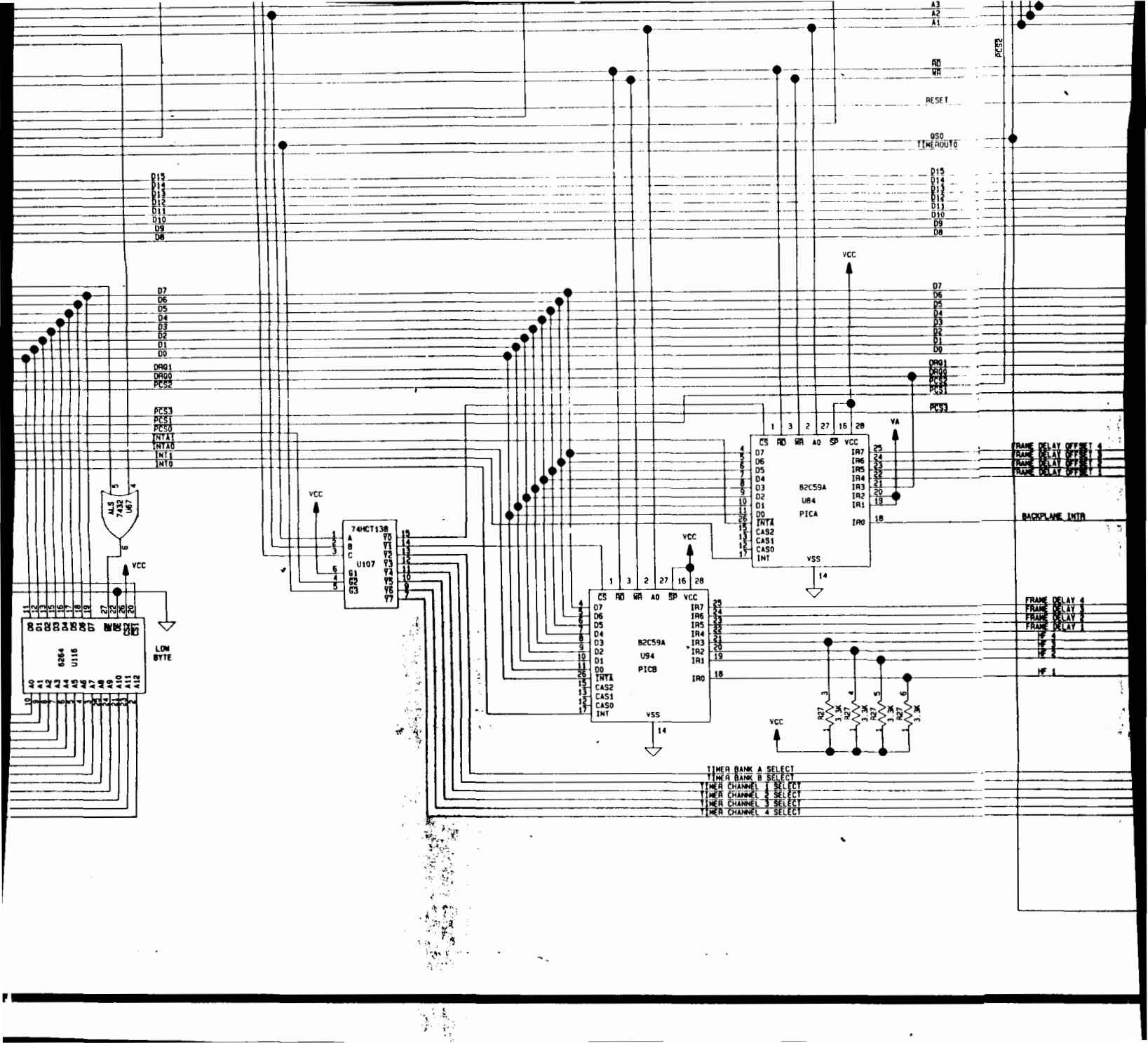

+5V
GND
F07
VCC
VA
330
R66
150uf
C64
.1uf
C07
C17, 27, 662, 57, 77, 46, 97, 1151, 1041, 1031, 83, 74, 53, 73, 43, 13, 23, 331, 332, 14, 24, 34, 04, 03, 35, 41, 81
C661 .1uf
GND
24, A, F, H, N, P, V, W, BB
U56
74AS804
10K
R56
3.3K
R55
TEST
QSMD
QS1
QS0
HLDR
HOLD
ARDY
SRDY
S7
S6
S5
S4
S3
S2
S1
S0
AD15
AD14
AD13
AD12
AD11
AD10
AD9
AD8
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
U05
74HCT573
U15
74HCT573
OE
CLK
D0
D1
D2
D3
D4
D5
D6
D7
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
A19
A18
A17
80186

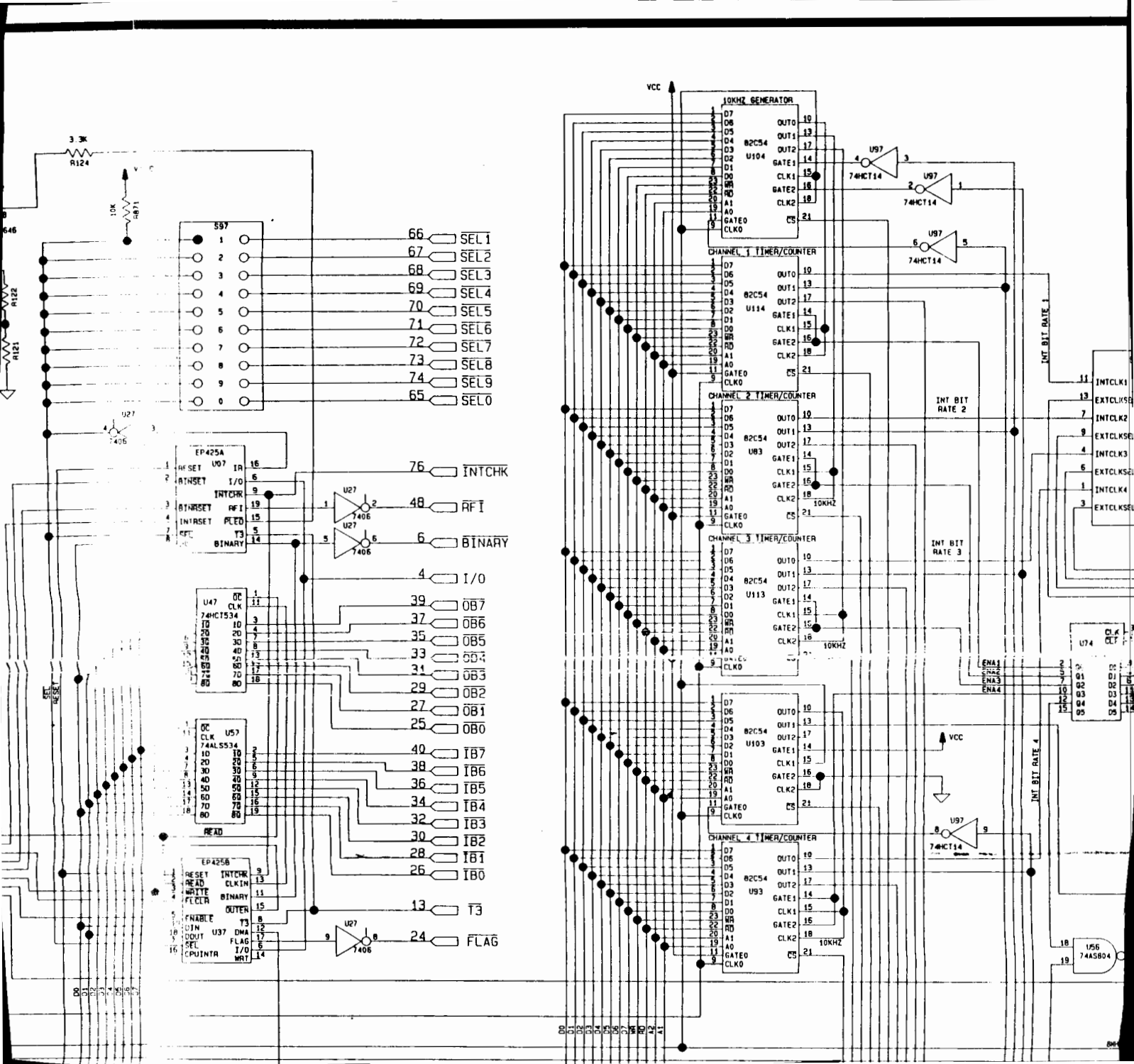

U25
74HCT573
U36
74ALS245
U46
74ALS245
CLKOUT
RESET
D7/R
X1
X2
20pf
C062
20pf
C061
ADS
DEN
VCC
DRQ1
DRQ0
PCS7
PCS6
PCS5
PCS4
PCS3
PCS2
PCS1
PCS0
INTA1
INTA0
INT1
INT0
TMRIN1
TMRIN0
TMROUT1
TMROUT0
NMI
INT3
INT2
INT1
INT0
VSS
U67
7432
ALS
U77
AS
7404
R65
3.3K
R66
3.3K
R4
3.3K
U27
7406
S27
R37
1K
R67
10K
STOP
U27
7406
U37
74HCT14
R72
330K
CR67
1N4148
C69
10uf

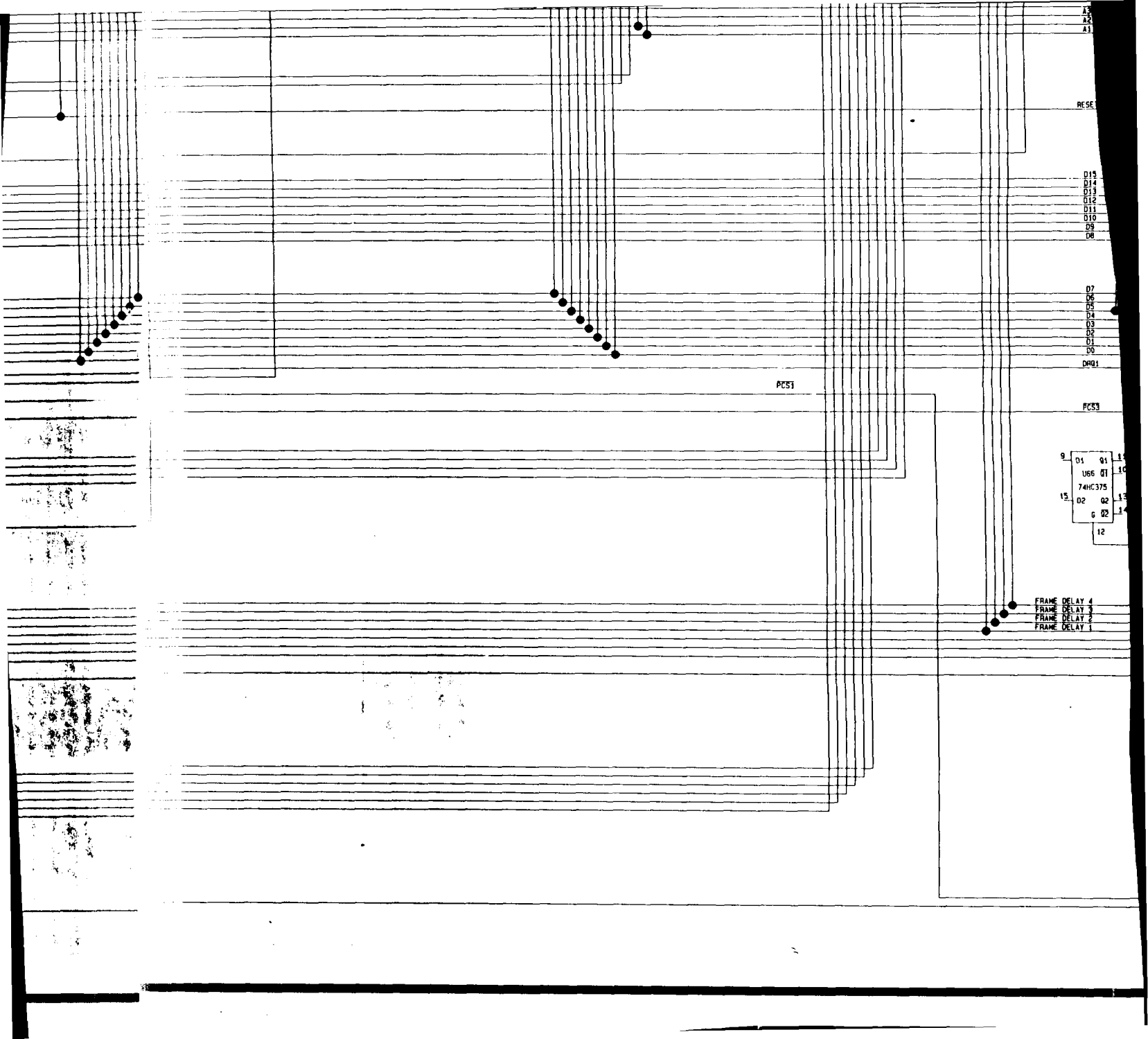

VCC
U56
74AS804
100
R343
R342
R344
62
R341
U35
/J351/J352
8208
BS
AH8
AH7
AH6
AH5
AH4
AH3
AH2
AH1
AH0
AL8
AL7
AL6
AL5
AL4
AL3
AL2
AL1
AL0
PCTL
RD
WR
CLK
PE
AACR
PDI
RESET
VCC
VCC
RFRQ
RAS1
RAS0
AD8
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
CASS1
CAS0
WE
VSS
VSS
VSS
VSS
PD41256
U131
U132
U343
U342
WE
RAS
CAS
DOUT
DIN
A19
A18
A17
A16
PE
EP425J
U43
D1
Q1
U66
OE
74HC375
D2
Q2
G
Q2
U77
AS
R27
3.3K

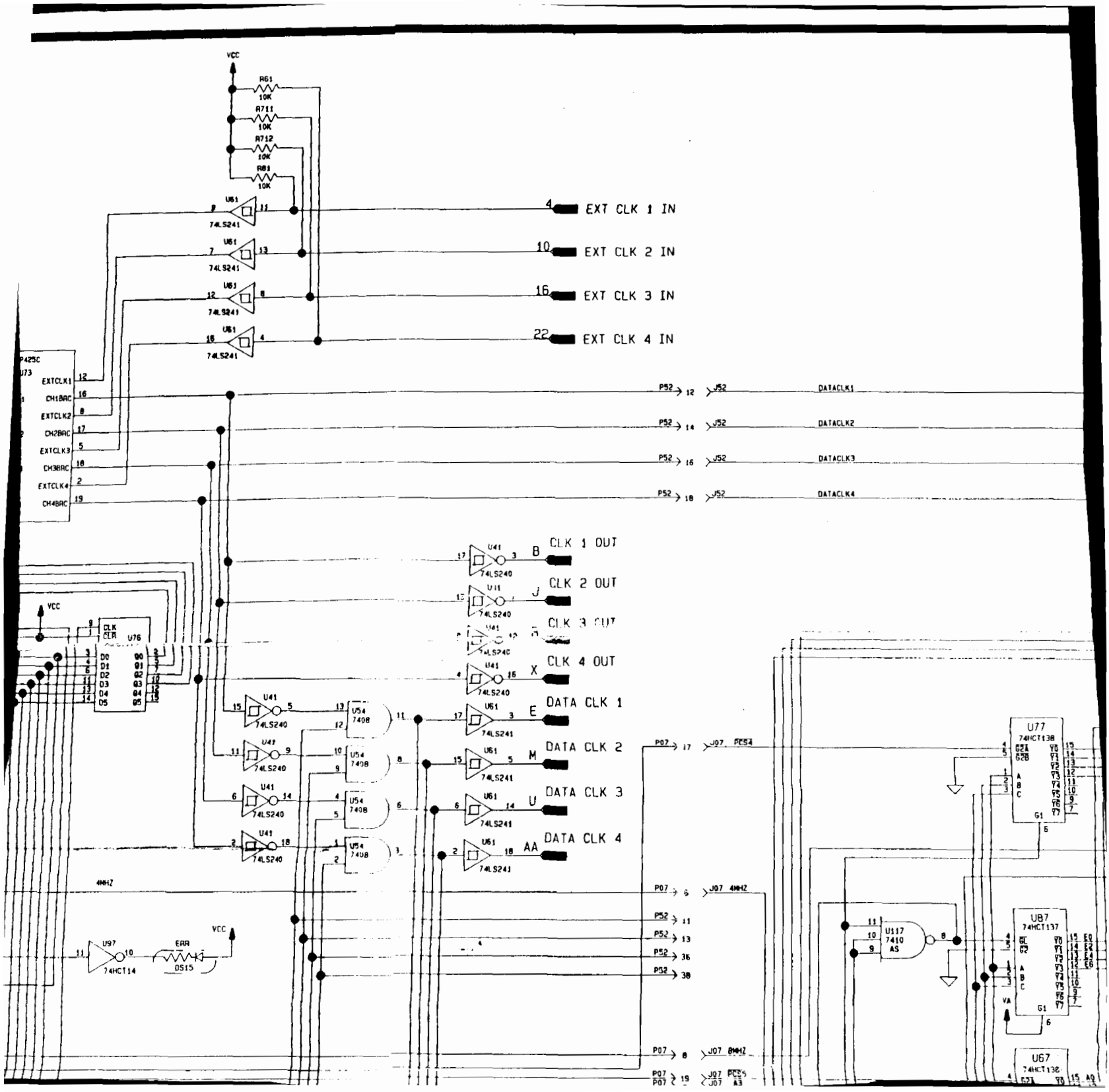

R36
3K
HIGH BYTE
U96
27512
/U96
LOW BYTE
U86
27512
/U86
U106
5264
ALS
7432
U67
VCC
7404
7404

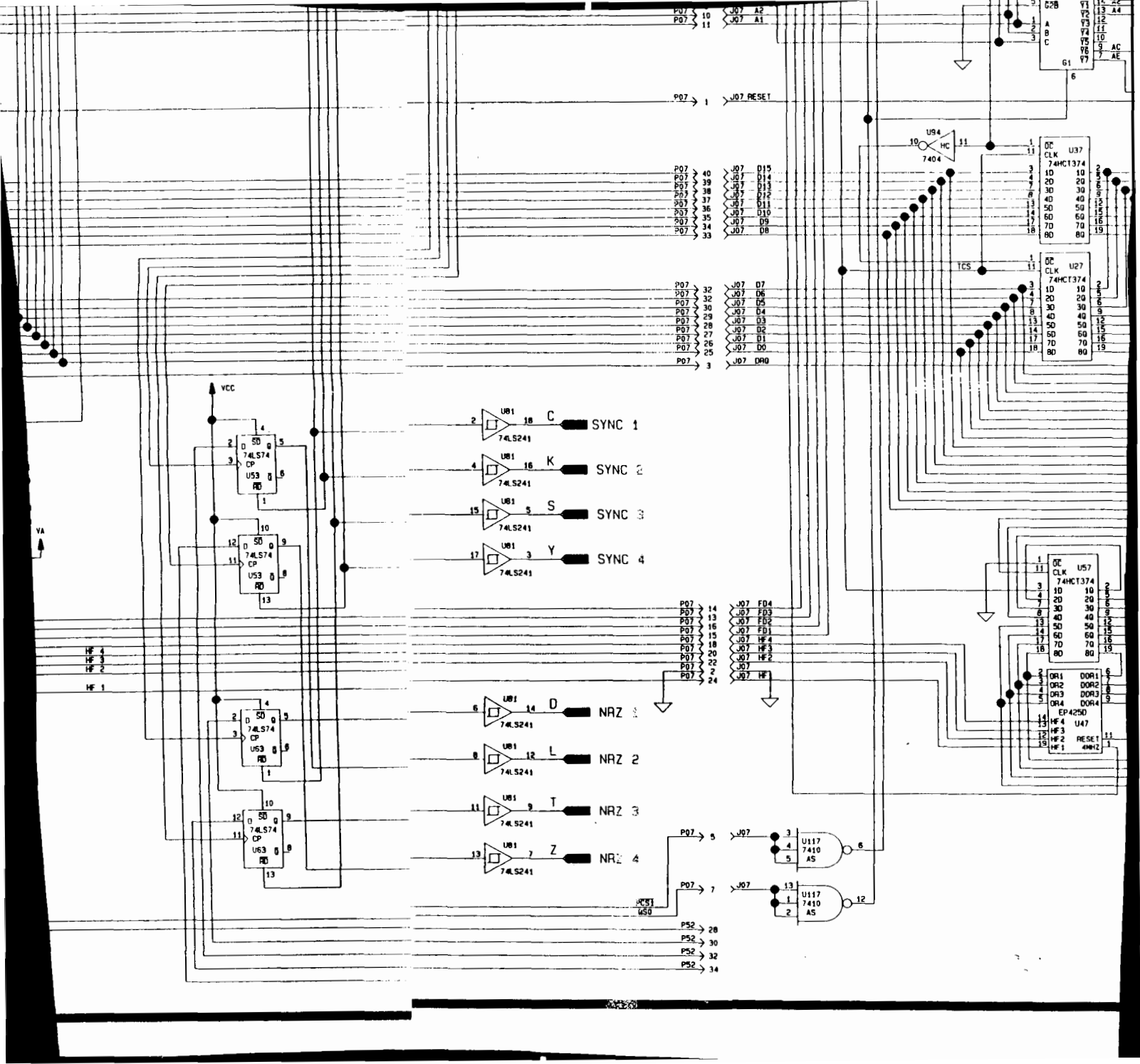

3.3K
R13
U03
74HCT245
U231
U232
U233
U331
U332
U333
U341
U243
U242
U241
U142
U141
PD41256
U04
74HCT245
3.3K
R14
VCC
330
R123
POWER LED
DS01
Q12
2N3
Q021
2N3646
10K
1K
-15V
33K
R022
Q022
2N3906
1K
R021
+15V
U67
7432
ALS
U56
74AS804
U77
AS
7404
75pf
C771
A5
VCC
74HCT138
U17


A3
A2
A1
AD
WR
RESET
QSO
TIMEROUT0
D15
D14
D13
D12
D11
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
D0
DRQ1
DRQ0
PCS2
PCS3
PCS1
PCS0
INTA1
INTA0
INT1
INT0
VCC
ALS 7432 U67
74HCT138
U107
A
B
C
G1
G2
G3
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
6264 U116
LOW BYTE
B2C59A
U84
PICA
B2C59A
U94
PICB
CS
RD
WR
A0
SP
VCC
D7
D6
D5
D4
D3
D2
D1
D0
INTA
CAS2
CAS1
CAS0
INT
VSS
IR7
IR6
IR5
IR4
IR3
IR2
IR1
IR0
VA
R27
3.3K
FRAME DELAY OFFSET 4
FRAME DELAY OFFSET 3
FRAME DELAY OFFSET 2
FRAME DELAY OFFSET 1
BACKPLANE INTR
FRAME DELAY 4
FRAME DELAY 3
FRAME DELAY 2
FRAME DELAY 1
HF 4
HF 3
HF 2
HF 1
TIMER BANK A SELECT
TIMER BANK B SELECT
TIMER CHANNEL 1 SELECT
TIMER CHANNEL 2 SELECT
TIMER CHANNEL 3 SELECT
TIMER CHANNEL 4 SELECT

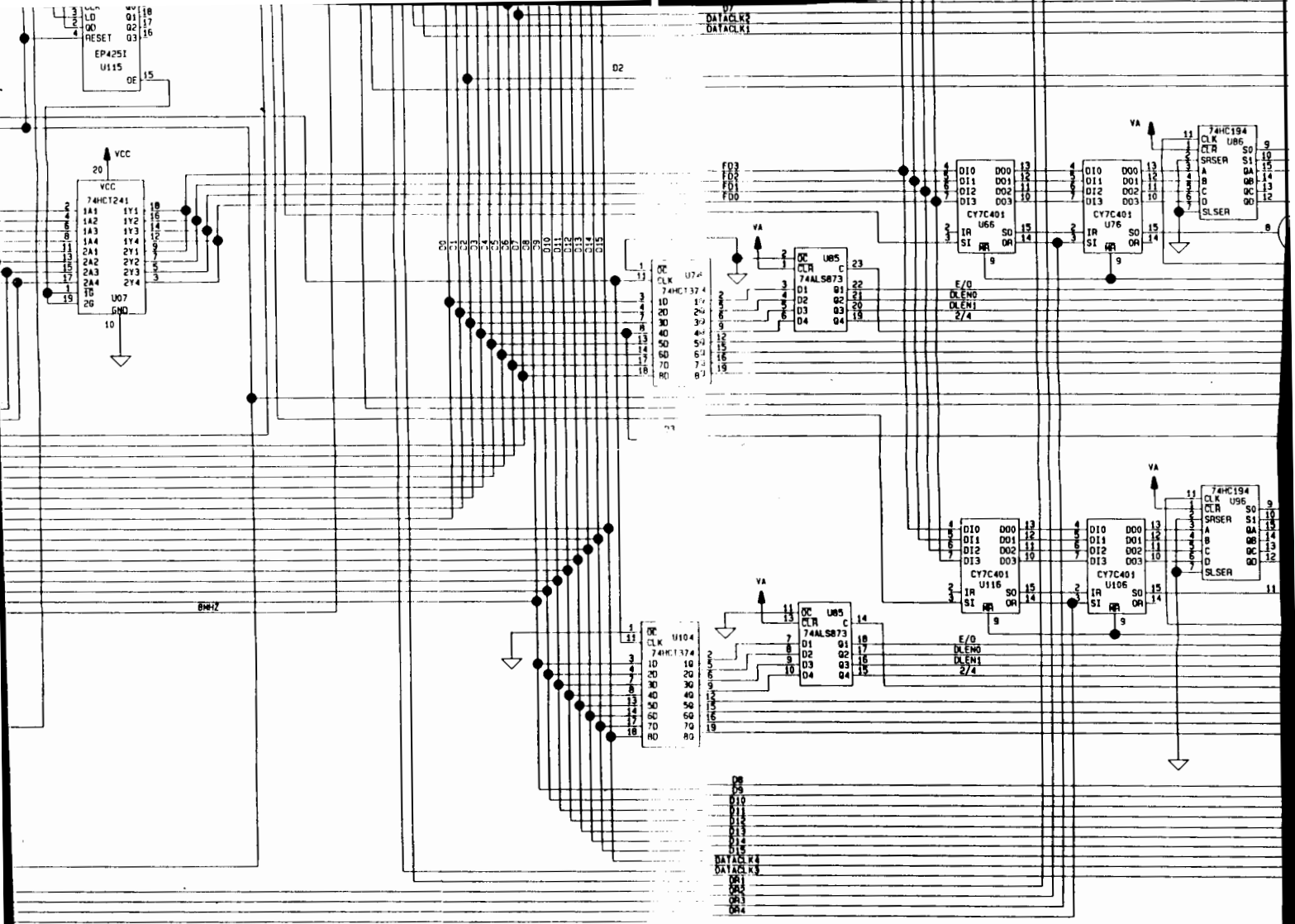

3.3K
R124
10K
R871
R122
R121
U97
74HCT14
SEL1
SEL2
SEL3
SEL4
SEL5
SEL6
SEL7
SEL8
SEL9
SEL0
U27
7406
EP425A
U07
RESET
ATNSET
INTCHK
BINRSET
INTRSET
RFI
FLED
T3
BINARY
INTCHK
RFI
BINARY
I/O
U47
74HCT534
OB7
OB6
OB5
OB4
OB3
OB2
OB1
OB0
U57
74ALS534
IB7
IB6
IB5
IB4
IB3
IB2
IB1
IB0
READ
EP425B
U37
CLKIN
OUTER
ENABLE
DIN
DOUT
SEL
CPUINTR
DMA
FLAG
WRT
T3
FLAG
SET
RESET
VCC
10KHZ GENERATOR
82C54
U104
CHANNEL 1 TIMER/COUNTER
U114
CHANNEL 2 TIMER/COUNTER
U83
CHANNEL 3 TIMER/COUNTER
U113
U103
CHANNEL 4 TIMER/COUNTER
U93
10KHZ
INT BIT RATE 1
INT BIT RATE 2
INT BIT RATE 3
INT BIT RATE 4
INTCLK1
EXTCLKSEL
INTCLK2
EXTCLKSEL
INTCLK3
EXTCLKSEL
INTCLK4
EXTCLKSEL
U74
ENA1
ENA2
ENA3
ENA4
U56
74AS804


A3
A2
A1
RESET
D15
D14
D13
D12
D11
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
D0
DAQ1
PCS1
PCS3
9
D1
Q1
U66
74HC375
15
D2
Q2
G
12
FRAME DELAY 4
FRAME DELAY 3
FRAME DELAY 2
FRAME DELAY 1

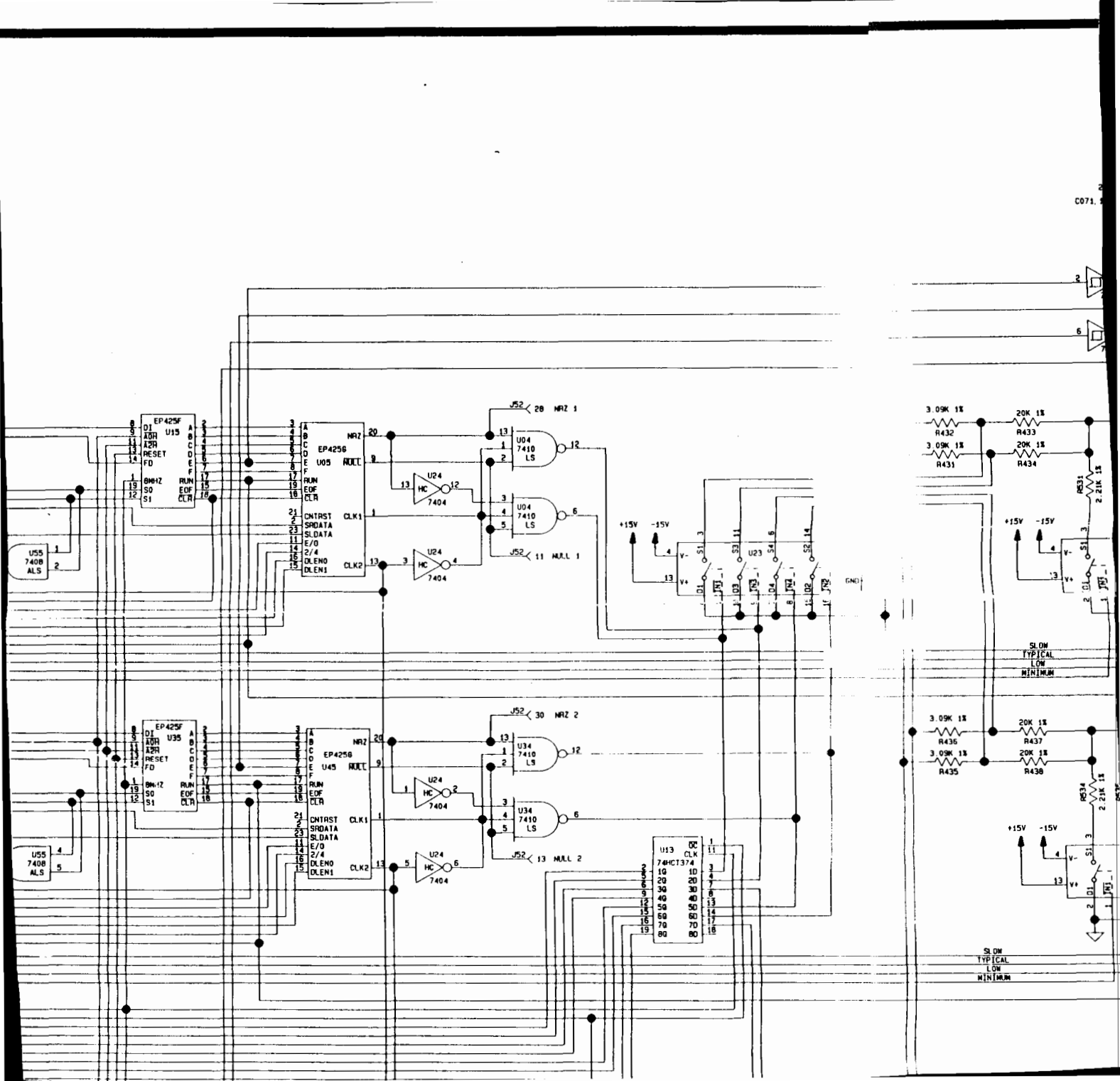

VCC
R61 10K
R711 10K
R712 10K
R81 10K
U61 74LS241
EXT CLK 1 IN
EXT CLK 2 IN
EXT CLK 3 IN
EXT CLK 4 IN
P425C U73
EXTCLK1
CH1BRC
EXTCLK2
CH2BRC
EXTCLK3
CH3BRC
EXTCLK4
CH4BRC
P52 12 J52 DATACLK1
P52 14 J52 DATACLK2
P52 16 J52 DATACLK3
P52 18 J52 DATACLK4
U41 74LS240
CLK 1 OUT
CLK 2 OUT
CLK 3 OUT
CLK 4 OUT
U76
U54 7408
DATA CLK 1
DATA CLK 2
DATA CLK 3
DATA CLK 4
4MHZ
U97 74HCT14
ERR
0S15
P07 17 J07 PCS4
P07 6 J07 4MHZ
P52 11
P52 13
P52 36
P52 38
P07 8 J07 8MHZ
P07 19 J07 PCS5
U117 7410 AS
U77 74HCT138
U87 74HCT137
U67 74HCT138

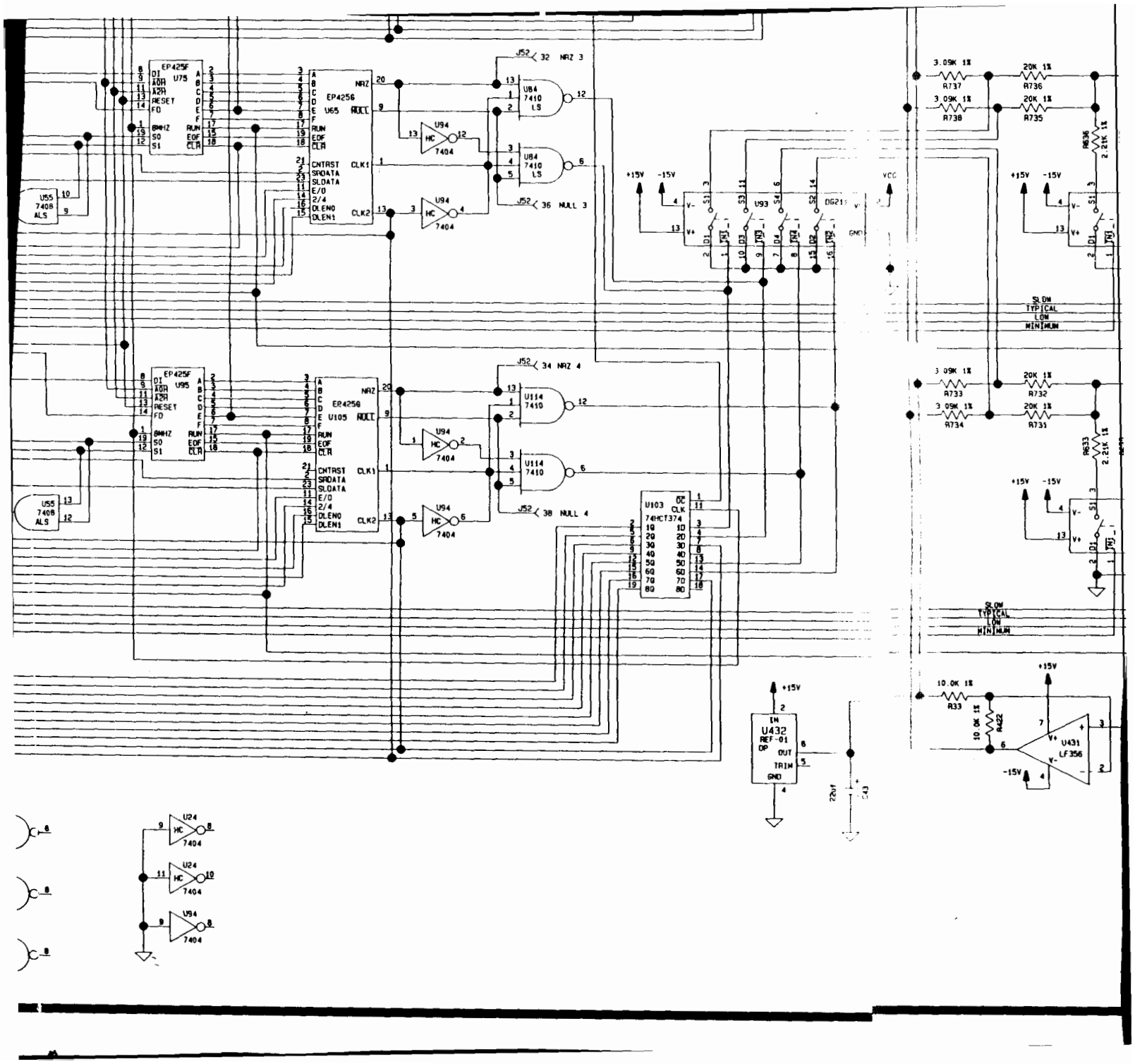

VCC
VA
U81
74LS241
SYNC 1
SYNC 2
SYNC 3
SYNC 4
NRZ 1
NRZ 2
NRZ 3
NRZ 4
74LS74
U53
U63
U94
7404
74HCT374
U37
U27
U57
EP4250
U47
U117
7410
J07 RESET
J07 D15
J07 D14
J07 D13
J07 D12
J07 D11
J07 D10
J07 D9
J07 D8
J07 D7
J07 D6
J07 D5
J07 D4
J07 D3
J07 D2
J07 D1
J07 D0
J07 DA0
J07 FD4
J07 FD3
J07 FD2
J07 FD1
J07 HF4
J07 HF3
J07 HF2
J07 HF1
P07
P52
TCS
4MHZ

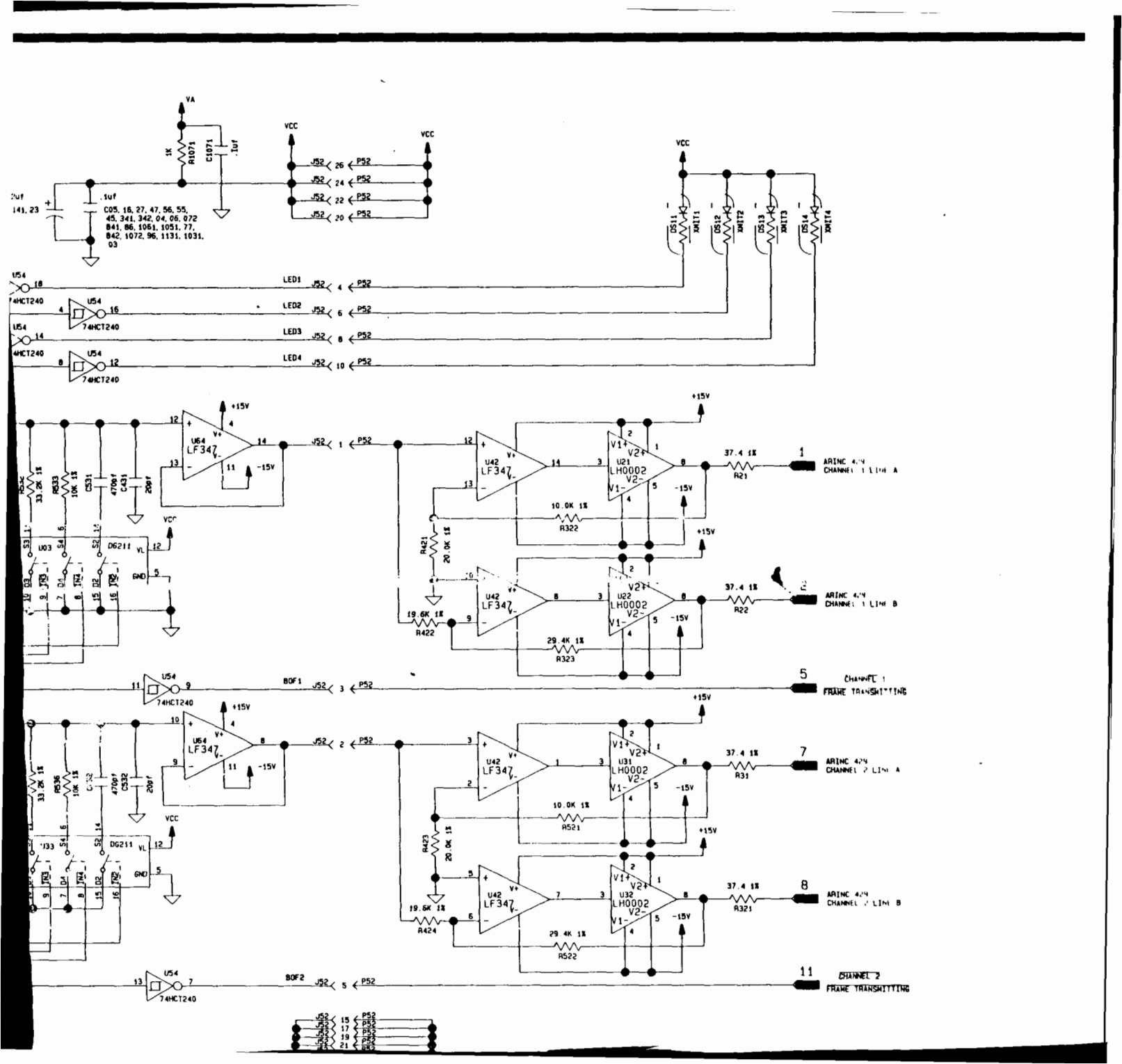

D0
D1
VA
BMHZ
EP425H
EP425E
U97
U107
74HC161
74HC1374
U14
U44
74ALS873
U25
CY7C401
U06
U16
U56
U46
74HC194
U26
U36
E/O
DLEN0
DLEN1
2/4
SASER
SLSER

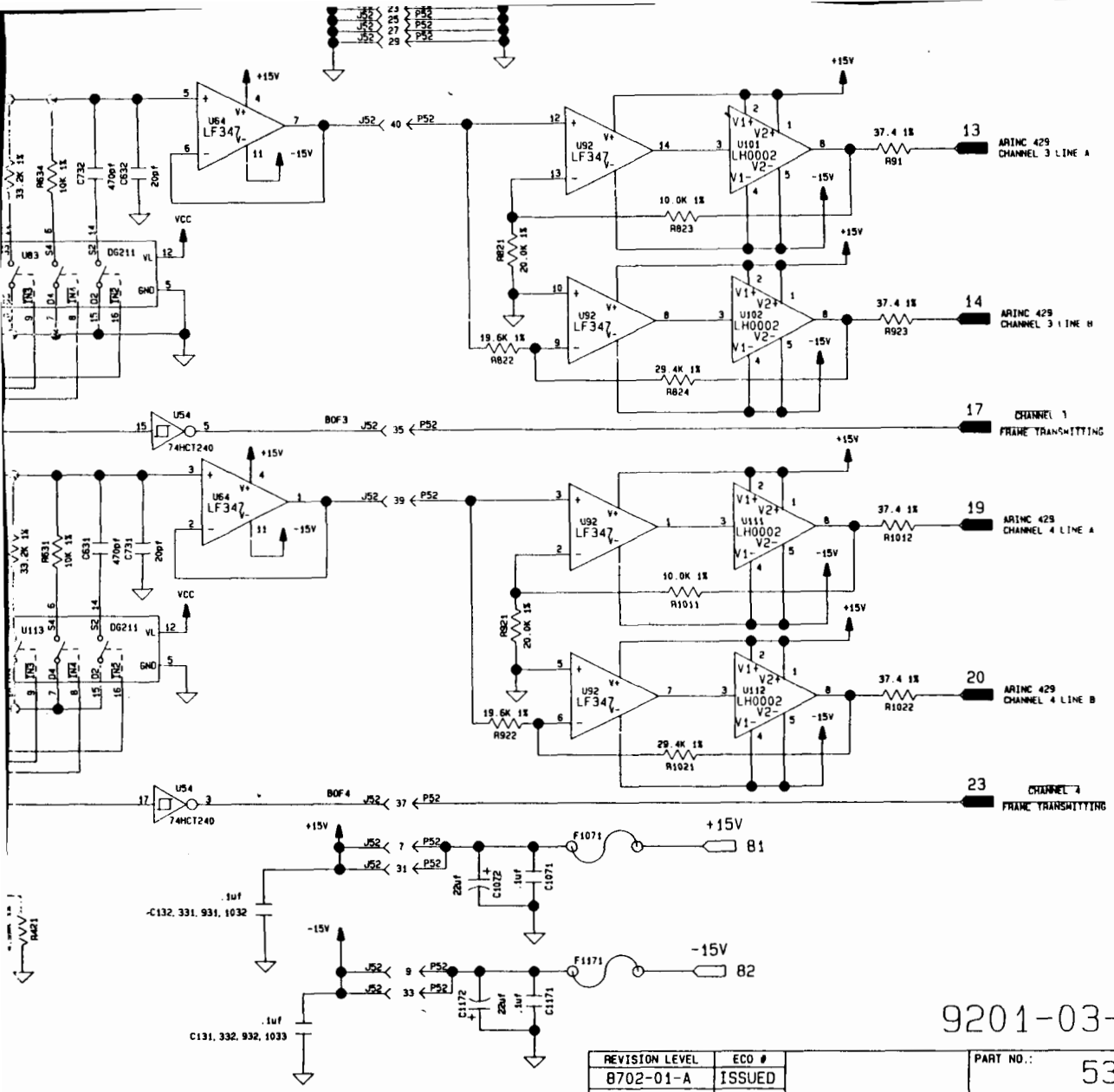


41530-42501-9009


EP425F
U15
EP425B
U05
NRZ
RDCL
RUN
EOF
CLR
CNTRST
SRDATA
SLDATA
E/D
2/4
DLEN0
DLEN1
CLK1
CLK2
U24
HC
7404
U04
7410
LS
J52
28 NRZ 1
11 NULL 1
U55
7408
ALS
+15V
-15V
U23
S1
S2
S3
S4
D1
D2
D3
D4
GND
3.09K 1%
20K 1%
R432
R433
R431
R434
R531
2.21K 1%
SLOW
TYPICAL
LOW
MINIMUM
EP425F
U35
EP425B
U45
30 NRZ 2
13 NULL 2
U34
U13
74HCT374
CLK
R436
R437
R435
R438
R534


EP425F U75
EP4256 U65
U55 74LS08
U84 7410 LS
U94 HC 7404
J52 32 NRZ 3
J52 36 NULL 3
EP425F U95
EP4256 U105
U114 7410
J52 34 NRZ 4
J52 38 NULL 4
U103 74HCT374
U93 DG213
+15V
-15V
VCC
GND
3.09K 1% R737
20K 1% R736
3.09K 1% R738
20K 1% R735
2.21K 1% R636
3.09K 1% R733
20K 1% R732
3.09K 1% R734
20K 1% R731
2.21K 1% R633
SLOW
TYPICAL
LOW
MINIMUM
10.0K 1% R33
10.0K 1% R422
U431 LF356
U432 REF-01
22uf C43
U24 HC 7404


VA
VCC
1K
R1071
C1071
.1uf
.1uf
C05, 16, 27, 47, 56, 55, 45, 341, 342, 04, 06, 072 B41, 86, 1051, 1051, 77, B42, 1072, 96, 1131, 1031, 03
J52 26 P52
J52 24 P52
J52 22 P52
J52 20 P52
DS11 XMIT1
DS12 XMIT2
DS13 XMIT3
DS14 XMIT4
U54
74HCT240
LED1 J52 4 P52
LED2 J52 6 P52
LED3 J52 8 P52
LED4 J52 10 P52
+15V
-15V
U64 LF347
U42 LF347
U21 LH0002
U22 LH0002
U31 LH0002
U32 LH0002
DG211
R33 10K 1%
C531 470pf
C431 20pf
R421 20.0K 1%
R422 19.6K 1%
R322 10.0K 1%
R323 29.4K 1%
R21 37.4 1%
R22 37.4 1%
R31 37.4 1%
R321 37.4 1%
R521 10.0K 1%
R522 29.4K 1%
R423 20.0K 1%
R424 19.6K 1%
R536 10K 1%
C532 470pf
C532 20pf
BOF1 J52 3 P52
BOF2 J52 5 P52
1 ARINC 429 CHANNEL 1 LINE A
2 ARINC 429 CHANNEL 1 LINE B
5 CHANNEL 1 FRAME TRANSMITTING
7 ARINC 429 CHANNEL 2 LINE A
8 ARINC 429 CHANNEL 2 LINE B
11 CHANNEL 2 FRAME TRANSMITTING



9201-03-B

REVISION LEVEL	ECO #
8702-01-A	ISSUED
8703-02-A	
8706-02-B	557
8706-02-C	
8808-02-D	714
9106-03-A	1683
9201-03-B	1922

COLORADO DATA SYSTEMS

PART NO.: 53A-425

DESCRIPTION: QUAD ARINC 429 CARD

P.C.B. NUMBER: 41530-42500

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