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53A-450 WIRE-WRAP CARD

OPERATING MANUAL

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53A-450 WIRE-WRAP CARD

OPERATING MANUAL

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53A-450 WIRE-WRAP CARD

DESCRIPTION

The 53A-450 Wire-Wrap Card is a printed circuit board assembly for use in a CDS 53/63 System. The card is provided with standard interface circuitry, including data and timing gates, flag circuitry, interrupt circuitry, and address selection logic. In the remaining space, a hole pattern is provided on a 0.1 inch grid which allows for the installation of wire-wrap sockets.

The 53A-450 Wire-Wrap Card is intended to be used to create special circuit interfaces to the 53A System which are not performed by any of the standard system cards. The effort involved in the design and construction of these special interfaces can be substantially reduced through the proper use of the Wire-Wrap Card.

CONTROLS AND INDICATORS

The following controls and indicators are provided to select and display the functions of the 53A-450 Card's operating environment.

Address-Select Switch

The 53A-450 Card has a miniature 10-position switch labeled "ADDRESS" that selects the 53A-450 Card's address (0-9) in the 53/63 Series System. The switch's cover opens to allow the address to be reselected. A screwdriver with a narrow, flat blade should be used to turn the cam-action wiper to the desired address position.

Power LED

The Power LED provides a valuable diagnostic tool by giving the system programmer a visual indication of the action which the system is currently taking. Whenever the 53A-450 Card is addressed by the system controller, the Power LED goes out. The LED remains out until another function card is addressed. Since only one function card can be addressed at a time, an unlit Power LED indicates the function card with which the system controller is currently communicating. The Power LED being lit not only indicates that the 53A-450 Card is unaddressed, but that all required dc power (5V dc, ±15V dc) is being supplied.

Fuses

A two amp fuse is provided on the 5V power bus and protects the 53A System from overload conditions. If the fuse has blown, the Power LED will not light.

SPECIFICATIONS

Function:	Allows creation of special circuit interfaces to the 53A System which are not performed by any of the standard system cards.
Circuitry Provided:	Data Input Data Output Reset/Stop Gates Timing Gates Command Decode Gates Flag Flip-Flop Interrupt Flip-Flop Address Selection Logic Encode Driving/Sensing Buffered Crystal Time Base (2 MHz, 1 MHz, 100 Kc)
Logic Levels:	TTL Compatible.
Mounting Position:	Any orientation.
Cooling:	Provided by the fan in the 53/63 Card Cage.
Temperature:	-10°C to +65°C, operating (assumes ambient temperature of 55° and airflow to assure less than 10°C temperature rise). -40°C to +70°C storage.
Humidity:	Less than 95% R.H., noncondensing.
Dimensions:	197mm High, 220mm Deep, 13mm Wide (7.75" x 8.66" x 0.5")
Dimensions, Shipping:	When ordered with a 53A-002 Card Cage, this card will be plugged into one of the Card Cage system slots. When ordered alone, the shipping dimensions are: 254mm X 254mm X 127mm (10" X 10" X 5")
Weight:	0.23Kg. (0.5 lbs.)
Weight, Shipping:	When ordered with a 53A-002 Card Cage, this card will be plugged into one of the Card Cage System slots. When ordered alone, the shipping weight is: 0.64 Kg. (1.4 lbs.)
Required Equipment:	CDS 53A-780 Hooded Connector
Equipment Supplied:	53A-450 Wire-Wrap Card Spare Fuse (Part #42202-52001) Operating Manual (Part #00000-14500) Service Manual (Part #00000-24500)

53A SYSTEM OVERVIEW

The 53A System is just what its name implies, an "ASCII Party Line System". The main objectives of the system are to allow a system controller such as a computer or calculator to address one of a number of possible interfaces and communicate with the interface using ASCII characters.

Throughout this and other CDS manuals the terms input and output are used. Input means data input by the system controller from the 53A System. Output means data output by the system controller to the 53A System.

The mainframe (from left to right) has 13 card slots which provide for:

1. One Chaining Card for connecting up to 10 53A-002 Card Cages to a single I/0 port of the system controller.

2. One Communications Card for communicating with the system controller. The user is free to choose different electrical characteristics and communication formats between the system controller and the 53A System by changing Communications Cards - i.e., ASCII 8-bit parallel, IEEE-488, EIA RS-232C, buffered EIA RS-232C. However, with any format the data transfer will always be ASCII characters and decimal notation.

3. One Control Card which performs a hardware function for the 53A System analogous to a software executive in a computer. The card identifies system level commands, provides address control, provides a central interrupt register, and initiates system timing signals.

4. Ten System Cards which plug into system card slots numbered 0 through 9. The Wire-wrap card will plug into one of these slots. The backplane wiring is identical for all 10 slots.

NOTE: In the sections that follow, Pin Numbers given in parentheses, i.e. (Pin #81) refer to Backplane Pin Assignments. Numbers given in brackets, i.e. [52] refer to Signal Access Points on the Wire-Wrap Card itself.

Backplane

The backplane of the 53A System supports a communications scheme, for the system cards, which is bi-directional 8-bit parallel ASCII characters plus flag, control and I/0. In addition, many functions are available on the backplane which will aid the designer in the development of a special purpose card. These functions include:

1. Address Select/Interrupt Lines (0-9). The Control Card handles all address selection and interrupt signals for the 53A System.

2. Timing pulses T3 through T14. The Control Card provides a non-overlapping temporal reference which may be used to sequence the logic on the Wire-Wrap Card.

3. The ASCII characters A, B, C, I, J, K, P, Q, R, and S are decoded by the Control Card. A line representing each of these characters is available on the backplane.

4. Precision time base. The Control Card provides a 2 MHz, 1 MHz and 100 KHz crystal controlled time base that can be utilized by the Wire-Wrap Card.

5. Stop Line. The Stop line can be used by the Wire-Wrap Card to set a preset or initial condition.

6. Restart Line. The Restart line can be used by the Wire-Wrap Card to set a preset or initial condition on power-up only.

7. Binary Line. The Binary line can be used by the Wire-Wrap Card in order that it may input/output 8-bit binary, as well as ASCII, characters.

8. An analog bus is available on the backplane to route analog signals between system cards.

9. Power supply voltages +5V and ±15V are available to the Wire-Wrap Card. (±15V requires 53A-062 internal power supply.)

Addressing

The 10 address select lines (0-9) are actually bi-directional signals used both for selecting an active System Card and identifying interrupting System Cards.

Before commands or data can be input or output from a system card, that card must be addressed. A system card is addressed by sending @XY from the system controller to the 53A System. The @ character is a delimiter used by the 53A System. The X in the command sequence is the mainframe address (0-9) which has been selected by a switch on the Control Card. The Y in the command sequence is the system card address (0-9) selected on the Card's address select switch.

When the Control Card detects an @ character output from the system controller it will automatically unaddress any previously addressed system card. The very next character following the @ must be the Control Card's address or the Control Card will ignore all future characters and commands except character decodes (A, B, C, I, J, K, P, Q, R, and S).

If the character following the Control Card address is a numeral (0-9) the Control Card will pull the corresponding address select line on the backplane (Pins #65 through 74) low. The line will remain low until the Control Card detects another @ character output by the system controller or the STOP* line is pulled low.

The Wire-Wrap Card will utilize the address line by inhibiting all its input and output logic unless the address line selected by the Wire-Wrap Card's address select switch is low.

Interrupt

System cards cannot "interrupt" in a usual sense. If an unselected card's flag were to set, the entire 53A System would go into the "busy" condition and the controller could do nothing to regain control short of using the STOP signal.

A system card that wants to interrupt the system controller will do so by setting the Request For Interrupt (RFI) line (Pin #48 on the backplane) low. This line can go low at anytime and should remain low until the interrupting condition is cleared.

After the system controller has detected the interrupt it will send the ASCII characters @XS to the 53A System to determine which card or cards caused the interrupt. The X in the command sequence represents the mainframe address selected on the Control Card (for a detailed explanation of this command sequence see the 53A-171 Control Card Operating Manual). When the command sequence @XS is received by the Control Card, the Control Card will pull the Interrupt Check (INT CHK) line (Pin #76 on the backplane) low. Any system cards that have pulled the RFI line low should then pull their own address line low no later than 50 nanoseconds after the INT CHK line goes low, and maintain this condition until at least 10 nanoseconds, but no more than 100 nanoseconds after the INT CHK returns high.

NOTE: If the interrupt circuitry provided on the Wire-Wrap Card is utilized, these timing requirements will automatically be met.

Timing Pulses

The falling edge of the CONTROL line (Pin #5) will cause the Control Card to initiate non-overlapping timing pulses T1 through T14. T1 and T2 are used internally by the Control Card and only T3 through T14 are available on the backplane.

The first available timing pulse, T3 will occur from 2 to 2.5 microseconds after the falling edge of CONTROL. The timing pulses T4 through T14 will follow T3 at 500 nanosecond intervals and will be nominally 200 nanoseconds and a minimum of 150 nanoseconds wide. The one exception to this rule is the case where the FLAG is cleared prior to the timing pulse T14 occurring. As soon as the Wire-Wrap Card or any system card clears the FLAG, all timing pulses will cease and the data on the backplane will no longer be valid. The Wire-Wrap Card must be prepared to accept another control cycle, either input or output, immediately upon clearing the FLAG.

Character Decode Lines

If an ASCII character A, B, C, I, J, K, P, Q, R, or S is output from the system controller to the 53A System, the Control Card will decode the character and pull the corresponding line (Pin #63, 64, 9, 1, 54, 55, 56, 57, 11 or 12) low respectively. In addition to pulling the character decode line low the corresponding ASCII character will be present on the output data lines OB0 through OB7. Only one character decode line can be set low at any one time.

The FLAG* (See FLAG Section) must be set and cleared by the system card that was addressed even though the character was decoded by the Control Card. The character decode line will go low and remain low in all card cages of a chained system until the system controller clears control (control line returns high as a result of a returned FLAG*).

The Control Card will not decode these characters if the characters are input from the 53A system to the system controller or if they are output from the system controller while the BINARY* line (Pin #6) is low.

The character decode line will go low within 550 nanoseconds after the falling edge of CONTROL* and will remain low for at least 100 nanoseconds after the rising edge of FLAG*.

HALT and STOP

The HALT Command @XH is a method of programmatically pulling the STOP* line (Pin #3) low. The @ character is a delimiter used by the 53A System. The X in the command sequence is the mainframe address (0-9) which has been selected on the Control Card. When the @XH command is output from the system controller, the 53A System STOP* line in the mainframe defined by X will set low until the next character is output. This line will also remain low for approximately 10 milliseconds after power-up.

The STOP* line can also be pulled low directly by the system controller via the Communications Card being used:

A. The 53A-121 Communications Card pulls the STOP* line low whenever the CLEAR line on its front edge connector is pulled low.

B. The 53A-123 Communications Card pulls the STOP* line low whenever the STOP IN line on its front edge connector is set true.

C. The 53A-124 Communications Card pulls the STOP* line low whenever the CLEAR IN line on its front edge connector is pulled low.

D. The 53A-127 Communications Card pulls the STOP* line low whenever the system controller sets the IEEE-488 IFC line.

Pulling the STOP* line low unaddresses and sets the initial (preset) conditions of all system cards which use the STOP* signal in all mainframes of a chained system. Pulling the STOP* line low via the Communications Card or turning the power off and back on are the only methods of clearing a system that has hung-up from an illegal operation - i.e., a request for input from a nonexistent system card.

CONTROL

The CONTROL* line on the backplane is set (low) and cleared (returned high) by the Communications Card. This line is used by the Control Card to initiate timing pulses whenever the system controller (calculator or computer) has data for output to the 53A System or is ready for data input from the 53A System.

The CONTROL* signal isn't used by the standard CDS 53A System cards to sequence circuit operations. We recommend that the designer avoid this signal in the design of the Wire-Wrap Card. The reason is that the Control Card performs operations after CONTROL* goes low but before T3* occurs (on T1* and T2*) which may cause changes in the system's current operating modes. For example, if the output character is an @, the system card presently addressed when CONTROL* goes low will be unaddressed by the time T3* goes low.

FLAG

The FLAG* is a signal from either the Control Card or an addressed system card. The FLAG* is sent to the system controller (calculator or computer) via the Communications Card to signal the completion of a control cycle for input or output data.

The following design rules apply for the FLAG*:

1. The FLAG* may be set (low) simultaneously with the falling edge of T3* or any time thereafter by an addressed system card.

2. The FLAG* must be set (low) for a minimum of 200 nanoseconds, the width of one timing pulse.

3. An unaddressed system card must not set the FLAG*.

4. If no system card is addressed, it is the responsibility of the Control Card to set and clear the FLAG*.

5. An addressed system card must set and clear the FLAG* for all input and output characters even though some of these characters may not be used by the system card that is addressed. The reason for this is that many system controllers will automatically output ASCII characters (such as CR, LF, leading zeroes, leading or trailing blanks, plus and minus sign, decimal point, E, comma, and NULL characters) even though they aren't included in the user's software program or have a particular function on the card.

6. If the input or output operation is completed prior to timing pulse T14 occurring, one of the timing pulse signals can be used to set the flag flip-flop. The flag flip-flop can then be cleared by another timing pulse. If the card operation continues past timing pulse T14, the user must provide circuitry to pulse the Flag set [54] and Flag clear [55] at the appropriate times.

7. Depending on whether the Wire-Wrap Card is in input or output, there are additional constraints on when the Flag must be set and cleared. See the subsections entitled, Step 1: Understanding Output Data, and Step 2: Understanding Input Data.

WIRE-WRAP CARD OVERVIEW

There are six basic steps required in order to produce an operable special purpose card using the Wire-Wrap Card:

Step 1: Understanding Output Data

Prior to the falling edge of CONTROL* a single ASCII character is output (I/O line low) from the system controller to the 53A System. The output data lines [21 through 28] and the I/O line [53] on the Wire-Wrap Card will be valid at least 10 nanoseconds before the falling edge of CONTROL* [36] and will remain valid at least 40 nanoseconds after the rising edge of FLAG* (Pin #24).

All system cards of the ASCII Party Line System are designed to receive output data from the system controller just as though the system controller was communicating with a high speed data terminal. The system controller will output data to the 53/63 System directly from the user's application program via ASCII characters using decimal notation. To insure that the Wire-Wrap Card will correctly receive data from any controller language (i.e., BASIC, FORTRAN, COBOL and etc.), and any Communications Card interface, the designer should obey the following design rules:

1. Avoid the use of the @ character as a command character or as data for the Wire-Wrap Card since this character is reserved as an address delimiter for the 53A System.

2. Avoid using quotation marks, NULL, CR, LF, DELL, lower case letters, any nonprinting characters or edit characters such as back arrow to sequence card operations. Many system controllers either can't output these characters or in some cases, characters such as CR, LF will automatically be output on a regular basis.

3. Avoid using the 8th ASCII bit as a data bit, since it is a parity bit and many system controllers will automatically set this bit as odd or even without the programmer having any control over it.

4. Expect numbers to be output by the system controller in decimal notation with the most significant digit first. Some controllers, though, may not output a CR/LF to terminate a data string. It is recommended that the Wire-Wrap Card designer require data strings output to his card be terminated with an upper case ASCII letter. By using an ASCII letter to terminate a string, the programmer will be free to string together commands and data to many system cards within a single line of program code. This will not only simplify programming but will increase the speed of execution. From the Wire-Wrap card designers point of view, the upper case ASCII letter terminator provides a very convenient signal at the end of an output data string that says "now go act on the data you have received".

5. Watch out for the problem of leading zeros. If the number to be output by the system controller was 123 there wouldn't be a problem. But what if the required number was 009? It is difficult for some system controllers to output leading zeros. If the Wire-Wrap card is to receive numeric data 0 through 999, the card should function correctly if the number nine is received as 009 or 9 without leading zeros.

6. Avoid using the 53A System I/0 or address select lines for strobe pulses. Instead, use the timing pulses T3 through T14 or the decoded backplane characters (A, B, C, I, J, K, P, Q, R, S).

   For example, if the card were to use the address line to produce a strobe pulse for latching data, the card would have to be unaddressed and then re-addressed between each character transferred.

7. It is best to sequence card functions using single character commands that will have a logical meaning to the eventual user of the card, i.e., C for Clear of Close, A for Amplitude, etc. Avoid the use of "special" bit patterns output from the system controller to sequence hardware functions. Doing so may quickly solve a hardware problem, but will almost always create a software nightmare later. If the 10 decoded backplane characters (A, B, C, I, J, K, P, Q, R, S) don't meet your needs, it is best to decode the required characters on the Wire-Wrap Card itself.

8. If the Wire-Wrap circuit needs a precision clock, don't use the timing pulses. The Control Card can be set for different timing pulse rates. For precision pulses use either the 2 MHz, 1 MHz or 100 KHz time bases provided; [63], [62], [61] respectively.

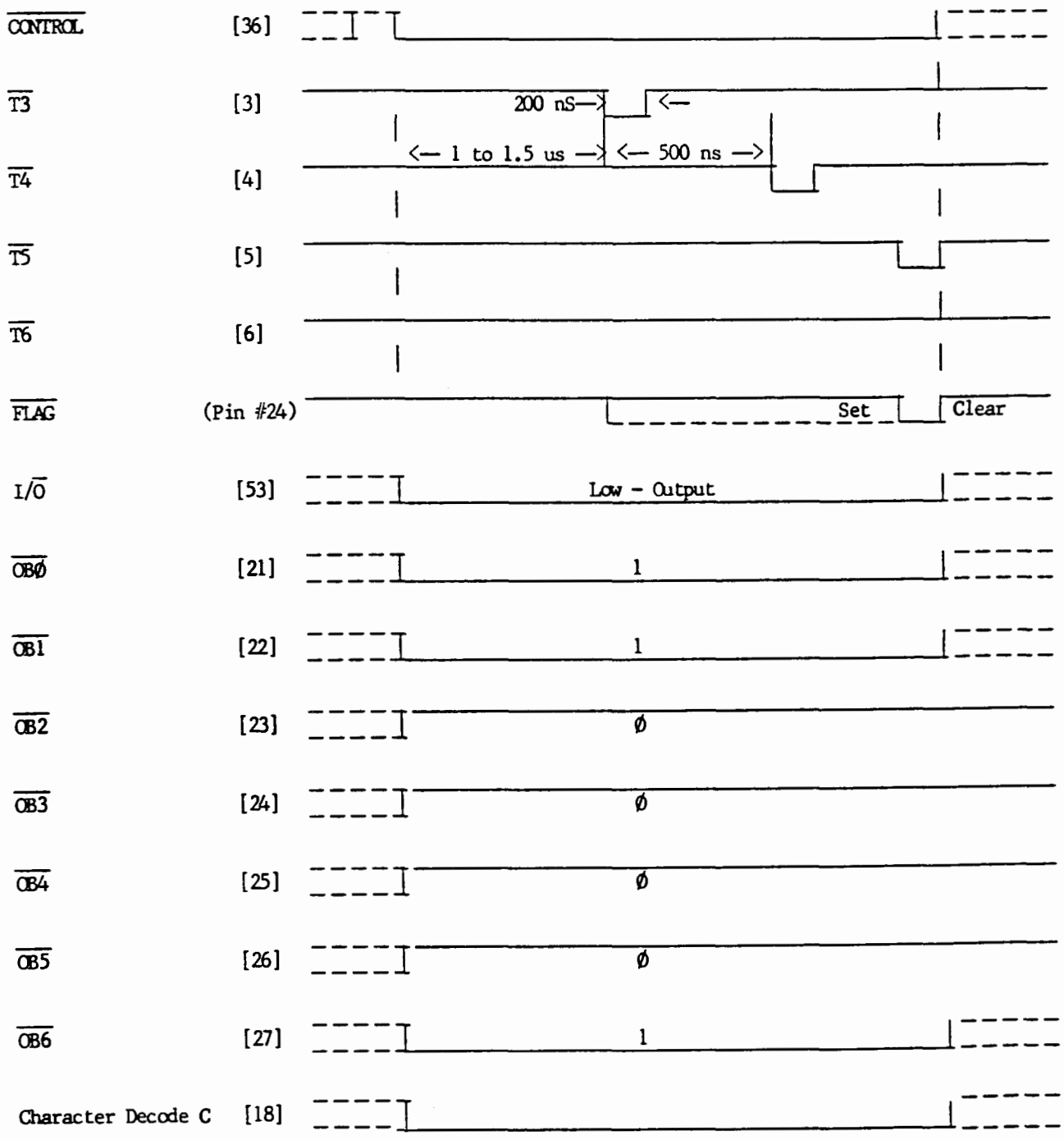


Figure 450-1: Timing Diagram - Output Character C from System Controller

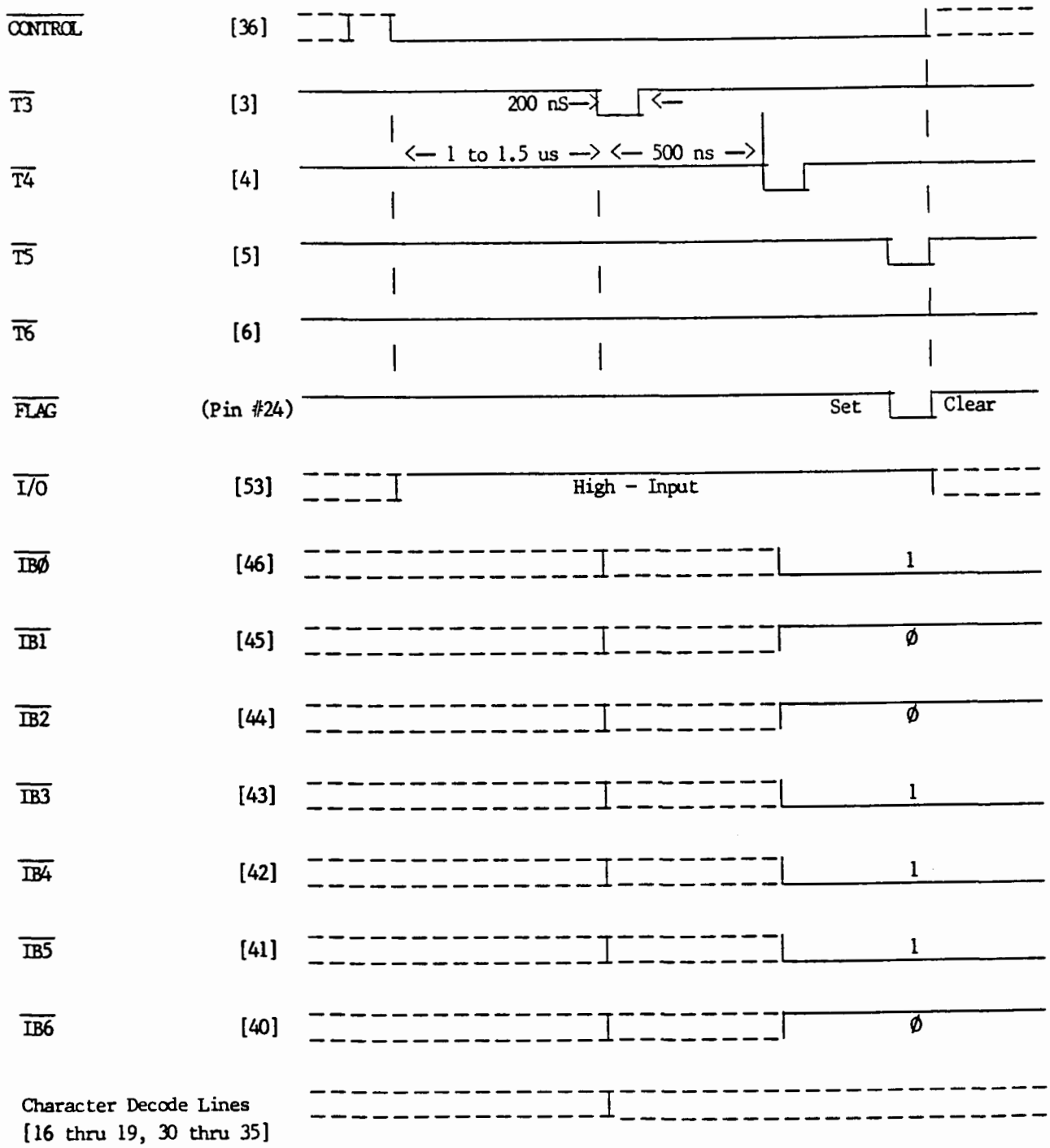


Figure 450-2: Timing Diagram for ASCII Character 9 Input

Figure 450-1 shows a timing diagram for an ASCII character C output from the system controller. From the diagram it can be seen that the data lines (OB0 through OB6), I/O line, and Character Decode line C will be valid well before T3 and will remain valid until FLAG is cleared. In this example FLAG was cleared on T5 and therefore T6 through T14 did not appear. The parity bit OB7 will also be valid during this time; however, its state wasn't shown since this would depend on whether odd or even parity was output by the system controller.

The output data is sourced by the Communications Card to the Wire-Wrap Card. The receiving circuits on the Wire-Wrap Card for the output data lines [21 through 28], timing pulses [3 through 14], letter decodes [16 through 19, 30 through 35], control [36] and binary [37] are tri-state receivers whose outputs are only active when the Wire-Wrap Card is addressed and the control card is not checking interrupt status (@XS command). When the Wire-Wrap Card is unaddressed or the control card is checking interrupt status, these low true lines will "float" at the tri-state high impedance level and are, therefore, susceptible to possible noise spikes.

If the circuitry used by the Wire-Wrap Card designer to receive these signals cannot tolerate possible noise spikes on these lines when the Wire-Wrap Card is unaddressed, it is recommended that used lines be pulled up to +5V with a 10K resistor. Dip resistors such as Beckman 898-1R-10K (15 resistors per package) provide an efficient means of doing this.

Step 2: Understanding Input Data

Figure 450-2 shows a timing diagram for an ASCII character 9 input (I/O line high) by the system controller from the system card. The system controller can accept an ASCII input character any time after CONTROL is set low. As shown, FLAG can be set (low) by the Wire-Wrap Card any time after T3, however, the signal presented to the backplane must be valid for at least 200 nanoseconds before FLAG is set. FLAG must remain low for a minimum of 200 nanoseconds, one timing pulse, before being cleared. The data must remain valid on the backplane until the next T3 or the card is unaddressed.

The IB bus data is not driven active by the 53A-450 Card unless the I/O line is high (to guarantee proper operation of serial polling in a 53/63 IEEE-488 system, the IB data bus may only be driven when the card is addressed and the I/O line is high).

In practice, CONTROL isn't used by system cards and input operations start with T3. Data will be valid on the backplane at TN. FLAG will be set with the falling edge of T(N+1) and cleared with the rising edge of T(N+1). The data will remain valid on the backplane until the next T3 or the card is unaddressed.

Numbers should be presented to the system controller with the most significant digit first and the last character of any string should be terminated by Carriage-Return and Line-Feed characters.

Step 3: Understanding The Electrical Parameters

On the schematic diagram of the 53A-450 Wire-Wrap Card, the schematic symbols are to be interpreted in accordance with MIL-STD-866B. Table I and Table II list the available signal connection points with a brief explanation of their function. The logic levels are all standard TTL[1] and logic-loading references are all in terms of standard TTL inputs (See: Table III - Signal Access Points - Input/Output Loading).

The following power budget guidelines should be used when designing circuits which will be implemented using the 53A-450 Wire-Wrap Card.

1. Vcc (+5.0V) and ground busses are routed at the top and bottom of the Wire-Wrap Card, respectively. A 0.1 microfarad capacitor (typically ceramic) should be provided between Vcc and ground for each set of four or five ICs. The current drain on the 5V should not exceed 1.5A.

2. If the ±15V supply is to be used, it must be by-passed with 15 to 33 microfarad capacitors (typically miniature electrolytics) to ground. The current budget is 1.0 A for the entire 53A-002 Card Cage.

Step 4: Design

This step is, of course, largely a function of the desired characteristics of the circuit to be designed. Considerable attention must be paid to keeping the design within the scope of the Wire-Wrap Card (number of ICs, number of discrete components, power supply drains, etc.). Making maximum use of the circuitry and signals already provided on the Card will help minimize problems in this area.

Step 5: Wire-Wrap The Card

IC sockets are designed to accept most standard wire-wrap tools. A Gardner Denver 14XA2 wire-wrap gun or equivalent with appropriate wrapping bit and shield and AWG 30 wire is recommended. The Vcc and ground connections to the ICs should be installed first. The signal wire (IC interconnections) should be installed "point-to-point" along the shortest possible path in order to reduce the ill effects of cross-coupling. Discrete components may be installed on plug-in DIP component platforms or soldered into the printed board pads provided as required.

Step 6: Checkout

CAUTION:

Failure to turn off power before removing or inserting a card may cause damage to the card.

Once the card has been wire-wrapped, it may be checked for proper operation in the 53A system. The descriptions of the signals in Table I and Table II will facilitate this effort. If the circuit fails to operate correctly, the following steps represent an orderly approach to checking out the interface functions:

1. Verify that the supply voltages on the card are correct.

2. Verify that the card has been selected (Power LED out).

3. Verify that the STOP LED on the Control Card isn't lit.
4. Verify that the proper I/0 mode prevails. The Control Card I/0 LED will be out for Output and lit for Input. Output is data from the system controller to the 53A system.

5. Verify that CONTROL is going low (Control LED on the Control Card lit) for each character transfer.

6. Verify that circuit operations don't start until T3.

7. Verify that all input data is valid on the backplane for at least 200 nanoseconds before FLAG is set.

8. Verify that all input data is valid on the backplane after FLAG is cleared until the next T3 or until the card is unaddressed. If the 53A-450 is not being used in a chained 53/63 system, the data needs to be valid for only 500 nanoseconds after the trailing edge of FLAG. To accommodate future use in a chained system, however, it is highly recommended that data be held valid until the beginning of the next cycle or until the card is unaddressed.

9. Verify that FLAG has a minimum pulse width of at least 200 nanoseconds.

10. Verify that the data bits are correct (proper ASCII character code).

11. Verify that the design function of the wire-wrapped circuit has been properly achieved.

If problems are encountered which require circuit modifications, they may be easily accomplished on the Wire-Wrap Card. Trouble-shooting access can be enhanced with the use of the 53A-850 Extender Board.

TABLE I - Backplane

Wire-Wrap Card Signal Access Point Number	Pin #	Backplane Signal Name	Backplane Function/Description
Bus-Top Edge of Card	1	5V Supply Bus	Basic integrated circuit supply voltage.
	2	5V Supply Bus	Current Budget 1.8A/Card.
56(Note 1)	3	STOP*	The STOP* line is pulled low by the Communications Card typically when the system controller is reset. To see how this line can be utilized, see the STOP and HALT Command sections of a 53A System card Operating Manual. The STOP* line is also pulled low by the programmable HALT Command @XH. Furthermore, this line will remain low for approximately 10 milliseconds after power-up. For more details on the @XH command see the 53A-171 Control Card Operation Manual.
53	4	I/0* Mode	Input/Output function identifier. High for input data (data from 53A System to system controller), low for output data. Line is driven by system controller via the Communications Card. The I/0 signal will be valid at least 10 nanoseconds before the falling edge of CONTROL* and will remain valid at least 40 nanoseconds after the rising edge of FLAG*.
36	5	CONTROL*	The Control line goes low when the system controller wishes to initiate a character transfer (input or output). The line is driven by the system controller via the Communications Card. This line should not be used in the Wire-Wrap Card design. Use T3 to initiate a character transfer instead.
37(Note 2)	6	BINARY*	This is a bi-directional signal that may be sourced and received by both system cards and the Communication Card.

Access Point Number	Pin #	Backplane Signal Name	Backplane Function/Description
			This line can be pulled low by the system controller via the Communications Card, or it may automatically be pulled low by some system cards such as the 53A-430 UART Card. If the 53A System is in output and this line is low, the system is said to be in "I/0 Lock" since the Control Card is inhibited from acting on the address delimiter (@) output from the system controller and addressing a new system card. When the BINARY* line is low the @ character will be passed through the 53A System as data and the user will have the ability to output eight bit binary data. The BINARY* line should also be used when inputting binary data since it disables parity bit generation on the control card, thus allowing the Wire-Wrap Card to return 8-bit binary data to the system controller. As an output to the wire-wrap, BINARY* will be valid at least 10 nanoseconds before the falling edge of CONTROL* and will remain valid at least 40 nanoseconds after the rising edge of FLAG*. As an input from the Wire-Wrap card BINARY* should be set low at least 200 nanoseconds before the falling edge of FLAG* at the beginning of the protected or "I/0 Locked" series of operations and returned high no sooner than 10 microseconds after the rising edge of FLAG* at the end of the protected operation. Recommended design is to return a <CR> and <LF> character following the protected operation and to set BINARY* back high at T3* of the <CR> character. The circuit for directly driving the backplane binary line must be an open collector device capable of sinking 36mA to a level of 0.2V maximum.
	7	+18V Supply Bus	Not available at this time.
	8	Reserved	Not for use by the 53A-450 Wire-Wrap Card.
18	9	C*	This line will be pulled low by the Control Card whenever the Control Card detects an ASCII C output by the system controller to the 53A System.

Access Point Number	Pin #	Backplane Signal Name	Backplane Function/Description
			This signal will go low no more than 550 nanoseconds after the falling edge of control and will remain low for at least 100 nanoseconds after the rising edge of FLAG*.
19	10	I*	Same as Pin #9 except the ASCII character is I.
34	11	R*	Same as Pin #9 except the ASCII character is R.
35	12	S*	Same as Pin #9 except the ASCII character is S.
3	13	T3*	A timing signal generated by the Control Card and utilized by all system cards to sequence card logic. This signal goes low 1 to 1.5 microseconds after the falling edge of CONTROL* (Pin #5) and stays low for a minimum 150 nanoseconds.
4	14	T4*	The same as Pin #13 except the signal goes low 0.5 microseconds after T3*.
5	15	T5*	The same as Pin #13 except the signal goes low 1.0 microseconds after T3*.
6	16	T6*	The same as Pin #13 except the signal goes low 1.5 microseconds after T3*.
7	17	T7*	The same as Pin #13 except the signal goes low 2.0 microseconds after T3*.
8	18	T8*	The same as Pin #13 except the signal goes low 2.5 microseconds after CONTROL*.
9	19	T9*	The same as Pin #13 except the signal goes low 3 microseconds after T3*.
10	20	T1O*	The same as Pin #13 except the signal goes low 3.5 microseconds after T3*.
11	21	T11*	The same as Pin #13 except the signal goes low 4.0 microseconds after T3*.
12	22	T12*	The same as Pin #13 except the signal goes low 4.5 microseconds after T3*.
58(Note 3)	23	RESTART*	The backplane RESTART* line is pulled low by 59 (Note 4) the Control Card for a minimum of 10 milliseconds after 5V power is applied to the 53A System Backplane.

Access Point Number	Pin #	Backplane Signal Name	Backplane Function/Description
			This line can also be pulled low by any system card that wishes a restart time longer than 10 milliseconds. The effect of the restart line is to cause all system cards to go to their initial condition on power-up and to prevent the system from sending data until all cards are up and ready. Whenever RESTART* is low, STOP* will also be low. However, the reverse is not true.
	24	FLAG*	"Hand-Shaking" signal. System cards set this line low for a minimum of 200 nanoseconds to indicate to the system controller (via the Communications Card) that the output character has been accepted or the data is valid for the requested input character.
21	25	OB0*	Output data bit 0 Low true data from the system controller to the 53A System.
46(Note 1)	26	IB0*	Input data bit Low true data from the 53A System to the system controller.
22	27	OB1*	Output data bit 1.
45(Note 1)	28	IB1*	Input data bit 1.
23	29	IB2*	Output data bit 2.
44(Note 1)	30	IB2*	Input data bit 2.
24	31	OB3*	Output data bit 3.
43(Note 1)	32	IB3*	Input data bit 3.
25	33	OB4*	Output data bit 4.
42(Note 1)	34	IB4*	Input data bit 4.
26	35	OB5*	Output data bit 5.
41(Note 1)	36	IB5*	Input data bit 5.
27	37	OB6*	Output data bit 6.
40(Note 1)	38	IB6*	Input data bit 6.
28	39	OB7*	Output data bit 7.

Access Point Number	Pin #	Backplane Signal Name	Backplane Function/Description
39(Note 1)	40	IB7*	Input data bit 7.
	41	Sig. S. Bus	Scanner Common "Spare" or fourth wire. Pin #41, 42, 43, 44 and 45 comprise the backplane analog buss. The buss is used to route analog signals from 53A-331 Reed Relay Scanner Cards to instruments.
	42	Sig. L. Bus	Scanner Common "Low" signal.
	43	Sig. G. Bus	Scanner Common "Guard" signal.
	44	Sig. G. Bus	
	45	Sig. H. Bus	Scanner Common "High" signal.
64(Note 4), 65(Note 5)	46	ENCODE	This backplane line is pulled low by the 53A-331 Reed Relay Scanner Card whenever a scanner channel is closed. The encode signal is used to trigger instrumentation and is accessed by the backplane 86-Pin connector or by the backplane Analog Output Connector (P41). This Wire-Wrap Card can issue an encode command by pulling this line (See Note 2) low for a minimum of 500 microseconds.
	47	60 Hz Synch.	Not available at this time.
	48	RFI*	The Request For Interrupt (RFI) line is pulled low by a system card whenever it requires service from the system controller. This line may go low at anytime and should remain low until the card is serviced. The driving circuit must be open-collector capable of sinking 36 mA to a level of 0.2V maximum. See Table II, Additional Wire-Wrap Card Signals, 48, 49, 50.
13	49	T13*	The same as Pin #13 except the signal goes low 5.0 microseconds after T3*.
14	50	T14*	The same as Pin #13 except the signal goes low 5.5 microseconds after T3*.
	51	Reserved	Not for use by the 53A-450 Wire-Wrap Card.
	52	Reserved	Not for use by the 53A-450 Wire-Wrap Card.
	53	Reserved	Not for use by the 53A-450 Wire-Wrap Card.

Access Point Number	Pin #	Backplane Signal Name	Backplane Function/Description
30	54	J	Same as Pin #9 except the ASCII character is J.
31	55	K	Same as Pin #9 except the ASCII character is K.
32	56	P	Same as Pin #9 except the ASCII character is P.
33	57	Q	Same as Pin #9 except the ASCII character is Q.
63	58	2 MHz	This signal is from the crystal time base located on the Control Card.
	59	Reserved	Not for use by the 53A-450 Wire-Wrap Card.
61	60	100 KHz	This signal is from the crystal time base located on the Control Card.
	61	-18V Supply Bus	Not available at this time.
62	62	1 MHz	This signal is from the crystal time base located on the Control Card.
16	63	A*	Same as Pin #9 except the ASCII character is A.
17	64	B*	Same as Pin #9 except the ASCII character is B.
	65	SELECT 0*	This line will be pulled low by the Control Card whenever the Control Card detects @XY characters transmitted from the system controller to the 53A System. The X in the command sequence represents the mainframe address (0-9) selected on the Control Card. The Y in the command sequence represents this select code "0". The address of the Wire-Wrap Card can be set for "0" by setting the card's address select switch to the "0" position. This line is bi-directional and is used both for selecting an active system card and for identifying interrupting system cards. When the Wire-Wrap Card with address 0 is selected, the SELECT 0* line will go low at least 1.5 microseconds prior to the falling edge of T3 associated with the next character after Y in the command sequence @XY. The line will remain low until another @ character is output to the control card. The line will go high approximately 500 nanoseconds after the falling edge of the control pulse associated with the @ character.

Access Point Number	Pin #	Backplane Signal Name	Backplane Function/Description
			When the Wire-Wrap Card sources the Select signal to identify itself as an interrupting device, the line must be driven by an open-collector device capable of sinking 36mA to a level of 0.2V maximum. Circuitry has been provided on the Wire-Wrap Card to handle both receiving the SELECT 0 signal (Wire-Wrap Card addressed [52]) and sourcing the SELECT 0* signal (Wire-Wrap Card identifies itself as an interrupting system card [48], [49], [50]). See: Table III, Additional Wire-Wrap Card Signals, for a description of [48], [49], [50] and [52].
	66	SELECT 1*	Same as Pin #65 except Y equals 1.
	67	SELECT 2*	Same as Pin #65 except Y equals 2.
	68	SELECT 3*	Same as Pin #65 except Y equals 3.
	69	SELECT 4*	Same as Pin #65 except Y equals 4.
	70	SELECT 5*	Same as Pin #65 except Y equals 5.
	71	SELECT 6*	Same as Pin #65 except Y equals 6.
	72	SELECT 7*	Same as Pin #65 except Y equals 7.
	73	SELECT 8*	Same as Pin #65 except Y equals 8.
	74	SELECT 9*	Same as Pin #65 except Y equals 9.
	75	SCAN CLEAR*	The SCAN CLEAR* is a bi-directional signal issued from any scanner card (such as the 53A-331 Reed Relay Scanner Card) immediately after the scanner card has received a command from the system controller to close a scanner channel. The signal will open "clear" any other scanner channel in the system thereby preventing a short circuit caused by more than one scanner channel being closed at one time. The SCAN CLEAR* signal is routed from mainframe-to-mainframe via the Analog Chaining connector on the backplane.

Access Point Number	Pin #	Backplane Signal Name	Backplane Function/Description
			The signal will be low for a minimum of 500 microseconds. The signal can be received by a standard TTL gate with an input loading of 1 TTL load, but must be driven with an open collector device capable of sinking 500mA to a level of 0.2V maximum.
	76	INT CHK*	The Interrupt Check (INT CHK) line will be pulled low by the Control Card at any time it wishes to check the address of interrupting system cards. The Control Card will first return all Address Select lines (Pins #65 through 74) high before pulling the INT CHK* line low. The signal can be received by a Schmitt trigger which presents no more than one TTL load to the backplane.
	77	Reserved	Not for use by the 53A-450 Wire-Wrap Card.
	77	Reserved	Not for use by the 53A-450 Wire-Wrap Card.
	78	Reserved	Not for use by the 53A-450 Wire-Wrap Card.
	79	Reserved	Not for use by the 53A-450 Wire-Wrap Card.
	80	Reserved	Not for use by the 53A-450 Wire-Wrap Card.
	81	+15V Supply Bus	+15 volt when 53A-062 internal power supply is installed in mainframe. The power budget is one ampere per mainframe for 53A-062 Rev Level 02-A and below, two amperes for Rev Level 03-A and above.
	82	-15V Supply Bus	Same as Pin #81 except -15 volts.
	83	Ground for 18V	Not available at this time.
	84	Ground for 18V	
Bus-Bottom	85	Ground Bus	Power ground and logic signal ground.
Edge of	86	Ground Bus	Both system ground (DC power ground) and
Chassis Card			ground (AC power ground) are provided on the barrier terminal block on the rear of the Card Cage. The Card Cage is shipped with both grounds tied together by a shorting bar on the barrier terminal block at the rear of the mainframe.

NOTES:

1 Backplane Signal Active Low, Wire-Wrap Signal Active High
2 Receive Only.
3 RESTART REC, High True
4 RESTART XMIT, Low True
5 ENCODE REC, High True
6 ENCODE XMIT, Low True

TABLE II - Additional Wire-Wrap Card Signals

Wire-Wrap Card Signal Access Point Number	Signal Name	Function/Description
48	INT SET 2*	When the Wire-wrap Card wishes to initiate an interrupt to the 53A-171 control card, the interrupt flip-flop is set by pulsing INT SET 2* low for a minimum of 30 nanoseconds. The Wire-Wrap Card will then send a vectored priority interrupt to the control card each time the command sequence @XS is issued by the system controller until the interrupt flip flop is cleared (see INT CLR).
49	INT SET 1*	Performs same function as signal access point 48.
50	INT CLR*	The INT CLR* signal is pulsed low for a minimum of 30 nanoseconds to clear the interrupt flip-flop described under INT SEL* 1 OR 2.
52	SELECT*	The select line will go low whenever the Wire-Wrap Card is addressed (Power LED out). The line will go low at least 1.5 microseconds prior to the falling edge of T3 associated with the next character after Y in the command sequence @XY. The line will remain low until another @ character is output to the Control Card. The line will go high approximately 500 nanoseconds after the falling edge of the control pulse associated with the @ character.
54	FLAG SET*	Flag Set is pulsed low for a minimum of 30 nanoseconds to set the Wire-Wrap Card Flag flip-flop, which in turn sets the backplane Flag (Pin #24) low. The Flag flip-flop must remain set for a minimum of 200 nanoseconds (one timing pulse) to indicate to the system controller (via the Communications Card) that the output character has been accepted or the data is valid for the request input character.
55	FLG CLR*	FLG CLR* is pulsed low for a minimum of 30 nanoseconds to clear the Wire-Wrap Card Flag flip-flop.

TABLE III - Signal Access Points - Input/Output Loading

Wire Wrap Card Signal Access Point Number	Signal	True Sense	Standard TTL Fan-Out (In)
3	T3	Low-Tri State	15
4	T4	"	"
5	T5	"	"
6	T6	"	"
7	T7	"	"
8	T8	"	"
9	T9	"	"
10	T10	"	"
11	T11	"	"
12	T12	"	"
13	T13	"	"
14	T14	"	"
16	A	"	"
17	B	"	"
18	C	"	"
19	I	"	"
21	OB0	"	"
22	OB1	"	"
23	OB2	"	"
24	OB3	"	"
25	OB4	"	"
26	OB5	"	"
27	OB6	"	"
28	OB7	"	"
30	J	"	"
31	K	"	"
32	P	"	"
33	Q	"	"
34	R	"	"
35	S	"	"
36	CNTL	"	"
37	BNY	"	"
39	IB7	High	(1.25)
40	IB6	"	"
41	IB5	"	"
42	IB4	"	"
43	IB3	"	"
44	IB2	"	"
45	IB1	"	"
46	IB0	"	"

Wire Wrap Card Signal Access Point Number	Signal	True Sense	Standard TTL Fan-Out (In)
48	INT SET 2	Low	(1.25)
49	INT SET 1	Low	(1.25)
50	INT CLR	Low	(1.25)
52	SELECT	Low	10
53	I/O	High-Input Low-Output	10
54	FLG SET	Low	(1)
55	FLG CLR	Low	(1)
56	STOP	High	10
58	RESTART REC	High	10
59	RESTART XMIT	High	(1.25)
61	100 KHz	-	10
62	1 MHz	-	10
63	2 MHz	-	10
64	ENCODE RCV	High	10
65	ENCODE XMT	Low	(3)

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