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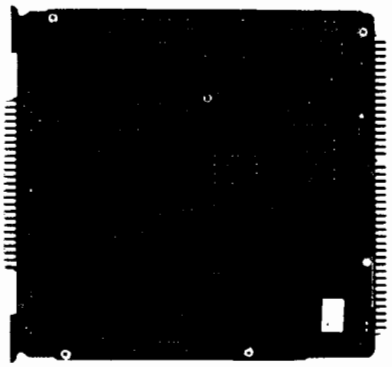
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53A-453 MIL-STD-1553A/B BUS SIMULATOR CARD

- **Functions as a Bus Controller, Remote Terminal (up to 32 RTs), or Bus Monitor**
- **MAC Air or 1553A/B output**
- **Programmable message rate and terminal response time**
- **Extensive error insertion and error detection of any word or message**
- **User definable number of data words can easily exceed 32**
- **Programmable analog output levels and input thresholds**



ORDERING INFORMATION

53A-453 - MIL-STD-1553A/B Bus Simulator Card
OPT 25 - Rise/Fall 100 nS
53A-653 - Data Cable
53A-780 - Hooded Connector

The MIL-STD-1553A/B Bus Simulator Card allows the system controller in an ATE System to test and simulate avionics devices via the MIL-STD-1553 data bus now being used in many military aircraft and communications systems. The Card functions either as a bus controller simulator, as a bus monitor, or as a single- or multi-remote terminal simulator with the capability of inducing and detecting various types of errors.

BUS CONTROLLER SIMULATOR

The user preloads the 53A-453 Card memory with the command and data words to be sent to each of up to 31 terminals plus broadcast mode. Individual terminal responses received by the 53A-453 Card are then stored in on-card memory by terminal number for later examination and analysis.

REMOTE TERMINAL SIMULATOR

The Card can simultaneously simulate up to 31 remote terminals. Response, data, and status words for each simulated remote terminal are pre-loaded in 53A-453 on-card memory. The preloaded messages are automatically transmitted when requested by the bus controller. All received data from the bus controller are stored in on-card memory for later evaluation.

BUS MONITOR

All 1553 bus traffic is observed and stored. The user can control the point at which monitoring and storing of up to 30,000 1553 words is initiated and terminated.

BITE

Seven LEDs provide Built-In-Test Equipment ("BITE") for the 53A-453 Card. One LED indicates that 1553 communication is occurring, three LEDs indicate the mode of operation, and two additional LEDs indicate sync and error status. A programmable self-test capability is included that can be invoked at any time.

Specifications

Modes (programmable):
Bus controller simulator, remote terminal simulator, or bus monitor.

Word Format:
Manchester bi-phase 20-bit word per MIL-STD-1553A/B.

Message Format:
Programmable command or status word plus a user-definable number of data words that can easily exceed the 32-word maximum of MIL-STD-1553.

Message Capability:
Any number of messages may be specified up to available buffer size.

Message Rate:
Bus Controller Mode, (time from end of one controller output to start of next controller output) programmable from 14 µsec to 65,535 µsec on an individual message basis. Remote Terminal Mode, (terminal response time) programmable from 4.25 µsec to 65,535.25 µsec on an individual message basis. Bus Monitor Mode, message rate is defined by active devices on bus.

1553 Bus Coupling:
Direct, 1:1 ratio, 55 Ohm isolation; Transformer Stub, 1.4:1 turns ratio.

Output Transformer:
Qualified to MIL-T-21038/27.

Buffer Capability:
30,000 20-bit words, user allocable between 32 terminal receive buffers.

1553 Analog Output:
Programmable as follows:

Direct Coupled.

Termination*	Output Range*	Nominal Step Size
35Ω	0.20 to 8.20	0.03V PTP
70Ω	0.30 to 13.75	0.05V PTP
1000Ω	0.75 to 34.40	0.19V PTP

*V PTP at 1553 bus with bus terminated in specified load.

Transformer Coupled.
70 Ohms nominal, 0.60 to 24.2V PTP; 0.09V PTP nominal step size.

Current Drive, 260 mA RMS max, direct-coupled output; 380 mA max, transformer-coupled output. Transition Time, >150 nsec and <250 nsec measured between 10% and 90% on waveform. Switch changeable to >220 nsec and <350 nsec.

1553 Analog Input:
Threshold, programmable from 0.50 to 9.00V PTP at direct-coupled input in 34 mV increments nominal (equivalent to 0.35 to 6.36V PTP at transformer coupled input in 24 mV increments nominal). Maximum Input, 40V PTP differential.

Message Synchronization:
The start of remote terminal operation or data collection may be synchronized to a user-specified pattern word received from the 1553 bus controller.

Induced Error Capability:
Programmable on an individual word basis for incorrect parity, Manchester error, dropped bit error, sync pattern error, incorrect bit count (±1 bit), incorrect bit transition time (±150 nsec), inter-message gap.
Programmable on an individual message basis for incorrect terminal response time, word count error, incorrect remote terminal status.

Other types of errors that may be induced are no remote terminal response, incompatible data flow ("bus crash"), Gaussian and common mode noise, incorrect message length, response time error.

Error Detection:
The following errors are detected and are distinguished on a priority basis; parity error, Manchester error, sync error, too many bits, too few bits, dropped bit, terminal response time (programmable 4 to 31 µsec), incorrect bit transition time, word count error, message format error, no data error, inter-word gap error.

Format Checking:
Internal firmware checks for the following:
Mode Code Commands, presence or absence of a data word and direction of data, usage of broad-cast command, illegal mode code in RT to RT transfer.
Broadcast Commands, absence of a response (normal and RT to RT transfer).
RT to RT Transfer, response by both RT's, consistent RT numbers, proper use of T/R bit, word count of both RT's consistent with actual word count, RT to RT broadcast checked for no response by a receive RT, illegal use of mode codes.
Other Format Checks, reserved bits no set, instrumentation bit not set in status word, no data words following a status word with busy bit set (even if requested), message error bit set, broadcast received and dynamic controller acceptance bits set only in response to transmit status mode command.

Data Throughput (via IEEE-488):
Required time to load 33 word data list, trigger, and read the one word status:
Normal, 105 msec*.
High Speed Mode, 50 msec*.
*Assumes IEEE-488 with less than 320 µsec bus turn-around time.
Blocked binary readback mode only appends CR/LF after all data in a buffer has been read. In IEEE-488 DMA transfers, this also applies to the EOI line.

Time Base:
16 MHz crystal oscillator. Optional external clock input from 15 MHz to 17 MHz.

Auxiliary Outputs (TTL):
Data Word Sync, High True, 1 µsec pulse at the end of each received word.
Position Identification Pulse, 125 nsec wide pulse occurring when user selected output word(s) are transmitted.
Status Error Output, Low True, 125 nsec min pulse, occurring each time a status word is received with message error bit set.
Reconstructed Received Data, NRZ, Low True, serial.
Reconstructed Received Data Clock, TTL.
Transmitted Data, NRZ, Low True, serial.
Transmitted Data Clock, TTL.
Receiving Data, Open Collector Output with on-card pull-up (10 KOhms), High True.

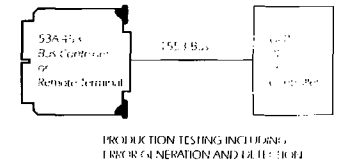
Auxiliary Inputs:
External Trigger, TTL, Low True pulse, 50 nsec min width.
External Halt, TTL, Low True pulse, 50 nsec min width.
Transmitter Output Disable, TTL, Low True.
Common Mode Voltage, ±10V max, DC to 4 MHz.

Programmed By:
ASCII Characters.
Data may be programmed directly in Binary.

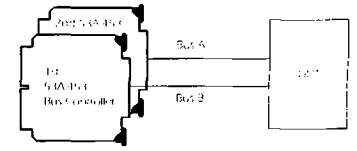
Recommended Cable:
53A-653.
53A-780.

Available Option:
OPT 25, rise/fall 100 nS.

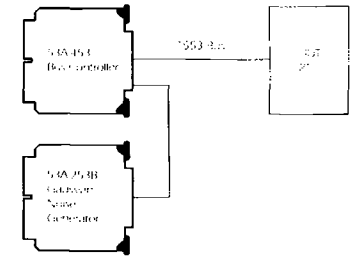
Typical Applications



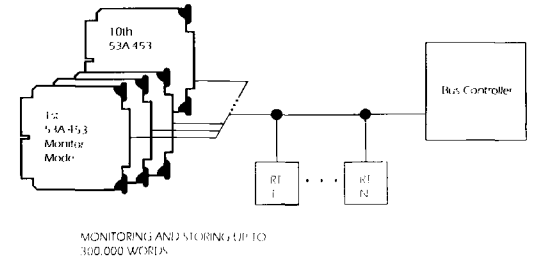
PRODUCTION TESTING INCLUDING ERROR GENERATION AND BUS SIMULATION



DUAL REDUNDANT BUS SIMULATION



1553 BUS ERROR RATE TESTING



MONITORING AND STORING UP TO 300,000 WORDS

8

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