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Notice

Hewlett-Packard to Agilent Technologies Transition

This manual may contain references to HP or Hewlett-Packard. Please note that Hewlett-Packard's former test and measurement, semiconductor products and chemical analysis businesses are now part of Agilent Technologies. To reduce potential confusion, the only change to product numbers and names has been in the company name prefix: where a product name/number was HP XXXX the current name/number is now Agilent XXXX. For example, model number HP8648 is now model number Agilent 8648.

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Service Guide

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HP 1660C/CS/CP-Series Logic Analyzers

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HP 1660C-Series, HP 1660CS-Series, and HP 1660CP-Series Logic Analyzers

The HP 1660C-Series are 100-MHz State/500 MHz Timing Logic Analyzers.

The HP 1660CS-Series includes all the features of the HP 1660C-Series, as well as a 2-channel, 1 GSa/s oscilloscope.

The HP 1660CP-Series includes all the features of the HP 1660C-Series, as well as a 32-channel pattern generator.

Features

Some of the main features of the HP 1660C-Series Logic Analyzers are as follows:

- 128 data channels and 6 clock/data channels in the HP 1660C
- 96 data channels and 6 clock/data channels in the HP 1661C
- 64 data channels and 4 clock/data channels in the HP 1662C
- 32 data channels and 2 clock/data channels in the HP 1663C
- 3.5-inch flexible disk drive
- 540 MB hard disk drive
- HP-IB, RS-232-C, and Centronics printer interfaces
- Variable setup/hold time
- 4k states deep memory on all channels with 8k states in half channel mode
- Marker measurements
- 12 levels of trigger sequencing for state and 10 levels of sequential triggering for timing
- 100 MHz time and number-of-states tagging
- Full programmability
- DIN mouse
- DIN keyboard support

The HP 1660CP-Series Logic Analyzers also include the following features:

- 32 channels of stimulus
- Maximum output rate of 200 MHz in half-channel mode and 100 MHz in full-channel mode
- Memory depth of 258,048 vectors
- Support for TTL, 3-state TTL/3.3v, 3-state TTL/CMOS, ECL terminated, ECL unterminated, and differential ECL (without pod).

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The HP 1660CS-Series Logic Analyzers also include the following features:

- 1 GSa/s digitizing for 250 MHz bandwidth single shot oscilloscope
- 8000 samples per channel
- Automatic pulse parameters
  displays time between markers, acquires until specified time between markers is captured, performs statistical analysis on time between markers
- Lightweight miniprobes

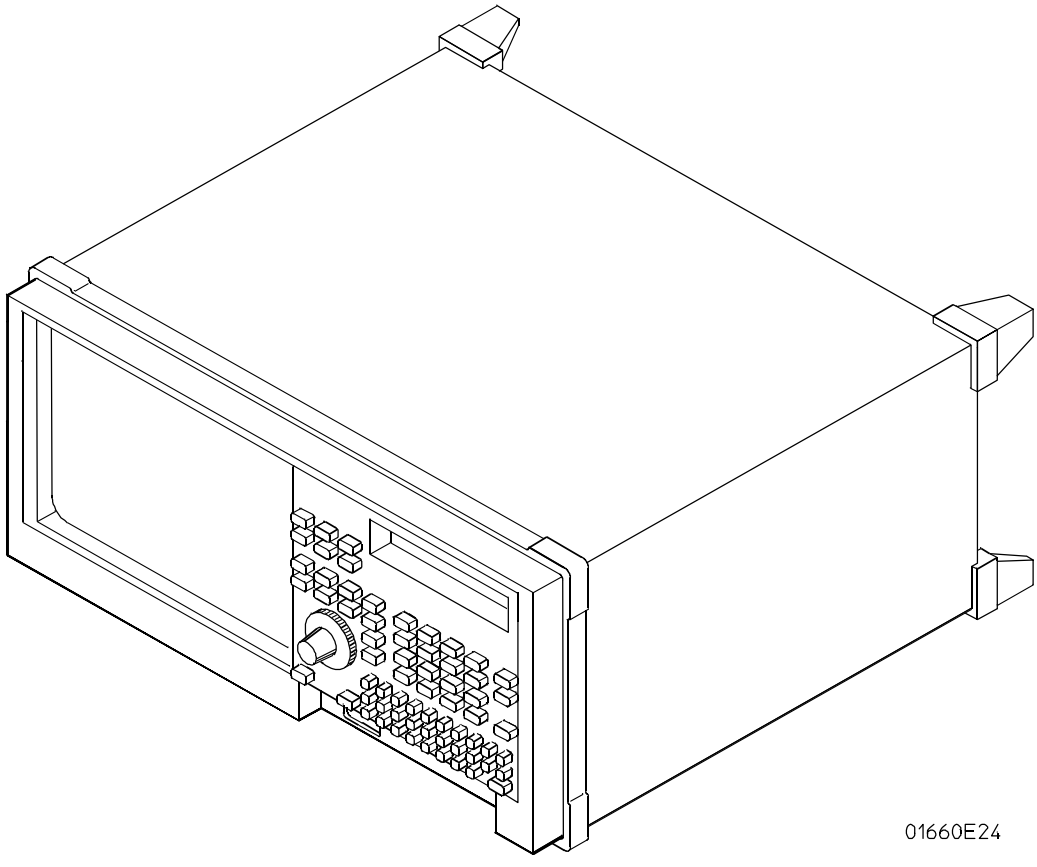
Options

The HP 1660C-Series, HP 1660CP-Series, and HP 1660CS-Series Logic Analyzers can be ordered with the optional Thinlan and Ethertwist LAN ports.

Service Strategy

The service strategy for this instrument is the replacement of defective assemblies. This service guide contains information for finding a defective assembly by testing and servicing the HP 1660C/CS/CP-Series Logic Analyzers.

This logic analyzer can be returned to Hewlett-Packard for all service work, including troubleshooting. Contact your nearest Hewlett-Packard Sales Office for more details.



The HP 1660-Series Logic Analyzer

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In This Book

This book is the service guide for the HP 1660C/CS/CP-Series Logic Analyzers and is divided into eight chapters.

Chapter 1 contains information about the logic analyzer and includes accessories, specifications and characteristics, and equipment required for servicing.

Chapter 2 tells how to prepare the logic analyzer for use.

Chapter 3 gives instructions on how to test the performance of the logic analyzer.

Chapter 4 contains calibration instructions for the logic analyzer.

Chapter 5 contains self-tests and flowcharts for troubleshooting the logic analyzer.

Chapter 6 tells how to replace assemblies of the logic analyzer and how to return them to Hewlett-Packard.

Chapter 7 lists replaceable parts, shows an exploded view, and gives ordering information.

Chapter 8 explains how the logic analyzer works and what the self-tests are checking.

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General Information

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General Information

This chapter lists the accessories, the specifications and characteristics, and the recommended test equipment.

Accessories

The following accessories are supplied with the HP 1660C/CS/CP-series logic analyzers.

Accessories Supplied	HP Part Number	Qty
Probe tip assemblies	01650-61608	Note 1
Probe cables	01660-61605	Note 2
Grabbers (20 per pack)	5090-4356	Note 1
Probe ground (5 per pack)	5959-9334	Note 1
Demo Training Kit	E2433-60012	1
HP 1660C User's Guide	01660-99016	1*
Symbol Utility (disk and manual)	E2450A	1
Accessories Pouch	01660-84501	1
RS-232-C Loopback Connector	01650-63202	1
PS2 Mouse	A2839B	1

* The HP 1660CS and HP 1660CP have their own User's Guide. For those products, the HP 1660C User's Guide is not shipped.

Note 1 Quantities:	Note 2 Quantities:
8 - 1660C.CS	4 - 1660C.CS
6 - 1661C.CS	3 - 1661C.CS
4 - 1662C.CS	2 - 1662C.CS
2 - 1663C.CS	1 - 1663C.CS

CP-Series Additional Accessories

Accessories Supplied	HP Part Number	Qty
Data Output Cable	16522-61601	4
Clock Output Cable	16522-61602	1
HP 1660CP User's Guide	01660-97023	1

CS-Series Additional Accessories

Accessories Supplied	HP Part Number	Qty
10:1 probes	10430A	2
BNC miniprobe adapter	1250-1454	1
HP 1660CS User's Guide	01660-99019	1

Accessories Available

Other accessories available for the HP 1660C/CS/CP Series Logic Analyzer are listed in the *Accessories for HP Logic Analyzers* brochure.

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Specifications (logic analyzer)

The specifications are the performance standards against which the product is tested.

Maximum State Speed	100 MHz
Minimum State Clock Pulse Width*	3.5 ns
Minimum Master to Master Clock Time*	10.0 ns
Minimum Glitch Width*	3.5 ns
Threshold Accuracy	± (100 mV + 3% of threshold setting)
Setup/Hold Time:*	
Single Clock, Single Edge	0.0/3.5 ns through 3.5/0.0 ns, adjustable in 500-ps increments
Single Clock, Multiple Edges	0.0/4.0 ns through 4.0/0.0 ns, adjustable in 500-ps increments
Multiple Clocks, Multiple Edges	0.0/4.5 ns through 4.5/0.0 ns, adjustable in 500-ps increments

* Specified for an input signal VH = –0.9 V, VL = –1.7 V, slew rate = 1 V/ns, and threshold = –1.3 V.

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Specifications (oscilloscope)

The HP 1660CS Logic Analyzers also include the following specifications:

Bandwidth (*,1)	DC to 250 MHz (real time, dc-coupled)
Time Interval Measurement Accuracy(*, 2)	±[(0.005% X Δt)+ (2 x 10^{-6} x delay setting)+150 ps]
DC Offset Accuracy(*)	±(1.0% of channel offset + 2.0% of full scale)
Voltage Measurement Accuracy(*, 3)	± [(1.5% of full scale + offset accuracy) + (0.008 x V/div)]
Trigger Sensitivity(*)	DC to 50 MHz: 0.063 x full scale, 50 to 250 MHz: 0.125 x full scale
Input R (selectable) (*)	1 MΩ: ±1%, 50 Ω: ±1%

* Specifications (valid within ± 10° C of auto-calibration temperature, excluding bandwidth–see note 1 for bandwidth specification.)

1. Upper bandwidth reduces by 2.5 MHz for every degree C above 35° C.

2. Specification applies to the maximum sampling rate. At lower rates, the specification is:± [(0.005% x Δt)+(2 x 10^{-6} x delay setting) + (0.15 x sample interval)] for bandwidth limited signals (t_r = 1.4 x sample interval). Sample interval is defined as $\frac{1}{sample\ rate}$

3. Digitizing level = (#vertical divisions)$(\frac{1}{2})(\frac{1}{LSB})$, where LSB=$2^{\#\ bits\ in\ ADC}$

Specifications (pattern generator)

There are no specifications for the pattern generator portion of the HP 1660CP-Series Logic Analyzers.

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Characteristics (logic analyzer)

These characteristics are not specifications, but are included as additional information.

		Full Channel	Half Channel
Maximum State Clock Rate		100 MHz	100 MHz
Maximum Conventional Timing Rate		250 MHz	500 MHz
Maximum Transitional Timing Rate		125 MHz	250 MHz
Maximum Timing with Glitch Rate		N/A	125 MHz
Memory Depth		4K	8K*
Channel Count:			
	HP 1660C,CP,CS	136	68
	HP 1661C,CP, CS	102	51
	HP 1662C,CP,CS	68	34
	HP 1663C,CP,CS	34	17

* For all modes except glitch.

Characteristics (oscilloscope)

The HP 1660CS Logic Analyzers also include the following characteristics:

Maximum Sample Rate	1 Gigasample per second
Number of Channels	2
Rise Time(1)	1.4 ns
ADC	8-bit real time
Vertical Resolution	8 bits over 4 vertical divisions (± 0.4%)
Waveform Record Length	8000 points
Vertical (DC) Gain Accuracy(2)	±1.25% of full scale
Input Coupling	1 MΩ: ac and DC, 50 Ω: DC only
Input C	Approximately 7 pF

1. Rise time is calculated from the formula: $t_r = \frac{0.35}{bandwidth}$
2. Vertical gain accuracy decreases 0.08% per degree C from software calibration temperature.

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Characteristics (pattern generator)

The HP 1660CP Logic Analyzers also include the following characteristics:

Output channels	16 channels at 200 MHz clock; 32 channels at 100 MHz clock
Memory depth	258,048 vectors
Logic levels (data pods)	TTL, 3-state TTL/3.3v, 3-state TTL/CMOS, ECL terminated, ECL unterminated, and differential ECL (without pod)
Data inputs	3-bit pattern - level sensing (clock pod)
Clock outputs	Synchronized to output data, delay of 11 ns in 9 steps (clock pod)
Clock input	DC to 200 MHz (clock pod)
Internal clock period	Programmable from 5 ns to 250 μs in a 1, 2, 2.5, 4, 5, 8 sequence
External clock period (user supplied)	DC to 200 MHz
External clock duty cycle	2 ns minimum high time
Maximum number of "IF condition" blocks at 50 MHz clock	1
Maximum number of different macros	100
Maximum number of lines in a macro	1024
Maximum number of macro invocations	1,000
Maximum number of Repeat loop invocations	1,000
Maximum number of Wait event patterns	4

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Supplemental Characteristics (logic analyzer)



Probes

Input Resistance	100 kΩ, ± 2%
Input Capacitance	~ 8 pF
Minimum Voltage Swing	500 mV, peak-to-peak
Threshold Range	± 6.0 V, adjustable in 50-mV increments, CAT I
Maximum Input Voltage	± 40 volts, CAT I

State Analysis

State/Clock Qualifiers	1660/61C,CP,CS - 6; 1662C,CP,CS - 4; 1663C,CP,CS - 2
Time Tag Resolution*	8 ns or 0.1%, whichever is greater
Maximum Time Count Between States	34 seconds
Maximum State Tag Count*	4.29×10^9

Timing Analysis

Sample Period Accuracy	0.01 % of sample period
Channel-to-Channel Skew	2 ns, typical
Time Interval Accuracy	± [sample period + channel-to-channel skew +(0.01%)(time reading)]

Triggering

Sequencer Speed	125 MHz, maximum
State Sequence Levels	12
Timing Sequence Levels	10
Maximum Occurrence Counter Value	1,048,575
Pattern Recognizers	10
Maximum Pattern Width	136 channels in HP 1660C,CP,CS, 102 channels in HP 1661C,CP,CS, 68 channels in HP 1662C,CP,CS, 34 channels in HP 1663C,CP,CS
Range Recognizers	2
Range Width	32 bits each
Timers	2
Timer Value Range	400 ns to 500 seconds
Glitch/Edge Recognizers	2 (timing only)
Maximum Glitch/Edge Width	136 channels in HP 1660C,CP,CS, 102 channels in HP 1661C,CP,CS, 68 channels in HP 1662C,CP,CS, 34 channels in HP 1663C,CP,CS

*Maximum state clock rate with time or state tags on is 100 MHz. When all pods are assigned to a state or timing machine, time or state tags halve the memory depth.

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Measurement and Display Functions

Displayed Waveforms 24 lines maximum, with scrolling across 96 waveforms.

Measurement Functions

Run/Stop Functions Run starts acquisition of data in specified trace mode.

Stop In single trace mode or the first run of a repetitive acquisition, Stop halts acquisition and displays the current acquisition data. For subsequent runs in repetitive mode, Stop halts acquisition of data and does not change the current display.

Trace Mode Single mode acquires data once per trace specification. Repetitive mode repeats single mode acquisitions until Stop is pressed or until the time interval between two specified patterns is less than or greater than a specified value, or within or not within a specified range.

Indicators

Activity Indicators Provided in the Configuration and Format menus for identifying high, low, or changing states on the inputs.

Markers Two markers (X and O) are shown as vertical dashed lines on the display.

Trigger Displayed as a vertical dashed line in the Timing Waveform display and as line 0 in the State Listing display.

Data Entry/Display

Labels Channels may be grouped together and given a 6-character name. Up to 126 labels in each analyzer may be assigned with up to 32 channels per label.

Display Modes State listing, State Waveforms, Chart, Compare Listing, Compare Difference Listing, Timing Waveforms, and Timing Listings. State Listing and Timing Waveforms can be time-correlated on the same displays.

Timing Waveform Pattern readout of timing waveforms at X or O marker.

Bases Binary, Octal, Decimal, Hexadecimal, ASCII (display only), Two's Complement, and User-defined symbols.

Symbols 1,000 maximum. Symbols can be downloaded over RS-232 or HP-IB.

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Marker Functions

Time Interval The X and O markers measure the time interval between a point on a timing waveform and the trigger, two points on the same timing waveform, two points on different waveforms, or two states (time tagging on).

Delta States (state analyzer only) The X and O markers measure the number of tagged states between one state and trigger or between two states.

Patterns The X and O markers can be used to locate the *nth* occurrence of a specified pattern from trigger, or from the beginning of data. The O marker can also find the *nth* occurrence of a pattern from the X marker.

Statistics X and O marker statistics are calculated for repetitive acquisitions. Patterns must be specified for both markers, and statistics are kept only when both patterns can be found in an acquisition. Statistics are minimum X to O time, maximum X to O time, average X to O time, and ratio of valid runs to total runs.

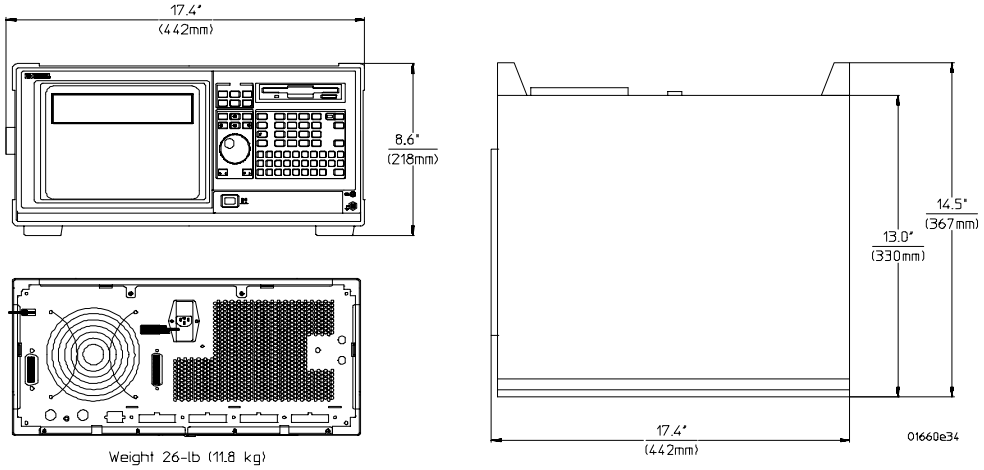
Auxiliary Power

Power through cables	1/3 amp at 5 V maximum per cable, CAT I, Pollution degree 2.

Operating Environment

Temperature	Instrument, 0 °C to 55 °C (+32 °F to 131 °F). Probe lead sets and cables, 0 °C to 65 °C (+32 °F to 149 °F).
Humidity	Instrument, probe lead sets, and cables, up to 80% relative humidity at +40 °C (+122 °F).
Altitude	To 3067 m (10,000 ft).
Vibration	Operating: Random vibration 5 to 500 Hz, 10 minutes per axis, ≈0.3 g (rms). Non-operating: Random vibration 5 to 500 Hz, 10 minutes per axis, ≈ 2.41 g (rms); and swept sine resonant search, 5 to 500 Hz, 0.75 g (0-peak), 5 minute resonant dwell at 4 resonances per axis.

Dimensions



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Product Regulations

Safety	IEC 1010-1:1990+A1 / EN 61010-1:1993 UL3111 CSA-C22.2 No. 1010.1:1993
EMC	This product meets the requirement of the European Communities (EC) EMC Directive 89/336/EEC.
Emissions	EN55011/CSIPR 11 (ISM, Group1,Class A equipment) IEC 555-2 and IEC 555-3

Immunity	EN50082-1	Code[1]	Notes[2]
	IEC 801-2 (ESD)4kV CD, 8kV AD	1	
	IEC 801-3 (Rad.) 3V/m	1	
	IEC 801-4 (EFT) 1kV	1	

[1]Performance Codes:
1 PASS - Normal operations, no effect.
2 PASS - Temporary degradation, self recoverable.
3 PASS - Temporary degradation, operator intervention required.
4 FAIL - Not recoverable, component damage.

Supplemental Characteristics (oscilloscope)

Vertical (at BNC)

Vertical Sensitivity Range (1:1 Probe)	4 mV/div to 10 V/div in 1-2-4 increments
DC Offset Range (1:1 Probe)	

Vertical Sensitivity	Available Offset
4 mV/div to 100 mV/div	±2 V
>100 mV/div to 500 mV/div	±10 V
>500 mV/div to 2.5 V/div	±50 V
>2.5 V/div to 10 V/div	±250 V

Probe Factors	Any integer ratio from 1:1 to 1000:1
Maximum Safe Input Voltage	1 MΩ: ±250 V [DC + peak ac (< 10 KHz)], CAT II 50 Ω: ±5 VRMS
Channel-to-Channel Isolation	DC to 50 MHz: 40 dB, 50 MHz to 250 MHz: 30 dB

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Timebase

Range	1 ns/div to 5 s/div
Resolution	20 ps

Delay Pre-trigger Range

Time/div Setting	Available Delay
1 µs to 5 s/div	-8 x (s/div)
1 ns to 500 ns/div	-4 µs

Delay Post-trigger Range

Time/div Setting	Available Delay
100 ms to 5 s/div	2.5 ks
1 µs to 50 ms/div	33,500 x (s/div)
1ns to 500 ns/div	16.7 ms

Triggering

Trigger Level Range: Within display window (full scale and offset)

Trigger Modes

Immediate	Triggers immediately after arming condition is met.
Edge	Triggers on rising or falling edge of any internal channel, count adjustable from 1 to 32,000.
Pattern	Triggers on entering or exiting a specified pattern of both internal channels, count adjustable from 1 to 32,000.
Pattern Duration	Triggers on pattern duration specified across one or both channels. Modes are "Present<", "Present>", and "Range." Patterns longer than 20 ns but shorter than 160 ms can be detected.
Pattern Occurrence	Triggers on entering or exiting a specified pattern across one or both channels.
Auto-Trigger	If enabled, the module will self-trigger if no trigger condition is found within approximately 50 ms after arming.
Events Delay	The trigger can be set to occur on the nth edge or pattern, as specified by the user. The number of events (n) can be set from 1 to 32,000 events. Maximum count frequency is 70 MHz.
Intermodule	Arms another measurement module or triggers the rear panel BNC.
External	If enabled, the oscilloscope will trigger on an ECL level signal (-1.3 V).

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Digitizer

Resolution	8 bits (1 part in 256)
Digitizing Rate	Up to 1 Gigasample per second
Digitizing Technique	Real-time digitizing; each 8000 samples are acquired on a single acquisition
Acquisition Memory Size	8000 samples per channel

Waveform Display

Displayed Waveforms	Eight waveform windows maximum, with scrolling across 96 waveforms.
Display Formats	Waveforms can be displayed in an overlapping and/or non-overlapping format. Display capability of A-B and A+B is also provided.
Display Resolution	500 points horizontal, 240 points vertical.

Display Modes

Normal (Single)	New acquisition replaces old acquisition on screen.
Accumulate	New acquisition is displayed in addition to previous acquisitions until screen is erased.
Average	New acquisitions are averaged with old acquisitions, with the updated waveform displayed until erased. Maximum number of averages is 256.
Overlay	Up to 8 acquired waveforms from separate channels can be overlayed in the same display area.
Connect-the-dots	Provides a display of the sample points connected by straight lines.
Waveform Reconstruction	When there is insufficient data to fill every horizontal location, a post acquisition reconstruction filter fills in missing data points for time base < 50 ns/div.
Waveform Math	Display capability of A-B and A+B functions is provided.

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Measurement and Display Functions

Time Markers Two vertical markers, X and O, are provided for measurements of time and voltage. Capabilities are: measure voltage at point where X and O markers cross each analog waveform; measure time from trigger to X, trigger to O, and X to O; automatic marker placement by specifying percentage of edge, edge number, and rising or falling edge type; run until X to O > than, < than, in range, and not in range provides selective event search; X to O statistics (mean, max, and min) provide analysis of time interval deviation.

Voltage Markers Two horizontal markers, A and B, are provided for voltage measurements. These markers can each be placed on any acquisition channel trace. A delta voltage display provides delta V between markers on the same channel or between channels.

Automatic Search Searches for a percentage voltage level at a positive or negative edge, count adjustable from 1 to 100.

Auto Search Statistics Mean, maximum, and minimum values for elapsed time from X to O markers for multiple runs. Number of valid runs and total number of runs available.

Automatic Measurements The following pulse parameter measurements can be performed automatically:

Frequency	Rise time	+ pulse width
Period	Fall time	–pulse width
V p-p	Preshoot	$V_{amplitude}$*
	Overshoot	

(*gives difference between top and base voltages; only available over bus)

Grid Graticules can be displayed in background of waveform.

Setup Aids

Autoscale Autoscales the vertical and horizontal ranges, offset, and trigger level to display the input signals. Requires a frequency between 50 Hz and 250 MHz.

Presets Scales the vertical range, offset, and trigger level to predetermined values for displaying ECL or TTL waveforms.

Calibration Vertical, trigger, delay, and all defaults. Calibration factors stored in NV-RAM on the circuit board.

Probe Compensation Source External BNC supplies a square wave approximately 0.0 mV to -800 mV into the open circuit at approximately 1000 Hz.

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Recommended test equipment (logic analyzer)

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part	Use*
Pulse Generator	100 MHz, 3.5 ns pulse width, < 600 ps rise time	HP 8133A Option 003	P,T
Digitizing Oscilloscope	≥ 6 GHz bandwidth, < 58 ps rise time	HP 54750A, with HP 54751A plugin	P
Function Generator	Accuracy ≤ $(5)(10^{-6})$ × frequency, DC offset voltage ±6.3 V	HP 3325B Option 002	P
Digital Multimeter	0.1 mV resolution, 0.005% accuracy	HP 3458A	P
BNC-Banana Cable		HP 11001-60001	P
BNC Tee	BNC (m)(f)(f)	HP 1250-0781	P
Cable	BNC (m)(m) 48 inch	HP 10503A	P,T
SMA Coax Cable (Qty 3)	18 GHz bandwidth	HP 8120-4948	P
Adapter (Qty 4)	SMA(m)-BNC(f)	HP 1250-1200	P, T
Adapter	SMA(f)-BNC(m)	HP 1250-2015	P
Coupler (Qty 4)	BNC (m)(m)	HP 1250-0216	P, T
20:1 Probes (Qty 2)		HP 54006A	P
BNC Test Connector, 17x2 (Qty 1)**			P
BNC Test Connector, 6x2 (Qty 4)**			P,T
Digitizing Oscilloscope	> 100 MHz Bandwidth	HP 54600B	T
BNC Shorting Cap		HP 1250-0074	T
BNC-Banana Adapter		HP 1251-2277	T
Light Power Meter		United Detector 351	A
Alignment Tool		8710-1300	A

*A = Adjustment P = Performance Tests T = Troubleshooting
**Instructions for making these test connectors are in chapter 3, "Testing Performance."

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Recommended test equipment (oscilloscope)

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part	Use*
Signal Generator	Frequency: 1 - 250 MHz at approx. 170 mV RMS Output Accuracy: ± 1 dB 1 MHz time base accuracy 0.25 ppm	HP 8656B Option 001	P
DC Power Supply	Range: –35.000 to +35.000 Vdc, ±1 mV	HP 3245A Option 002	P
Digital Multimeter	0.1 mV resolution Accuracy: better than 0.005% Resistance measurement: better than 0.25% accuracy	HP 3458A	P
Power Meter/Sensor	1 - 250 MHz ±3% accuracy	HP 436/8482A	P
Power Splitter	Outputs differ by <0.15 dB	HP 11667B	P
Blocking Capacitor	BNC (m)(f), 0.18 µF, ±200 V	HP 10240B	P
BNC Shorting Cap		HP 1250-0074	P
Adapter	BNC (f)(f) (UG-914/U)	HP 1250-0080	C
Adapter	BNC(f)-to-Dual Banana Plug	HP 1251-2277	P
Adapter	Type N(m)-to-BNC(f)	HP 1250-0780	P
BNC Tee	BNC (m)(f)(f)	HP 1250-0781	P,C
Cable	Type N(m-to-m) 24-inch	HP 11500B	P
Cable	50 Ω BNC (m-to-m) 48-inch	HP 10503A	P, C
Cable (2)	50 Ω BNC (m-to-m) 9 inch	HP 10502A	C

*P = Performance Tests C = Calibration

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Recommended test equipment (pattern generator)

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part	Use*
Oscilloscope	≥ 500 MHz Bandwidth	HP 54522A	T
Probe	500 MHz Bandwidth	HP 10441A	T
Output Data Pod	no substitute	10460A - series	T

* T = Troubleshooting

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2



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To operate the user interface 2–3
To set the line voltage 2–3
To degauss the display 2–4
To clean the logic analyzer 2–4
To test the logic analyzer 2–4

Preparing for Use

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Preparing For Use

This chapter gives you instructions for preparing the logic analyzer for use.

Power Requirements

The logic analyzer power source requirements are either 115 V ac or 230 V ac, –22 % to +10 %, single phase, 48 to 66 Hz, 200 Watts maximum power.

Operating Environment

The operating environment is listed in chapter 1. Note the noncondensing humidity limitation listed below. Condensation within the instrument can cause poor operation or malfunction. Provide protection against internal condensation.

The logic analyzer will operate at all specifications within the temperature and humidity range given in chapter 1. However, reliability is enhanced when operating the logic analyzer within the following ranges:

- Temperature: +20 °C to +35 °C (+68 °F to +95 °F)
- Humidity: 20% to 80% noncondensing

Storage

Store or ship the logic analyzer in environments within the following limits:

- Temperature: -40 °C to + 75 °C (-40 °F to + 167 °F
- Humidity: Up to 90% at 65 °C
- Altitude: Up to 15,300 meters (50,000 feet)

Protect the logic analyzer from temperature extremes which cause condensation on the instrument.

To inspect the logic analyzer

1. Inspect the shipping container for damage.

   If the shipping container or cushioning material is damaged, keep them until you have checked the contents of the shipment and checked the instrument mechanically and electrically.

2. Check the supplied accessories.

   Accessories supplied with the logic analyzer are listed in "Accessories" in chapter 1.

3. Inspect the product for physical damage.

   Check the logic analyzer and the supplied accessories for obvious physical or mechanical defects. If you find any defects, contact your nearest Hewlett-Packard Sales Office. Arrangements for repair or replacement are made, at Hewlett-Packard's option, without waiting for a claim settlement.

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To apply power

1. Check that the line voltage selector, located on the rear panel, is on the correct setting and the correct fuse is installed.
   See also, "To set the line voltage" on this page.
2. Connect the power cord to the instrument and to the power source.
   This instrument is equipped with a three-wire power cable. When connected to an appropriate AC power outlet, this cable grounds the instrument cabinet. The type of power cable plug shipped with the instrument depends on the country of destination. Refer to chapter 7, "Replaceable Parts," for option numbers of available power cables and plug configurations.
3. Turn on the instrument power switch located on the bottom of the front panel.

To operate the user interface

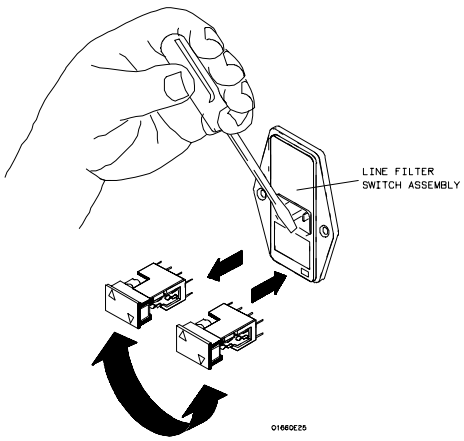
To select a field on the logic analyzer screen, use the arrow keys to highlight the field, then press the Select key. For more information about the logic analyzer interface, refer to the *HP 1660-Series Logic Analyzer User's Guide*.

To set the HP-IB address or to configure for RS-232-C, refer to the *HP 1660-Series Logic Analyzer User's Guide*.

To set the line voltage

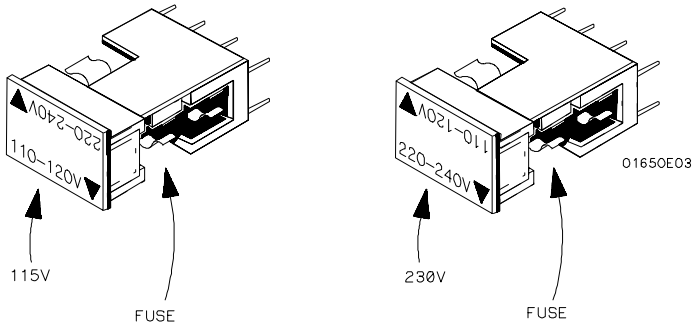
When shipped from HP, the line voltage selector is set and an appropriate fuse is installed for operating the instrument in the country of destination. To operate the instrument from a power source other than the one set, perform the following steps.

1. Turn the power switch to the Off position, then remove the power cord from the instrument.
2. Remove the fuse module by carefully prying at the top center of the fuse module until you can grasp it and pull it out by hand.



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3 Reinsert the fuse module with the arrow for the appropriate line voltage aligned with the arrow on the line filter assembly switch.



4 Reconnect the power cord. Turn on the instrument by setting the power switch to the On position.

To degauss the display

If the logic analyzer has been subjected to strong magnetic fields, the CRT might become magnetized and display data might become distorted. To correct this condition, degauss the CRT with a conventional external television type degaussing coil.

To clean the logic analyzer

With the instrument turned off and unplugged, use mild soap and water to clean the front and cabinet of the logic analyzer. Harsh soap might damage the water-base paint.

To test the logic analyzer

- If you require a test to verify the specifications, start at the beginning of chapter 3, "Testing Performance."
- If you require a test to initially accept the operation, perform the self-tests in chapter 3.
- If the logic analyzer does not operate correctly, go to the beginning of chapter 5, "Troubleshooting."

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3

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Testing Performance

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Testing Performance

This chapter tells you how to test the performance of the logic analyzer against the specifications listed in chapter 1. To ensure the logic analyzer is operating as specified, you perform software tests (self-tests) and manual performance tests on the analyzer. The logic analyzer is considered performance-verified if all of the software tests and manual performance tests have passed. The procedures in this chapter indicate what constitutes a "Pass" status for each of the tests.

The Logic Analyzer Interface

To select a field on the logic analyzer screen, use the arrow keys to highlight the field, then press the Select key. For more information about the logic analyzer interface, refer to the *HP 1660 Series Logic Analyzer User's Guide*.

Test Strategy

For a complete test, start at the beginning with the software tests and continue through to the end of the chapter. For an individual test, follow the procedure in the test. The examples in this chapter were performed using an HP 1660CS. Other analyzers in the series will have appropriate pods showing on the screen.

With the HP 1660CS-series Logic Analyzers, ensure that the operational accuracy calibration has been done before doing the performance verification tests (see chapter 4).

The performance verification procedures starting on page 3–8 are each shown from power-up. To exactly duplicate the setups in the tests, save the power-up configuration to a file on a disk, then load that file at the start of each test.

If a test fails, check the test equipment setup, check the connections, and verify adequate grounding. If a test still fails, the most probable cause of failure would be the acquisition board or oscilloscope board.

Test Interval

Test the performance of the logic analyzer against specifications at two-year intervals or if it is replaced or repaired.

Performance Test Record

A performance test record for recording the results of each procedure is located at the end of this chapter. Use the performance test record to gauge the performance of the logic analyzer over time.

Test Equipment

Each procedure lists the recommended test equipment. You can use equipment that satisfies the specifications given. However, the procedures are based on using the recommended model or part number. Before testing the performance of the logic analyzer, warmup the instrument and the test equipment for 30 minutes.

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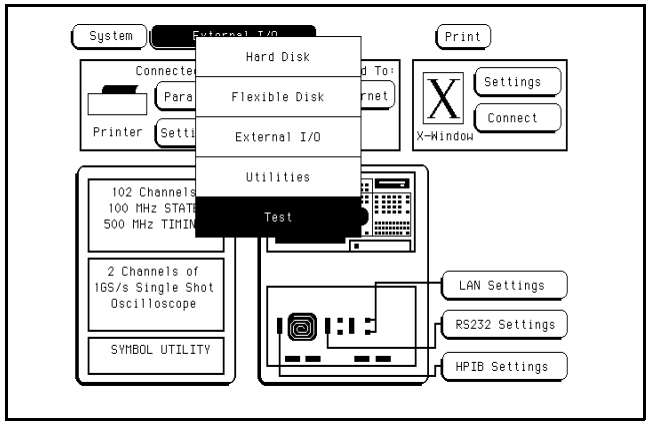
To perform the self-tests

The self-tests verify the correct operation of the logic analyzer. Self-tests can be performed all at once or one at a time. While testing the performance of the logic analyzer, run the self-tests all at once.

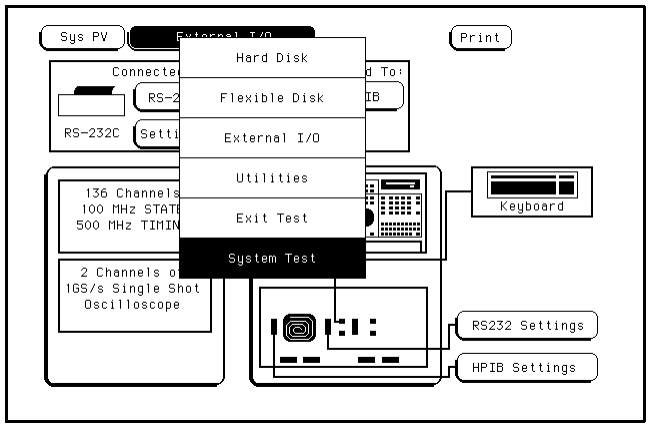
The performance verification (PV) self-tests consist of system PV tests, analyzer PV tests, and oscilloscope PV tests (HP 1660CS series only).

These procedures assume the files on the PV disk have been copied to the /SYSTEM subdirectory on the hard disk drive. If they have not already been copied, insert the PV disk in the flexible disk drive before starting this procedure.

1. Disconnect all inputs, then turn on the power switch. Wait until the power-up tests are complete.
2. Press the System key. Select the field next to System, then select Test in the pop-up menu.



3. Select the box labeled Load Test System, then select Continue.
4. Press the System key. Select the field next to Sys PV, then select System Test in the pop-up menu.



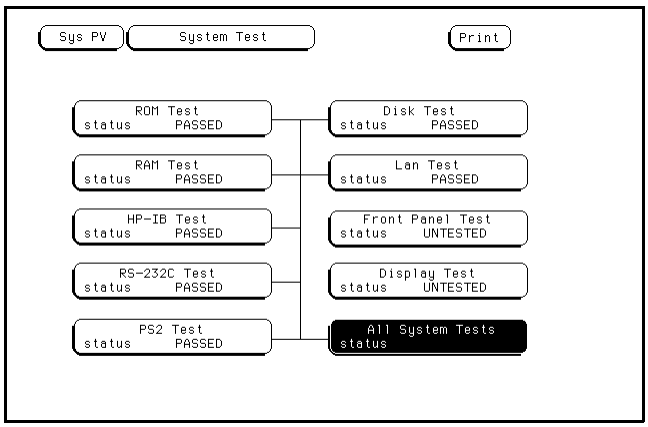
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5 Install a formatted disk that is not write-protected into the disk drive. Connect an RS-232-C loopback connector onto the RS-232-C port.

6 Select All System Tests.

You can run all tests at one time, except for the Front Panel Test and Display Test, by running All System Tests. To see more details about each test when troubleshooting failures, you can run each test individually. This example shows how to run all tests at once.

When the tests finish, the status for each test shows PASSED or FAILED, and the status for the All System Tests changes from UNTESTED to TESTED. Note that the Front Panel Test and Display Test remain UNTESTED.



7 Select the Front Panel Test.

A screen duplicating the front panel appears on the screen.

a Press each key on the front panel. The corresponding key on the screen will change from a light to a dark color. Test the knob by turning it in both directions.

b Note any failures, then press the Done key a second time to exit the Front Panel Test. The status of the test changes from UNTESTED to TESTED.

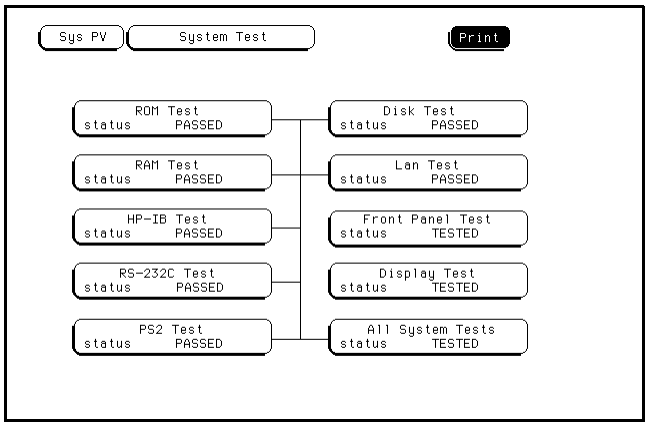
8 Select the Display Test.

A white grid pattern is displayed. These display screens are not normally used, but can be used to adjust the display. Refer to chapter 4, "Calibrating and Adjusting" for display adjustments.

a Select Continue and the screen changes to full bright.

b Select Continue and the screen changes to half bright.

c Select Continue and the test screen shows the Display Test status changed to Tested.

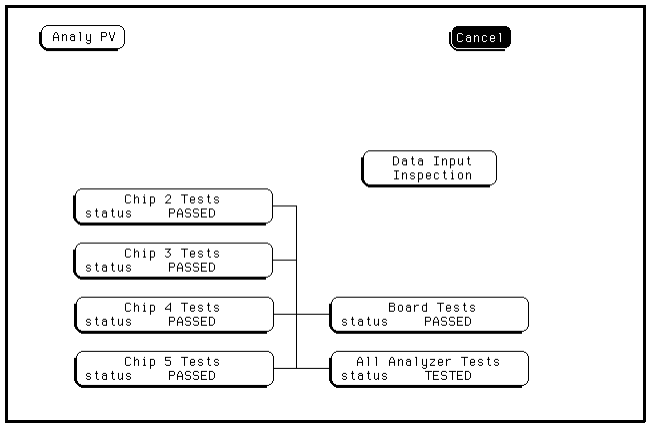


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9 Select Sys PV, then select Analy PV in the pop-up menu. In the Analy PV menu, Select All Analyzer Tests.

You can run all tests at one time, except for the Data Input Inspection, by running All Analyzer Tests. To see more details about each test when troubleshooting failures, you can run each test individually. This example shows how to run all tests at once.

When the tests finish, the status for each test shows Passed or Failed, and the status for the All Analyzer Tests changes from Untested to Tested.

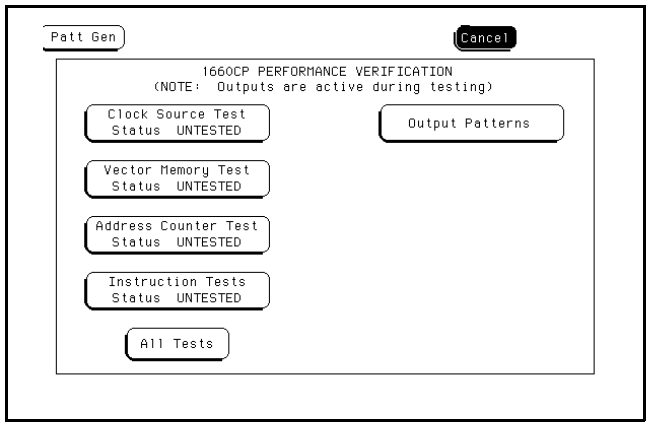


10 Record the results of the tests on the performance test record at the end of this chapter.

11 For the HP 1660CP-series Logic Analyzers, Select Analy PV, then select Patt Gen in the pop-up menu. In the Patt Gen menu select All Tests.

You can run all tests at one time (except the Output Patterns routine) by selecting All Tests. To see more details about each test, you can run each test individually. This example shows how to run all tests at once.

When the tests finish, the status for each test shows Passed or Failed.



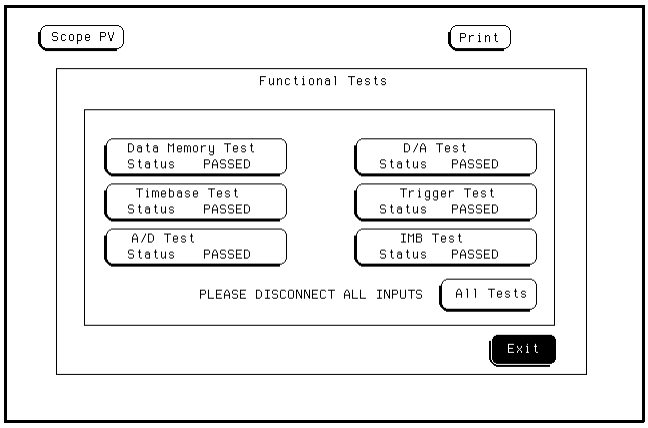
12 Record the results of the tests on the performance test record at the end of this chapter, then continue with step 15.

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13 For the HP 1660CS-series Logic Analyzers, Select Analy PV, then select Scope PV in the pop-up menu. In the Scope PV menu, select Functional Tests then select All Tests.

You can run all tests at one time, except for the Data Input Inspection, by running All Tests. To see more details about each test when troubleshooting failures, you can run each test individually. This example shows how to run all tests at once.

When the tests finish, the status for each test shows Passed or Failed.



14 Record the results of the tests on the performance test record at the end of this chapter.

15 To exit the test system, press the System key, then press the Select key. Select Exit Test, then select Exit Test System.

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To make the test connectors (logic analyzer)

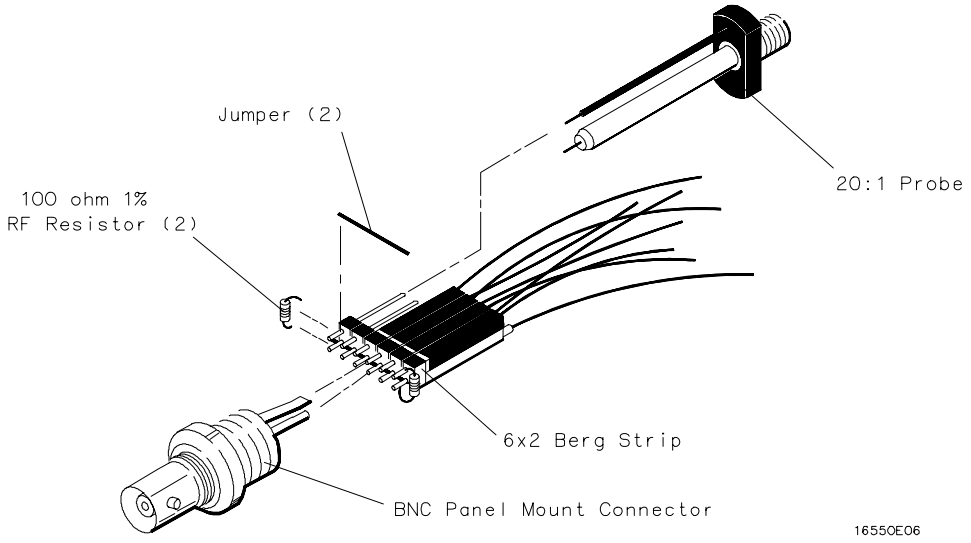
The test connectors connect the logic analyzer to the test equipment. The following materials are required to make the test connectors.

Materials Required

Description	Recommended Part	Qty
BNC (f) Connector	HP 1250-1032	5
100 Ω 1% resistor	HP 0698-7212	8
Berg Strip, 17-by-2		1
Berg Strip, 6-by-2		4
20:1 Probe	HP 54006A	2
Jumper wire		

1 Build four test connectors using BNC connectors and 6-by-2 sections of Berg strip.

- **a** Solder a jumper wire to all pins on one side of the Berg strip.
- **b** Solder a jumper wire to all pins on the other side of the Berg strip.
- **c** Solder two resistors to the Berg strip, one at each end between the end pins.
- **d** Solder the center of the BNC connector to the center pin of one row on the Berg strip.
- **e** Solder the ground tab of the BNC connector to the center pin of the other row on the Berg strip.
- **f** On two of the test connectors, solder a 20:1 probe. The probe ground goes to the same row of pins on the test connector as the BNC ground tab.



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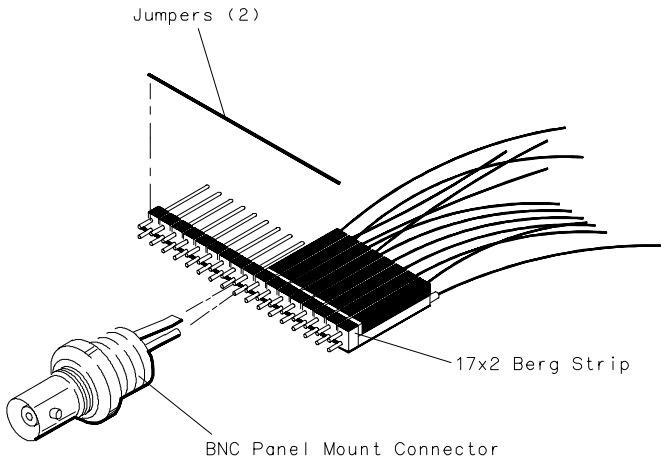
2 Build one test connector using a BNC connector and a 17-by-2 section of Berg strip.

a Solder a jumper wire to all pins on one side of the Berg strip.

b Solder a jumper wire to all pins on the other side of the Berg strip.

c Solder the center of the BNC connector to the center pin of one row on the Berg strip.

d Solder the ground tab of the BNC connector to the center pin of the other row on the Berg strip.



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To test the threshold accuracy (logic analyzer)

Testing the threshold accuracy verifies the performance of the following specification:

- Clock and data channel threshold accuracy.

These instructions include detailed steps for testing the threshold settings of pod 1. After testing pod 1, connect and test the rest of the pods one at a time. To test the next pod, follow the detailed steps for pod 1, substituting the next pod for pod 1 in the instructions.

Each threshold test tells you to record the voltage reading in the performance test record located at the end of this chapter. To check if each test passed, verify that the voltage reading you record is within the limits listed on the performance test record.

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part
Digital Multimeter	0.1 mV resolution, 0.005% accuracy	HP 3458A
Function Generator	Accuracy ≤ (5)(10^{-6}) × frequency, DC offset voltage ±6.3 V	HP 3325B Option 002
BNC-Banana Cable		HP 11001-60001
BNC Tee		HP 1250-0781
BNC Cable		HP 10503A
BNC Test Connector, 17x2		

Set up the equipment

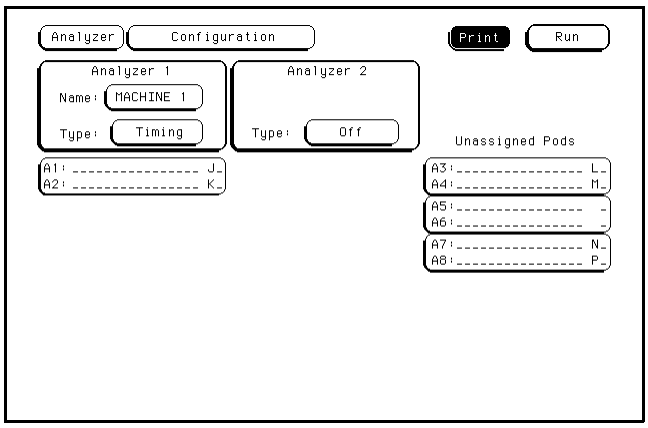
1. Turn on the equipment required and the logic analyzer. Let them warm up for 30 minutes before beginning the test.
2. Set up the function generator.
   a. Set up the function generator to provide a DC offset voltage at the Main Signal output.
   b. Disable any AC voltage to the function generator output, and enable the high voltage output.
   c. Monitor the function generator DC output voltage with the multimeter.

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Set up the logic analyzer

1 Press the Config key.

2 Unassign Pods 3 and 4, Pods 5 and 6, and Pods 7 and 8. To unassign the pods, select the pod field. In the pop-up menu, select Unassigned.

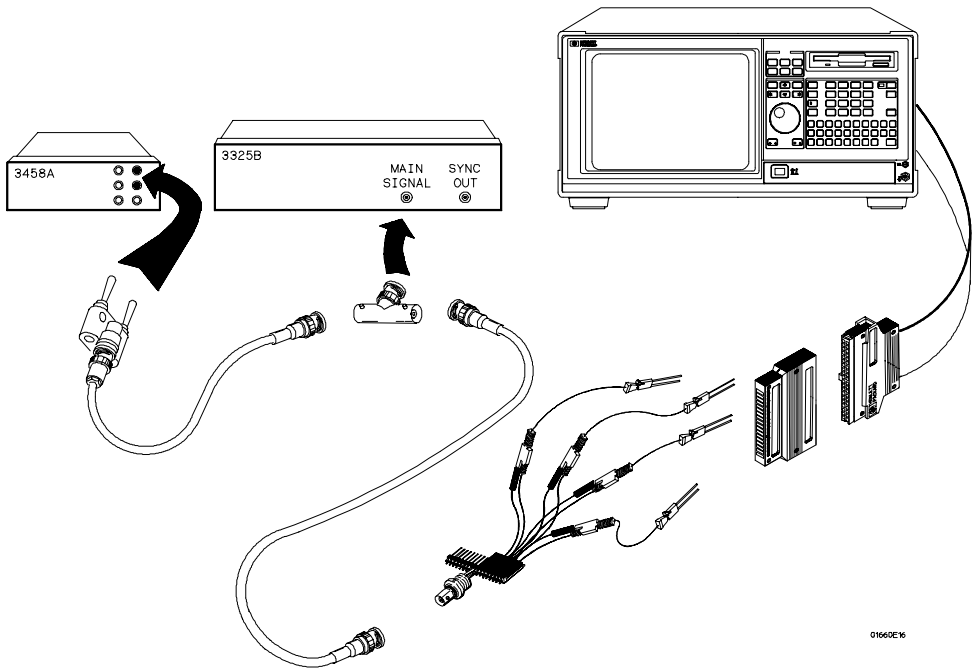


Connect the logic analyzer

1 Using the 17-by-2 test connector, BNC cable, and probe tip assembly, connect the data and clock channels of pod 1 to one side of the BNC Tee.

2 Using a BNC-banana cable, connect the voltmeter to the other side of the BNC Tee.

3 Connect the BNC Tee to the Main Signal output of the function generator.

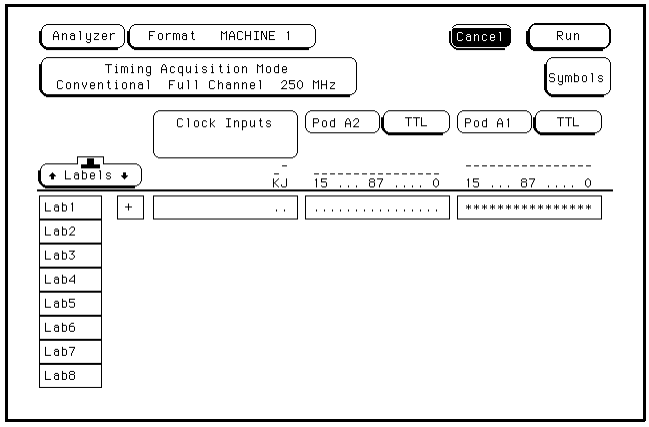


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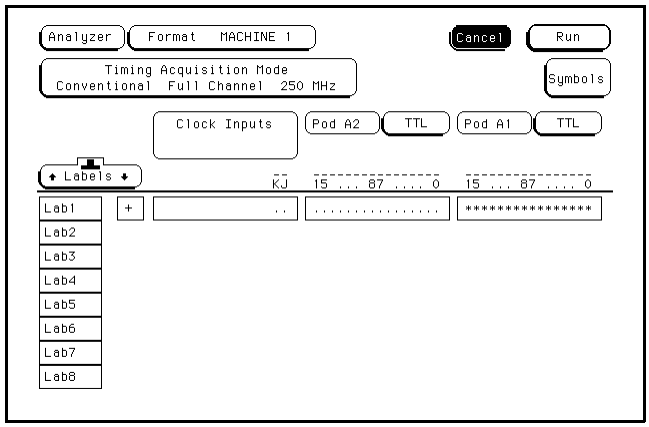
Test the TTL threshold

1. Press the Format key. Select the field to the right of Pod A1, then select TTL in the pop-up menu.
2. On the function generator front panel, enter 1.750 V ±1 mV DC offset. Use the multimeter to verify the voltage.

   The activity indicators for pod 1 should show all data channels and the J-clock channel at a logic high.

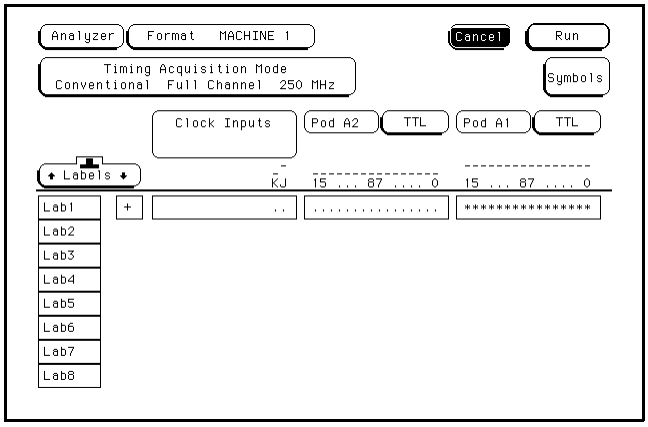


3. Using the Modify down arrow on the function generator, decrease offset voltage in 1-mV increments until all activity indicators for pod 1 show the channels at a logic low. Record the function generator voltage in the performance test record.



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4 Using the Modify up arrow on the function generator, increase offset voltage in 1-mV increments until all activity indicators for pod 1 show the channels at a logic high. Record the function generator voltage in the performance test record.

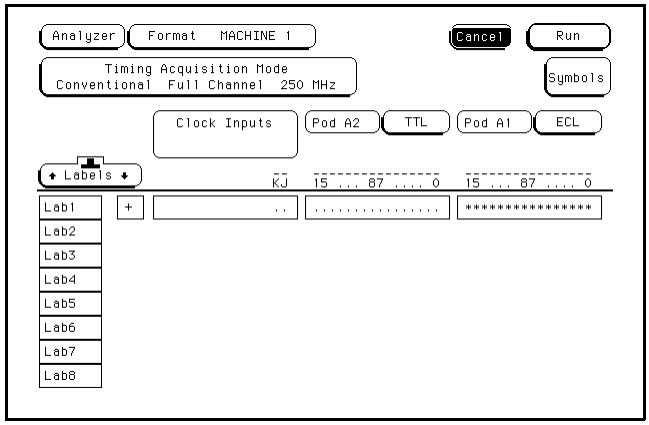


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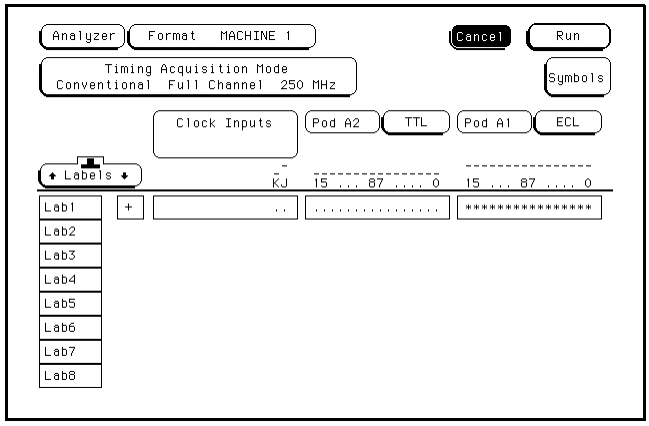
Test the ECL threshold

1. Select the field to the right of Pod A1, then select ECL in the pop-up menu.
2. On the function generator front panel, enter –1.160 V ±1 mV DC offset. Use the multimeter to verify the voltage.

   The activity indicators for pod 1 should show all data channels and the J-clock channel at a logic high.
3. Using the Modify down arrow on the function generator, decrease offset voltage in 1-mV increments until all activity indicators for pod 1 show the channels are at a logic low. Record the function generator voltage in the performance test record.



4. Using the Modify up arrow on the function generator, increase offset voltage in 1-mV increments until all activity indicators for pod 1 show the channels are at a logic high. Record the function generator voltage in the performance test record.



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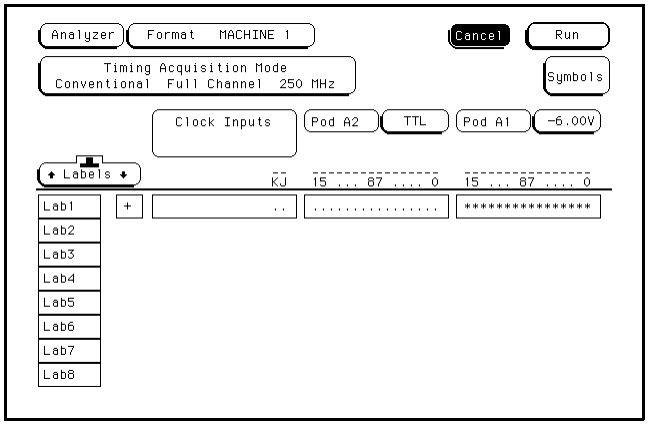
Test the – User threshold

1 Move the cursor to the field to the right of Pod A1. Type –6.00, then use the left and right cursor control keys to highlight V. Press the Select key.

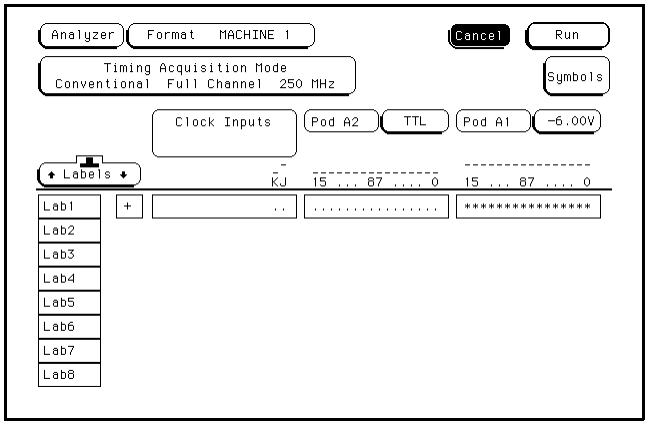
2 On the function generator front panel, enter –5.718 V ±1 mV DC offset. Use the multimeter to verify the voltage.

The activity indicators for pod 1 should show all data channels and the J-clock channel at a logic high.

3 Using the Modify down arrow on the function generator, decrease offset voltage in 1-mV increments until all activity indicators for pod 1 show the channels at a logic low. Record the function generator voltage in the performance test record.



4 Using the Modify up arrow on the function generator, increase offset voltage in 1-mV increments until all activity indicators show the channels at a logic high. Record the function generator voltage in the performance test record.

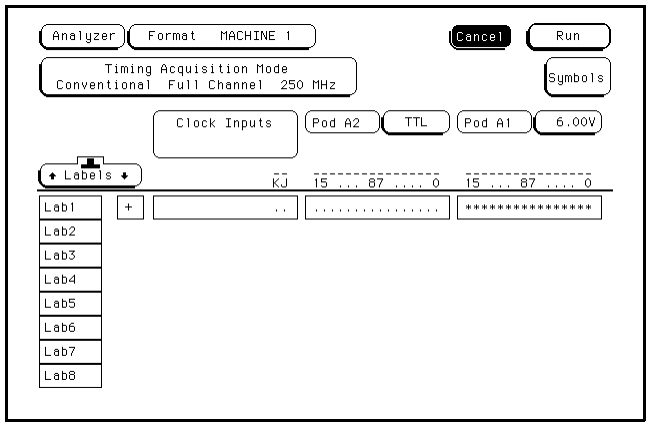


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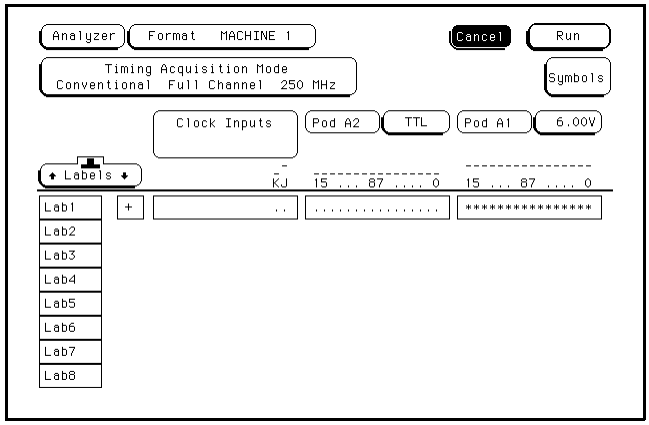
Test the + User threshold

1. Move the cursor to the field to the right of Pod A1. Type +6.00, then use the left and right cursor control keys to highlight V. Press the Select key.
2. On the function generator front panel, enter +6.282 V ±1 mV DC offset. Use the multimeter to verify the voltage.

   The activity indicators for pod 1 should show all data channels and the J-clock channel at a logic high.
3. Using the Modify down arrow on the function generator, decrease offset voltage in 1-mV increments until all activity indicators for pod 1 show the channels at a logic low. Record the function generator voltage in the performance test record.



4. Using the Modify up arrow on the function generator, increase offset voltage in 1-mV increments until all activity indicators for pod 1 show the channels at a logic high. Record the function generator voltage in the performance test record.



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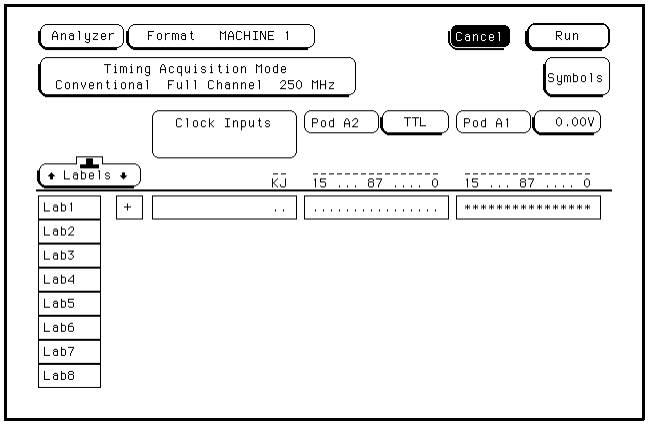
Test the 0 V User threshold

1 Move the cursor to the field to the right of Pod A1. Type 0, then press the Select key.

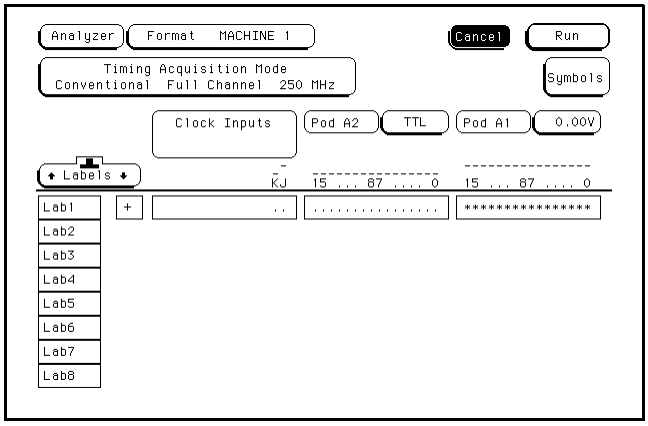
2 On the function generator front panel, enter +0.102 V ±1 mV DC offset. Use the multimeter to verify the voltage.

The activity indicators for pod 1 should show all data channels and the J-clock channel at a logic high.

3 Using the Modify down arrow on the function generator, decrease offset voltage in 1-mV increments until all activity indicators for pod 1 show the channels at a logic low. Record the function generator voltage in the performance test record.



4 Using the Modify up arrow on the function generator, increase offset voltage in 1-mV increments until all activity indicators for pod 1 show the channels at a logic high. Record the function generator voltage in the performance test record.



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Test the next pod

1. Using the 17-by-2 test connector and probe tip assembly, connect the data and clock channels of the next pod to the output of the function generator until all pods have been tested.

   To unassign a pod pair and assign the next pod pair to be tested, press the Config key. Select the pod pairs, then select assign or unassign in the pop-up menu.

2. Start with "Test the TTL threshold" on page 3–11, substituting the next pod to be tested for pod 1.

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To test the glitch capture (logic analyzer)

Testing the glitch capture verifies the performance of the following specification:

- Minimum detectable glitch.

This test checks the minimum detectable glitch on sixteen data channels at a time.

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part
Pulse Generator	100 MHz 3.5 ns pulse width, < 600 ps rise time	HP 8133A Option 003
Digitizing Oscilloscope	≥ 6 GHz bandwidth , < 58 ps rise time	HP 54750A, with HP 54751A plugin
SMA Coax (Qty 3)	18 GHz bandwidth	HP 8120-4948
Adapter (Qty 4)	SMA(m)-BNC(f)	HP 1250-1200
Coupler (Qty 4)	BNC (m)(m)	HP 1250-0216
BNC Test Connector, 6x2 (Qty 4)		

Set up the equipment

1 Turn on the equipment required and the logic analyzer. Let them warm up for 30 minutes before beginning the test if you have not already done so.

2 Set up the pulse generator.

Pulse Generator Setup

Timebase	Channel 2	Period	Channel 1
Mode: Int	Mode: Pulse	Divide: Divide ÷ 1	Mode: Pulse
Period: 22.000 ns	Divide: PULSE ÷ 1	Ampl: 0.50 V	Delay: 0.000 ns
	Width: 3.500 ns	Offs: 0.00 V	Width: 3.500 ns
	High: –0.90 V		High: –0.90 V
	Low: –1.70 V		Low: –1.70 V
	COMP: Disabled (LED Off)		COMP: Disabled (LED Off)

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3 Set up the oscilloscope.

Oscilloscope Setup

Time Base	Display	Delta V	Delta T
Time/Div: 1.00 ns/div	mode: avg	V markers on	T markers on
delay: 17.7000 ns	# of avg: 16	marker 1 position: Chan 1	start on: Pos Edge 1
	screens: dual	marker 2 position: Chan 2	stop on: Pos Edge 1

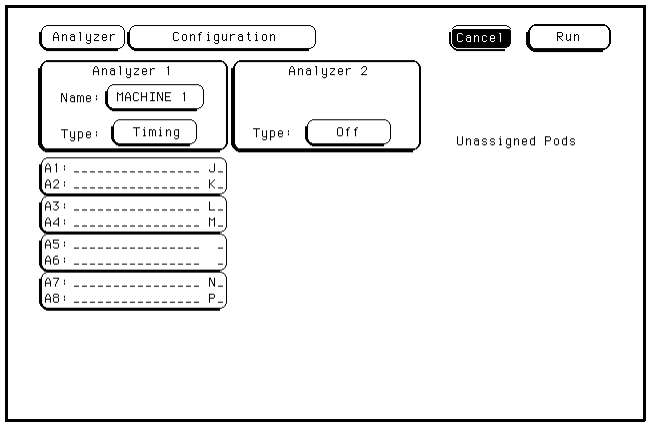
Channel

	Channel 1	Channel 2
Display	on	on
Probe Atten	20.00	20.00
Volts/Div	400 mV	400 mV
Offset	–1.3000 V	–1.3000 V

Set up the logic analyzer

1 Press the Config key. Assign all pod fields to Machine 1. To assign the pod fields, select the pod fields, then select Machine 1 in the pop-up menu.

2 In the Analyzer 1 box, select the Type field. Select Timing in the pop-up menu.



Connect the logic analyzer

1 Using SMA cables, connect the oscilloscope to the pulse generator channel 1 Output, channel 2 Output, and Trig Output.

2 Using the 6-by-2 test connectors, connect the first combination of logic analyzer clock and data channels listed in the table to the pulse generator.

You will repeat this test for the remaining combinations.

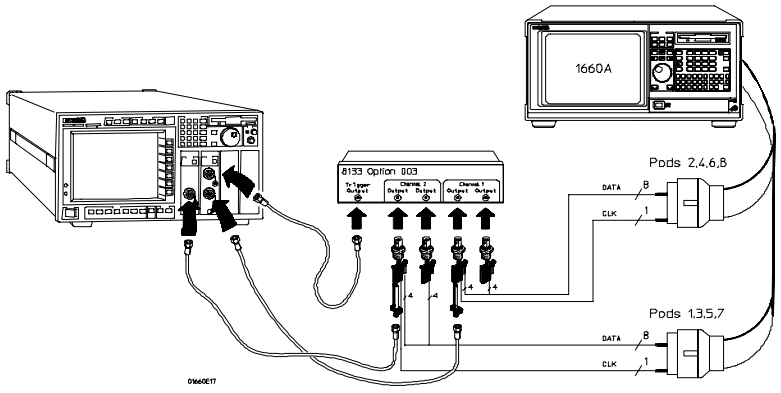
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The table includes all the HP 1660C/CS/CP Series. Use the pods that correspond to your logic analyzer:

- HP 1660C/CS/CP – pods 1 through 8
- HP 1661C/CS/CP – pods 1 and 2, pods 3 and 4, and pods 5 and 6
- HP 1662C/CS/CP – pods 1 and 2, and pods 3 and 4
- HP 1663C/CS/CP – pods 1 and 2

Connect the Logic Analyzer to the Pulse Generator

Testing Combinations	To HP 8133A Channel 2 Output	To HP 8133A Channel 2 $\overline{\text{Output}}$	To HP 8133A Channel 1 Output	To HP 8133A Channel 1 $\overline{\text{Output}}$
1	Pod 1 ch 0, 2, 4, 6, J-clock	Pod 1 ch 1, 3, 5, 7	Pod 3 ch 0, 2, 4, 6, L-clock	Pod 3 ch 1, 3, 5, 7
2	Pod 1 ch 8, 10, 12, 14, J-clock	Pod 1 ch 9, 11, 13, 15	Pod 3 ch 8, 10, 12, 14, L-clock	Pod 3 ch 9, 11, 13, 15
3	Pod 2 ch 0, 2, 4, 6, K-clock	Pod 2 ch 1, 3, 5, 7	Pod 4 ch 0, 2, 4, 6, M-clock	Pod 4 ch 1, 3, 5, 7
4	Pod 2 ch 8, 10, 12, 14, K-clock	Pod 2 ch 9, 11, 13, 15	Pod 4 ch 8, 10, 12, 14, M-clock	Pod 4 ch 9, 11, 13, 15
5	Pod 5 ch 0, 2, 4, 6, N-clock (1661C only)	Pod 5 ch 1, 3, 5, 7	Pod 7 ch 0, 2, 4, 6, N-clock (1660C only)	Pod 7 ch 1, 3, 5, 7
6	Pod 5 ch 8, 10, 12, 14, N-clock (1661C only)	Pod 5 ch 9, 11, 13, 15	Pod 7 ch 8, 10, 12, 14, N-clock (1660C only)	Pod 7 ch 9, 11, 13, 15
7	Pod 6 ch 0, 2, 4, 6, P-clock (1661C only)	Pod 6 ch 1, 3, 5, 7	Pod 8 ch 0, 2, 4, 6, P-clock (1660C only)	Pod 8 ch 1, 3, 5, 7
8	Pod 6 ch 8, 10, 12, 14, P-clock (1661C only)	Pod 6 ch 9, 11, 13, 15	Pod 8 ch 8, 10, 12, 14, P-clock (1660C only)	Pod 8 ch 9, 11, 13, 15



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Test the glitch capture on the connected channels

1 Set up the Format menu.

a Press the Format key.

b Select the field to the right of each pod, then select ECL in the pop-up menu. Use the knob to access pods not shown on the screen (to activate the knob for pods, use the cursor to select the Pods field and push Select).

c Select Timing Acquisition Mode, then select Glitch Half Channel 125 MHz.

2 Turn on the channels that correspond to the channels being tested.

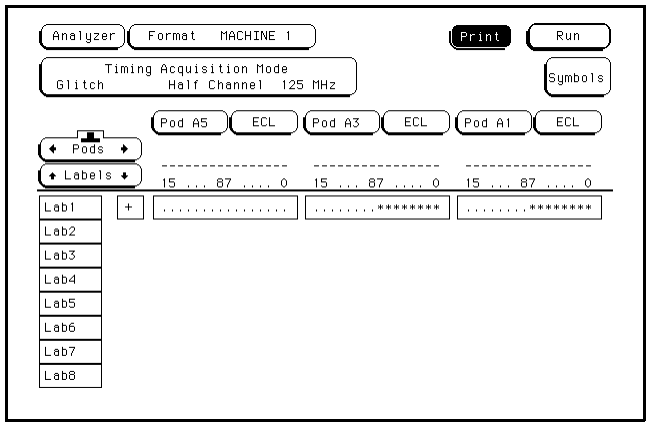
The channels being tested are the channels connected to the pulse generator in "Connect the logic analyzer."

a Select the pod field, then select one of the two pods in the pop-up. Move the cursor to the channel assignment field of the pod and press the Clear entry key until all channels of the pod are de-assigned (all periods). Press the Done key.

b Select the bit assignment field for the pod. Using the arrow keys, move the selector to a channel, then press the Select key. An asterisk means that the channel is turned on. Press the Done key when the channels being tested are turned on.

c Access the next pod, then turn on the channels being tested until all pod channels being tested are turned on.

d Turn on the clock/data channels that correspond to the clocks being tested. Turn off the data channels and clock/data channels that are not being tested.

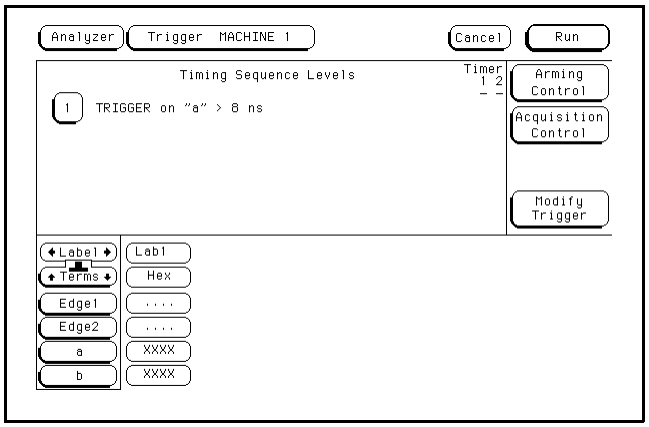


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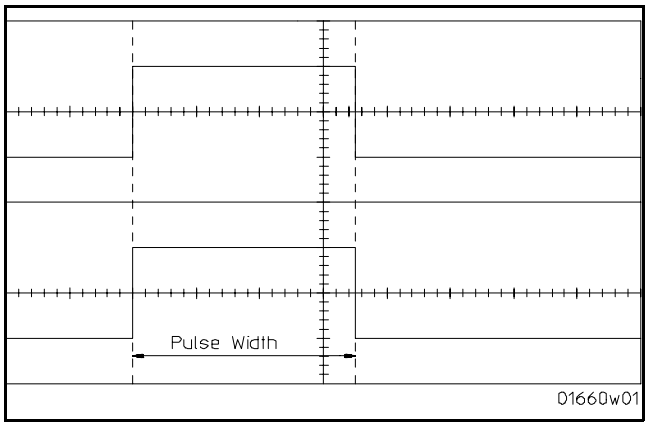
3 Set up the Trigger menu.

a Press the Trigger key.

b Select Modify Trigger, then select Clear Trigger, then select All.



4 Using the [Shift] + width: channel 1 and [Shift] + width: channel 2 of the oscilloscope, verify that the pulse widths of the pulse generator channels 1 and 2 are 3.450 ns, +50 ps or –100 ps. If necessary, adjust the pulse widths of the pulse generator channels 1 and 2.



5 Set up the Waveform menu to view all the channels.

a Select one of the Glitch labels, then select Delete All in the pop-up menu.

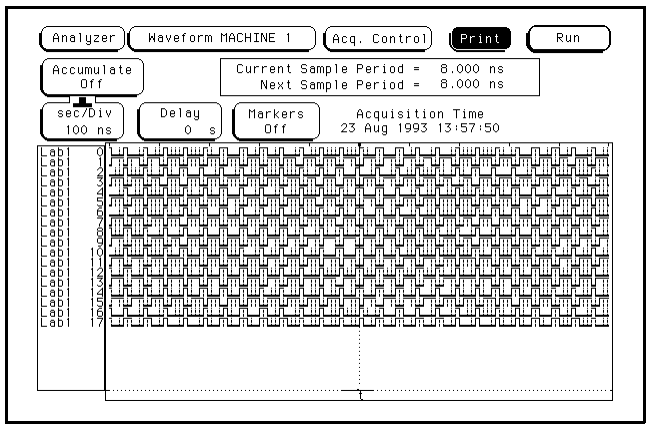
b Select All, then select continue.

c Press the Select key, then select Insert in the pop-up menu.

d Press the Select key, then select Sequential in the pop-up menu.

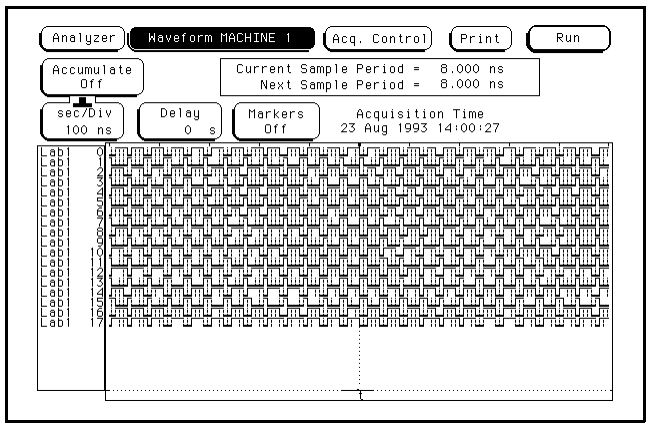
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6 On the logic analyzer, press the Run key. The display should be similar to the figure below.



7 On the pulse generator, enable Channel 1 and Channel 2 COMP (with the LED on).

8 On the logic analyzer, press the Run key. The display should be similar to the figure below. Record Pass or Fail in the performance test record.



Test the next channels

- Return to "Connect the logic analyzer" on page 3–19 and connect and test the next combination of data and clock channels until all pods are tested.

  To access pods 2, 4, 6, or 8 in the Format menu, select pods 1, 3, 5, or 7 fields, then select the other pod in the pop-up menu. Use the knob to access pods that are not shown on the screen.

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To test the single-clock, single-edge, state acquisition (logic analyzer)

Testing the single-clock, single-edge, state acquisition verifies the performance of the following specifications:

- Minimum master-to-master clock time
- Maximum state acquisition speed
- Setup/Hold time for single-clock, single-edge, state acquisition
- Minimum clock pulse width

This test checks two combinations of data channels using a single-edge clock at three selected setup/hold times.

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part
Pulse Generator	100 MHz 3.5 ns pulse width, < 600 ps rise time	HP 8133A option 003
Digitizing Oscilloscope	≥ 6 GHz bandwidth, < 58 ps rise time	HP 54750A, with HP 54751A plugin
Adapter	SMA(m)-BNC(f)	HP 1250-1200
SMA Coax Cable (Qty 3)	18 GHz bandwidth	HP 8120-4948
Coupler	BNC(m)(m)	HP 1250-0216
BNC Test Connector, 6x2 (Qty 4)		

Set up the equipment

1 Turn on the equipment required and the logic analyzer. Let them warm up for 30 minutes before beginning the test if you have not already done so.

2 Set up the pulse generator.

a Set up the pulse generator according to the following table.

Pulse Generator Setup

Timebase	Channel 2	Period	Channel 1
Mode: Int	Mode: Pulse	Divide: Divide ÷ 2	Mode: Pulse
Period: 10.000 ns	Divide: PULSE ÷ 2	Ampl: 0.50 V	Delay: 0.000 ns
	Width: 3.500 ns	Offs: 0.00 V	Width: 3.500 ns
	High: –0.90 V		High: –0.90 V
	Low: –1.70 V		Low: –1.70 V

b Disable the pulse generator channel 1 COMP (with the LED off).

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3 Set up the oscilloscope. If the oscilloscope was not configured for the previous test, then do the following steps.

a Select Setup, then select Default Setup.

b Configure the oscilloscope according to the following table.

Oscilloscope Setup

Acquisition	**Display**	**Trigger**	**[Shift] Δ Time**
Averaging: On # of averages: 16	Graticule Graphs: 2	Level: -250 mV	Stop src: channel 2 [Enter]

Channel 1	**Channel 2**	**Define meas**
Alternate Scale Attenuation: 20.00:1 Scale: 200 mV/div Offset: –1.300 V	Alternate Scale Attenuation: 20.00:1 Scale: 200 mV/div Offset: -1.300 V	Thresholds: user-defined Units: Volts Upper: -980 mV Middle: -1.30 V Lower: -1.62 V

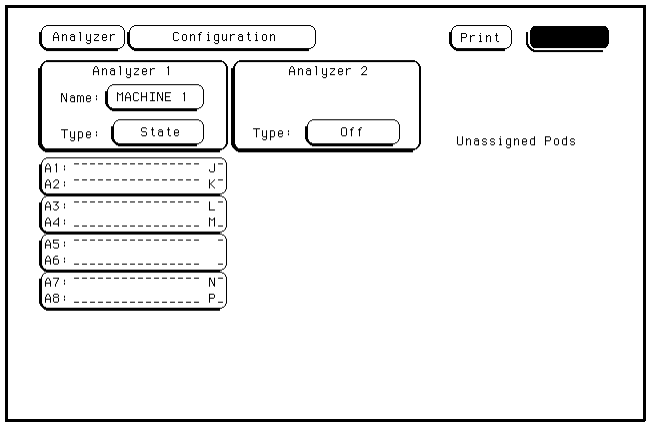
Set up the logic analyzer

1 Set up the Configuration menu.

a Press the Config key.

b In the Configuration menu, assign all pods to Machine 1. To assign the pods, select the pod fields, then select Machine 1 in the pop-up menu.

c Select the Type field in the Analyzer 1 box, then select State.

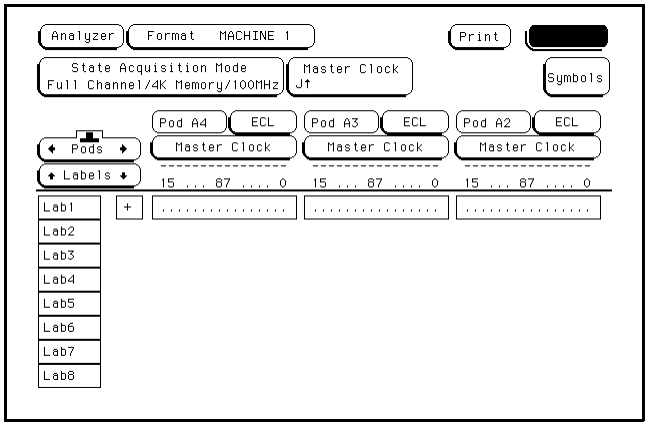


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2 Set up the Format menu.

a Press the Format key. Select State Acquisition Mode, then select Full Channel/4K Memory/100MHz.

b Select the field to the right of each pod, then select ECL in the pop-up menu. Use the knob to access pods not shown on the screen.



3 Set up the Trigger menu.

a Press the Trigger key. Select Modify Trigger, select Clear Trigger, then select All in the pop-up menu.

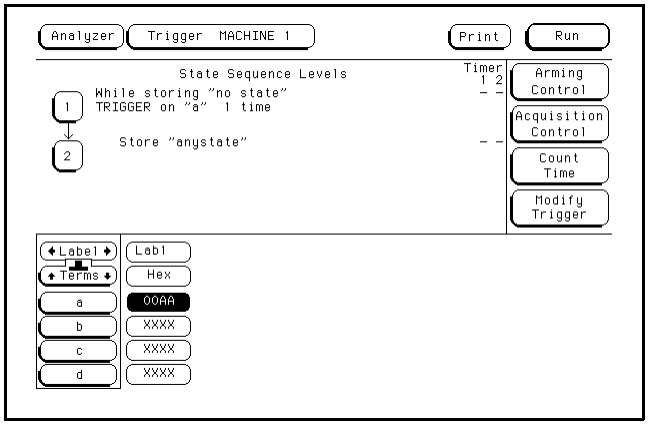
b Select Count Off. Press Select again, then select Time in the pop-up menu. Select Done to exit the menu.

c Select the field labeled 1 under the State Sequence Levels. Select the field labeled "anystate," then select "no state." Select Done to exit the State Sequence Levels menu.

d Select the field next to "a," under the label Lab1. Type the following for your logic analyzer, then press the Select key.

HP 1660C/CS – "00AA" HP 1662C/CS – "00AA"

HP 1661C/CS – "002A" HP 1663C/CS – "000A"



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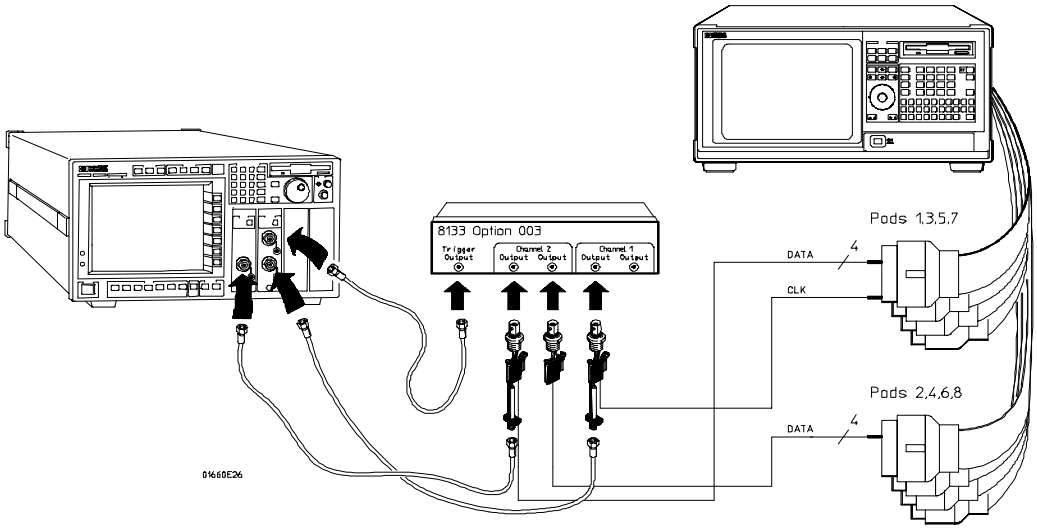
Connect the logic analyzer

1 Using the 6-by-2 test connectors, connect the first combination of logic analyzer clock and data channels listed in one of the following tables to the pulse generator.
If you are testing an HP 1660C or HP 1661C, you will repeat this test for the second combination.

2 Using SMA cables, connect the oscilloscope to the pulse generator channel 1 Output, channel 2 Output, and Trig Output.

Connect the HP 1660C/CS/CP or HP 1661C/CS/CP Logic Analyzer to the Pulse Generator

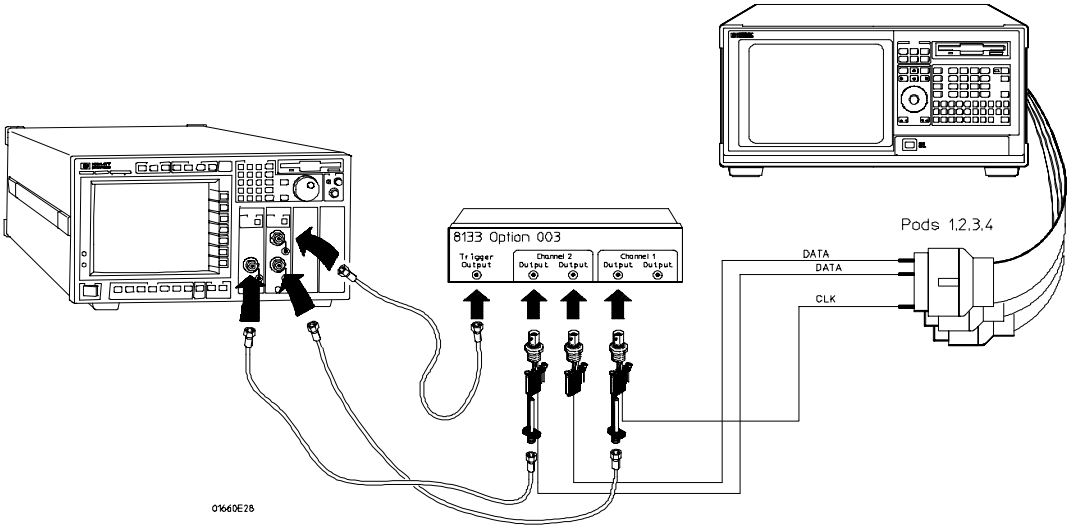
Testing Combinations	Connect to HP 8133A Channel 2 Output	Connect to HP 8133A Channel 2 Output	Connect to HP 8133A Channel 1 Output
1	Pod 1, channel 3 Pod 3, channel 3 Pod 5, channel 3 Pod 7, channel 3	Pod 2, channel 3 Pod 4, channel 3 Pod 6, channel 3 Pod 8, channel 3	J-clock
2	Pod 1, channel 11 Pod 3, channel 11 Pod 5, channel 11 Pod 7, channel 11	Pod 2, channel 11 Pod 4, channel 11 Pod 6, channel 11 Pod 8, channel 11	J-clock



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Connect the HP 1662C or HP 1663C Logic Analyzer to the Pulse Generator

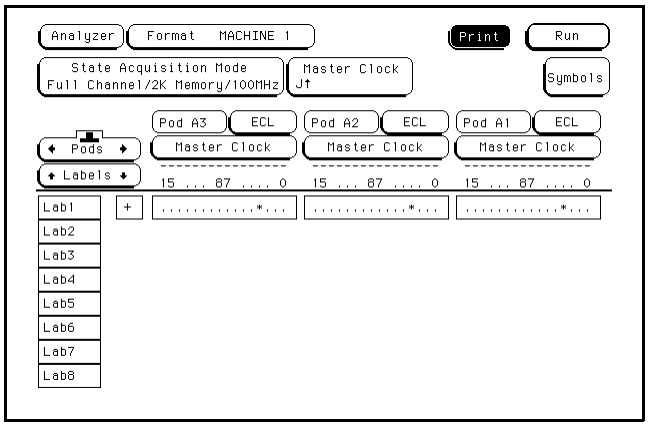
Testing Combination	Connect to HP 8133A Channel 2 Output	Connect to HP 8133A Channel 2 Output	Connect to HP 8133A Channel 1 Output
1	Pod 1, channel 3 Pod 2, channel 3 Pod 3, channel 3 Pod 4, channel 3	Pod 1, channel 11 Pod 2, channel 11 Pod 3, channel 11 Pod 4, channel 11	J-clock



3 Activate the data channels that are connected according to one of the previous tables.

a Press the Format key.

b Select the field showing the channel assignments for one of the pods being tested, then press the Clear entry key. Using the arrow keys, move the selector to the data channels to be tested, then press the Select key. An asterisk means that a channel is turned on. When all the correct channels of the pod are turned on, press the Done key. Follow this step for the remaining pods.

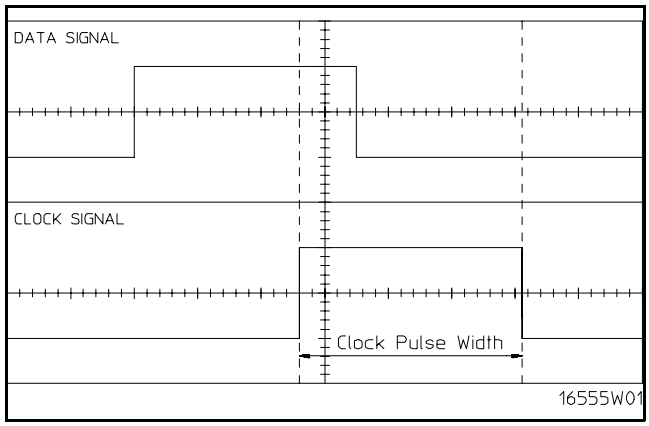


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Verify the test signal

1 Check the clock pulse width. Using the oscilloscope, verify that the clock pulse width is 3.500 ns, +0 ps or –100 ps.

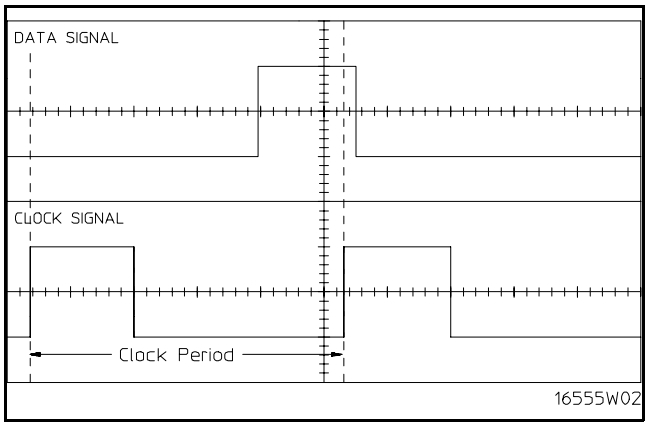
- **a** Enable the pulse generator channel 1, channel 2, and trigger outputs (LED off).
- **b** In the oscilloscope Timebase menu, select Scale: 1.000 ns/div.
- **c** In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the clock waveform so that the waveform is centered on the screen.
- **d** On the oscilloscope, select [Shift] + width: channel 2, then select [Enter] to display the clock signal pulse width (+ width(2)).
- **e** If the pulse width is outside the limits, adjust the pulse generator channel 2 width until the pulse width is within limits.



2 Check the clock period. Using the oscilloscope, verify that the clock period is 10.000 ns, +0 ps or –250 ps.

- **a** In the oscilloscope Timebase menu, select Scale: 2.000 ns/div.
- **b** In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the clock waveform so that a rising edge appears at the left of the display.
- **c** On the oscilloscope, select [Shift] Period: channel 2, then select [Enter] to display the clock period (Period(2)). If the period is not less than 10.000 ns, go to step d. If the period is less than 10.000 ns, go to step 3.
- **d** In the oscilloscope Timebase menu, increase Position 10.000 ns. If the period is not less than 10.000 ns, decrease the pulse generator Chan 2 Doub in 10 ps increments until one of the two periods measured is less than 10.000 ns.

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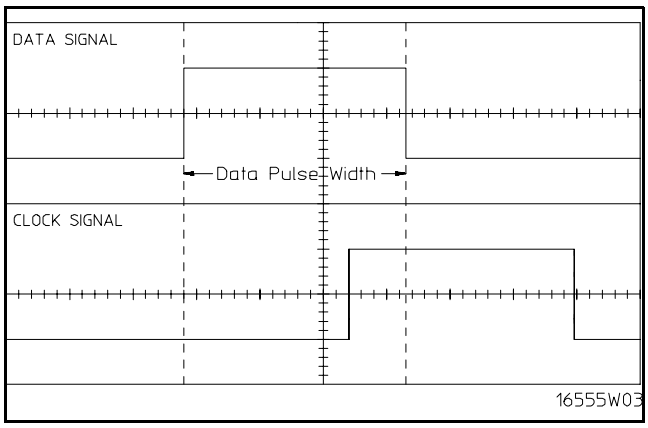
3 Check the data pulse width. Using the oscilloscope, verify that the data pulse width is 3.500 ns, +0 ps or –100 ps.

a On the Oscilloscope, select [Define meas] Define Δ Time - Stop edge: rising.

b In the oscilloscope timebase menu, select Position. Using the oscilloscope knob, position the rising edge of the clock waveform so that it is centered on the display.

c On the oscilloscope, select [Shift] Δ Time, then select [Enter] to display the setup time (Δ Time(1)-(2)).

d Adjust the pulse generator channel 1 Delay until the pulses are aligned according the the setup time of the setup/hold combination selected, +0.0 ps or -100 ps.



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Check the setup/hold combination

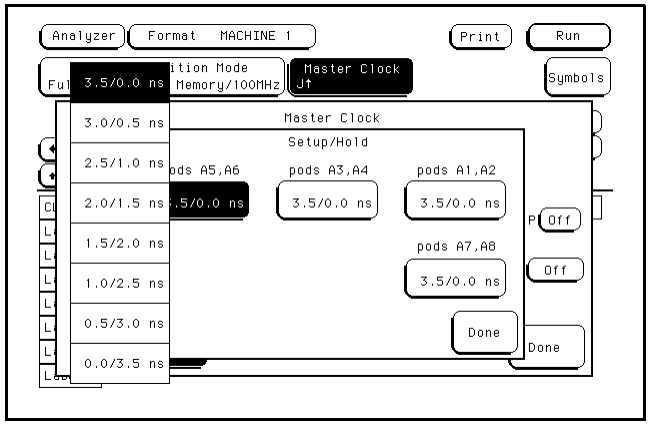
1 Select the logic analyzer setup/hold time.

a In the logic analyzer Format menu, select Master Clock.

b Select the Setup/Hold field, then select the setup/hold combination to be tested for all pods. The first time through this test, use the top combination in the following table.

Setup/Hold Combinations
3.5/0.0 ns
0.0/3.5 ns
1.5/2.0 ns

c Select Done to exit the setup/hold combinations.



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2 Disable the pulse generator channel 1 COMP (with the LED off).

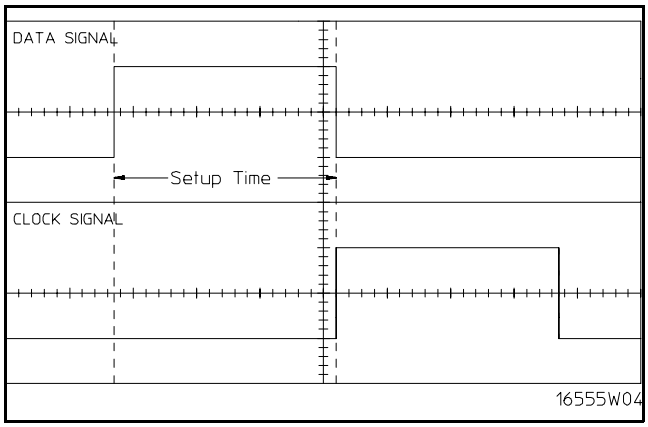
3 Using the Delay mode of the pulse generator channel 1, position the pulses according to the setup time of the setup/hold combination selected, +0.0 ps or –100 ps.

a On the Oscilloscope, select [Define meas] Define Δ Time - Stop edge: rising.

b In the oscilloscope timebase menu, select Position. Using the oscilloscope knob, position the rising edge of the clock waveform so that it is centered on the display.

c On the oscilloscope, select [Shift] Δ Time, then select [Enter] to display the setup time (Δ Time(1)-(2)).

d Adjust the pulse generator channel 1 Delay until the pulses are aligned according the the setup time of the setup/hold combination selected, +0.0 ps or -100 ps.



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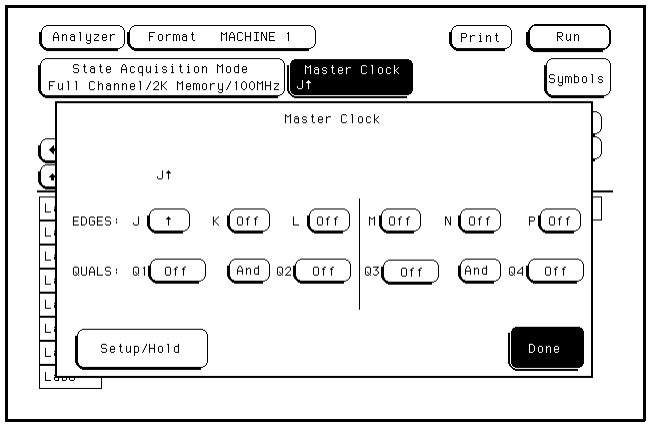
4 Select the clock to be tested.

a In the Master Clock menu, select the clock field to be tested, then select the clock edge as indicated in the table. The first time through this test, use the top clock and edge in the following table.

Clocks
J↑
K↑
L↑
M↑
N↑
P↑

b Connect the clock to be tested to the pulse generator channel 2 output.

c Select Done to exit the Master Clock menu.



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5 Note: This step is only done the first time through the test, to create a Compare file. For subsequent runs, go to step 6. **Use the following to create a Compare file:**

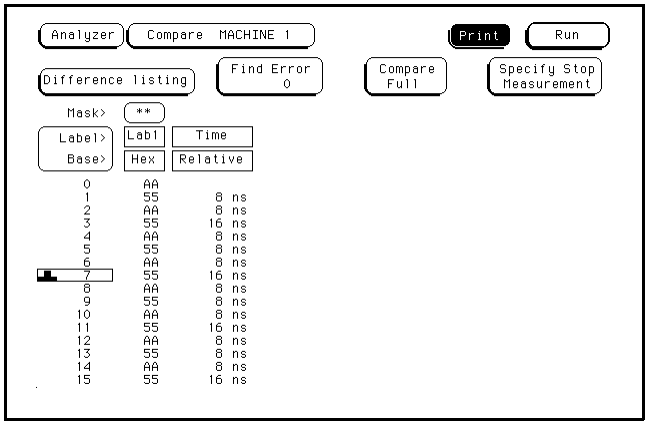
a Press Run. The display should show an alternating pattern of "AA" and "55". Verify the pattern by scrolling through the display.

b Press the List key. In the pop-up menu, use the RPG knob to move the cursor to Compare. Press Select.

c In the Compare menu, move the cursor to Copy Listing to Reference, then press the Select key.

d Move the cursor to Specify Stop Measurement and press the Select key. Press Select again to turn on Compare. At the pop up menu, select Compare. Move the cursor to the Equal field and press the Select key. At the pop up menu, select Not Equal. Press Done.

e Move the cursor to the Reference Listing field and select. The field should toggle to Difference Listing.



6 Press the blue shift key, then press the Run key. If two to four acquisitions are obtained without the "Stop Condition Satisfied" message appearing, then the test passes. Press Stop to halt the acquisition. Record the Pass or Fail results in the performance test record.

7 Test the next clock.

a Press the Format key, then select Master Clock.

b Turn off and disconnect the clock just tested.

c Repeat steps 4, 6, and 7 for the next clock edge listed in the table in step 4, until all listed clock edges have been tested.

8 Enable the pulse generator channel 1 COMP (with the LED on).

9 Check the clock pulse width.

a Enable the pulse generator channel 1, channel 2, and trigger outputs.

b In the oscilloscope Timebase menu, select Delay. Using the oscilloscope knob, position the clock waveform so that the waveform is centered on the screen.

c In the oscilloscope Delta V menu, set the Marker 1 Position to Chan 2, then set Marker 1 at –1.3000 V. Set the Marker 2 Position to Chan 2, then set Marker 2 at –1.3000 V.

d In the oscilloscope Delta T menu, select Start On Neg Edge 1. Select Stop on Pos Edge 1.

e If the pulse width is outside the limits, adjust the pulse generator channel 2 width and select the oscilloscope Precision Edge Find until the pulse width is within limits.

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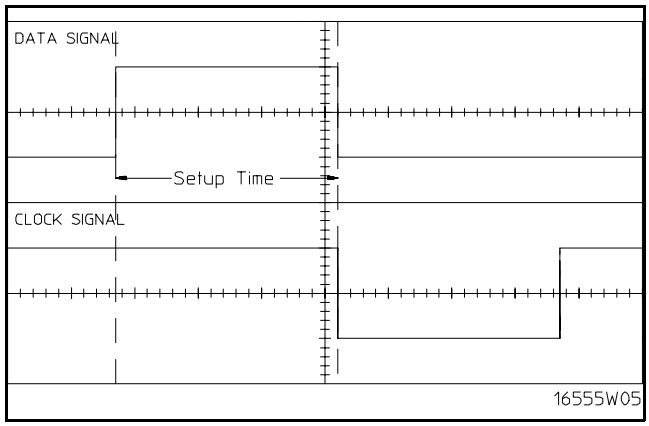
10 Using the Delay mode of the pulse generator channel 1, position the pulses according to the setup/hold combination selected, +0.0 ps or –100 ps.

a On the Oscilloscope, select [Define meas] Define Δ Time - Stop edge: falling.

b On the oscilloscope, select [Shift] - width: channel 2, then select [Enter] to verify the clock signal pulse width (- width(2)). If the pulse width is outside the limits, adjust the pulse generator channel 2 width until the clock pulse width is 3.480 ns, +20 ps or -80 ps.

c On the oscilloscope, select [Shift] Δ Time. Select Start src: channel 1, then select [Enter] to display the setup time (Δ Time(1)-(2)).

d Adjust the pulse generator channel 1 Delay until the pulses are aligned according the the setup time of the setup/hold combination selected, +0.0 ps or -100 ps.



11 Select the clock to be tested.

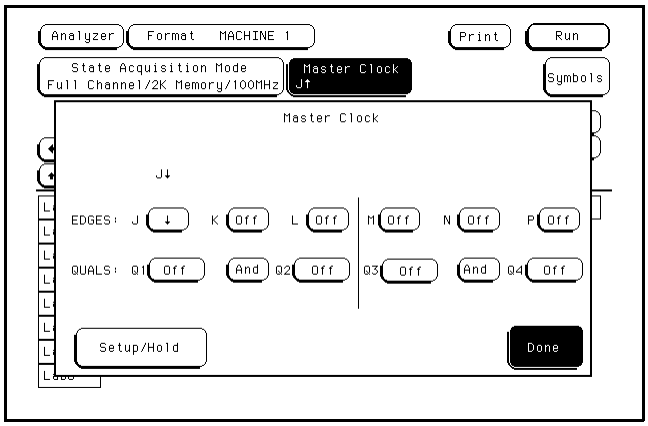
a In the Master Clock menu, select the clock field to be tested, then select the clock edge as indicated in the table. The first time through this test, use the top clock and edge.

Clocks
J↓
K↓
L↓
M↓
N↓
P↓

b Connect the clock to be tested to the pulse generator channel 2 output.

c Select Done to exit the Master Clock menu (see illustration next page).

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12 Press the blue shift key, then press the Run key. If two to four acquisitions are obtained without the "Stop Condition Satisfied" message appearing, then the test passes. Press Stop to halt the acquisition. Record the Pass or Fail results in the performance test record.

13 Test the next clock.

- **a** Press the Format key, then select Master Clock.
- **b** Turn off and disconnect the clock just tested.
- **c** Repeat steps 11, 12, and 13 for the next clock edge listed in the table in step 10, until all listed clock edges have been tested.

14 Test the next setup/hold combination.

- **a** In the logic analyzer Format menu, press Master Clock.
- **b** Turn off and disconnect the clock just tested.
- **c** Repeat steps 1 through 14 for the next setup/hold combination listed in step 1 on page 3–30, until all listed setup/hold combinations have been tested.

When aligning the data and clock waveforms using the oscilloscope, align the waveforms according to the setup time of the setup/hold combination being tested, +0.0 ps or –100 ps.

Test the next channels

Connect the next combination of data channels and clock channels, then test them.

Start on page 3–27, "Connect the logic analyzer," connect the next combination, then continue through the complete test.

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To test the multiple-clock, multiple-edge, state acquisition (logic analyzer)

Testing the multiple-clock, multiple-edge, state acquisition verifies the performance of the following specifications:

- Minimum master to master clock time
- Maximum state acquisition speed
- Setup/Hold time for multiple-clock, multiple-edge, state acquisition
- Minimum clock pulse width

This test checks two combinations of data using multiple clocks at three selected setup/hold times.

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part
Pulse Generator	100 MHz 3.5 ns pulse width, < 600 ps rise time	HP 8133A option 003
Digitizing Oscilloscope	≥ 6 GHz bandwidth, < 58 ps rise time	HP 54750A, with HP 54751A plugin
Adapter	SMA(m)-BNC(f)	HP 1250-1200
SMA Coax Cable (Qty 3)	18 GHz bandwidth	HP 8120-4948
Coupler	BNC(m)(m)	HP 1250-0216
BNC Test Connector, 6x2 (Qty 4)		

Set up the equipment

1 Turn on the equipment required and the logic analyzer. Let them warm up for 30 minutes before beginning the test if you have not already done so.

2 Set up the pulse generator.

a Set up the pulse generator according to the following table.

Pulse Generator Setup

Timebase	Channel 2	Period	Channel 1
Mode: Int	Mode: Pulse	Divide: Divide ÷ 2	Mode: Pulse
Period: 10.000 ns	Divide: PULSE ÷ 2	Ampl: 0.50 V	Delay: 0.000 ns
	Width: 4.500 ns	Offs: 0.00 V	Width: 3.500 ns
	High: –0.90 V		High: –0.90 V
	Low: –1.70 V		Low: –1.70 V

b Disable the pulse generator channel 1 COMP (with the LED off).

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3 Set up the oscilloscope. If the oscilloscope was not configured for the previous test, then do the following steps.

a Select Setup, then select Default Setup.

b Configure the oscilloscope according to the following table.

Oscilloscope Setup

Acquisition	**Display**	**Trigger**	**[Shift] Δ Time**
Averaging: On # of averages: 16	Graticule Graphs: 2	Level: -250 mV	Stop src: channel 2 [Enter]

Channel 1	**Channel 2**	**Define meas**
Alternate Scale Attenuation: 20.00:1 Scale: 200 mV/div Offset: –1.300 V	Alternate Scale Attenuation: 20.00:1 Scale: 200 mV/div Offset: -1.300 V	Thresholds: user-defined Units: Volts Upper: -980 mV Middle: -1.30 V Lower: -1.62 V

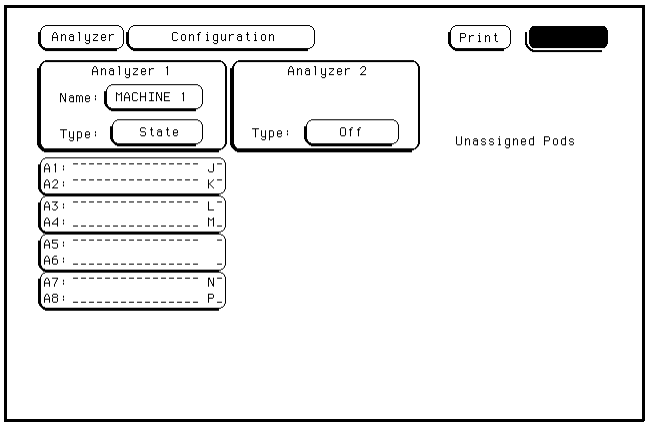
Set up the logic analyzer

1 Set up the Configuration menu.

a Press the Config key.

b In the Configuration menu, assign all pods to Machine 1. To assign pods, select the pod fields, then select Machine 1.

c In the Analyzer 1 box, select the Type field, then select State.

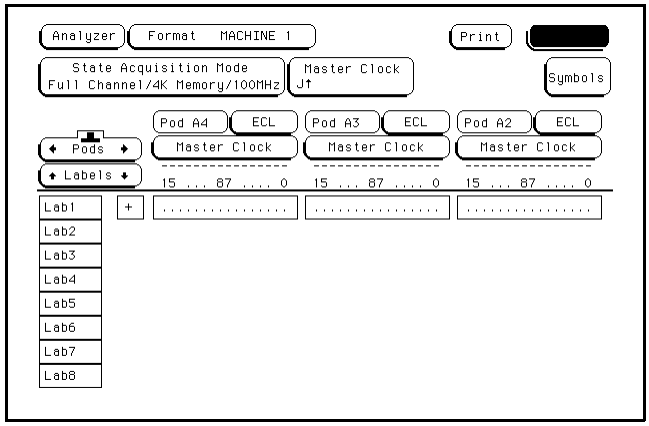


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2 Set up the Format menu.

a Press the Format key. Select State Acquisition Mode, then select Full Channel/4K Memory/100MHz.

b Select the field to the right of each Pod field, then select ECL. The screen does not show all Pod fields at one time. Use the knob to access more Pod fields.



3 Set up the Trigger menu.

a Press the Trigger key. Select Modify Trigger, then select Clear Trigger, then select All.

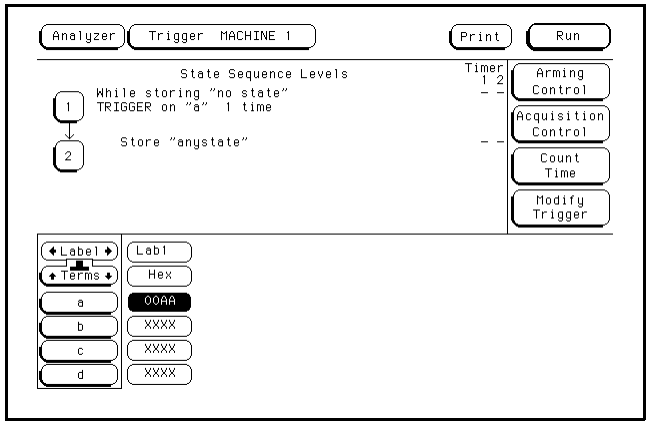
b Select the Count Off field, then select Time in the pop-up menu. Select Done to exit the menu.

c Select the field labeled 1 under the State Sequence Levels. Select the field labeled "anystate", then select "no state." Select Done to exit the State Sequence Levels menu.

d Select the field next to the pattern recognizer "a," under the label Lab1. Type the following for your logic analyzer, then press Select.

HP 1660C/CS/CP – "00AA" HP 1662C/CS/CP – "00AA"

HP 1661C/CS/CP – "002A" HP 1663C/CS/CP – "000A"



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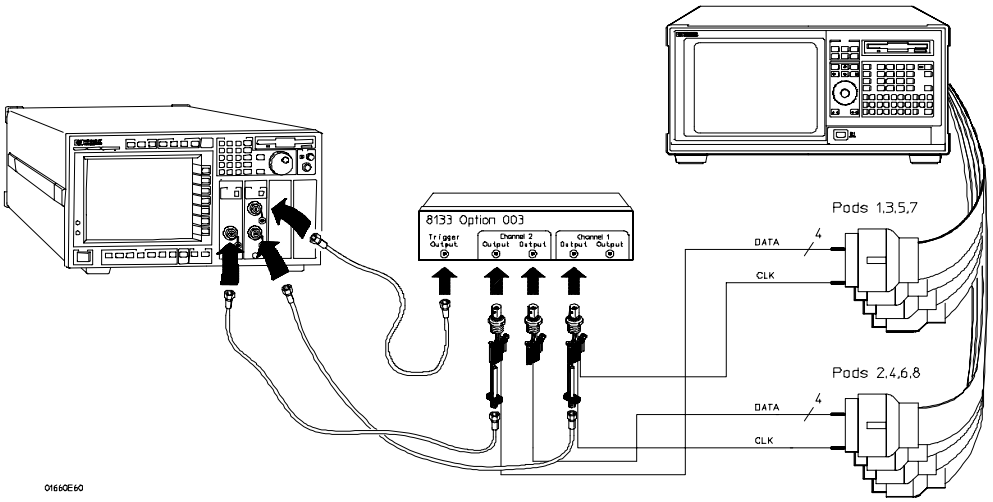
Connect the logic analyzer

1 Using the 6-by-2 test connectors, connect the first combination of logic analyzer clock and data channels listed in one of the following tables to the pulse generator.
If you are testing an HP 1660C or HP 1661C, you will repeat this test for the second combination.

2 Using SMA cables, connect channel 1, channel 2, and trigger of the oscilloscope to the pulse generator.

Connect the HP 1660C/CS/CP or HP 1661C/CS/CP Logic Analyzer to the Pulse Generator

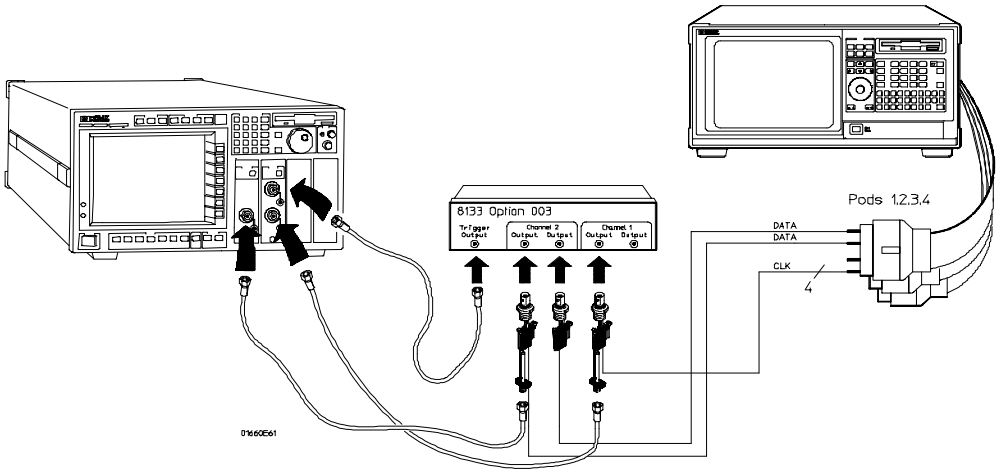
Testing Combinations	Connect to HP 8133A Channel 2 Output	Connect to HP 8133A Channel 2 Output	Connect to HP 8133A Channel 1 Output
1	Pod 1, channel 3 Pod 3, channel 3 Pod 5, channel 3 Pod 7, channel 3	Pod 2, channel 3 Pod 4, channel 3 Pod 6, channel 3 Pod 8, channel 3	J-clock M-clock N-clock
2	Pod 1, channel 11 Pod 3, channel 11 Pod 5, channel 11 Pod 7, channel 11	Pod 2, channel 11 Pod 4, channel 11 Pod 6, channel 11 Pod 8, channel 11	J-clock M-clock N-clock



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Connect the HP 1662C/CS/CP or HP 1663C/CS/CP Logic Analyzer to the Pulse Generator

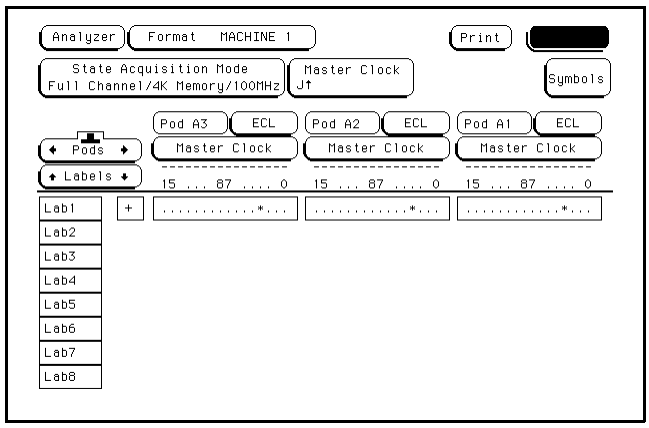
Testing Combination	Connect to HP 8133A Channel 2 Output	Connect to HP 8133A Channel 2 Output	Connect to HP 8133A Channel 1 Output
1	Pod 1, channel 3 Pod 2, channel 3 Pod 3, channel 3 Pod 4, channel 3	Pod 1, channel 11 Pod 2, channel 11 Pod 3, channel 11 Pod 4, channel 11	J-clock K-clock L-clock M-clock



3 Activate the data channels that are connected according to one of the previous tables.

a Press the Format key.

b Select the field showing the channel assignments for one of the pods being tested. Press the Clear entry key. Using the arrow keys, move the selector to the data channels to be tested, then press the Select key. An asterisk means that a channel is turned on. When all the correct channels of the pod are turned on, press the Done key. Follow this step for the remaining pods.

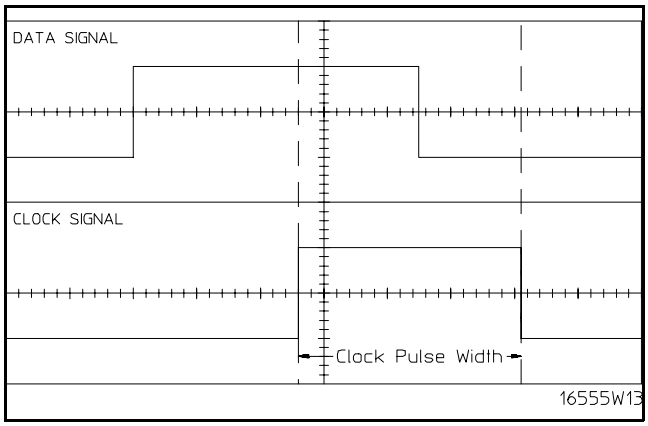


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Verify the test signal

1 Check the clock pulse width. Using the oscilloscope, verify that the clock pulse width is 3.500 ns, +0 ps or –100 ps.

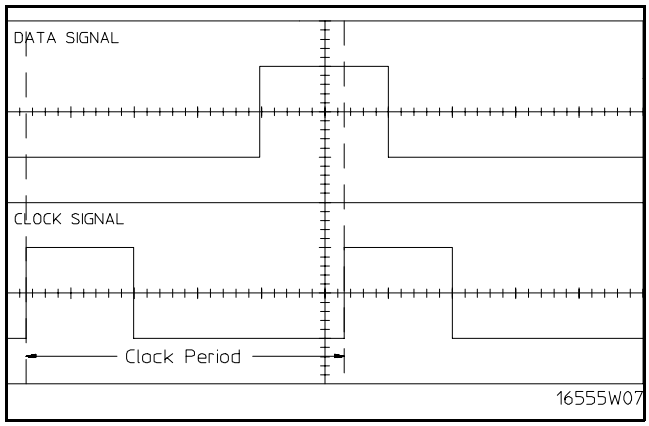
- **a** Enable the pulse generator channel 1, channel 2, and trigger outputs (LED off).
- **b** In the oscilloscope Timebase menu, select Scale: 1.000 ns/div.
- **c** In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the clock waveform so that the waveform is centered on the screen.
- **d** On the oscilloscope, select [Shift] + width: channel 2, then select [Enter] to display the clock signal pulse width (+ width (2)).
- **e** If the pulse width is outside the limits, adjust the pulse generator channel 2 width until the pulse width is within limits.



2 Check the clock period. Using the oscilloscope, verify that the clock period is 10.000 ns, +0 ps or –250 ps.

- **a** In the oscilloscope Timebase menu, select Scale: 2.000 ns/div.
- **b** In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the clock waveform so that a rising edge appears at the left of the display.
- **c** On the oscilloscope, select [Shift] Period: channel 2, then select [Enter] to display the clock period (Period(2)). If the period is not less than 10.000 ns, go to step d. If the period is less than 10.000 ns, go to step 3.
- **d** In the oscilloscope Timebase menu, increase Position 10.000 ns. If the period is not less than 10.000 ns, decrease the pulse generator Chan 2 Doub in 10 ps increments until one of the two periods measured is less than 10.000 ns.

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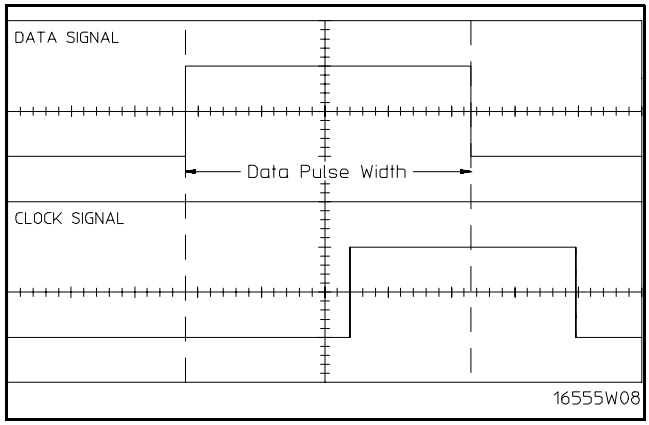
3 Check the data pulse width. Using the oscilloscope verify that the data pulse width is 4.500 ns, +0 ps or −100 ps.

a In the oscilloscope Timebase menu, select Scale: 1.000 ns/div.

b In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the data waveform so that the waveform is centered on the screen.

c On the oscilloscope, select [Shift] + width: channel 1, then select [Enter] to display the data signal pulse width (+ width (1)).

d If the pulse width is outside the limits, adjust the pulse generator channel 1 width until the pulse width is within limits.



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Check the setup/hold with single clock edges, multiple clocks

1 Select the logic analyzer setup/hold time.

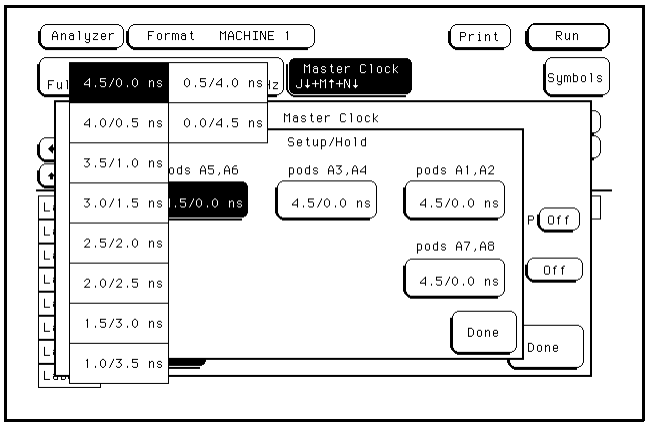
a In the logic analyzer Format menu, select Master Clock.

b Select and activate any two clock edges.

c Select the Setup/Hold field and select the setup/hold to be tested for all pods. The first time through this test, use the top combination in the following table.

Setup/Hold Combinations
4.5/0.0 ns
0.0/4.5 ns
2.0/2.5 ns

d Select Done to exit the setup/hold combinations.



2 Disable the pulse generator channel 1 COMP (with the LED off).

3 Using the Delay mode of the pulse generator channel 1, position the pulses according to the setup time of the setup/hold combination selected, +0.0 ps or –100 ps.

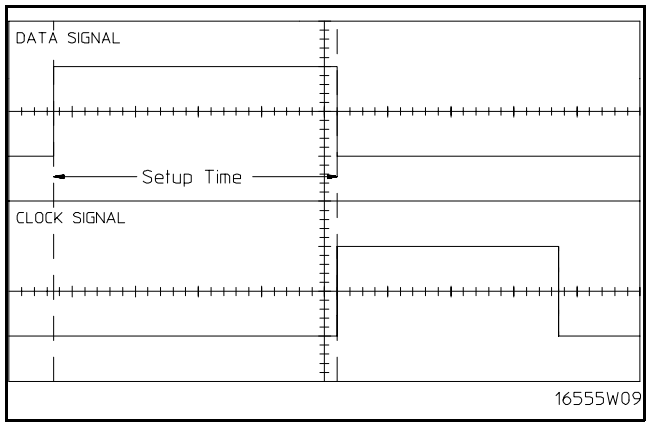
a On the Oscilloscope, select [Define meas] Define Δ Time - Stop edge: rising.

b In the oscilloscope timebase menu, select Position. Using the oscilloscope knob, position the rising edge of the clock waveform so that it is centered on the display.

c On the oscilloscope, select [Shift] Δ Time, then select [Enter] to display the setup time (Δ Time(1)-(2)).

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d Adjust the pulse generator channel 1 Delay until the pulses are aligned according the the setup time of the setup/hold combination selected, +0.0 ps or -100 ps.



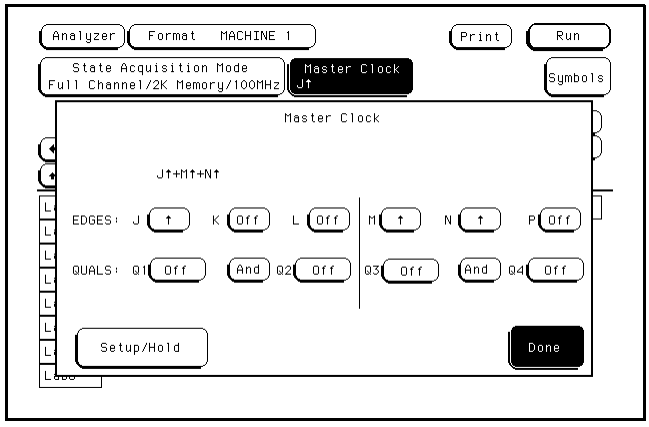
4 Select the clocks to be tested.

a Select the clock field to be tested and then select the clock edges as indicated in the table. The first time through this test, use the top clocks and edges (HP 1660C/CS/CP and HP 1661C/CS/CP). Note that the clocks used depends on which logic analyzer you have.

Clocks	
HP 1660C/CS/CP and HP 1661C/CS/CP	**HP 1662C/CS/CP and HP 1663C/CS/CP**
J↑ + M↑ + N↑ K↑ + L↑ + P↑	J↑ + K↑ + L↑ + M↑

b Connect the rising edge clocks to the pulse generator channel 2 output.

c Select Done to exit the Master Clock menu.



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5 If you have not already created a Compare file for the previous test (single-clock, single-edge state acquisition, page 32), use the following steps to create one. For subsequent passes through this test, skip this step and go to step 6.

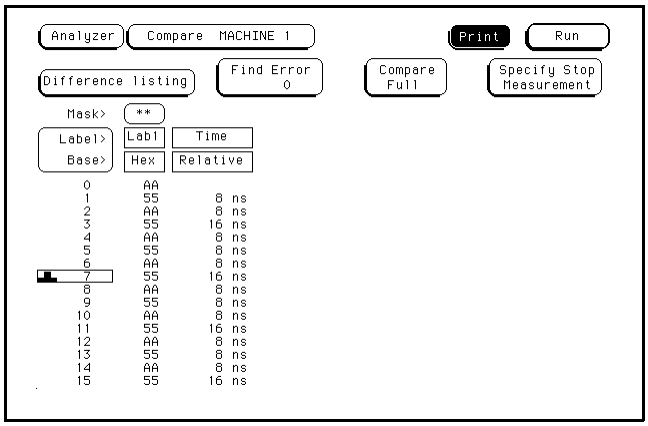
a Press Run. The display should show an alternating pattern of "AA" and "55". Verify the pattern by scrolling through the display.

b Press the List key. In the pop up menu, use the RPG knob to move the cursor to Compare. Press Select.

c In the Compare menu, move the cursor to Copy Listing to Reference, then press the Select key.

d Move the cursor to Specify Stop Measurement and press the Select key. Press Select again to turn on Compare. At the pop up menu, select Compare. Move the cursor to the Equal field and press the Select key. At the pop up menu, select Not Equal. Press Done.

e Move the cursor to the Reference Listing field and select. The field should toggle to Difference Listing.



6 Press the blue shift key, then press the Run key. If 2 - 4 acquisitions are obtained without the "Stop Condition Satisfied" message appearing, then the test passes. Press Stop to halt the acquisition. Record the Pass or Fail results in the performance test record.

7 Enable the pulse generator channel 1 COMP (with the LED on).

8 Check the clock pulse width.

a Enable the pulse generator channel 1, channel 2, and trigger outputs (with the LED off).

b In the oscilloscope Timebase menu, select Delay. Using the oscilloscope knob, position the clock waveform so that the waveform is centered on the screen.

c In the oscilloscope Delta V menu, set the Marker 1 Position to Chan 2, then set Marker 1 at –1.3000 V. Set the Marker 2 Position to Chan 2, then set Marker 2 at –1.3000 V.

d In the oscilloscope Delta T menu, select Start On Neg Edge 1. Select Stop On Pos Edge 1.

e If the pulse width is outside of the limits, adjust the pulse generator channel 2 width and select the oscilloscope Precision Edge Find until the pulse width is within limits.

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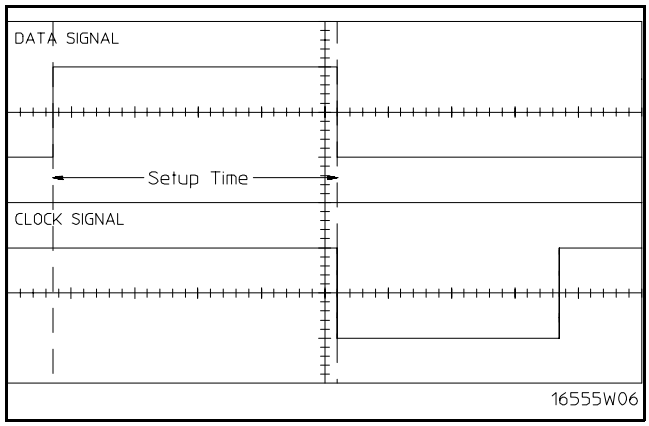
9 Using the Delay mode of the pulse generator channel 1, position the pulses according to setup time of the setup/hold combination selected, +0.0 ps or –100 ps.

a On the Oscilloscope, select [Define meas] Define Δ Time - Stop edge: falling.

b On the oscilloscope, select [Shift] - width: channel 2, then select [Enter] to verify the clock signal pulse width (- width (2)). If the pulse width is outside the limits, adjust the pulse generator channel 2 width until the clock pulse width is 3.480 ns, +20 ps or -80 ps.

c On the oscilloscope, select [Shift] Δ Time. Select Start src: channel 1, then select [Enter] to display the setup time (Δ Time (1)-(2)).

d Adjust the pulse generator channel 1 Delay until the pulses are aligned according the the setup time of the setup/hold combination selected, +0.0 ps or -100 ps.

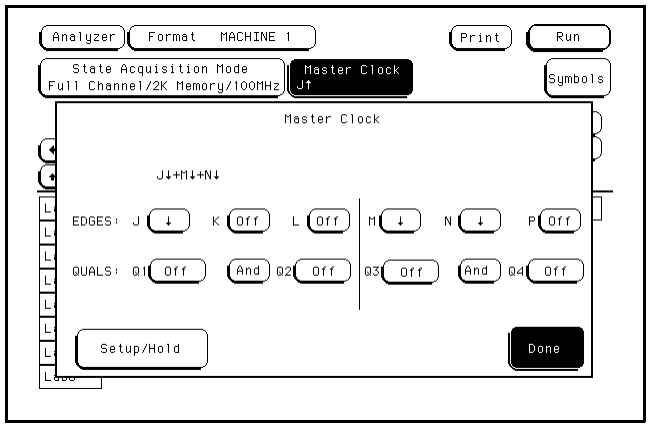


10 Select the clocks to be tested.

a Select the clock field to be tested, then select the clock edges as indicated in the table. The first time through this test, use the top clocks and edges (HP 1660C/CS/CP and HP 1661C/CS/CP).

Clocks	
HP 1660C/CS/CP and HP 1661C/CS/CP	**HP 1662C/CS/CP and HP 1663C/CS/CP**
J↓ + M↓ + N↓ K↓ + L↓ + P↓	J↓ + K↓ + L↓ + M↓

b Select Done to exit the Master Clock menu.



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11 Press the blue shift key, then press the Run key. If 2 - 4 acquisitions are obtained without the "Stop Condition Satisfied" message appearing, then the test passes. Press Stop to halt the acquisition. Record the Pass or Fail results in the performance test record.

12 Test the next clocks.

a In the logic analyzer Format menu, select Master Clock.

b Turn off and disconnect the clocks just tested.

c Repeat steps 2 through 12 for the next clock edges listed in the table in step 4, until all listed clock edges have been tested.

13 Test the next setup/hold combination.

a In the logic analyzer Format menu, select Master Clock.

b Turn off and disconnect the clocks just tested.

c Repeat steps 1 through 12 for the next setup/hold combination listed in step 1 on page 3-42, until all listed setup/hold combinations have been tested.

When aligning the data and clock waveforms using the oscilloscope, align the waveforms according to the setup time of the setup/hold combination being tested, +0.0 ps or –100 ps.

Test the next channels

Connect the next combination of data channels and clock channels, then test them.

Start on page 3–40 "Connect the logic analyzer," connect the next combination, then continue through the complete test.

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To test the single-clock, multiple-edge, state acquisition (logic analyzer)

Testing the single-clock, multiple-edge, state acquisition verifies the performance of the following specifications:

- Minimum master to master clock time
- Maximum state acquisition speed
- Setup/Hold time for single-clock, multiple-edge, state acquisition
- Minimum clock pulse width

This test checks two combinations of data using a multiple-edge single clock at three selected setup/hold times.

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part
Pulse Generator	100 MHz 3.5 ns pulse width, < 600 ps rise time	HP 8133A option 003
Digitizing Oscilloscope	≥ 6 GHz bandwidth, < 58 ps rise time	HP 54750A, with HP 54751A plugin
Adapter	SMA(m)-BNC(f)	HP 1250-1200
SMA Coax Cable (Qty 3)	18 GHz bandwidth	HP 8120-4948
Coupler	BNC(m)(m)	HP 1250-0216
BNC Test Connector, 6x2 (Qty 4)		

Set up the equipment

1 Turn on the equipment required and the logic analyzer. Let them warm up for 30 minutes before beginning the test if you have not already done so.

2 Set up the pulse generator according to the following table.

Pulse Generator Setup

Timebase	Channel 2	Period	Channel 1
Mode: Int	Mode: Square	Divide: Divide ÷ 2	Mode: Pulse
Period: 10.000 ns	Divide: SQUARE ÷ 2	Ampl: 0.50 V	Delay: 0.000 ns
	Delay: 0.000 ns	Offs: 0.00 V	Width: 4.00 ns
	High: –0.90 V		High: –0.90 V
	Low: –1.70 V		Low: –1.70 V
	COMP: Disabled (LED Off)		COMP: Disabled (LED Off)

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3 Set up the oscilloscope. If the oscilloscope was not configured for the previous test, then do the following steps.

a Select Setup, then select Default Setup.

b Configure the oscilloscope according to the following table.

Oscilloscope Setup

Acquisition	**Display**	**Trigger**	**[Shift] Δ Time**
Averaging: On # of averages: 16	Graticule Graphs: 2	Level: -250 mV	Stop src: channel 2 [Enter]

Channel 1	**Channel 2**	**Define meas**
Alternate Scale Attenuation: 20.00:1 Scale: 200 mV/div Offset: –1.300 V	Alternate Scale Attenuation: 20.00:1 Scale: 200 mV/div Offset: -1.300 V	Thresholds: user-defined Units: Volts Upper: -980 mV Middle: -1.30 V Lower: -1.62 V

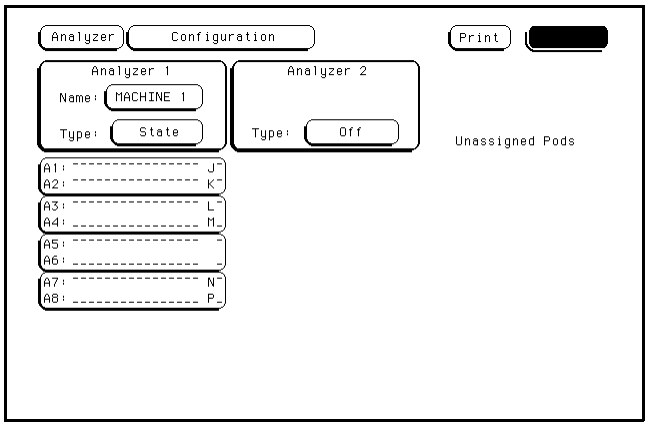
Set up the logic analyzer

1 Set up the Configuration menu.

a Press the Config key.

b In the Configuration menu, assign all pods to Machine 1. To assign all pods, select the pod fields, then select Machine 1.

c Select the Type field in the Analyzer 1 box, then select State.

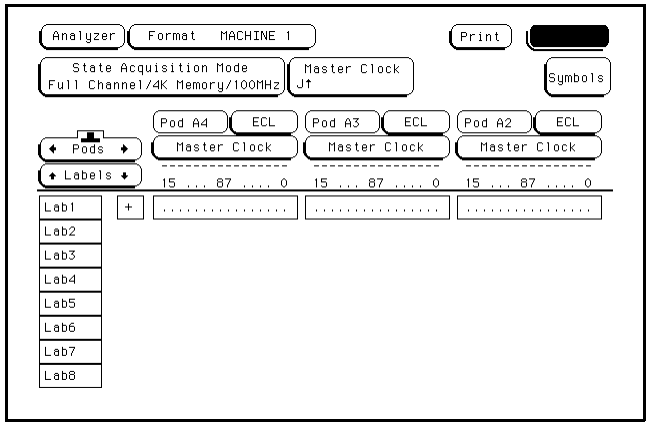


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2 Set up the Format menu.

a Press the Format key. Select State Acquisition Mode, then select Full Channel/4K Memory/100MHz.

b Select the field to the right of each pod field, then select ECL. The screen does not show all pod fields at one time. Use the knob to access pod fields not shown on the screen.



3 Set up the Trigger menu.

a Press the Trigger key. Select Modify Trigger, select Clear Trigger, then select All in the pop-up menu.

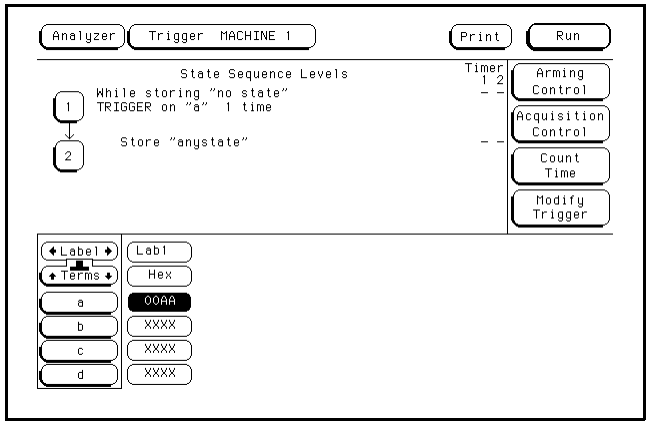
b Select Count Off. Press Select again, then select Time in the pop-up menu. Select Done to exit the menu.

c Select the field labeled 1 under the State Sequence Levels. Select the field labeled "anystate," then select "no state." Select Done to exit the State Sequence Levels menu.

d Select the field next to "a," under the label Lab1. Type the following for your logic analyzer, then press the Select key.

HP 1660C/CS/CP – "00AA" HP 1662C/CS/CP – "00AA"

HP 1661C/CS/CP – "002A" HP 1663C/CS/CP – "000A"



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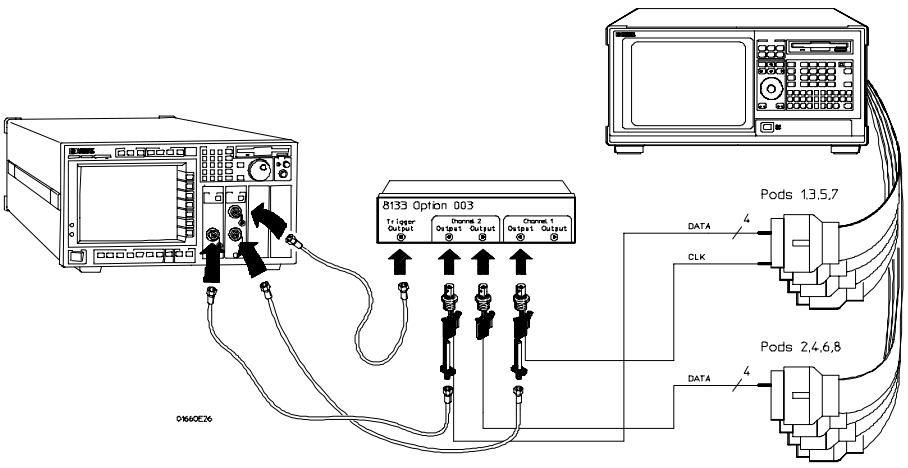
Connect the logic analyzer

1 Using the 6-by-2 test connectors, connect the first combination of logic analyzer clock and data channels listed in one of the following tables to the pulse generator.
If you are testing an HP 1660C or HP 1661C, you will repeat this test for the second combination.

2 Using the SMA cables, connect channel 1, channel 2, and trigger from the oscilloscope to the pulse generator.

Connect the HP 1660C/CS/CP or HP 1661C/CS/CP Logic Analyzer to the Pulse Generator

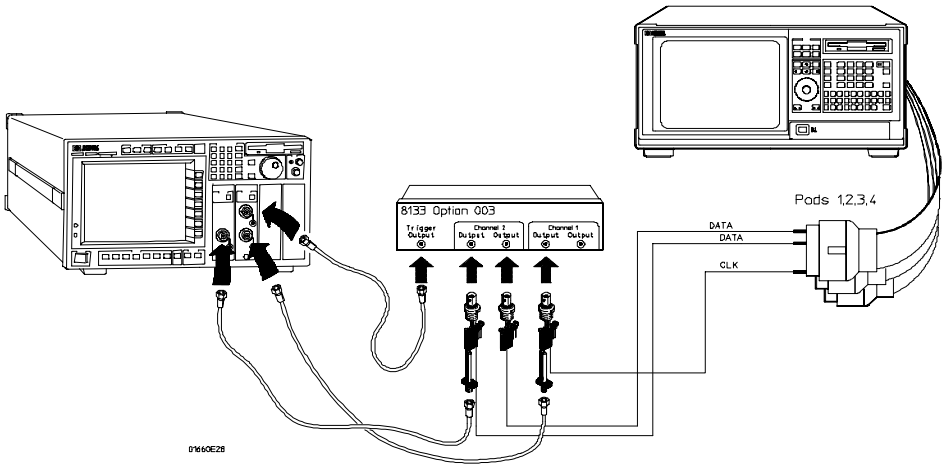
Testing Combinations	Connect to HP 8133A Channel 2 Output	Connect to HP 8133A Channel 2 $\overline{\text{Output}}$	Connect to HP 8133A Channel 1 Output
1	Pod 1, channel 3 Pod 3, channel 3 Pod 5, channel 3 Pod 7, channel 3	Pod 2, channel 3 Pod 4, channel 3 Pod 6, channel 3 Pod 8, channel 3	J-clock
2	Pod 1, channel 11 Pod 3, channel 11 Pod 5, channel 11 Pod 7, channel 11	Pod 2, channel 11 Pod 4, channel 11 Pod 6, channel 11 Pod 8, channel 11	J-clock



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Connect the HP 1662C/CS/CP or HP 1663C/CS/CP Logic Analyzer to the Pulse Generator

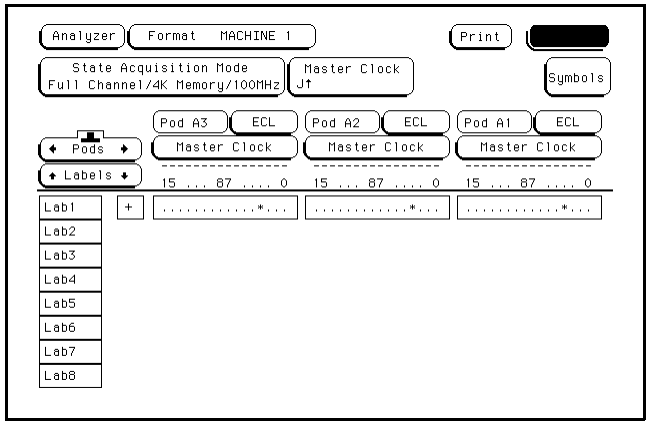
Testing Combination	Connect to HP 8133A Channel 2 Output	Connect to HP 8133A Channel 2 $\overline{\text{Output}}$	Connect to HP 8133A Channel 1 Output
1	Pod 1, channel 3 Pod 2, channel 3 Pod 3, channel 3 Pod 4, channel 3	Pod 1, channel 3 Pod 2, channel 3 Pod 3, channel 3 Pod 4, channel 3	J-clock



3 Activate the data channels that are connected according to one of the previous tables.

a Press the Format key.

b Select the field showing the channel assignments for one of the pods being tested. Press the Clear entry key. Using the arrow keys, move the selector to the data channels to be tested, then press the Select key. An asterisk means that a channel is turned on. When all the correct channels of the pod are turned on, press the Done key. Follow this step for the remaining pods.

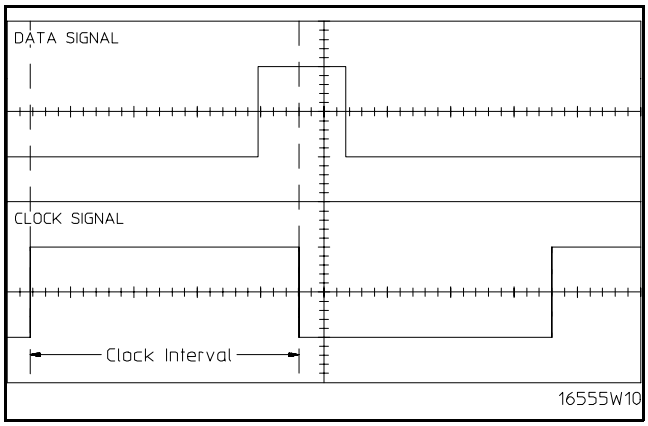


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Verify the test signal

1 Check the clock period. Using the oscilloscope, verify that the master-to-master clock time is 10.000 ns, +0 ps or -250 ps.

- **a** Enable the pulse generator channel 1, channel 2, and trigger outputs (LED off).
- **b** In the oscilloscope Timebase menu, select Scale: 2.500 ns/div.
- **c** In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the clock waveform so that a rising edge appears at the left of the display.
- **d** On the oscilloscope, select [Shift] + width: channel 2, then select [Enter] to display the master-to-master clock time (+ width(2)). If the positive-going pulse width is more than 10.000 ns, go to step d. If the positive-going pulse width is less than or equal to 10.000 ns but greater than 9.750 ns, go to step 2.
- **e** On the oscilloscope, select [Shift] - width: channel 2, then select [Enter] (- width(2)). If the negative pulse width is less than or equal to 10.000 ns but greater than 9.750 ns, go to step 2.
- **f** Decrease the pulse generator Period in 100 ps increments until the oscilloscope + width (2) or - width (2) read less than or equal to 10.000 ns, but greater than 9.750 ns.



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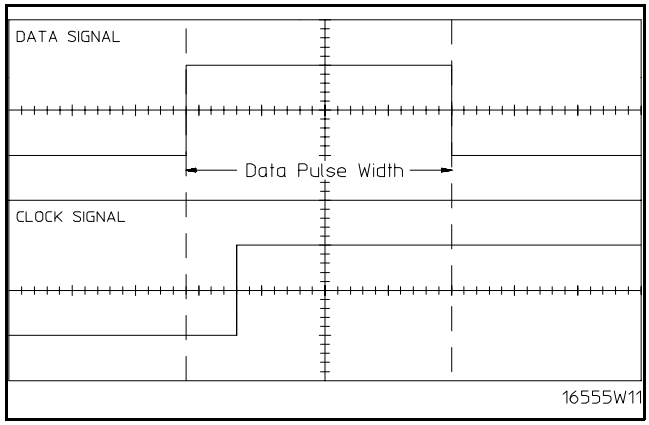
2 Check the data pulse width. Using the oscilloscope, verify that the data pulse width is 4.000 ns, +0 ps or –100 ps.

a In the oscilloscope Timebase menu, select Scale: 1.000 ns/div.

b In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the data waveform so that the waveform is centered on the screen.

c On the oscilloscope, select [Shift] + width: channel 1, then select [Enter] to display the data signal pulse width (+ width(1)).

d If the pulse width is outside the limits, adjust the pulse generator channel 1 width until the pulse width is within limits.



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Check the setup/hold with single clock, multiple clock edges

1 Select the logic analyzer setup/hold time.

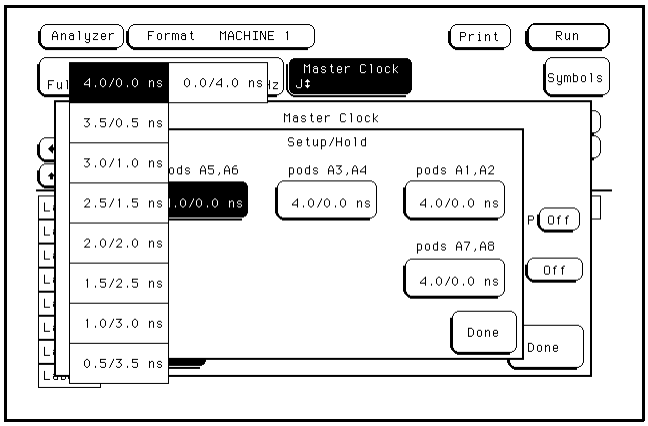
a In the logic analyzer Format menu, select Master Clock.

b Select and activate any multiple clock edge.

c Select the Setup/Hold field, then select the setup/hold to be tested for all pods. The first time through this test, use the top combination in the following table.

Setup/Hold Combinations
4.0/0.0 ns
0.0/4.0 ns
2.0/2.0 ns

d Select Done to exit the setup/hold combinations.



2 Using the Delay mode of the pulse generator channel 2, position the pulses according to the setup time of the setup/hold combination selected, +0.0 ps or –100 ps.

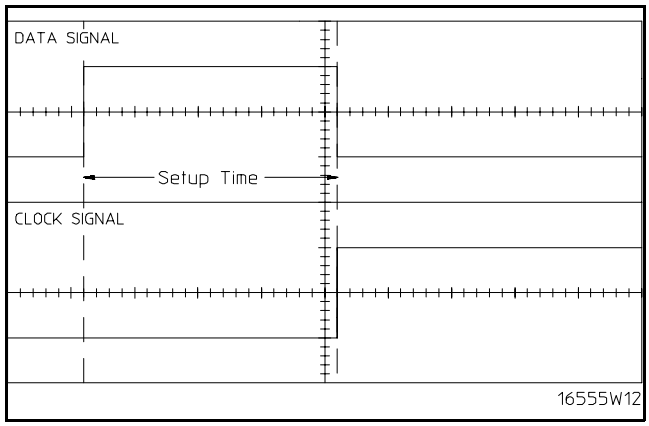
a On the Oscilloscope, select [Define meas] Define Δ Time - Stop edge: rising.

b In the oscilloscope timebase menu, select Position. Using the oscilloscope knob, position the falling edge of the data waveform so that it is centered on the display.

c On the oscilloscope, select [Shift] Δ Time. Select Start src: channel 1, then select [Enter] to display the setup time (Δ Time(1)-(2)).

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d Adjust the pulse generator channel 2 Delay until the pulses are aligned according the the setup time of the setup/hold combination selected, +0.0 ps or -100 ps.



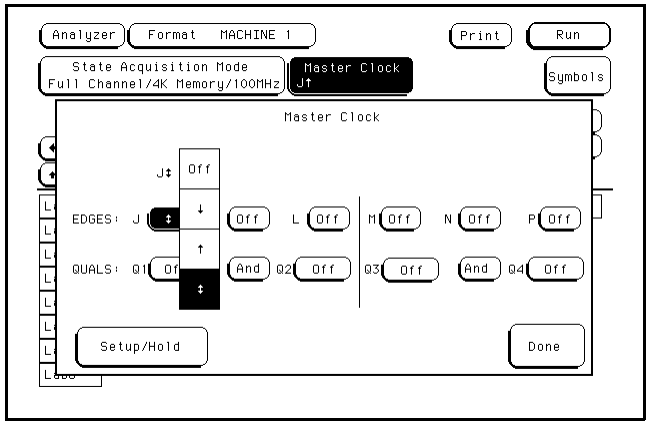
3 Select the clock to be tested.

a Select the clock field to be tested, then select the clock as indicated in the table. The first time through this test, use the top multiple-edge clock in the following table.

Clocks
J↕
K↕
L↕
M↕
N↕
P↕

b Connect the clock to be tested to the pulse generator channel 2 output.

c Select Done to exit the Master Clock menu.



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4 If you have not already created a Compare file for the previous test (single-clock, single-edge state acquisition, page 32), use the following steps to create one. For subsequent passes through this test, skip this step and go to step 5.

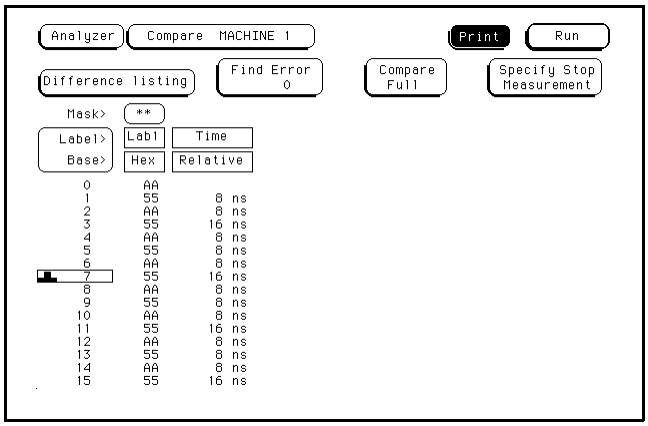
a Press Run. The display should show an alternating pattern of "AA" and "55". Verify the pattern by scrolling through the display.

b Press the List key. In the pop up menu, use the RPG knob to move the cursor to Compare. Press Select.

c In the Compare menu, move the cursor to Copy Listing to Reference, then press the Select key.

d Move the cursor to Specify Stop Measurement and press the Select key. Press Select again to turn on Compare. At the pop up menu, select Compare. Move the cursor to the Equal field and press the Select key. At the pop up menu, select Not Equal. Press Done.

e Move the cursor to the Reference Listing field and select. The field should toggle to Difference Listing.



5 Press the blue shift key, then press the Run key. If 2 - 4 acquisitions are obtained without the "Stop Condition Satisfied" message appearing, then the test passes. Press Stop to halt the acquisition. Record the Pass or Fail results in the performance test record.

6 Test the next clock.

a Press the Format key, then select Master Clock.

b Turn off and disconnect the clock just tested.

c Repeat steps 4, 6 and 7 for the next clock listed in the table in step 4, until all clocks have been tested.

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7 Test the next setup/hold combination.

a In the logic analyzer Format menu, select Master Clock.

b Turn off and disconnect the clock just tested.

c Repeat steps 1 through 6 for the next setup/hold combination listed in step 1 on page 3–54, until all listed setup/hold combinations have been tested.

When aligning the data and clock waveforms using the oscilloscope, align the waveforms according to the setup time of the setup/hold combination being tested, +0.0 ps or –100 ps.

Test the next channels

- Connect the next combination of data channels and clock channels, then test them.

  Start on page 3–52, "Connect the logic analyzer," connect the next combination, then continue through the complete test.

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To test the time interval accuracy (logic analyzer)

Testing the time interval accuracy does not check a specification, but does check the following:

- 125 MHz oscillator

This test verifies that the 125 MHz timing acquisition synchronizing oscillator is operating within limits.

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part
Pulse Generator	100 MHz 3.5 ns pulse width, < 600 ps rise time	HP 8133A option 003
Function Generator	Accuracy ≤ (5)(10^{-6}) × frequency	HP 3325B Option 002
SMA Cable		HP 8120-4948
Adapter	BNC(m)-SMA(f)	HP 1250-2015
BNC Test Connector, 6x2		

Set up the equipment

1 Turn on the equipment required and the logic analyzer. Let them warm up for 30 minutes if you have not already done so.

2 Set up the pulse generator according to the following table.

Pulse Generator Setup

Timebase	Channel 1	Trigger
Mode: Ext	Mode: Square	Divide: Divide ÷ 1
Period: 25.000 ns	Delay: 0.000 ns	Ampl: 0.50 V
	High: –0.90 V	Offs: 0.00 V
	Low: –1.70 V	
	COMP: Disabled (LED off)	

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3 Set up the function generator according to the following table.

Function Generator Setup
Freq: 40.000 00 MHz
Amptd: 1.00 V
Modulation: Off

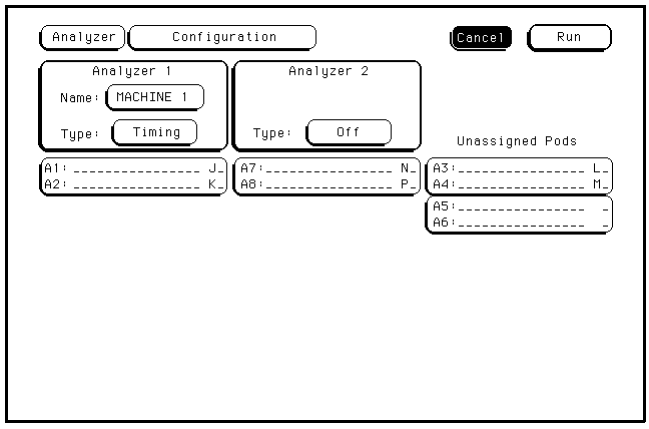
Set up the logic analyzer

1 Set up the Configuration menu.

a Press the Config key.

b In the Configuration menu, assign Pod 1 to Machine 1. To assign Pod 1, select the Pod 1 field, then select Machine 1.

c In the Analyzer 1 box, select the Type field, then select Timing.



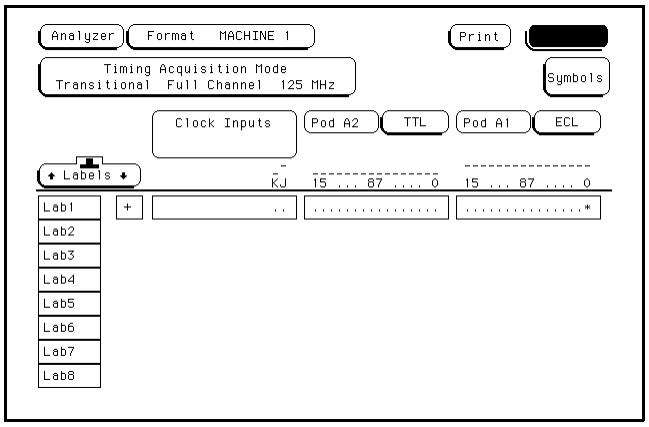
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2 Set up the Format menu.

a Press the Format key. Select Timing Acquisition Mode, then select Conditional Halt Channel 500 MHz.

b Select the field to the right of the Pod 1 field, then select ECL.

c Select the field showing the channel assignments for Pod 1. Deactivate all channels by pressing the Clear entry key. Using the arrow keys, move the selector to Channel 0. Press the Select key to put an asterisk in the channel position, activating the channel, then press the Done key.



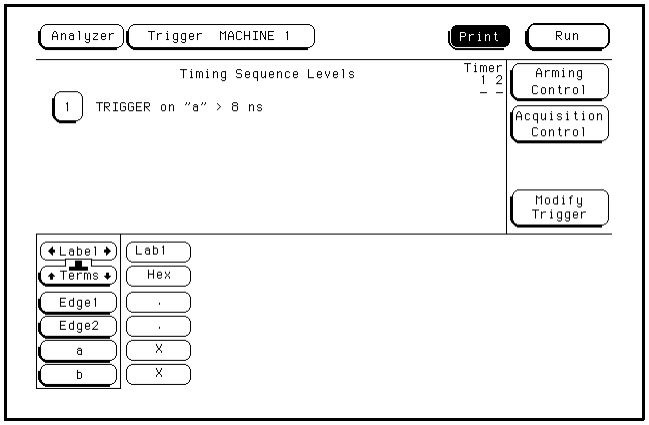
3 Set up the Trigger menu.

a Select Acquisition Control. Select the Acquisition Mode field, and the acquisition mode should toggle to Manual.

b Select Trigger Position. In the Pop-up menu, select Start.

c Select the Sample Period field. In the numeric pop-up menu, select 8 ns.

d Press the Done key to exit the Acquisition Control menu.



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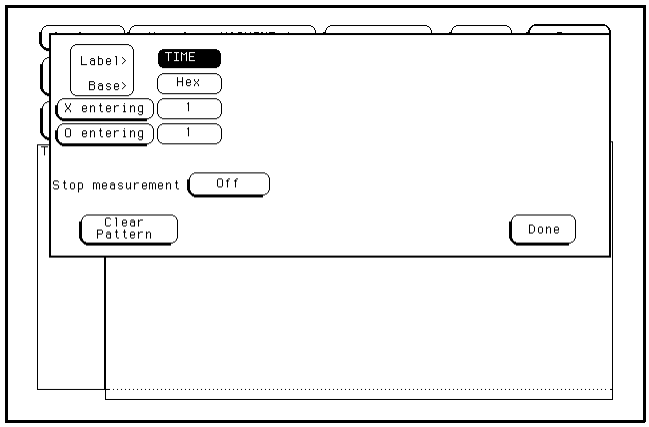
4 Set up the Waveform menu.

a Press the Waveform key.

b Move the cursor to the sec/Div field, then use the RPG knob to dial in 100 ns.

c Select the Markers Off field, then select Pattern.

d Select the Specify Patterns field. Select X entering 1 and O entering 1.

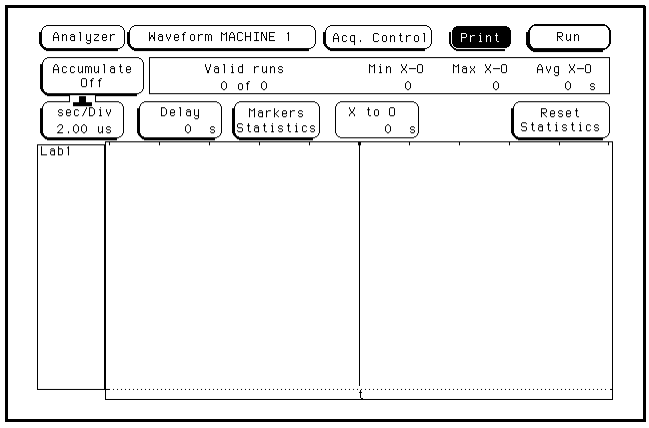


e Select Done to exit the Specify Patterns menu.

f Move the cursor to the X-pat field. Type 1, then press Done.

g Move the cursor to the O-pat field. Type 1901, then press Done.

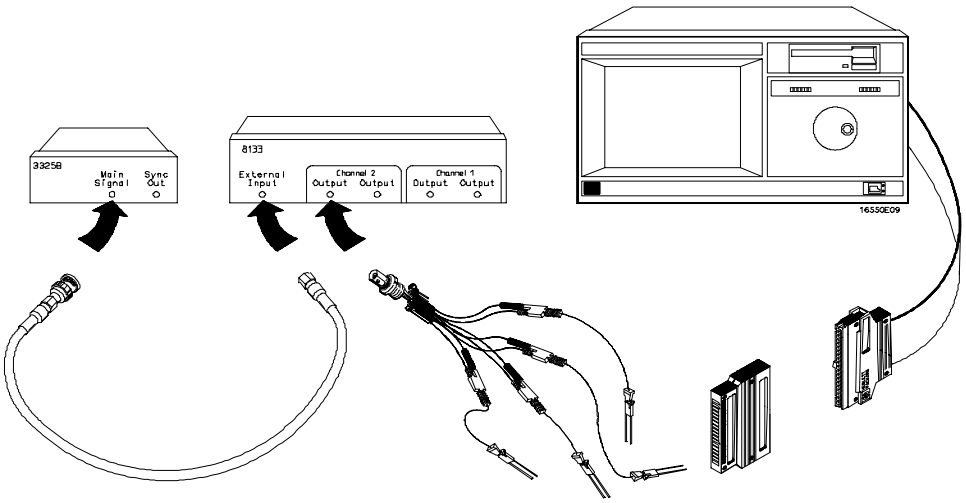
h Select the Markers Patterns field, then select Statistics. Select Reset Statistics to initialize the statistics fields.



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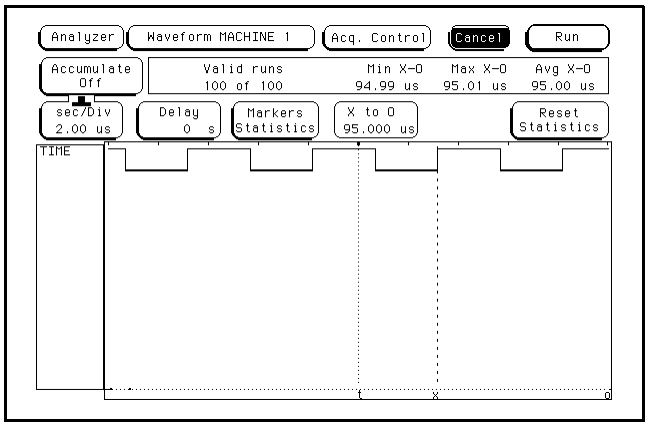
Connect the logic analyzer

1. Using a 6-by-2 test connector, connect channel 0 of Pod 1 to the pulse generator channel 1 output.
2. Using the SMA cable and the BNC adapter, connect the External Input of the pulse generator to the Main Signal of the function generator.



Acquire the data

1. Enable the pulse generator channel 1 output (with the LED off).
2. Press the blue key, then press the Run key to select Run-Repetitive. Allow the logic analyzer to acquire data for at least 100 valid runs as indicated in the pattern statistics field. Observe the X to O time field and ensure the X marker to O marker time is between 47.496 and 47.504 µs during the test.
3. When the logic analyzer has acquired more than 100 valid runs, press Stop. The Min X-O field, Max X-O field, and the Avg X-O field in the logic analyzer Pattern Statistics menu should read 47.50 µs. Record the results in the performance test record.



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To test the CAL OUTPUT ports (oscilloscope)

Testing the CAL OUTPUT ports does not check a specification, but does check the following:

- DC CAL OUTPUT voltage
- AC CAL OUTPUT voltage

This test verifies that the CAL OUTPUT voltages are operating within limits, so that they can provide accurate calibration for the instrument operational accuracy calibration and probe calibration.

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part
Digital Multimeter	0.1 mV resolution, better than 0.005% accuracy	HP 3458A
Cable	BNC (m)(m) 48-inch	HP 10503A
Adapter	BNC (f) to Dual Banana Plug	HP 1251-2277

Set up the equipment

Turn on the equipment required and the logic analyzer. Let them warm up for 30 minutes if you have not already done so.

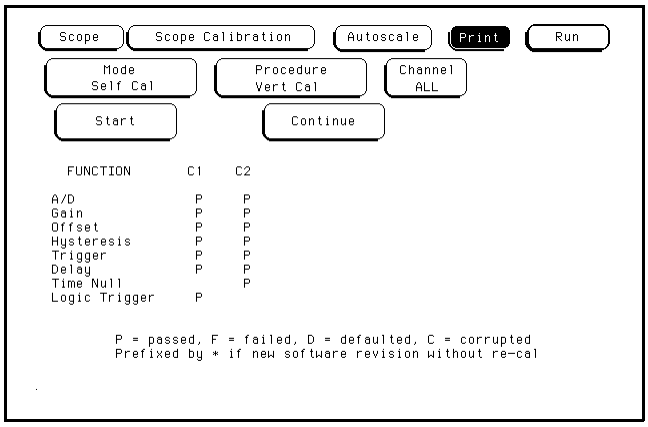
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Set up the logic analyzer

1 Set up the Calibration menu.

a Press the Waveform key.

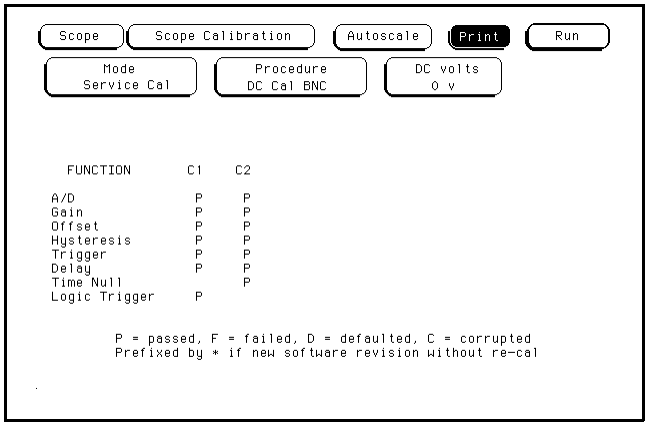
b Press the Waveform key again. At the pop up, select Scope Calibration.



c Select the Mode field, then select Service Cal.

d Select the Procedure field, then select DC Cal BNC.

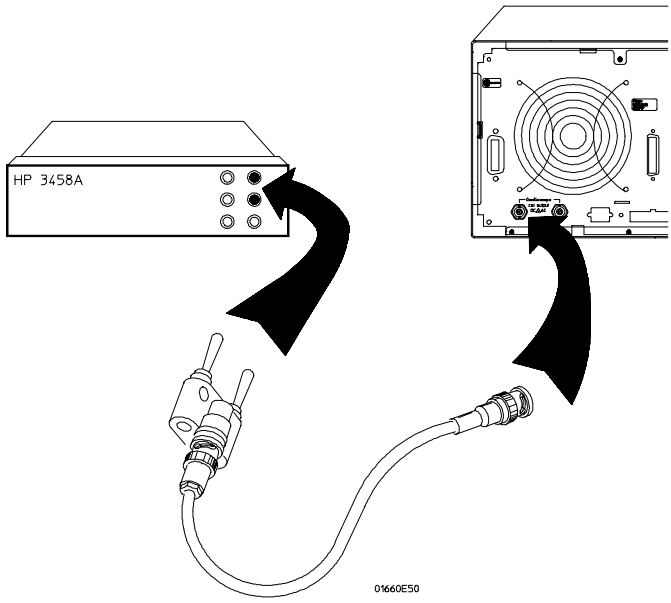
e Select the DC volts field, and set it to O V.



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Verify the DC CAL OUTPUT port

1 Using the BNC-to-banana adapter, connect the BNC cable between the multimeter and the oscilloscope DC CAL OUTPUT connector.



2 The digital voltmeter should read close to 0.0000 V. Record the reading to four decimal places. V_1 = _____.

3 In the Calibration menu set the DC Volts to 5 V.

4 The digital voltmeter should read close to 5.0000 V. Record the reading to four decimal places. V_2 = _____.

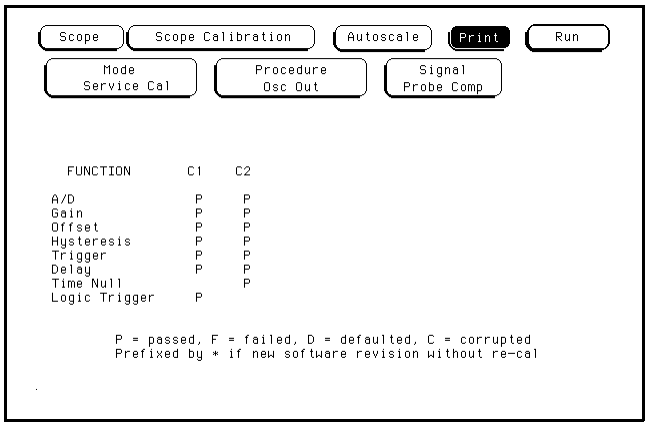
5 In the Calibration menu set the DC Volts to 0 V.

6 Subtract V_1 from V_2. The difference should be between 4.990 and 5.010 V. Record the reading in the performance test record.

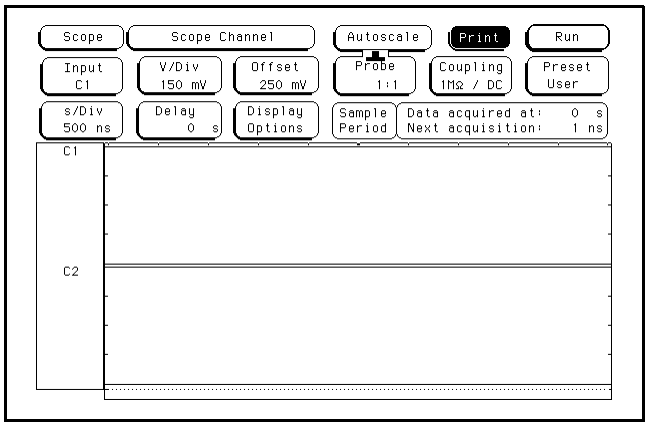
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Set up the logic analyzer

1 Set up the Calibration menu.
   a Select the Procedure field, then select Osc Out.
   b Select the Signal field, then select Probe Comp.



2 Set up the Channel menu.
   a Press the Chan key.
   b Select the Coupling field, then select 1MΩ / DC.
   c Move the cursor to the Probe field, then use the RPG knob to dial in 1:1.



Verify the AC CAL OUTPUT port

1 Using the BNC cable, connect channel 1 of the oscilloscope to the AC CAL OUTPUT connector.
2 In the Calibration menu select Autoscale.
3 Press the Meas key. Verify that the waveform is approximately 0.8 Vp_p at approximately 1.0000 KHz. Record the reading in the performance test record.

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To test the input resistance (oscilloscope)

Testing the input resistance verifies the performance of the following specification:

- Input resistance

This test checks the input resistance at the 50 Ω and 1 MΩ settings in the Coupling field.

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part
Digital Multimeter	Measure resistance (4-wire) better than 0.25% accuracy	HP 3458A
Cables (2)	BNC (m)(m) 48-inch	HP 10503A
Adapter	BNC Tee (m)(f)(f)	HP 1250-0781
Adapters (2)	BNC (f) to Dual Banana Plug	HP 1251-2277

Set up the equipment

1. Turn on the equipment required and the logic analyzer. Let them warm up for 30 minutes if you have not already done so.
2. Set up the multimeter to make a 4-wire resistance measurement.

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Set up the logic analyzer

1 Set up the Channel menu.

a Press the Config key.

b At the pop up menu, select Scope Channel.

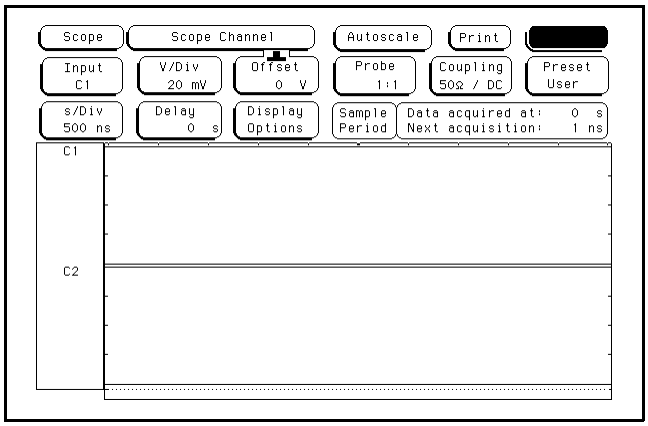
c Select the Input field, then select C1.

d Move the cursor to the Probe field, then use the RPG knob to dial in 1:1.

e Move the cursor to the V/Div field, then use the RPG knob to dial in 20 mV.

f Move the cursor to the Offset field. Set the Offset to 0 V by typing 0, then pressing the Select key.

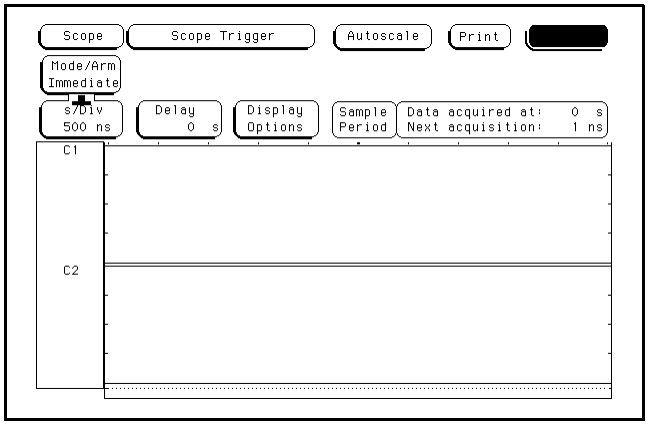
g Select the Coupling field, then select 50Ω / DC.



2 Set up the Trigger menu.

a Press the Trigger key.

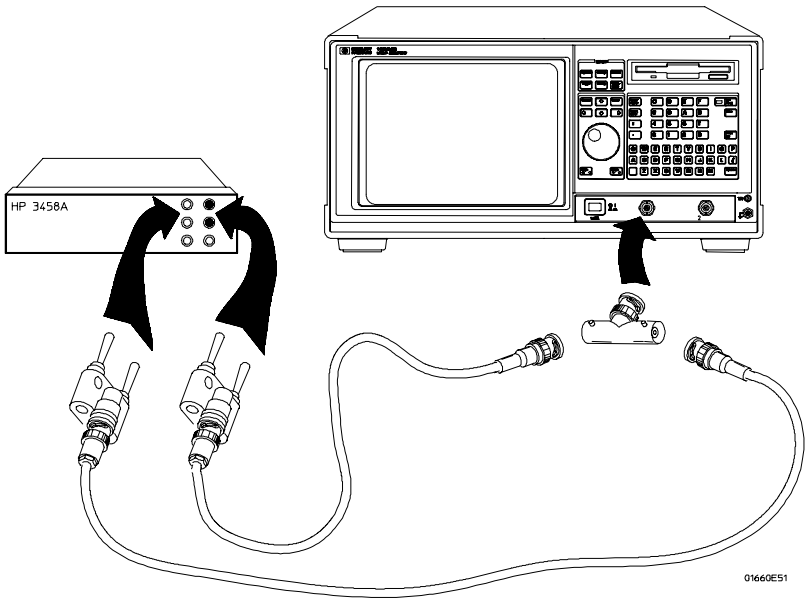
b Select the Mode/Arm field, then select Immediate.



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Connect the logic analyzer

Using the BNC-to-banana adapters, connect one end of each BNC cable to the 4-wire resistance connections on the multimeter, and connect the free ends of the cables to the BNC Tee. Connect the male end of the BNC tee to the channel 1 input of the oscilloscope module.



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Acquire the data

1. Press the RUN key. The clicking of attenuator relays should be audible. Verify resistance readings on the digital multimeter of 50 Ω ± 0.5 Ω (49.5 to 50.5 Ω). Record the reading in the performance test record.
2. In the Channel menu change the Coupling field to 1MΩ / DC. The clicking of attenuator relays should be audible.
3. Press the RUN key. Verify resistance readings on the digital multimeter of 1 MΩ ± 10 kΩ (0.990 to 1.010 MΩ). Record the reading in the performance test record.
4. In the Channel menu change the Coupling field to 50 Ω/DC and V/Div to 200 mV/Div. Repeat steps 1 through 3.
5. In the Channel menu change the Coupling field to 50 Ω /DC and V/Div to 1 V/Div. Repeat steps 1 through 3.
6. In the Channel menu change the Coupling field to 50 Ω /DC and V/Div to 4 V/Div. Repeat steps 1 through 3.
7. Connect the male end of the BNC tee to the channel 2 input of the oscilloscope module.
8. Repeat from "Set up the logic analyzer" for channel 2, replacing channel 1 with channel 2 where applicable.

See Also

If a reading is not within limits, then the attenuator for the out-of-bounds channel should be replaced (see chapter 6).

Perform an operational accuracy calibration

At this point, an operational accuracy calibration should be performed. Follow the procedure "To calibrate the oscilloscope" in chapter 4, "To calibrate the oscilloscope."

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To test the voltage measurement accuracy (oscilloscope)

Testing the voltage measurement accuracy verifies the performance of the following specification:

- Voltage measurement accuracy

This test verifies the DC voltage measurement accuracy of the instrument, using a dual cursor measurement that nullifies offset error.

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part
DC Power Supply	–14 Vdc to +14 Vdc, 0.1 mV resolution	HP 6114A
Digital Multimeter	Better than 0.1% accuracy	HP 3458A
Cable	BNC (m)(m) 48-inch	HP 10503A
Adapter (cable to power supply)	BNC (f) to Dual Banana Plug	HP 1251-2277
Adapter	BNC tee (m)(f)(f)	HP 1250-0781
Blocking Capacitor	BNC (m)(f) 0.18 µF, ±200 V	HP 10240B
BNC Shorting Cap		HP 1250-0074

Set up the equipment

Turn on the equipment required and the logic analyzer. Let them warm up for 30 minutes if you have not already done so.

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Set up the logic analyzer

1 Set up the Channel menu.

a Press the Config key. In the pop up menu, select Scope Channel.

b Select the Input field, then select C1.

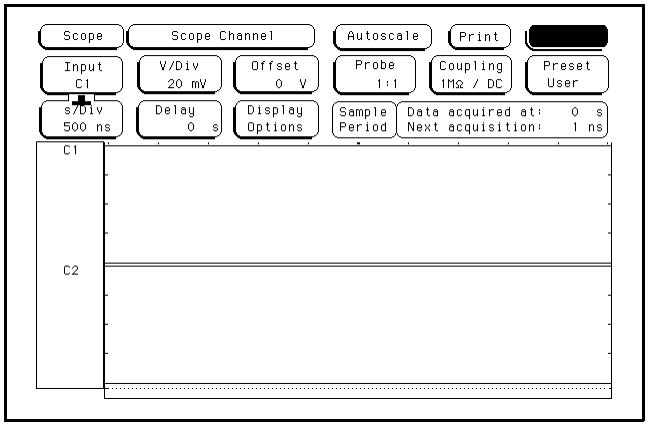
c Move the cursor to the Probe field, then use the RPG knob to dial in 1:1.

d Select the Coupling field, then select 1MΩ / DC.

e Move the cursor to the s/Div field, then use the RPG knob to dial in 500 ns.

CAUTION

Set the Channel Coupling field to 1MΩ / DC or damage to the equipment will result.



2 Set up the Display menu.

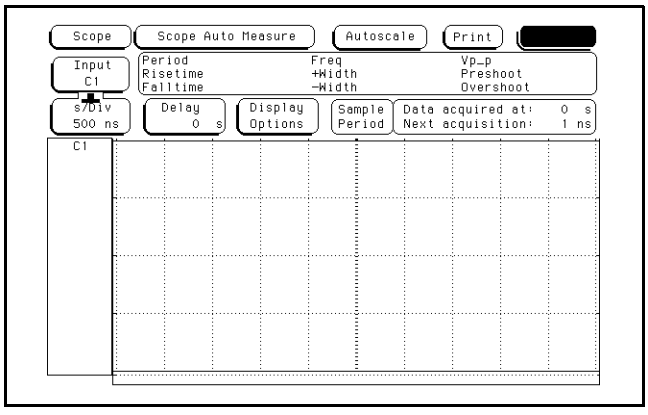
a Press the Display key.

b Select the Mode field, then select Average.

c Move the cursor to the Average # field. Type 8 on the front-panel keyboard, then press Done.

d Select the Grid field and set it to On.

e In the Waveform selection menu, delete channel 2. If channel 1 is not inserted, insert channel 1.



3 Set up the Trigger menu.

a Press the Trigger key.

b Select the Mode/Arm field, then select Immediate.

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4 Set up the Marker menu.

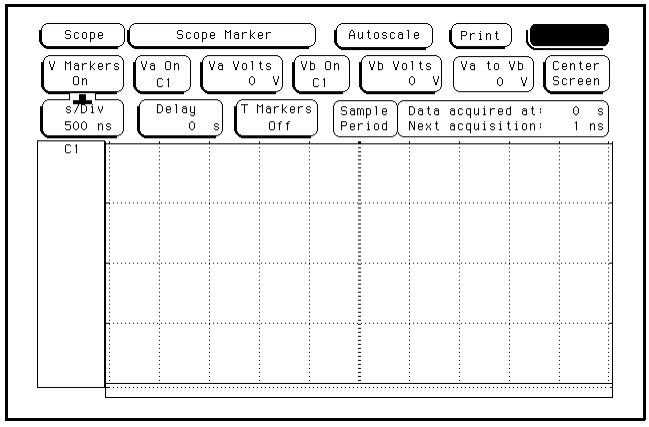
a Press the Marker key.

b Move the cursor to the V Markers field and press Select. The voltage markers should now be On.

c Select Va on C1.

d Select Vb on C1.

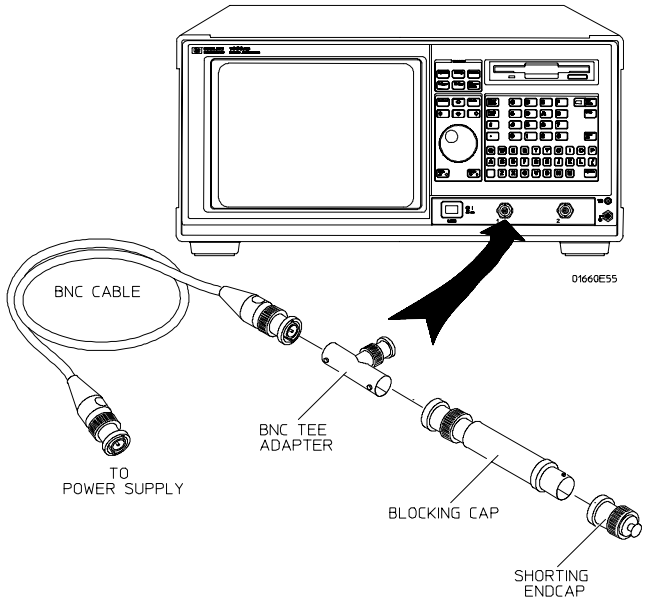
e If the T markers are On, turn the T markers Off by moving the cursor to the T markers field and pressing Select. Select Off.



Connect the logic analyzer

1 Using a BNC-to-banana adapter, connect one end of the cable to the power supply. Connect the BNC tee, the blocking capacitor, and the shorting endcap to the other end of the cable.

2 Monitor the power supply output with the Digital Multimeter.



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Acquire the data

Use the following table for steps 1 through 5.

Oscilloscope Settings		Voltage Readings		
V/Div	**Offset**	**Supply**	**Upper Limit**	**Lower Limit**
4 V/Div	-7.0 V	-14.0 V	-13.7 V	-14.3 V
1 V/Div	-1.75 V	-3.50 V	-3.43 V	-3.57 V
400 mV/Div	-700.0 mV	-1.40 V	-1.37 V	-1.43 V
40 mV/Div	-70.0 mV	-140.0 mV	-137.0 mV	-143.0 mV
40 mV/Div	70.0 mV	140.0 mV	143.0 mV	137.0 mV
400 mV/Div	700.0 mV	1.40 V	1.43 V	1.37 V
1 V/Div	1.75 V	3.50 V	3.57 V	3.43 V
4 V/Div	7.0 V	14.0 V	14.3 V	13.7 V

1. Set up the oscilloscope according to the table above.
   - **a** Press the Chan key.
   - **b** Move the cursor to the V/Div field, then use the RPG knob to dial in the V/Div values shown on the first line of the table.
   - **c** Move the cursor to the Offset field. Use the front-panel keyboard to enter the offset value shown on the first line of the table. Use the left and right cursor-control keys to select either mV or V.
2. Acquire the zero input voltage.
   - **a** Disconnect the power supply from the channel input.
   - **b** Press the blue shift key, then press the Run key. Wait for approximately five seconds (averaging complete), then press Stop.
   - **c** Press the Markers key. Move the cursor to the Va Volts field. Using the RPG knob, move the Va marker over the oscilloscope trace on the display.
3. Acquire the measured voltage.
   - **a** Connect the power supply to the channel input. Set the power supply voltage according to the first line of the table above.
   - **b** Press the blue shift key, then press the Run key. Wait for approximately five seconds (averaging complete), then press Stop.
   - **c** Press the Markers key. Move the cursor to the Vb Volts field. Using the RPG knob, move the Vb marker over the oscilloscope trace on the display.
   - **d** Record the voltage in the Va to Vb field in the performance test record.
4. Repeat steps 1 through 3 for the second line of the table, then for the rest of the lines of the table for channel 1.
5. Repeat from "Set up the logic analyzer" for channel 2, replacing channel 1 with channel 2 where applicable.

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To test the offset accuracy (oscilloscope)

Testing the offset accuracy verifies the performance of the following specification:

- Offset accuracy

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part
DC Power Supply	–35.000 to +35.000 Vdc, ± 1 mV resolution	HP 6114A
Digital Multimeter	Better than 0.1% accuracy	HP 3458A
Cable	BNC (m)(m) 48-inch	HP 10503A
Adapter (cable to power supply)	BNC (f) to Dual Banana Plug	HP 1251-2277
Adapter	BNC tee (m)(f)(f)	HP 1250-0781
Blocking Capacitor	BNC (m)(f) 0.18 µF, ±200 V	HP 10240B
BNC Shorting Cap		HP 1250-0074

Set up the equipment

Turn on the equipment required and the logic analyzer. Let them warm up for 30 minutes if you have not already done so.

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Set up the logic analyzer

1 Set up the Configuration menu.

a Press the Config key. At the pop up menu, select Scope Channel.

b Select the Input field, then select C1.

c Move the cursor to the Probe field, then use the RPG knob to dial in 1:1.

d Move the cursor to the V/Div field, then use the PRG knob to dial in 4.00 V.

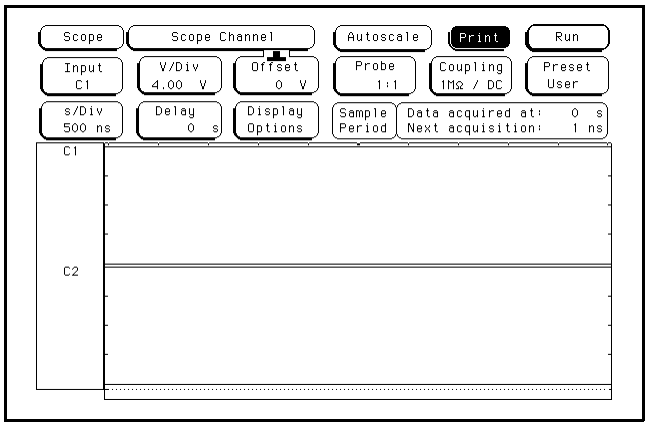
e Move the cursor to the Offset field. Set the offset to 0 by typing 0, then pressing the Select key.

f Select the Coupling field, then select 1MΩ / DC.

CAUTION

Set the Channel Coupling field to 1MΩ / DC or damage to the equipment will result.

g Move the cursor to the s/Div field, then use the RPG knob to dial in 500 ns.



2 Set up the Display menu.

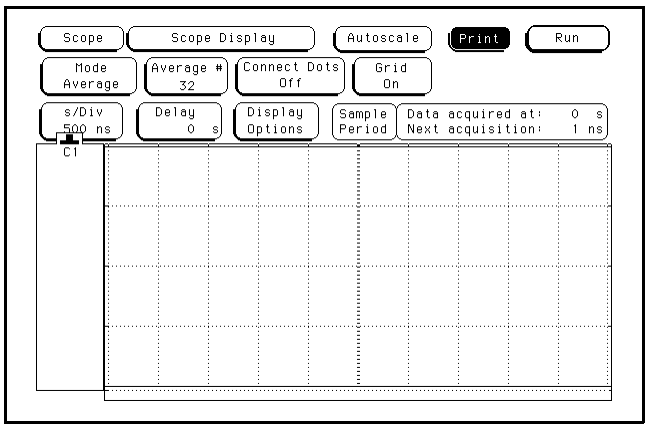
a Press the Display key.

b Select the Mode field, then select Average.

c Move the cursor to the Average # field. Type 32 on the front-panel keyboard, then press Done.

d Select the Grid field and set it to On.

e In the Waveform menu, delete channel 2. If channel 1 is not inserted, insert channel 1.



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3 Set up the Trigger menu.

a Press the Trigger key.

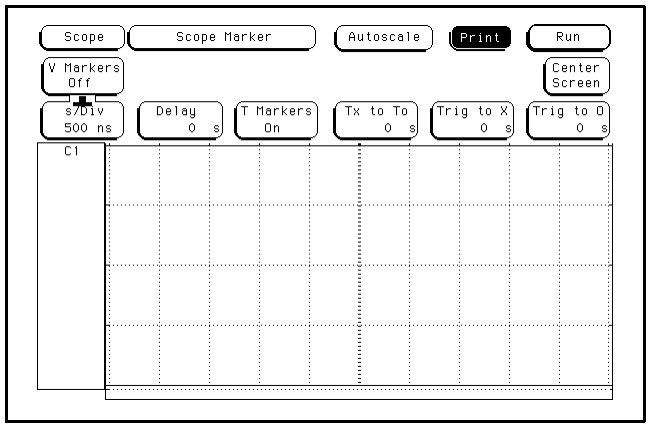
b Select the Mode/Arm field, then select Immediate.

4 Set up the Marker menu.

a Press the Marker key.

b Move the cursor to the T Markers field. Press Select, and then press On.

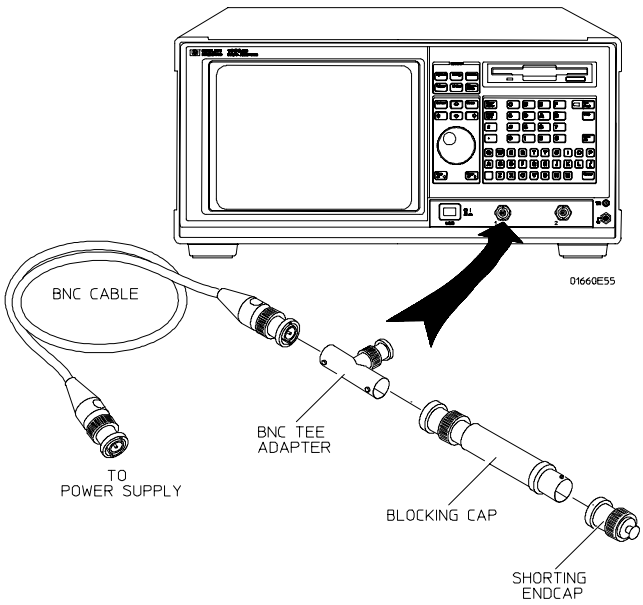
c If the V markers are On, turn the V markers Off by moving the cursor to the V markers field and pressing Select.



Connect the logic analyzer

1 Using a BNC-to-banana adapter, connect one end of the cable to the power supply. Connect the BNC tee, the blocking capacitor, and the shorting endcap to the other end of the cable.

2 Monitor the power supply output with the Digital Multimeter.



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Acquire the zero input data

1. Disconnect the power supply from the channel input.
2. Press the Chan key. Move the cursor to the V/Div field and press the Select key.
3. Press the blue shift key, then press the Run key. After approximately 15 seconds (averaging complete), press the Stop key. Read the voltage from the Markers voltage field (0.00 V ± 320 mV) and enter the value in the performance test record.
4. Use the RPG knob to dial in 1 V/Div. Press the blue shift key, then press the Run key. After approximately 15 seconds (averaging complete), press the Stop key. Read the voltage from the Markers voltage field (0.00 V ± 80 mV) and enter the value in the performance test record.
5. Use the RPG knob to dial in 100 mV/Div. Press the blue shift key, then press the Run key. After approximately 15 seconds (averaging complete), press the Stop key. Read the voltage from the Markers voltage field (0.00 V ± 8 mV) and enter the value in the performance test record.
6. Use the RPG knob to dial in 10 mV/Div. Press the blue shift key, then press the Run key. After approximately 15 seconds (averaging complete), press the Stop key. Read the voltage from the Markers voltage field (0.00 V ± 800 µV) and enter the value in the performance test record.

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Acquire the DC input data

Use the following table for steps 1 through 5.

Multimeter Settings

Scope Settings		Power Supply Settings	Scope Readings	
V/Div	**Offset**	**Supply**	**Minimum**	**Maximum**
1 V/Div	–35.00 V	–35.00 V	–35.4 V	–34.6 V
200 mV/Div	–10.00 V	–10.00 V	–10.1 V	–9.90 V
20 mV/Div	–2.00 V	–2.00 V	–2.02 V	–1.98 V
20 mV/Div	+2.00 V	+2.00 V	+1.98 V	+2.02 V
200 mV/Div	+10.00 V	+10.00 V	+9.90 V	+10.1 V
1 V/Div	+35.00 V	+35.00 V	+34.6 V	+35.4 V

1. Connect the power supply to the oscilloscope channel 1 input. Set the power supply according to the first line of the table above.
2. Set up the oscilloscope according to the table above.
   a. Move the cursor to the V/Div field, then use the RPG knob to dial in the V/Div value shown on the first line of the table.
   b. Move the cursor to the Offset field. Use the front-panel keyboard to type in the offset value shown in the first line of the table. Use the left and right cursor-control keys to select either mV or V. Press the Select key.
3. Acquire the measured voltage.
   a. Press the blue shift key, then press the Run key. After approximately 15 seconds (averaging complete), press the Stop key.
   b. Read the voltage from the Markers voltage field. The value should be between the minimum and maximum values listed in the table. Record the value in the performance test record.
4. Repeat steps 1 through 3 for the second line of the table, then for the rest of the lines of the table for channel 1.
5. Repeat from "Set up the logic analyzer" for channel 2, replacing channel 1 with channel 2 where applicable.

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To test the bandwidth (oscilloscope)

Testing the bandwidth verifies the performance of the following specification:

- Bandwidth

This test verifies the bandwidth (dc coupled) of the instrument from dc to 250 MHz.

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part
Signal Generator	1 - 250 MHz at approximately 170 mV rms	HP 8656B
Power Meter/Sensor	1 - 250 MHz ± 3% accuracy	HP 436/8482A
Power Splitter	Outputs differ by <0.15 dB	HP 11667B
Cable	Type N (m)(m) 24-inch	HP 11500B
Adapter	Type N (m) to BNC (f)	HP 1250-0780

Set up the equipment

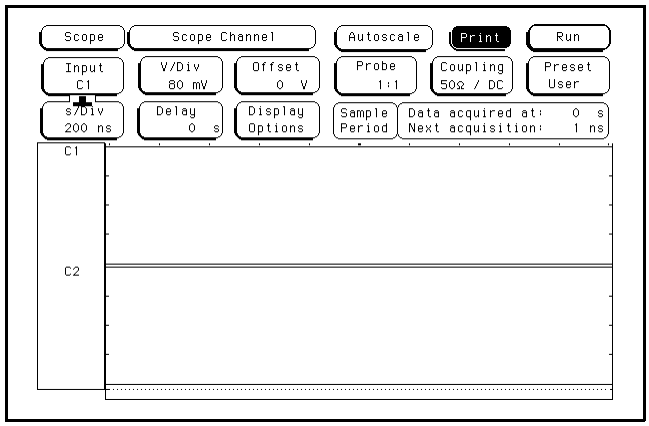
Turn on the equipment required and the logic analyzer. Let them warm up for 30 minutes if you have not already done so.

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Set up the logic analyzer

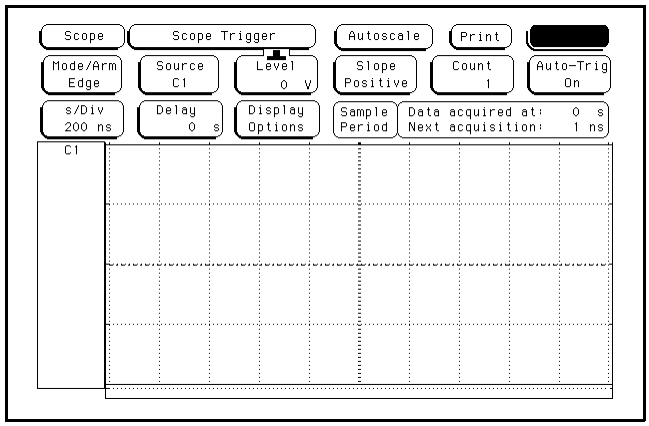
1 Set up the Configuration menu.

- **a** Press the Config key. At the pop up menu, select Scope Channel.
- **b** Select the Input field, then select C1.
- **c** Move the cursor to the Probe field, then use the RPG knob to dial in 1:1.
- **d** Move the cursor to the V/Div field. Type 80 on the front-panel keyboard, then use the left and right control keys to select mV. Press the Select key.
- **e** Move the cursor to the Offset field. Set the offset to 0 by typing 0, then pressing the Select key.
- **f** Select the Coupling field, then select 50Ω / DC.
- **g** Move the cursor to the s/Div field, then use the RPG knob to dial in 200 ns.



2 Set up the Display menu.

- **a** Press the Display key.
- **b** Select the Mode/Arm field, then select Average.
- **c** Move the cursor to the Average # field. Type 32 on the front-panel keyboard, then press Done.
- **d** Select the Grid field and set it to On.
- **e** In the Waveform selection menu, delete channel 2. If channel 1 is not inserted, insert channel 1.



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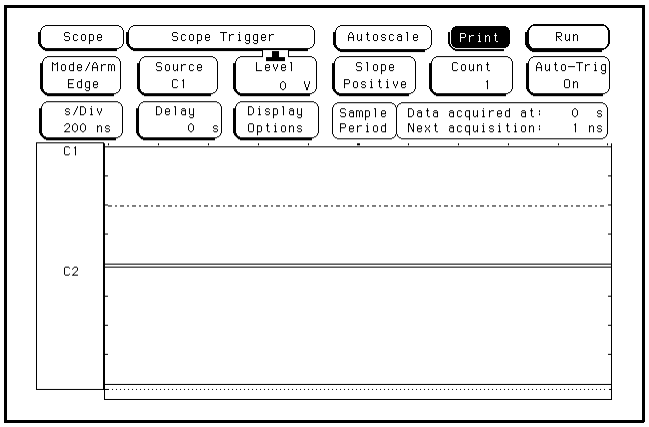
3 Set up the Trigger menu.

a Press the Trigger key.

b Select the Mode/Arm field, then select Edge.

c Select the Source field, then select C1.

d Move the cursor to the Level field. Set the trigger level to 0 by typing 0 in the front-panel keyboard, then pressing Select.

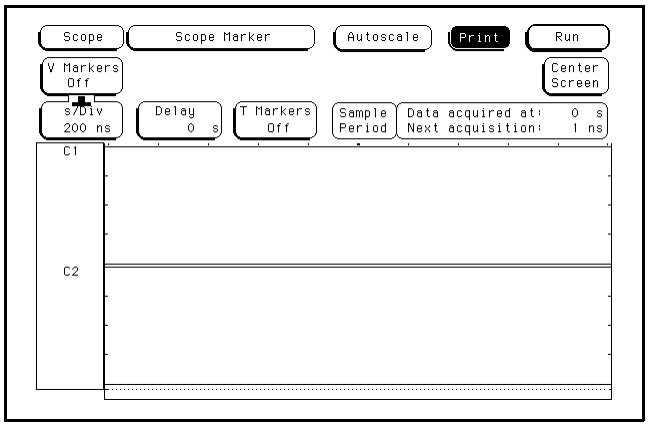


4 Turn off the voltage and time markers.

a Press the Marker key.

b Move the cursor to the V Markers field and press Select. The Select key should toggle the marker to Off.

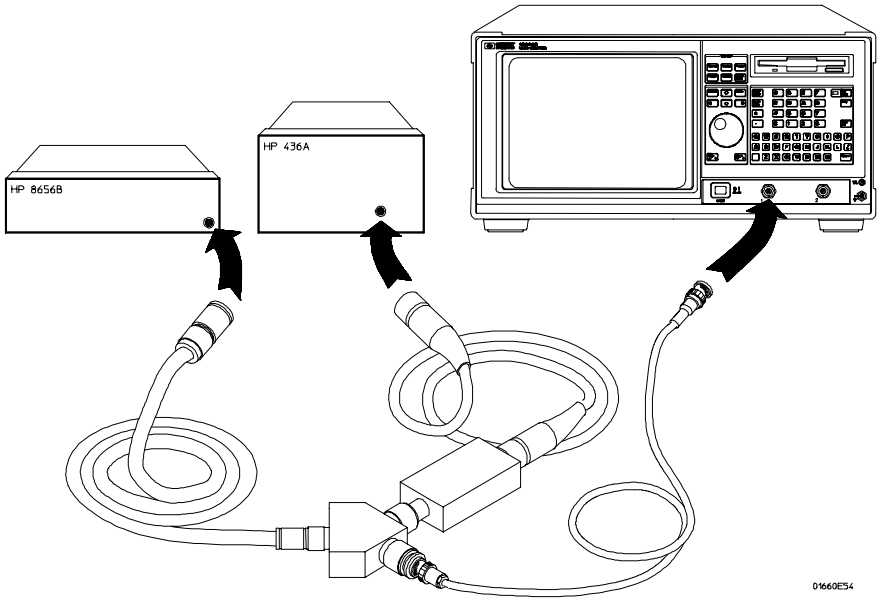
c Move the cursor to the T Markers field and press Select. At the pop up menu, select Off.



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Connect the logic analyzer

1. Using the N cable, connect the signal generator to the power splitter input. Connect the power sensor to one output of the power splitter.
2. Using the N-to-BNC adapter and the BNC cable, connect the other power splitter output to the channel 1 input of the oscilloscope.



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Acquire the data

1. Obtain the 1 MHz response.
   - **a** Set the signal generator for 1 MHz at –2.4 dBm.
   - **b** Press the blue shift key, then press the Run key. The signal on the screen should be two cycles at three divisions amplitude. After approximately 15 seconds (averaging complete), press the Stop key.
   - **c** Press the Meas key. Note the voltage reading in the $V_{p\text{-}p}$ field.
     $V_{1\ MHz}$ = _____ mV.
2. Set the signal generator for 250 MHz frequency.
   - **a** Set the power meter Cal Factor % to the 1 MHz value from the calibration chart on the power splitter. Press dB[REF] to set a 0 dB reference.
   - **b** Change the signal generator frequency to 250 MHz. Set the power meter Cal Factor % to the 250 MHz value from the chart.
   - **c** Adjust the signal generator amplitude for a power reading as close as possible to 0.0 dB[REL] and note the power reading. Reading = _____ dB.
3. Obtain the 250 MHz response.
   - **a** Use the RPG knob to dial in a s/Div value of 2 ns/Div.
   - **b** Press the blue shift key, then press the Run key. After approximately 15 seconds (averaging complete), press the Stop key.
   - **c** Note the voltage reading in the $V_{p\text{-}p}$ field V_{250MHz} = _____mV.
4. Determine the oscilloscope response.
   - **a** Calculate the response using the formula:

     $$response\ (dB) = 20\log_{10}\frac{V_{250Mhz}}{V_{1MHz}} = 20\log_{10}(_____) = _____dB$$

   - **b** Correct the result from step 4a above with any differences in the power meter from step 2c. Observe signs. For example:

     Result from step 4a = –2.3 dB
     Power meter reading = –0.2 dB[REL]
     then true response = (–2.3) – (–0.2) = –2.1dB

     (_____) – (_____) = _____ dB
   - **c** The result from step 4b should be ≤ –3.0 dB. Record the result in the performance test record.
5. Remove the power splitter from the oscilloscope channel 1 input and connect it to the channel 2 input.
6. Repeat from "Set up the logic analyzer" for channel 2, replacing channel 1 with channel 2 where applicable.

See Also

Failure of the bandwidth test can be caused by a faulty attenuator or main assembly (see chapter 6).

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To test the time measurement accuracy (oscilloscope)

Testing the time measurement accuracy verifies the performance of the following specification:

- Time Measurement accuracy

This test uses a precise frequency source to check the accuracy of time measurement functions.

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part
Signal Generator	200 MHz, timebase accuracy 0.25 ppm	HP 8656B Opt. 001
Cable	BNC (m)(m) 48-inch	HP 10503A
Adapter	Type N (m) to BNC (f)	HP 1250-0780

Set up the equipment

1. Turn on the equipment required and the logic analyzer. Let them warm up for 30 minutes if you have not already done so.
2. Set the signal generator to 181.81818 MHz (5.5 ns period) and approximately 600 mV rms.

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Set up the logic analyzer

1 Set up the Configuration menu.

a Press the Config key. At the pop up menu, select Scope Channel.

b Select the Input field, then select C1.

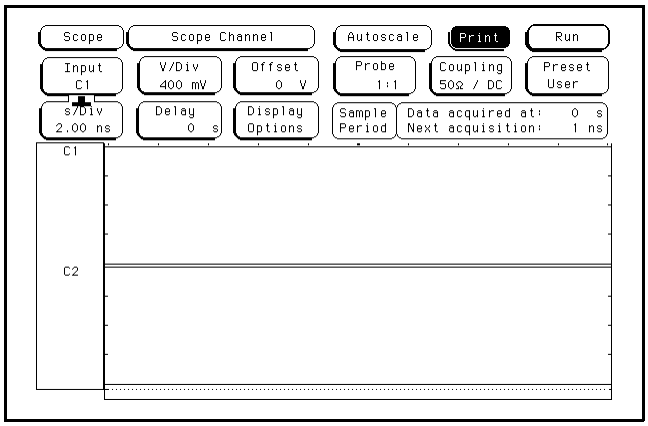
c Move the cursor to the Probe field, then use the RPG knob to dial in 1:1.

d Move the cursor to the V/Div field, then use the PRG knob to dial in 400 mV.

e Move the cursor to the Offset field. Set the offset to 0 by typing 0, then pressing the Select key.

f Select the Coupling field, then select 50Ω / DC.

g Move the cursor to the s/Div field, then use the RPG knob to dial in 2.00 ns.



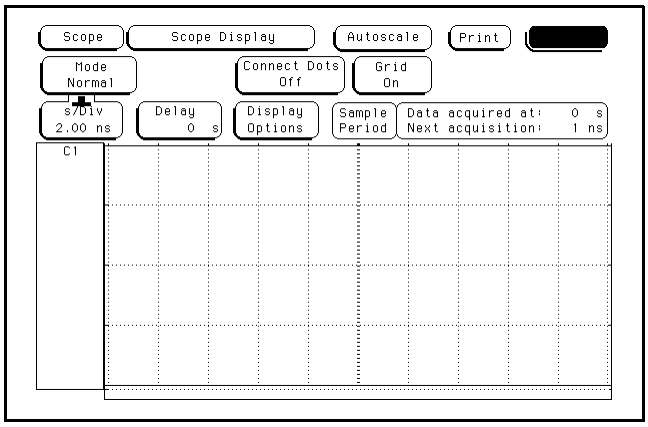
2 Set up the Display menu.

a Press the Display key.

b Select the Mode/Arm field, then select Normal.

c Select the Grid field and set it to On.

d In the Waveform selection menu, delete channel 2. If channel 1 is not inserted, insert channel 1.



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3 Set up the Trigger menu.

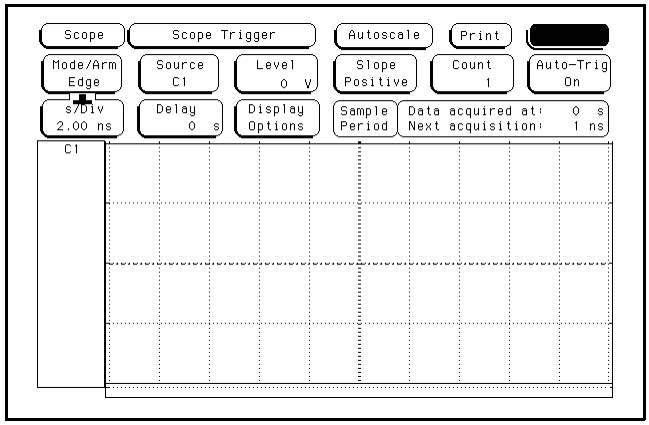
a Press the Trigger key.

b Select the Mode/Arm field, then select Edge.

c Select the Source field and set it to C1.

d Move the cursor to the Level field. Set the trigger level to 0 by typing 0 in the front-panel keyboard, then pressing Select.

e Select the Slope field and set it to Positive.



4 Set up the Markers menu.

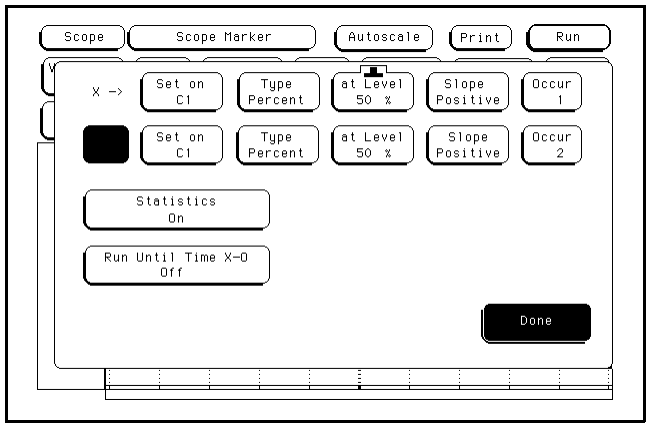
a Press the Marker key.

b Move the cursor to the T Markers field and press Select. At the pop up menu, select Auto.

c Select the X marker, and set it on C1 at Level 50%, Slope Positive, Occur 1 (use the RPG knob for Occur).

d Select the O marker, and set it on C1 at Level 50%, Slope Positive, Occur 2 (use the RPG knob for Occur).

e Select the Statistics field and set it to On.

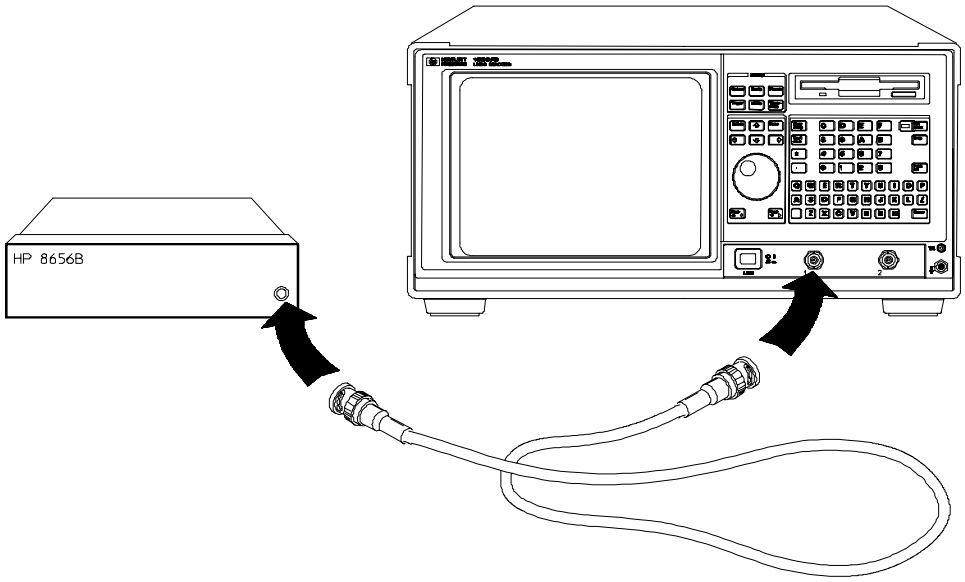


f Select Done.

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Connect the logic analyzer

Using the N-to-BNC adapter and the BNC cable, connect the signal generator output to the channel 1 input of the oscilloscope.



Acquire the data

1 Determine short time period accuracy.

- **a** Press the blue shift key, then press Run. If the waveform is clipping, reduce the signal generator output voltage level until the waveform no longer clips. After approximately two minutes, press the Stop key.
- **b** In the Statistics field, check to see that the Mean X - O field is approximately 5.500 ns. Check that both the Min X - O and the Max X - O are within 150 ps of the Mean X - O. Record the results in the performance test record.

2 Determine longer time period accuracy.

- **a** Press Select twice to call up the T Markers Auto menu.
- **b** Select the X marker Set On field. At the pop up menu, select Manual.
- **c** Move the cursor to the O marker Occur field. Press the 1 key, then press Select.
- **d** Press Done.
- **e** Press the Display key. Select the Mode field, then select Average. Move the cursor to the Average # field. Type 8 on the front-panel keyboard, then press Done.
- **f** Move the cursor to the Delay field. Type 99 on the front-panel keyboard, and use the left and right cursor-control keys to select "ns." Press done.
- **g** Press the Marker key. Press the blue shift key, then press the Run key. After approximately two minutes, press the Stop key.
- **h** In the Statistics field, check to see that the Mean X - O field is approximately 99 ns. Check that both the Min X - O and the Max X - O are within 150 ps of the Mean X - O. Record the results in the performance test record.

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To test the trigger sensitivity (oscilloscope)

Testing the trigger sensitivity verifies the performance of the following specifications:

- DC to 50 MHz: 0.063 x full scale (0.25 division)
- 50 MHz to 250 MHz: 0.125 x full scale (0.5 division)

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part
Signal Generator	50 MHz and 225 MHz, 30 - 80 mV RMS output	HP 8656B Opt. 001
Cable	BNC 48-inch	HP 10503B
Adapter	Type N (m) to BNC (f)	HP 1250-0780

Set up the equipment

Turn on the equipment required and the logic analyzer. Let them warm up for 30 minutes if you have not already done so.

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Set up the logic analyzer

1 Set up the Configuration menu.

a Press the Config key. At the pop up menu, select Scope Channel.

b Select the Input field, then select C1.

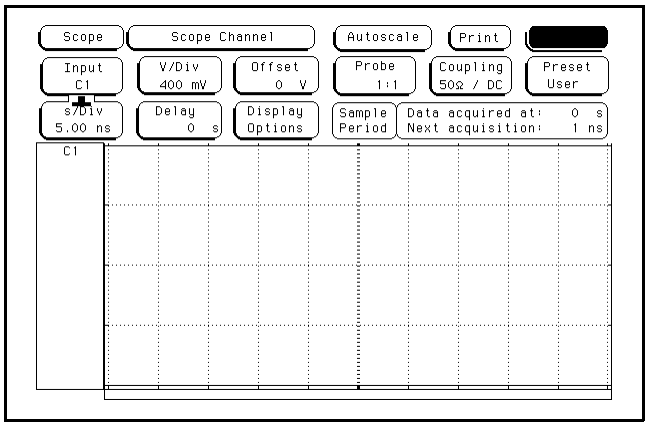
c Move the cursor to the Probe field, then use the RPG knob to dial in 1:1.

d Move the cursor to the V/Div field, then use the PRG knob to dial in 400 mV.

e Move the cursor to the Offset field. Set the offset to 0 by typing 0, then pressing the Select key.

f Move the cursor to the Coupling field, then press Select. Select 50Ω / DC.

g Move the cursor to the s/Div field, then use the RPG knob to dial in 5.00 ns.



2 Set up the Display menu.

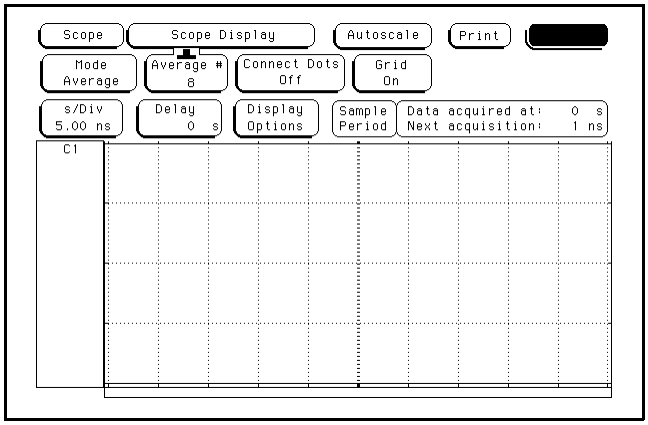
a Press the Display key.

b Select the Mode/Arm field, then select Average.

c Move the cursor to the Average # field. Enter "8" in the front-panel keyboard, then press Done.

d Select the Grid field and set it to On.

e In the Waveform selection menu, delete channel 2. If channel 1 is not inserted, insert channel 1.



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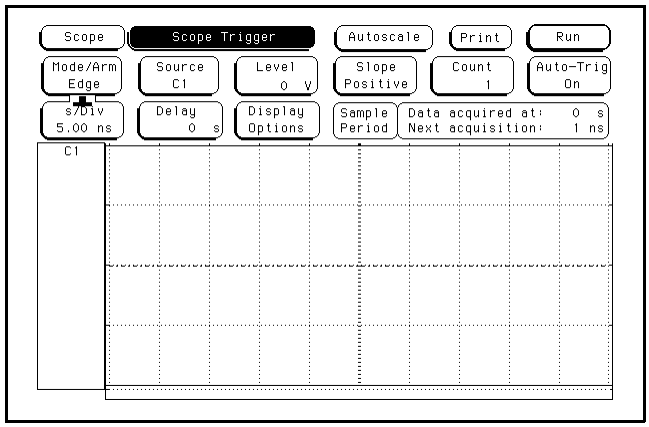
3 Set up the Trigger menu.

a Press the Trigger key.

b Select the Mode/Arm field, then select Edge.

c Select the Source field and set it to C1.

d Move the cursor to the Level field. Set the trigger level to 0 by typing 0 in the front-panel keyboard, then pressing Select.

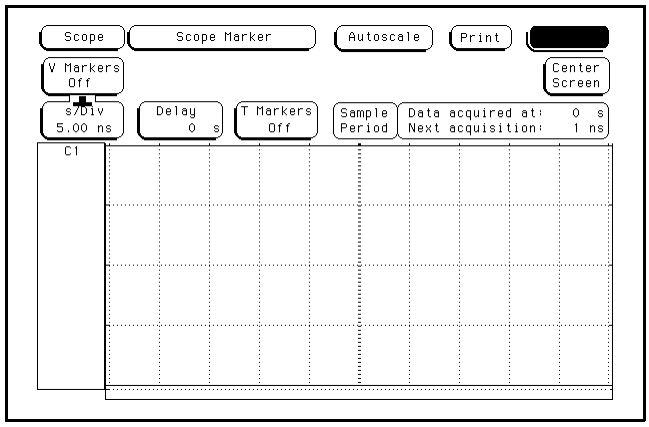


4 Turn off the voltage and time markers.

a Press the Marker key.

b Move the cursor to the V Markers field and press Select. The Select key should toggle the marker to Off.

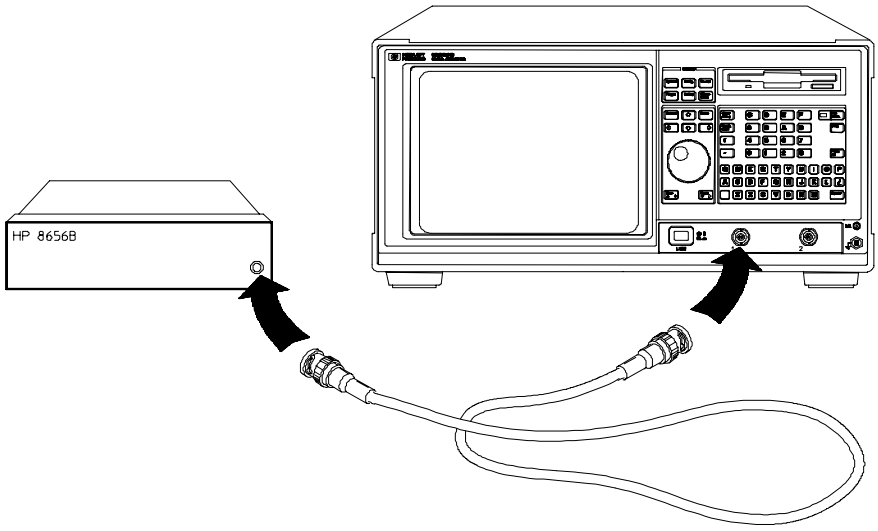
c Move the cursor to the T Markers field and press Select. At the pop up menu, select Off.



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Connect the logic analyzer

Using the N-to-BNC adapter and the BNC cable, connect the signal generator output to the channel 1 input of the oscilloscope.



Acquire the data

1. Test the upper bandwidth trigger sensitivity.
   - **a** Set the signal generator to provide a 225 MHz signal with 70 mV rms amplitude.
   - **b** Press the blue shift key, then press the Run key. Press the Trigger key.
   - **c** If the Auto triggered message appears (oscilloscope doesn't trigger), move the cursor to the Level field and use the RPG knob to adjust the trigger level until the oscilloscope triggers (Auto triggered message goes away).
   - **d** If the oscilloscope triggers, record a pass in the performance test record.
   - **e** Press Stop to halt the acquisition. Read the Vp-p field and record the voltage in the performance test record.
2. Test the lower bandwidth trigger sensitivity.
   - **a** Use the RPG knob to dial in s/Div of 20 ns.
   - **b** Set the signal generator to provide a 50 MHz signal with 35 mV rms amplitude.
   - **c** Press the blue shift key, then press the Run key.
   - **d** If the oscilloscope doesn't trigger, move the cursor to the Level field and use the RPG knob to adjust the trigger level until the oscilloscope triggers (Auto triggered message goes away).
   - **e** If the oscilloscope triggers, record a pass in the performance test record.
   - **f** Press Stop to halt the acquisition.
3. Remove the signal generator output from channel 1 and connect the BNC cable to channel 2. Repeat from "Set up the logic analyzer" for channel 2, replacing channel 1 with channel 2 where appropriate.

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Performance Test Record (logic analyzer)

HEWLETT PACKARD

HP 1660C/CS/CP-Series Logic Analyzer_____

Serial No._____ Work Order No._____

Recommended Test Interval - 2 Year/4000 hours Date_____

Recommended next testing_____ Temperature_____

Test	Settings		Results	
Self-Tests			Pass/Fail	_____
Threshold Accuracy	± (100 mV + 3% of threshold setting)			
			Limits	Measured
Pod 1	TTL, ±145 mV	TTL VL	+1.355 V	_____
		TTL VH	+1.645 V	_____
	ECL, ±139 mV	ECL VL	-1.439 V	_____
		ECL VH	-1.161 V	_____
	-User, ±280 mV	-User VL	-6.280 V	_____
		- User VH	-5.720 V	_____
	+User, ±280 mV	+ User VL	+5.720 V	_____
		+ User VH	+6.280 V	_____
	0 V, ±100 mV	0 V User VL	-100 mV	_____
		0 V User VH	+100 mV	_____
Pod 2	TTL, ±145 mV	TTL VL	+1.355 V	_____
		TTL VH	+1.645 V	_____
	ECL, ±139 mV	ECL VL	-1.439 V	_____
		ECL VH	-1.161 V	_____
	-User, ±280 mV	-User VL	-6.280 V	_____
		- User VH	-5.720 V	_____
	+User, ±280 mV	+ User VL	+5.720 V	_____
		+ User VH	+6.280 V	_____
	0 V, ±100 mV	0 V User VL	-100 mV	_____
		0 V User VH	+100 mV	_____
Pod 3	TTL, ±145 mV	TTL VL	+1.355 V	_____
		TTL VH	+1.645 V	_____
	ECL, ±139 mV	ECL VL	-1.439 V	_____
		ECL VH	-1.161 V	_____
	-User, ±280 mV	-User VL	-6.280 V	_____
		- User VH	-5.720 V	_____
	+User, ±280 mV	+ User VL	+5.720 V	_____
		+ User VH	+6.280 V	_____
	0 V, ±100 mV	0 V User VL	-100 mV	_____
		0 V User VH	+100 mV	_____

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Performance Test Record (continued)

Test	Settings		Results	
Threshold Accuracy (cont)			Limits	Measured
Pod 4	TTL, ±145 mV	TTL VL	+1.355 V	_____
		TTL VH	+1.645 V	_____
	ECL, ±139 mV	ECL VL	-1.439 V	_____
		ECL VH	-1.161 V	_____
	-User, ±280 mV	-User VL	-6.280 V	_____
		- User VH	-5.720 V	_____
	+User, ±280 mV	+ User VL	+5.720 V	_____
		+ User VH	+6.280 V	_____
	0 V, ±100 mV	0 V User VL	-100 mV	_____
		0 V User VH	+100 mV	_____
Pod 5	TTL, ±145 mV	TTL VL	+1.355 V	_____
		TTL VH	+1.645 V	_____
	ECL, ±139 mV	ECL VL	-1.439 V	_____
		ECL VH	-1.161 V	_____
	-User, ±280 mV	-User VL	-6.280 V	_____
		- User VH	-5.720 V	_____
	+User, ±280 mV	+ User VL	+5.720 V	_____
		+ User VH	+6.280 V	_____
	0 V, ±100 mV	0 V User VL	-100 mV	_____
		0 V User VH	+100 mV	_____
Pod 6	TTL, ±145 mV	TTL VL	+1.355 V	_____
		TTL VH	+1.645 V	_____
	ECL, ±139 mV	ECL VL	-1.439 V	_____
		ECL VH	-1.161 V	_____
	-User, ±280 mV	-User VL	-6.280 V	_____
		- User VH	-5.720 V	_____
	+User, ±280 mV	+ User VL	+5.720 V	_____
		+ User VH	+6.280 V	_____
	0 V, ±100 mV	0 V User VL	-100 mV	_____
		0 V User VH	+100 mV	_____
Pod 7	TTL, ±145 mV	TTL VL	+1.355 V	_____
		TTL VH	+1.645 V	_____
	ECL, ±139 mV	ECL VL	-1.439 V	_____
		ECL VH	-1.161 V	_____
	-User, ±280 mV	-User VL	-6.280 V	_____
		- User VH	-5.720 V	_____
	+User, ±280 mV	+ User VL	+5.720 V	_____
		+ User VH	+6.280 V	_____
	0 V, ±100 mV	0 V User VL	-100 mV	_____
		0 V User VH	+100 mV	_____
Pod 8	TTL, ±145 mV	TTL VL	+1.355 V	_____
		TTL VH	+1.645 V	_____
	ECL, ±139 mV	ECL VL	-1.439 V	_____
		ECL VH	-1.161 V	_____
	-User, ±280 mV	-User VL	-6.280 V	_____
		- User VH	-5.720 V	_____
	+User, ±280 mV	+ User VL	+5.720 V	_____
		+ User VH	+6.280 V	_____
	0 V, ±100 mV	0 V User VL	-100 mV	_____
		0 V User VH	+100 mV	_____

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Performance Test Record (continued)

Test	Settings	Results
Glitch Capture	Minimum Detectable Glitch 3.5 ns	Pass/Fail
	Pod 1	_____
	Pod 2	_____
	Pod 3	_____
	Pod 4	_____
	Pod 5	_____
	Pod 6	_____
	Pod 7	_____
	Pod 8	_____

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Performance Test Record (continued)

Test	Settings		Results			
Single-Clock, Single-Edge Acquisition				Pass/Fail		Pass/Fail
All Pods, Channel 3	Setup/Hold Time	3.5/0.0 ns	J↑ K↑ L↑ M↑ N↑ P↑	_____ _____ _____ _____ _____ _____	J↓ K↓ L↓ M↓ N↓ P↓	_____ _____ _____ _____ _____ _____
	Setup/Hold Time	0.0/3.5 ns	J↑ K↑ L↑ M↑ N↑ P↑	_____ _____ _____ _____ _____ _____	J↓ K↓ L↓ M↓ N↓ P↓	_____ _____ _____ _____ _____ _____
	Setup/Hold Time	1.5/2.0 ns	J↑ K↑ L↑ M↑ N↑ P↑	_____ _____ _____ _____ _____ _____	J↓ K↓ L↓ M↓ N↓ P↓	_____ _____ _____ _____ _____ _____
All Pods, Channel 11	Setup/Hold Time	3.5/0.0 ns	J↑ K↑ L↑ M↑ N↑ P↑	_____ _____ _____ _____ _____ _____	J↓ K↓ L↓ M↓ N↓ P↓	_____ _____ _____ _____ _____ _____
	Setup/Hold Time	0.0/3.5 ns	J↑ K↑ L↑ M↑ N↑ P↑	_____ _____ _____ _____ _____ _____	J↓ K↓ L↓ M↓ N↓ P↓	_____ _____ _____ _____ _____ _____
	Setup/Hold Time	1.5/2.0 ns	J↑ K↑ L↑ M↑ N↑ P↑	_____ _____ _____ _____ _____ _____	J↓ K↓ L↓ M↓ N↓ P↓	_____ _____ _____ _____ _____ _____

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Performance Test Record (continued)

Test	Settings		Results			
Multiple-Clock, Multiple-Edge Acquisition			Enable pulse generator, channel 2 COMP (LED on)		Disable pulse generator, channel 2 COMP (LED off)	
				Pass/Fail		Pass/Fail
All Pods, Channel 3	Setup/Hold Time	4.5/0.0 ns	J↑ + M↑ + N↑ K↑ + L↑ + P↑	_____ _____	J↓ + M↓ + N↓ K↓ + L↓ + P↓	_____ _____
	Setup/Hold Time	0.0/4.5 ns	J↑ + M↑ + N↑ K↑ + L↑ + P↑	_____ _____	J↓ + M↓ + N↓ K↓ + L↓ + P↓	_____ _____
	Setup/Hold Time	2.0/2.5 ns	J↑ + M↑ + N↑ K↑ + L↑ + P↑	_____ _____	J↓ + M↓ + N↓ K↓ + L↓ +P↓	_____ _____
All Pods, Channel 11	Setup/Hold Time	4.5/0.0 ns	J↑ + M↑ + N↑ K↑ + L↑ + P↑	_____ _____	J↓ + M↓ + N↓ K↓ + L↓ +P↓	_____ _____
	Setup/Hold Time	0.0/4.5 ns	J↑ + M↑ + N↑ K↑ + L↑ + P↑	_____ _____	J↓ + M↓ + N↓ K↓ + L↓ + P↓	_____ _____
	Setup/Hold Time	2.0/2.5 ns	J↑ + M↑ + N↑ K↑ + L↑ + P↑	_____ _____	J↓ + M↓ + N↓ K↓ + L↓ +P↓	_____ _____

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Performance Test Record (continued)

Test	Settings		Results
Single-Clock, Multiple-Edge Acquisition			Disable pulse generator, channel 1 COMP (LED off) Pass/Fail
All Pods, Channel 3	Setup/Hold Time	4.0/0.0 ns	J↕ _____ K↕ _____ L↕ _____ M↕ _____ N↕ _____ P↕ _____
	Setup/Hold Time	0.0/4.0 ns	J↕ _____ K↕ _____ L↕ _____ M↕ _____ N↕ _____ P↕ _____
	Setup/Hold Time	2.0/2.0 ns	J↕ _____ K↕ _____ L↕ _____ M↕ _____ N↕ _____ P↕
All Pods, Channel 11	Setup/Hold Time	4.0/0.0 ns	J↕ _____ K↕ _____ L↕ _____ M↕ _____ N↕ _____ P↕
	Setup/Hold Time	0.0/4.0 ns	J↕ _____ K↕ _____ L↕ _____ M↕ _____ N↕ _____ P↕ _____
	Setup/Hold Time	2.0/2.0 ns	J↕ _____ K↕ _____ L↕ _____ M↕ _____ N↕ _____ P↕ _____
Time Interval Accuracy			Pass/Fail
	min X-0	47.50 µs	_____
	max X-0	47.50 µs	_____
	avg X-0	47.50 µs	_____

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Performance Test Record (oscilloscope)

Test	Settings	Results	
Self-Tests		Pass/Fail	_____
DC CAL Output	5.000 Vdc ±10 mV	Limits	Measured
		4.990 Vdc 5.010 Vdc	_____
AC CAL Output	0.8 Vp_p ±10% 1.000 KHz ±10%	0.72 Vp_p 0.88 Vp_p	_____
		900 Hz 1100 Hz	_____
Input Resistance	50 Ω± 0.5 Ω (49.5 to 50.5 Ω) 1MΩ± 10 KΩ (0.990 to 1.010 MΩ)		
Channel 1		50 Ω @ 20 mV/Div	_____
		1 MΩ @ 20 mV/Div	_____
		50 Ω @ 200 mV/Div	_____
		1 MΩ @ 200 mV/Div	_____
		50 Ω @ 1 V/Div	_____
		1 MΩ @ 1 V/Div	_____
		50 Ω @ 4 V/Div	_____
		1 MΩ @ 4 V/Div	_____
Channel 2		50 Ω @ 20 mV/Div	_____
		1 MΩ @ 20 mV/Div	_____
		50 Ω @ 200 mV/Div	_____
		1 MΩ @ 200 mV/Div	_____
		50 Ω @ 1 V/Div	_____
		1 MΩ @ 1 V/Div	_____
		50 Ω @ 4 V/Div	_____
		1 MΩ @ 4 V/Div	_____

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Performance Test Record (oscilloscope)

Test	Settings	Results	
Voltage Measurement Accuracy		Limits	Measured
Channel 1	Zero Input	-13.7 V to -14.3 V	_____
		-3.43 V to -3.57 V	_____
		-1.37 V to -1.43 V	_____
		-137.0 mV to -143.0 mV	_____
		143.0 mV to 137.0 mV	_____
		1.43 V to 1.37 V	_____
		3.57 V to 3.43 V	_____
		14.3 V to 13.7 V	_____
Channel 2	Zero Input	-13.7 V to -14.3 V	_____
		-3.43 V to -3.57 V	_____
		-1.37 V to -1.43 V	_____
		-137.0 mV to -143.0 mV	_____
		143.0 mV to 137.0 mV	_____
		1.43 V to 1.37 V	_____
		3.57 V to 3.43 V	_____
		14.3 V to 13.7 V	_____
Offset Accuracy	**Zero-input offset**		
Channel 1	4 V/Div	0.00 V±320.0 mV	_____
	1 V/Div	0.00 V±80.0 mV	_____
	100 mV/Div	0.00 V±8.0 mV	_____
	10 mV/Div	0.00 V±800.0 µV	_____
Channel 2	4 V/Div	0.00 V±320.0 mV	_____
	1 V/Div	0.00 V±80.0 mV	_____
	100 mV/Div	0.00 V±8.0 mV	_____
	10 mV/Div	0.00 V±800.0 µV	_____
	DC-input offset		
Channel 1	-35.00 V	-35.4 V to -34.6 V	_____
	-10.00 V	-10.1 V to -9.90 V	_____
	-2.00 V	-2.02 V to -1.98 V	_____
	+2.00 V	+1.98 V to +2.02 V	_____
	+10.00 V	+9.90 V to +10.1 V	_____
	+35.00 V	+34.6 V to +35.4 V	_____
Channel 2	-35.00 V	-35.4 V to -34.6 V	_____
	-10.00 V	-10.1 V to -9.90 V	_____
	-2.00 V	-2.02 V to -1.98 V	_____
	+2.00 V	+1.98 V to +2.02 V	_____
	+10.00 V	+9.90 V to +10.1 V	_____
	+35.00 V	+34.6 V to +35.4 V	_____

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Performance Test Record (oscilloscope)

Test	Settings	Results
Bandwidth		Limit Measured
Channel 1		≤–3.0 dB _____
Channel 2		≤–3.0 dB _____
Time Measurement Accuracy	5.500 ns ± 150 ps	MEAN X-O _____ MIN X-O _____ MEAN X-O - MIN X-O _____ MAX X-O _____ MAX X-O - MEAN X-O _____
	99.000 ns ± 155 ps	MEAN X-O _____ MIN X-O _____ MEAN X-O - MIN X-O _____ MAX X-O _____ MAX X-O - MEAN X-O _____
Trigger Sensitivity		
Channel 1	Trigger Stable dc to 50 MHz Trigger Stable 50 MHz to 250 MHz	Pass/Fail _____ Pass/Fail _____
Channel 2	Trigger Stable dc to 50 MHz Trigger Stable 50 MHz to 250 MHz	Pass/Fail _____ Pass/Fail _____

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Performance Test Record (pattern generator)

Test	Settings	Results
Self-Tests		Pass/Fail _____

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4

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To calibrate the oscilloscope 4–3
Set up the equipment 4–3
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To adjust the CRT intensity 4–8

Calibrating and Adjusting

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Calibrating and Adjusting

This chapter gives you instructions for calibrating and adjusting the logic analyzer. Adjustments to the logic analyzer include adjusting the CRT monitor assembly.

To periodically verify the performance of the analyzer, refer to "Testing Performance" in chapter 3.

Logic analyzer calibration

The logic analyzer circuitry of the HP 1660C-series, HP 1660CP-series, and HP 1660CS-series Logic Analyzers does not require an operational accuracy calibration. To test the logic analyzer circuitry against specifications (full calibration), refer to chapter 3, Testing Performance.

The oscilloscope circuitry in the HP 1660CS-series Logic Analyzers requires an operational accuracy calibration by the user or service department under any of the following conditions:

- at six months intervals or every 1,000 hours
- if the ambient temperature changes more than 10° C from the temperature at full calibration
- to optimize measurement accuracy

To test the oscilloscope circuitry against specifications (full calibration), refer to chapter 3, Testing Performance.

The pattern generator circuitry in the HP 1660CP-series Logic Analyzers does not require an operational accuracy calibration.

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To calibrate the oscilloscope

Equipment Required

Equipment	Critical Specification	Recommended Model/Part	Qty
Cable (2)	BNC, 9-inch (equal length)	HP 10502A	1
Cable	BNC	HP 10503A	
Adapter	BNC tee (m)(f)(f)	HP 1250-0781	1
Adapter	BNC (f)(f) (ug-914/u)	HP 1250-0080	

Set up the equipment

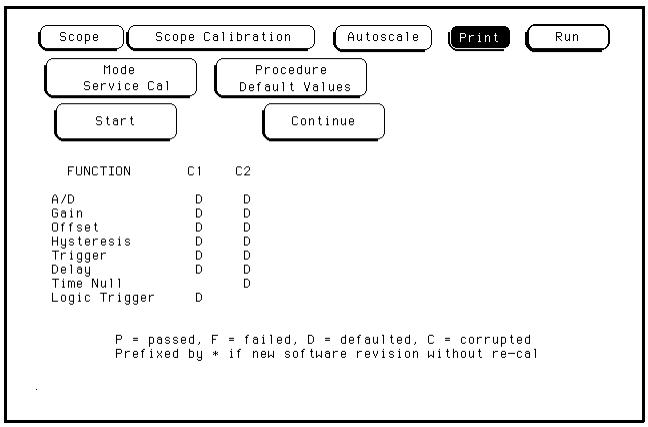
Turn on the logic analyzer. Let it warm up for 30 minutes if you have not already done so.

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Load the Default Calibration Factors

Note that once the default calibration factors are loaded, all calibrations must be done. This includes all of the calibrations in the Self Cal menu. The calibration must be performed in the exact sequence listed below.

1. Press the System key. Select System, then select Scope.
2. Select the menu field (top row, second from the left), then select Scope Calibration from the pop-up menu.
3. Select the Mode field, then select Service Cal from the pop-up menu.
4. Select the Procedure field, then select Default Values from the pop-up menu.
5. Select the Start field and follow the instructions on the display.



After you select the Start field, you can abort the calibration procedure by selecting either the Mode or Procedure fields if the Continue field is still displayed on the screen.

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Self Cal menu calibrations

Messages will be displayed as each calibration routine is completed to indicate calibration has passed or failed. The resulting calibration factors are automatically stored to nonvolatile RAM at the conclusion of each calibration routine.

The Self Cal menu lets you optimize vertical sensitivity (Vert Cal) for channels 1 and 2 individually or both channels on a board simultaneously. Also, the Self Cal menu lets you optimize delay (Delay) for channel 1 and 2 separately, then Time Null for channel 2 and the Logic Trigger.

1 Optimize Vert Cal of the Self Cal.

- **a** Connect two BNC 50-Ω, 9-inch cables to the BNC tee adapter. Connect the BNC 50Ω (f)(f) adapter to the BNC tee adapter, and connect the 48-inch BNC cable to the BNC 50Ω (f)(f) adapter. Once you select Start, the instrument will prompt you to connect the cables to the appropriate locations on the rear panel of the instrument.
- **b** Select the Mode field, then select Self Cal from the pop-up menu.
- **c** Select the Procedure field, then select Vert Cal from the pop-up menu.
- **d** Select the Channel field, then select a channel choice from the pop-up menu.
- **e** Select the Start field and follow the instructions on the display.
- **f** After completion of Vertical Calibration, remove the cables from the instrument.

2 Optimize Delay of the Self Cal.

- **a** Obtain a BNC 50-Ω, 48-inch cable. Once you select Start, the instrument will prompt you to connect the cable to the appropriate location on the rear panel of the instrument.
- **b** Select the Procedure field, then select Delay from the pop-up menu.
- **c** Select the Channel field, then select C1.
- **d** Select the Start field and follow the instructions on the display.
- **e** Repeat steps c and d for channel 2.
- **f** After completing all of the channel delay calibrations, remove the cable from the oscilloscope.

3 Optimize the Time Null of the Self Cal.

- **a** Connect two BNC 50-Ω, 9-inch cables to the BNC tee adapter. Connect the BNC 50Ω (f)(f) adapter to the BNC tee adapter, and connect the 48-inch BNC cable to the BNC 50Ω (f)(f) adapter. Once you select Start, the instrument will prompt you to connect the cables to the appropriate locations on the rear panel of the instrument.
- **b** Select the Procedure field, then select Time Null from the pop-up menu.
- **c** Select the Start field and follow the instructions on the display.
- **d** After completion of the Time Null calibration, remove the cables from the instrument.

4 Calibrate the Logic Trigger of the Self Cal.

- **a** Obtain a BNC 50-Ω, 48-inch cable.
- **b** Select Start. The instrument will prompt you to connect the cable to the appropriate location on the rear panel of the instrument.
- **c** Select the Procedure field, then select Logic Trigger from the pop-up menu.
- **d** Select the Start field and follow the instructions on the display.
- **e** After completion of the Logic Trigger calibration, remove the cable from the instrument.

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To adjust the CRT monitor alignment

This procedure must be performed by trained personnel. Adjustments are made with the cover removed and power applied.

WARNING

Do not touch the CRT monitor sweep board. High voltages exist on the sweep board that can cause personal injury.

Equipment Required

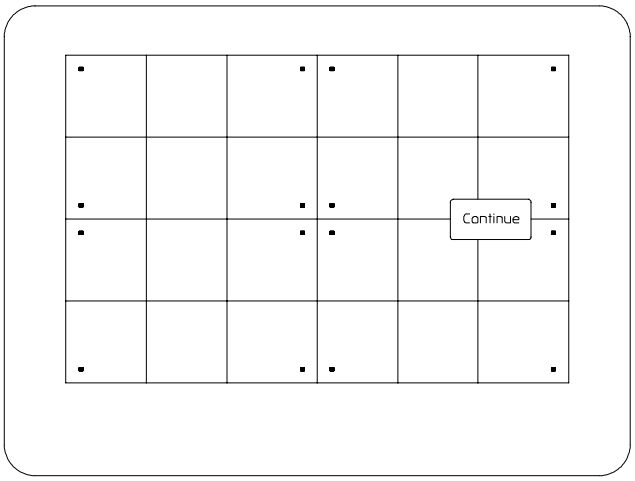
Equipment	Critical Specification	Recommended Model/Part
Alignment Tool	1	8710-1300

1. Turn off the logic analyzer, then disconnect the power cord. Remove the cover. Refer to chapter 6, "Replacing Assemblies," for instructions to remove the cover.
2. Connect the power cord, then turn on the logic analyzer.
3. Insert the disk containing the functional performance verification tests into the disk drive, then load the functional performance verification operating system into the logic analyzer.

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4 Enter the Sys PV tests, then enter the Display Test.

A grid pattern should appear.

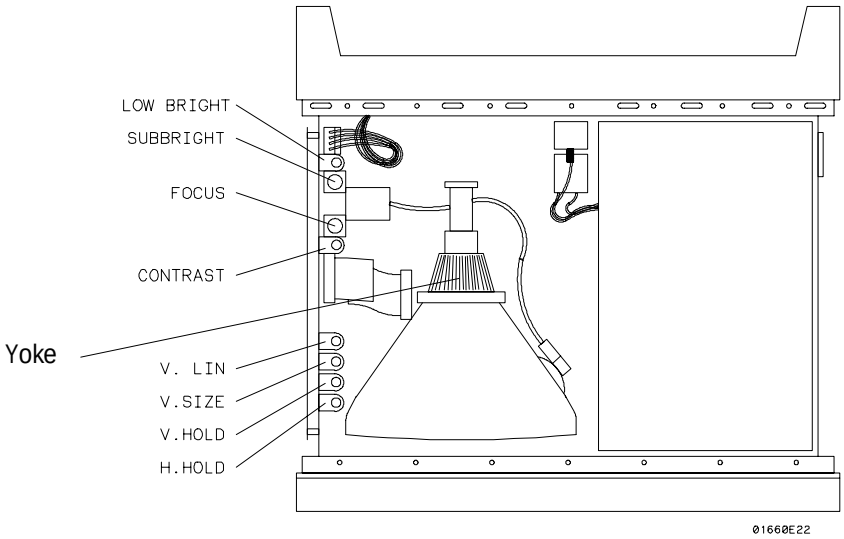


5 If the display is tilted (rotated), adjust the CRT yoke by rotating it to straighten the display.

You may need to loosen the screw on the yoke in order to rotate it. If so, ensure you tighten the screw after you have adjusted the yoke to the desired position.

WARNING

Do not touch the CRT monitor sweep board. High voltages exist on the sweep board that can cause personal injury.



6 If the grid pattern is not centered horizontally, adjust the H-Hold.

7 If you need to adjust the intensity, go to the next page.

If you are finished with the adjustments, turn off the instrument, then remove the power cord. Install the cover on the instrument.

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To adjust the CRT intensity

This procedure must be performed by trained personnel. Adjustments are made with the cover removed and power applied.

WARNING

Do not touch the CRT monitor sweep board. High voltages exist on the sweep board that can cause personal injury.

Equipment Required

Equipment	Critical Specification	Recommended Model/Part
Alignment Tool	1	8710-1300
Light Power Meter		United Detector 351

1 Turn off the logic analyzer, then disconnect the power cord. Remove the cover. Refer to chapter 6, "Replacing Assemblies," for instructions to remove the cover.

2 Connect the power cord, then turn on the logic analyzer.

3 Access the Display Test.

- If you just finished adjusting the CRT monitor alignment, go to step 4.
- To Access the Display Test, perform the following steps.

a Insert the disk containing the functional performance verification tests into the disk drive, then load the functional performance verification operating system into the logic analyzer.

b Enter the Sys PV tests and enter the Display Test. A grid pattern should appear.

4 Press the front panel Select key.

The display should show a full bright test screen.

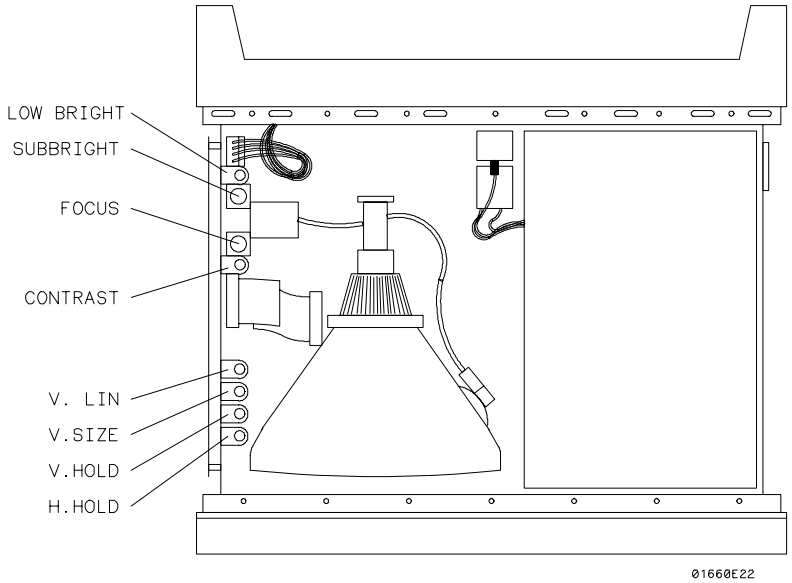
5 Turn the rear panel intensity adjustment to full bright.

6 Place the light power meter against the display at center screen.

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WARNING Do not touch the CRT monitor sweep board. High voltages exist on the sweep board that can cause personal injury.

7 The light power meter should read 137-154 cd/m^2. If the measurement is out of this range, use the adjustment tool to adjust the Contrast potentiometer on the monitor driver board.



8 Press the front panel Select key.

The display should show a half bright test screen.

9 Place the light power meter against the display at center screen. The light power meter should read 5-27 cd/m^2.

If the reading is not correct, try adjusting the contrast in step 7 closer to the limit.

10 Press the front panel Select key.

The logic analyzer should exit the Display Test.

11 Place the light power meter against the display at center screen. Adjust the rear panel intensity adjustment until the light power meter reads 45-55 cd/m^2.

12 Exit the functional performance verification tests.

13 Turn off the instrument, then remove the power cord. Install the cover on the instrument.

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5

To use the flowcharts 5–2
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Troubleshooting

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Troubleshooting

This chapter helps you troubleshoot the logic analyzer to find defective assemblies. The troubleshooting consists of flowcharts, self-test instructions, and tests. This information is not intended for component-level repair.

If you suspect a problem, start at the top of the first flowchart. During the troubleshooting instructions, the flowcharts will direct you to perform other tests.

The service strategy for this instrument is the replacement of defective assemblies. This instrument can be returned to Hewlett-Packard for all service work, including troubleshooting. Contact your nearest Hewlett-Packard Sales Office for more details.

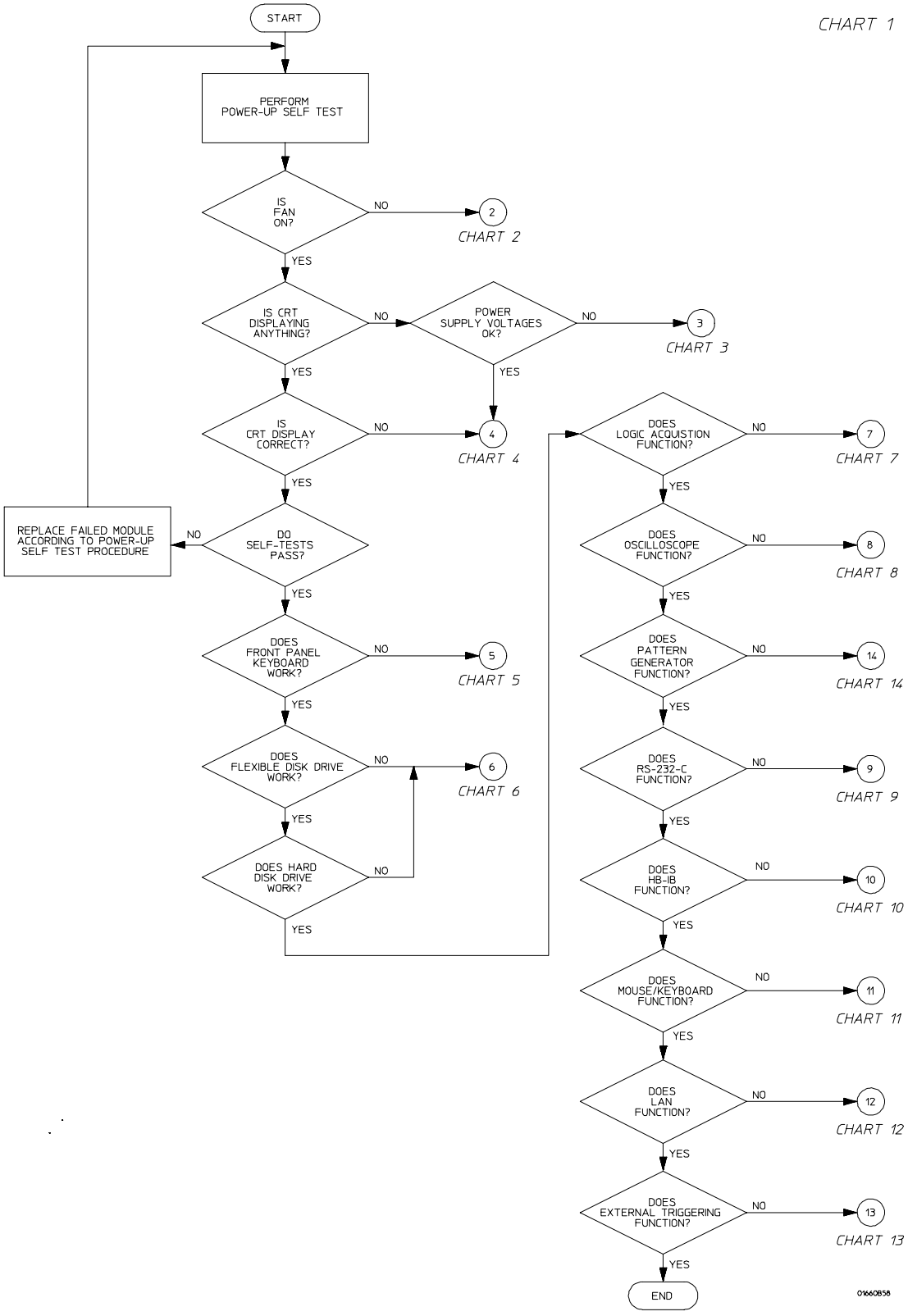
CAUTION

Electrostatic discharge can damage electronic components. Use grounded wriststraps and mats when you perform any service to this instrument or to the cards in it.

To use the flowcharts

Flowcharts are the primary tool used to isolate defective assemblies. The flowcharts refer to other tests to help isolate the trouble. The circled letters on the charts indicate connections with the other flowcharts. Start your troubleshooting at the top of the first flowchart.

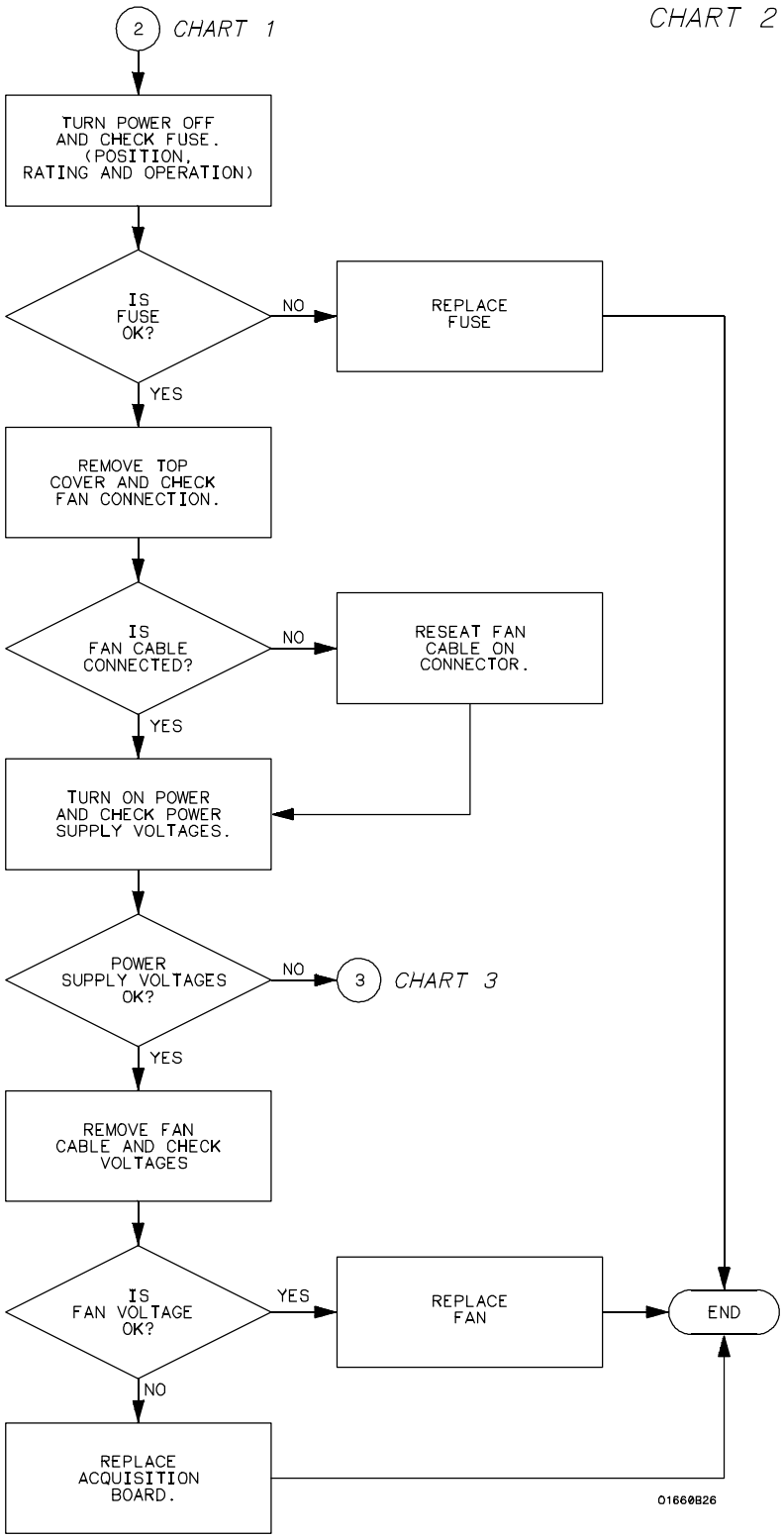
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Troubleshooting Flowchart 1

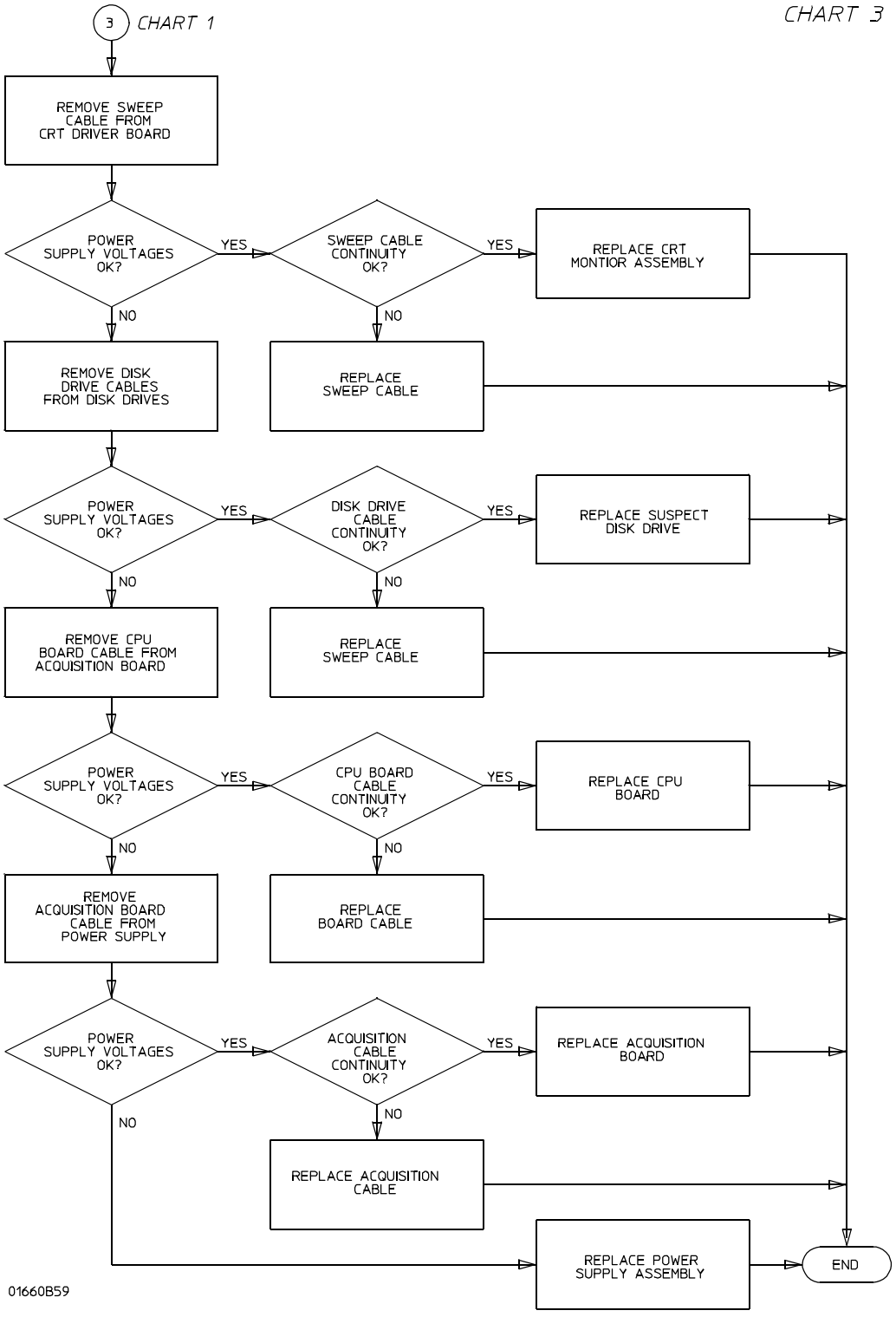
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To use the flowcharts



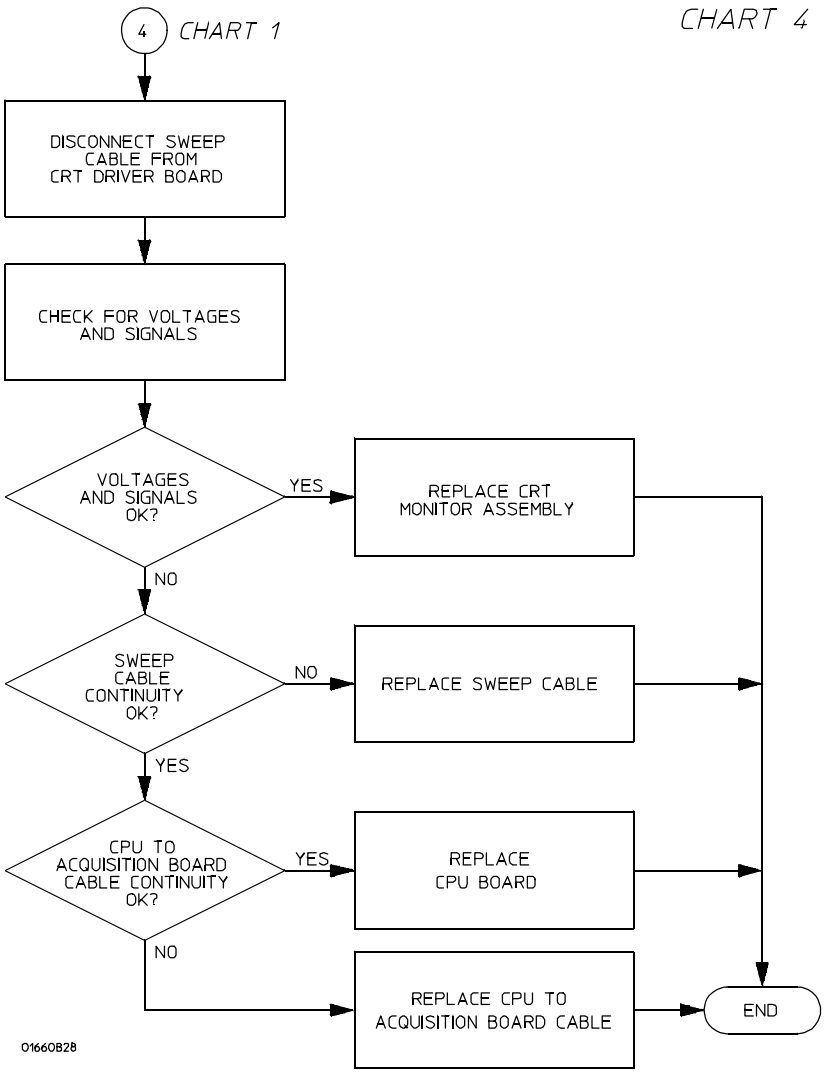
Troubleshooting Flowchart 2

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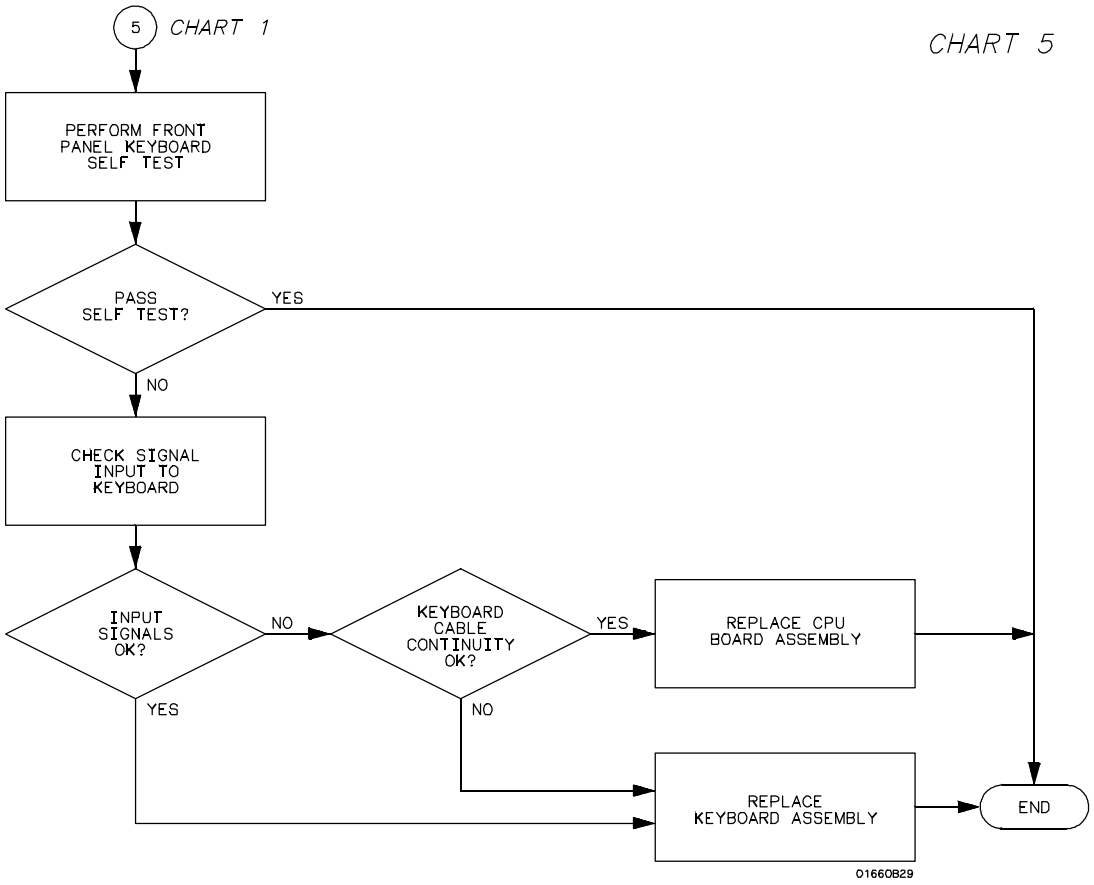
Troubleshooting Flowchart 3

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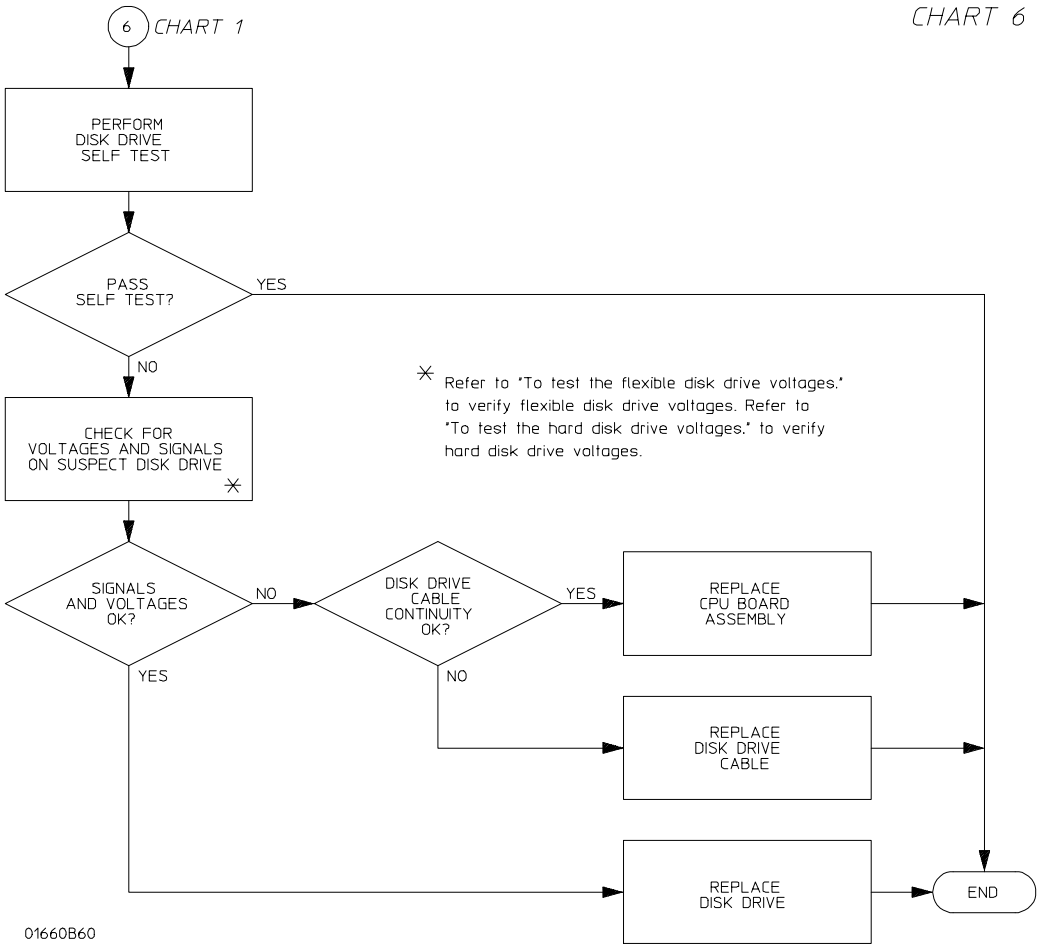
Troubleshooting Flowchart 4

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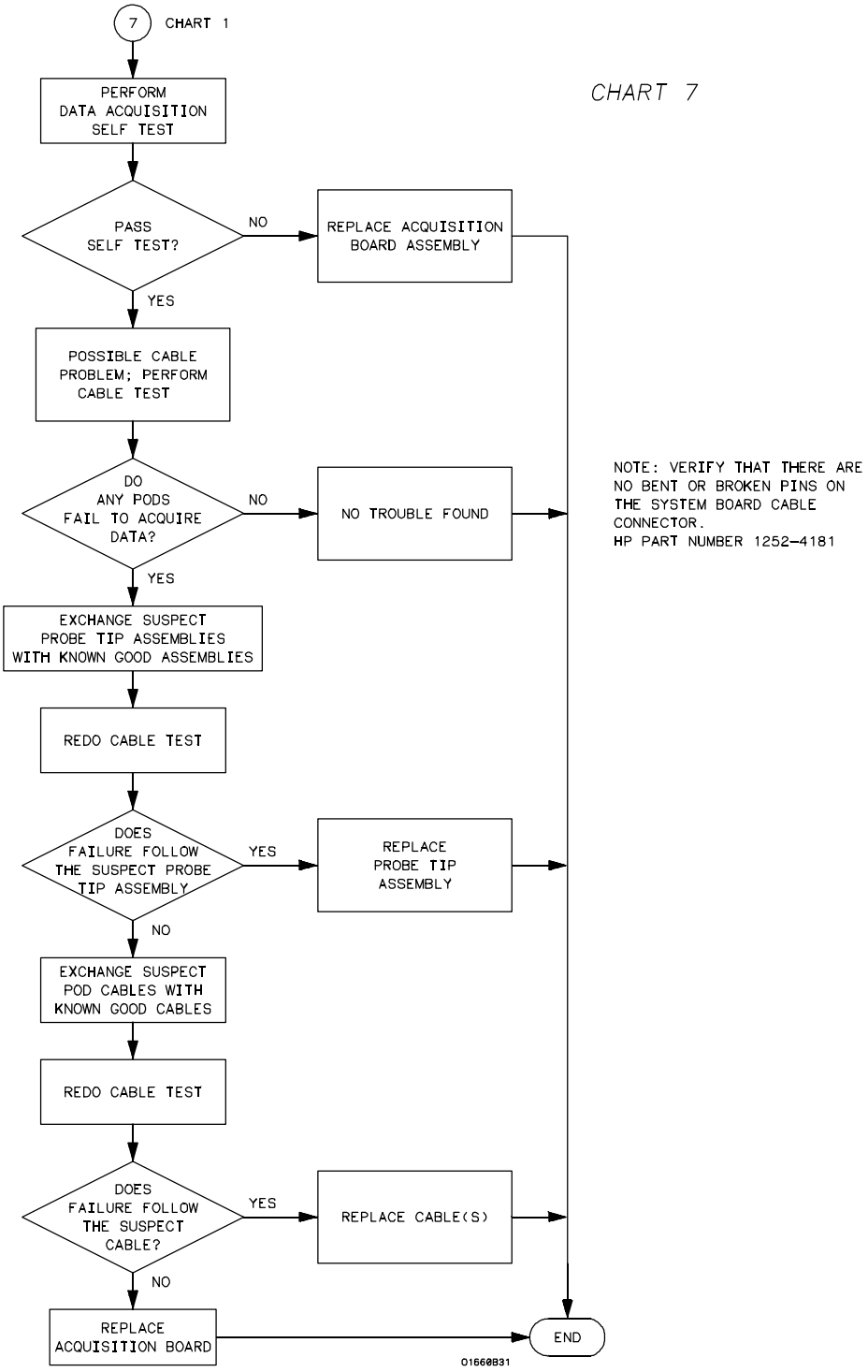
Troubleshooting Flowchart 5

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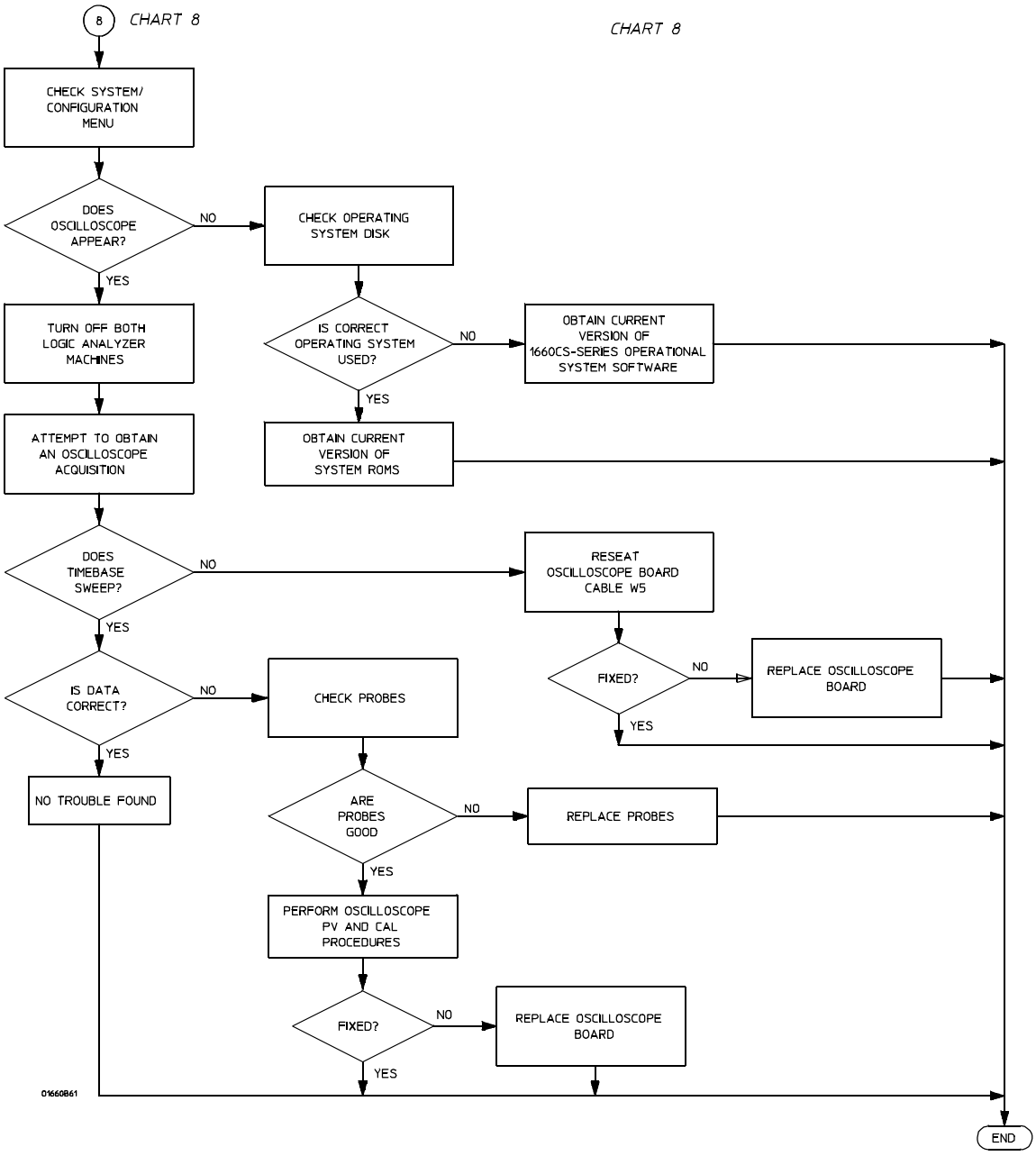
Troubleshooting Flowchart 6

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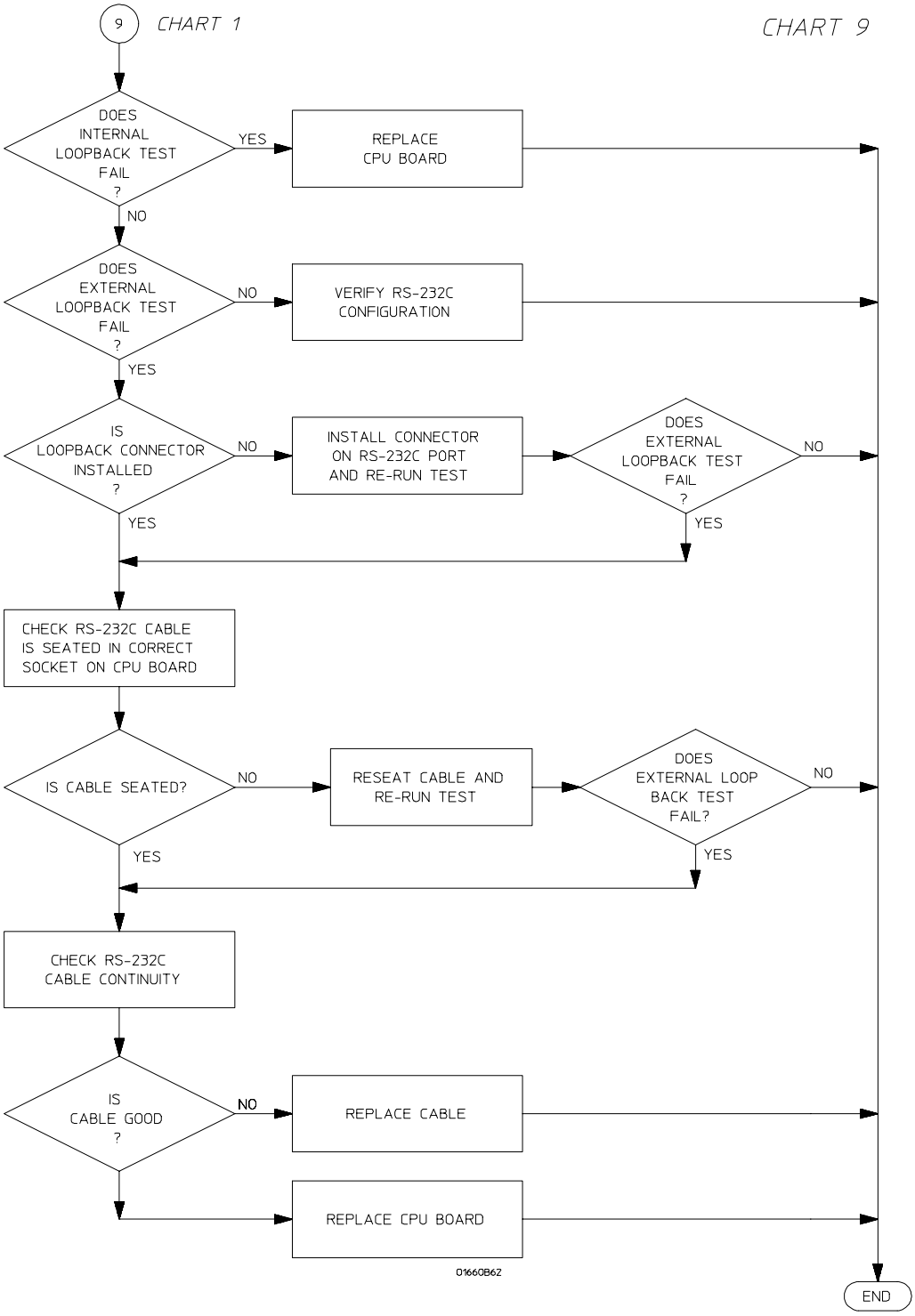
Troubleshooting Flowchart 7

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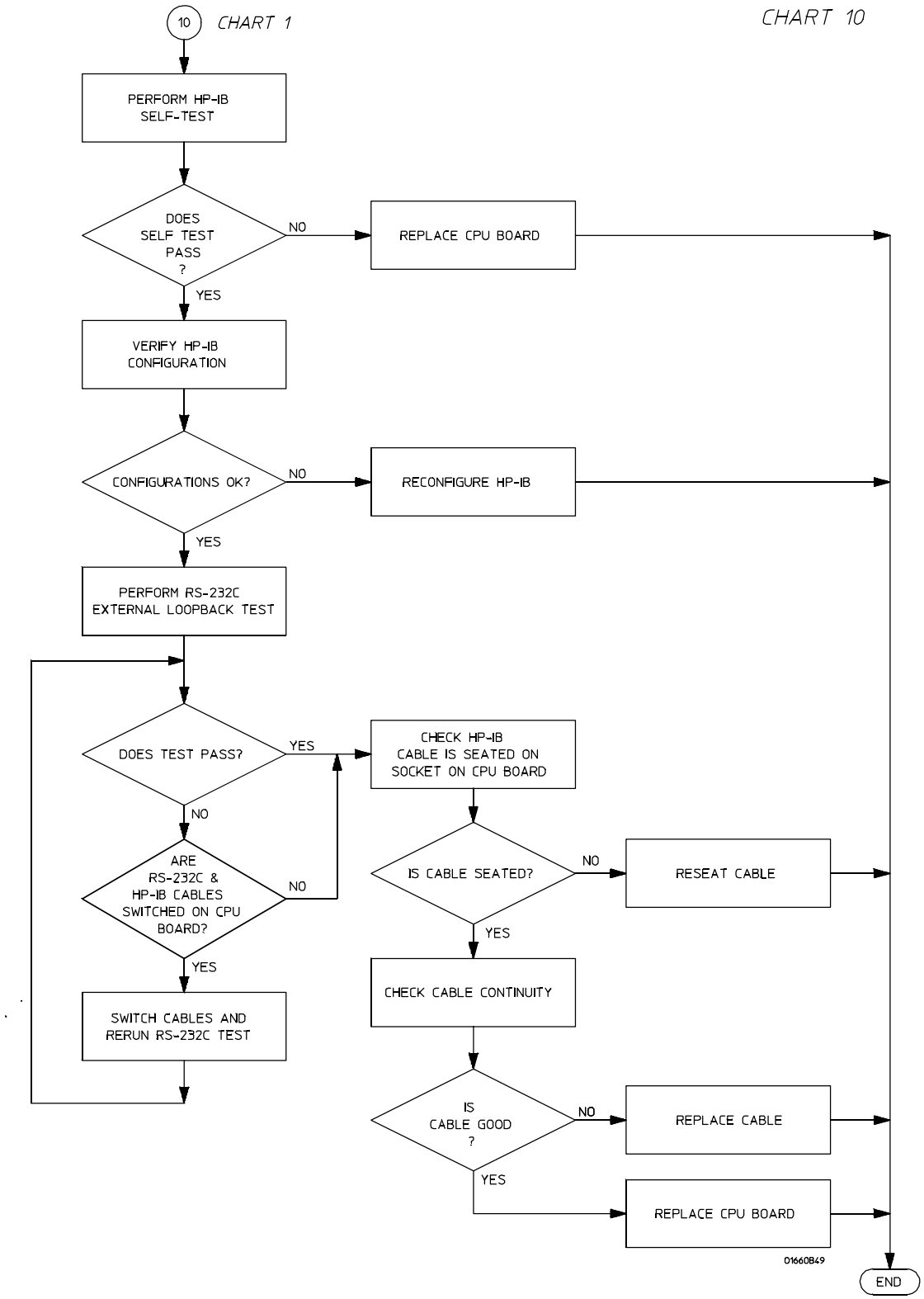
Troubleshooting Flowchart 8

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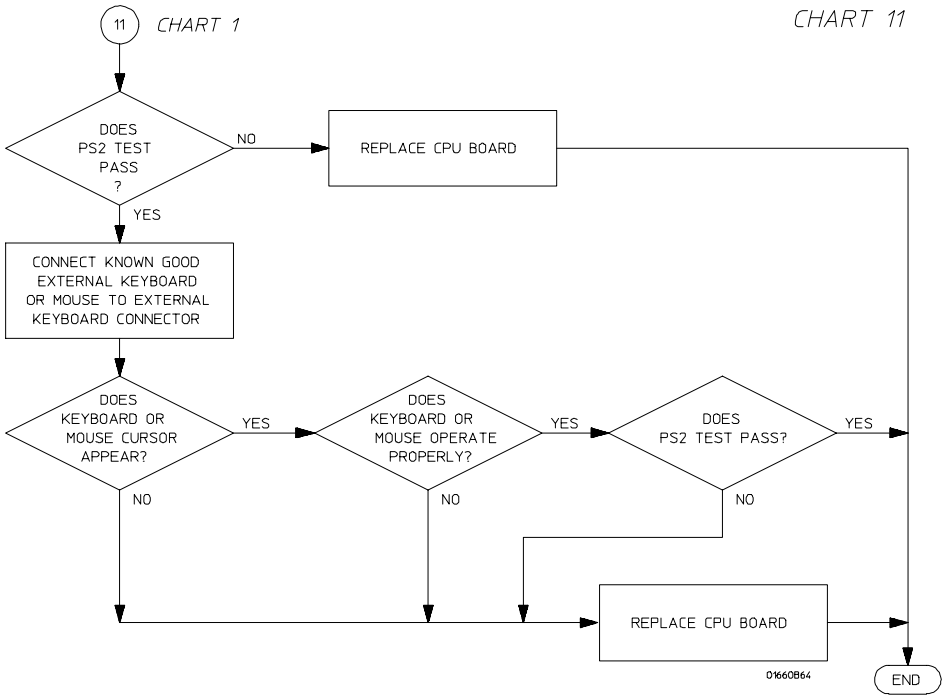
Troubleshooting Flowchart 9

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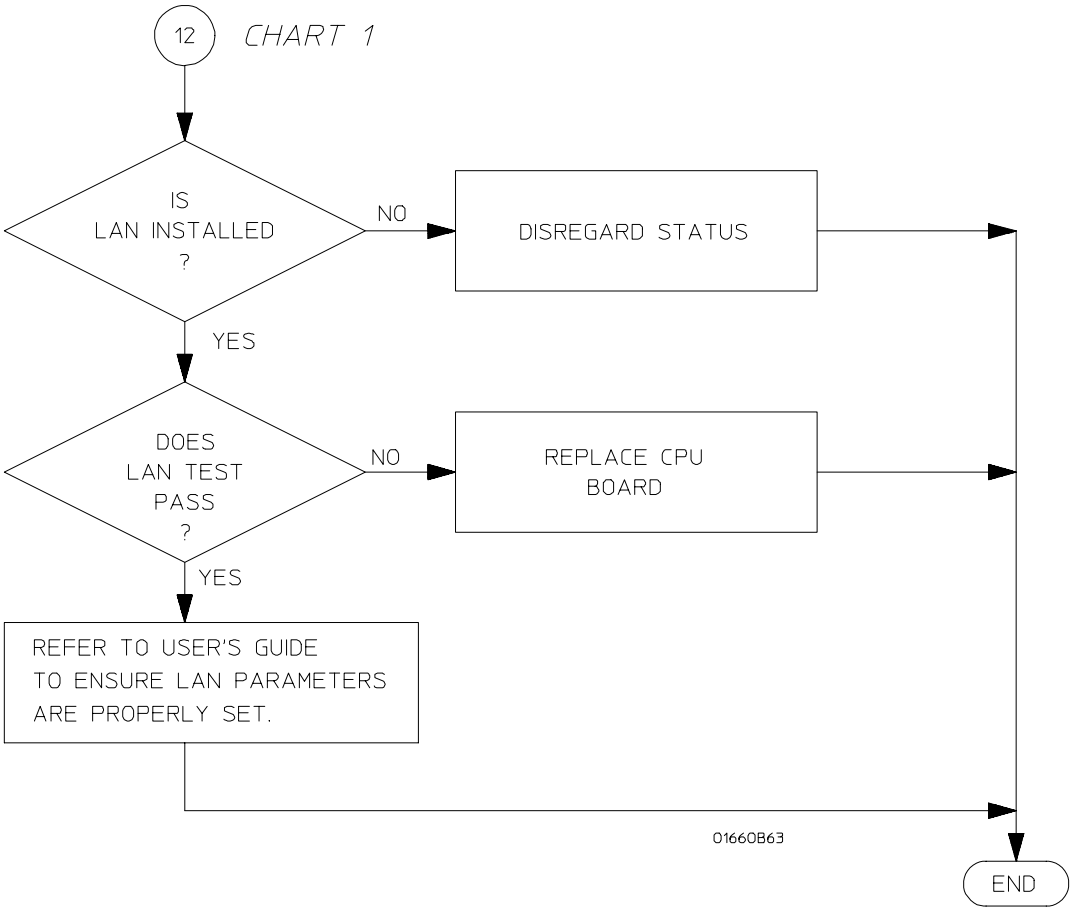
Troubleshooting Flowchart 10

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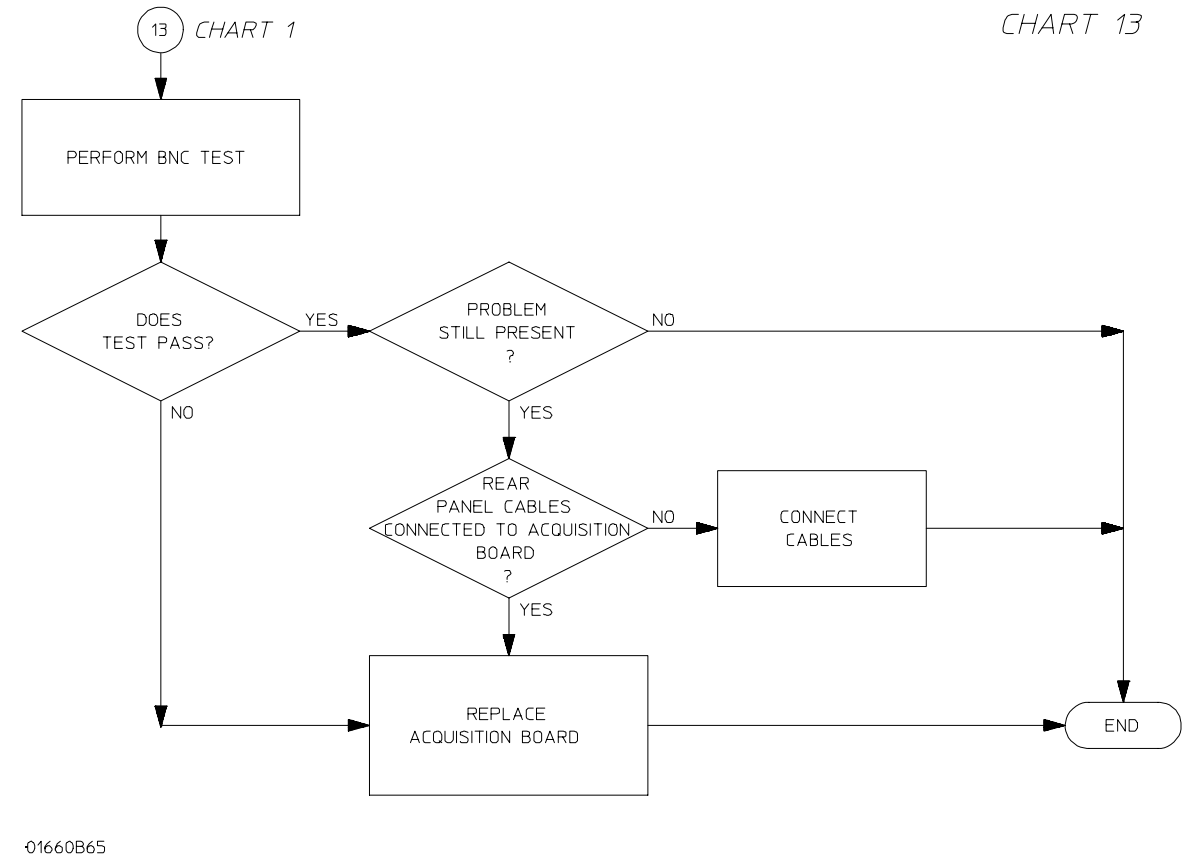
Troubleshooting Flowchart 11

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Troubleshooting Flowchart 12

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Troubleshooting Flowchart 13

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To use the flowcharts



Troubleshooting Flowchart 14

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To check the power-up tests

The logic analyzer automatically performs power-up tests when you apply power to the instrument. The revision number of the operating system shows in the upper-right corner of the screen during these power-up tests. As each test completes, either "passed" or "failed" prints on the screen in front of the name of each test.

1. Disconnect all inputs, then insert a formatted disk into the flexible disk drive.
2. Let the instrument warm up for a few minutes, then cycle power by turning off then turning on the power switch.

   If the instrument is not warmed up, the power-up test screen will complete before you can view the screen.
3. As the tests complete, check if they pass or fail.

   The Flexible Disk Test reports No Disk if a disk is not in the disk drive.

Performing Power-Up Self-Tests

passed	ROM text
passed	RAM test
passed	Interrupt test
passed	Display test
passed	PS2 Controller Test
passed	Hard Disk Test
No Disk	Flexible Disk Test

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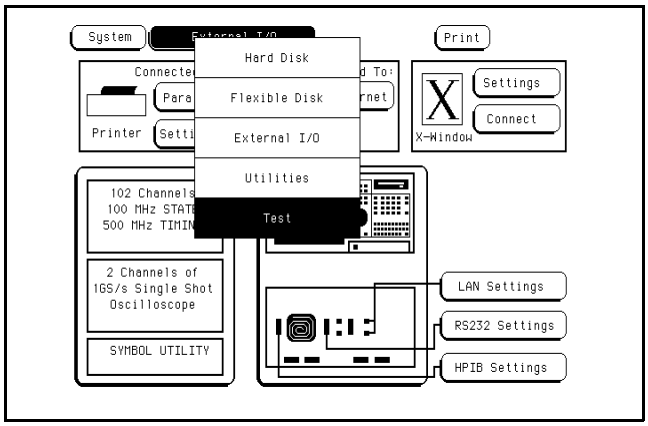
To run the self-tests

Self-tests identify the correct operation of major functional areas of the instrument. You can run all self-tests without accessing the interior of the instrument. If a self-test fails, the troubleshooting flowcharts instruct you to change a part of the instrument.

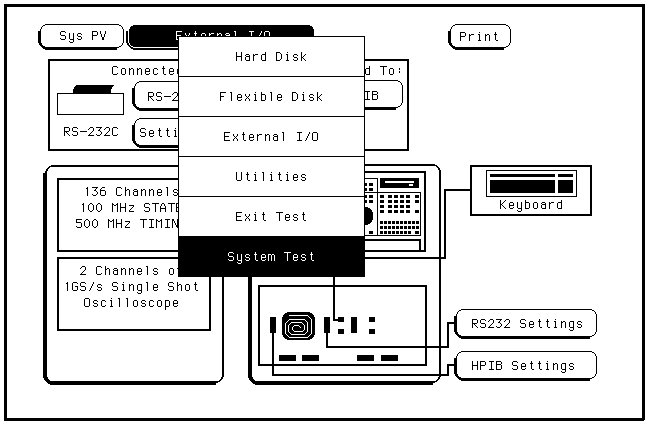
These procedures assume the files on the PV disk have been copied to the /SYSTEM subdirectory on the hard disk drive. If they have not already been copied, insert the PV disk in the flexible disk drive before starting this procedure.

1. If you just did the power-up self-tests, go to step 2.

   If you did not just do the power-up self-tests, disconnect all inputs, then turn on the power switch. Wait until the power-up tests are complete.
2. Press the System key, then select the field next to System. Then, select Test in the pop-up menu.



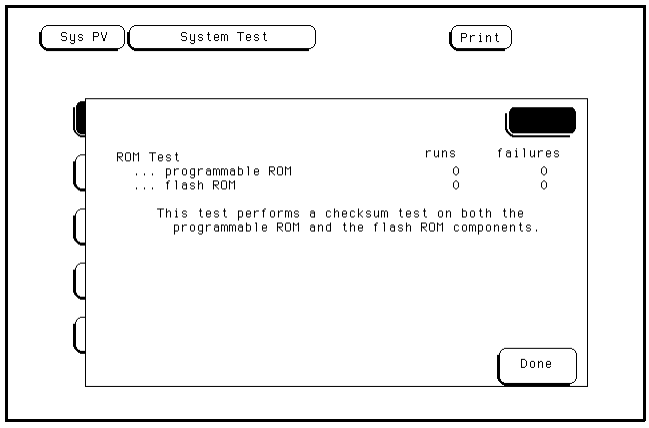
3. Select the box labeled Load Test System, then select Continue.
4. Press the System key, then select the field next to Sys PV. Select System Test to access the system tests.



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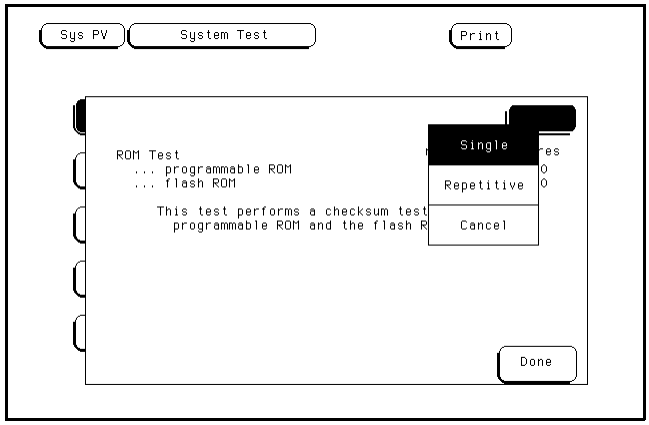
5 Select ROM Test. The ROM Test screen is displayed.

You can run all tests at one time by running All System Tests. To see more details about each test, you can run each test individually. This example shows how to run an individual test.

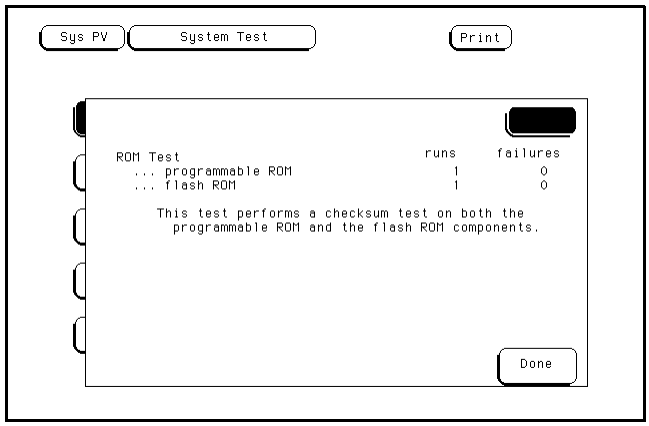


6 Select Run, then select Single.

To run a test continuously, select Repetitive. Select Stop to halt a repetitive test.

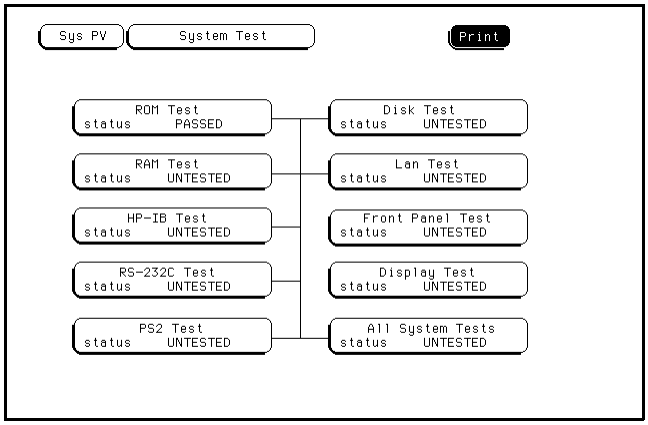


For a Single run, the test runs one time, and the screen shows the results.



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7 To exit the ROM Test, select Done. Note that the status changes to Passed or Failed.



8 Install a formatted disk that is not write protected into the flexible disk drive. Connect an RS-232-C loopback connector onto the RS-232-C port. Run the remaining System Tests in the same manner.

9 Select the Front Panel Test.

A screen duplicating the front-panel appears on the screen.

a Press each key on the front panel. The corresponding key on the screen will change from a light to a dark color.

b Test the knob by turning it in both directions.

c Note any failures, then press the Done key a second time to exit the Front Panel Test. The test screen shows the Front Panel Test status changed to Tested.

10 Select the Display Test.

A white grid pattern is displayed. These display screens can be used to adjust the display.

a Select Continue and the screen changes to full bright.

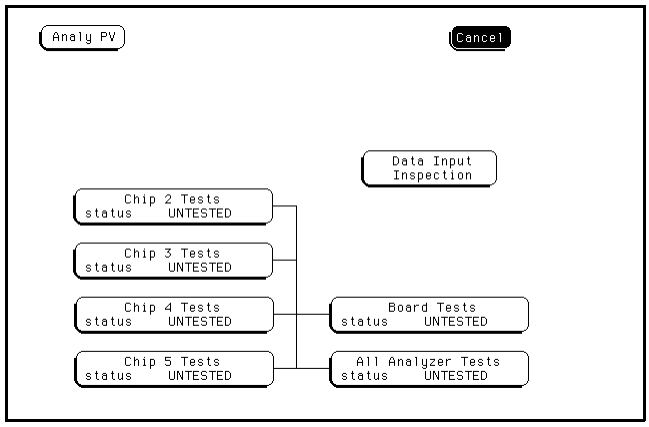
b Select Continue and the screen changes to half bright.

c Select Continue and the test screen shows the Display Test status changed to Tested.

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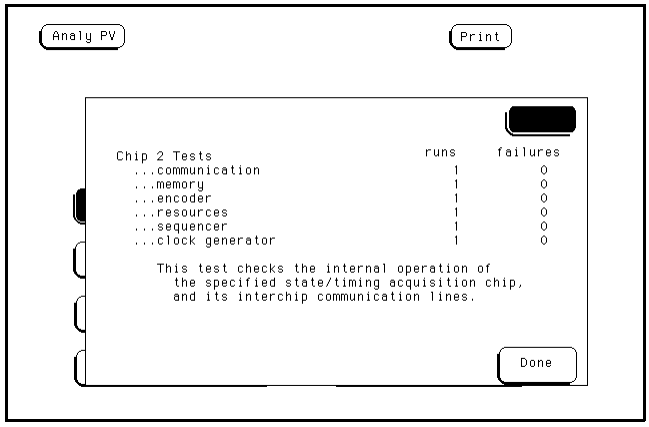
11 Select Sys PV, then select Analy PV in the pop-up menu. Select Chip 2 Tests.

You can run all the analyzer tests at one time by selecting All Analyzer Tests. To see more details about each test, you can run each test individually. This example shows how to run Chip 2 Tests. Chip 3, 4, and 5 Tests operate the same as Chip 2 Tests.



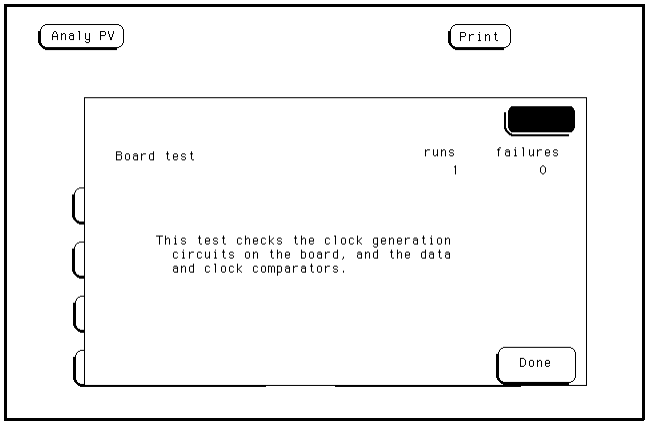
12 In the Chip 2 Tests menu, select Run, then select Single. The test runs one time, then the screen shows the results. When the test is finished, select Done. Then, perform the other Chip Tests.

To run a test continuously, select Repetitive. Select Stop to halt a Run Repetitive.

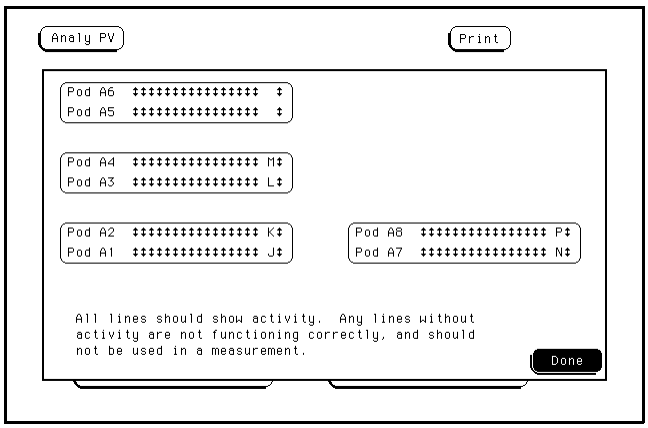


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13 Select Board Tests, then select Run. When the Board Tests are finished, select Done.



14 Select Data Input Inspection. All lines should show activity. Select Done to exit the Data Input Inspection.

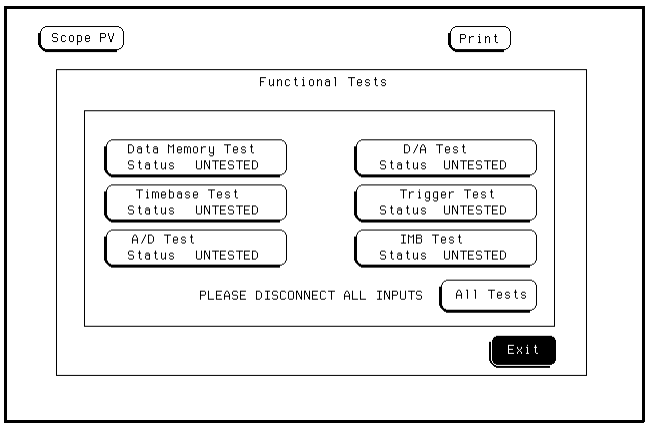


If you have an HP 1660C-series Logic Analyzer (no oscilloscope or pattern generator), go to step 19. If you have an HP 1660CP-series Logic Analyzer, go to step 18. If you have an HP 1660CS-series Logic Analyzer, continue with step 15.

15 Select Analy PV, then select Scope PV in the pop up menu. Select Functional Tests.

16 Select one of the Scope PV tests.

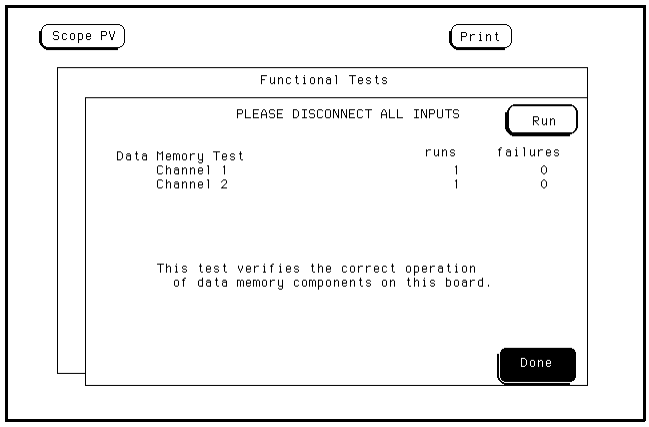
You can run all of the tests at one time by selecting All Tests, or you can run each test individually. For this example, select Data Memory Test.



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17 In the Data Memory Test menu, select Run, then select Single. The test runs one time, then the screen shows the results. When the test is finished, select Done.

To run a test continuously, select Repetitive. Select Stop to halt a Repetitive Run.

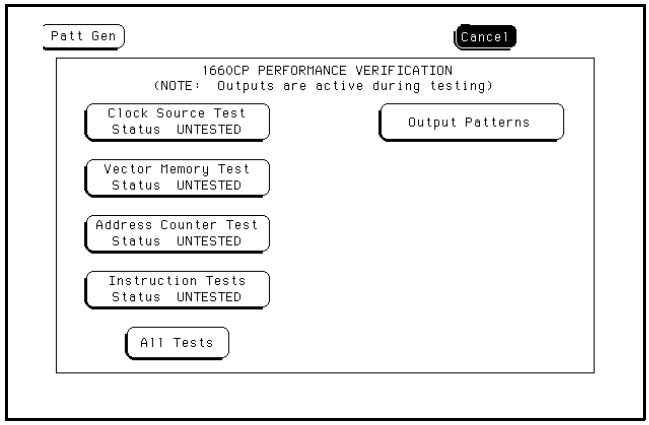


Go to step 19 to exit the test system.

18 For the HP 1660CP-series Logic Analyzers, Select Analy PV, then select Patt Gen in the pop-up menu. In the Patt Gen menu select Clock Source Test.

You can run all tests at one time (except the Output Patterns routine) by selecting All Tests. To see more details about each test, you can run each test individually. This example shows how to run the Clock Source Test. The Vector Memory Test, Address Counter Test, and Instruction Tests are run in a similar manner.

When the tests finish, the status for each test shows Passed or Failed. Select Done.



19 To exit the tests, press the System key. Select the field to the right of the Sys PV field.

20 Select the Exit Test System.

If you are performing the self-tests as part of the troubleshooting flowchart, return to the flowchart.

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To test the power supply voltages

To check the voltages, the power supply must be loaded by either the acquisition board or with an added resistor.

Refer to chapter 6, "Replacing Assemblies," for instructions to remove or replace covers and assemblies.

WARNING

Hazard voltages exist on the power supply, the CRT, and the CRT driver board. This procedure is to be performed by service-trained personnel aware of the hazards involved, such as fire and electrical shock.

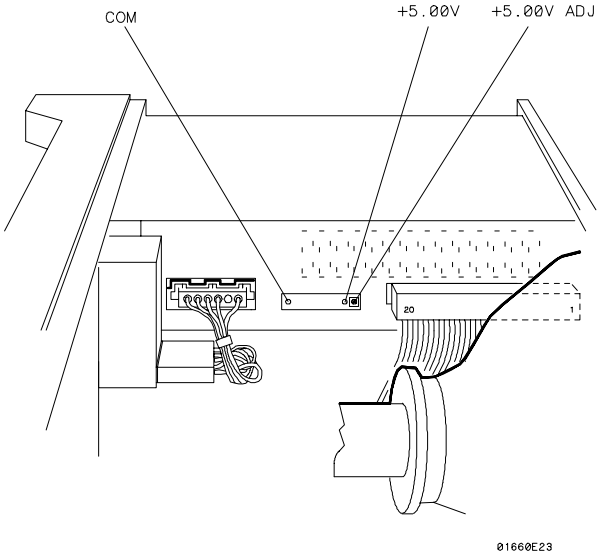
Loaded by the acquisition board

1. Turn off the instrument, then remove the power cable. Remove the cover of the instrument.
2. Connect the power plug, then turn on the instrument.
3. Check for the +5 V, as indicated by the figure below.

Loaded by the added resistor

1. Turn off the instrument, then remove the power cable. Remove the cover of the instrument and the disk drive assembly.
2. Remove the power supply far enough to disconnect the power supply cable from the acquisition board. Bring the end of the cable up and out of the instrument.

   Use the disconnected cable to load the supply and to make measurements.
3. Load the +5.00 V supply with a 2 Ω, 25 watt resistor.
   a. With a jumper wire, connect one end of the resistor to one of the 5.00 V pins (pins 1 through 4) on the supply cable.
   b. With another jumper wire, connect the other end of the resistor to one of the ground pins (pins 5 through 7) on the supply cable.
4. Connect the power plug, then turn on the instrument.
5. Check for the +5 V as indicated by the figure below.

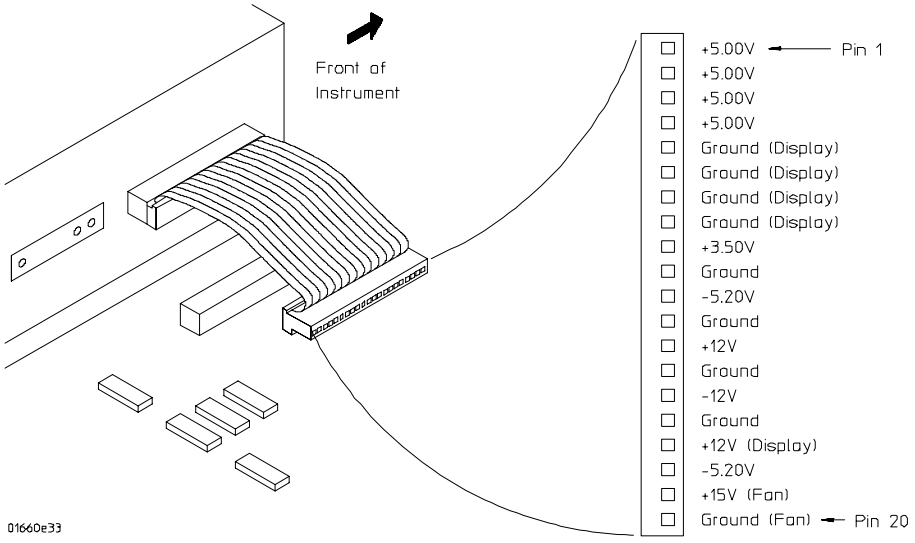


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6 Check for the voltages on the power supply cable using the values in the following table.

Signals on the Power Supply Cable

Pin	Signal	Pin	Signal
1	+5.00 V	11	–5.20 V
2	+5.00 V	12	Ground
3	+5.00 V	13	+12 V
4	+5.00 V	14	Ground
5	Ground (Digital)	15	–12 V
6	Ground (Digital)	16	Ground
7	Ground (Digital)	17	+12 V (Display)
8	Ground (Display)	18	–5.20 V
9	+3.50 V	19	+15 V (Fan)
10	Ground	20	Ground (Fan)



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To test the CRT monitor signals

Refer to chapter 6, "Replacing Assemblies," for instructions to remove or replace covers and assemblies.

WARNING

Hazard voltages exist on the power supply, the CRT, and the CRT driver board. This procedure is to be performed by service-trained personnel aware of the hazards involved, such as fire and electrical shock.

1 Remove the cover of the instrument.

2 Check the CRT monitor input cable for the signals and the power supplies listed in the table below. The cable is the wide ribbon cable connecting the monitor to the acquisition board.

CRT Monitor Cable Signals

Pin	Signal	Pin	Signal
1	NC	2	+12 V
3	Ground	4	Ground
5	+12 V	6	Ground
7	+12 V	8	Ground
9	+12 V	10	HSYNC
11	VSYNC	12	+12 V
13	Ground	14	Ground
15	Ground	16	Video
17	Ground	18	NC
19	Ground	20	NC

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To test the keyboard signals

Refer to chapter 6, "Replacing Assemblies," for instructions to remove covers and assemblies.

WARNING

Hazard voltages exist on the power supply, the CRT, and the CRT driver board. This procedure is to be performed by service-trained personnel aware of the hazards involved, such as fire and electrical shock.

1. Turn off the instrument and remove the power cable.
2. Without disconnecting the keyboard cable, follow the keyboard removal procedure to loosen the keyboard. Leave the keyboard in place in front of the instrument.
3. Reconnect the power cable, then turn on the instrument.
4. Run the PV Front Panel Test, pressing all of the keys.
5. If a random key is not operating, then go to the next step.

   If a group of keys do not work, then check the keyboard voltages and signals.

Keyboard Connector Signals

Pin	Signal	Pin	Signal
1	Keyboard Return	13	Keyboard Scan
2	"	14	"
3	"	15	"
4	"	16	"
5	"	17	"
6	"	18	"
7	"	19	LED
8	"	20	+5 V
9	Keyboard Scan	21	Ground
10	"	22	Knob
11	"	23	Ground
12	"	24	Knob

6. Allow the keyboard assembly to fall forward from the front panel. Separate the elastomeric keypad and keyboard panel from the PC board.
7. Using a paper clip or screwdriver, short the PC board trace of the non-operating key and look for an appropriate response on the display.
8. If the display responds as if the key were pressed, replace the elastomeric keypad.

   If the display does not respond as if the key were pressed, replace the keyboard.
9. Check the RPG connector.

   The RPG connector has a TTL pulse on pins 22 and 24 when the knob is being turned. Pin 20 of the connector is +5 V.

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To test the flexible disk drive voltages

Refer to chapter 6, "Replacing Assemblies," for instructions to remove or replace covers and assemblies.

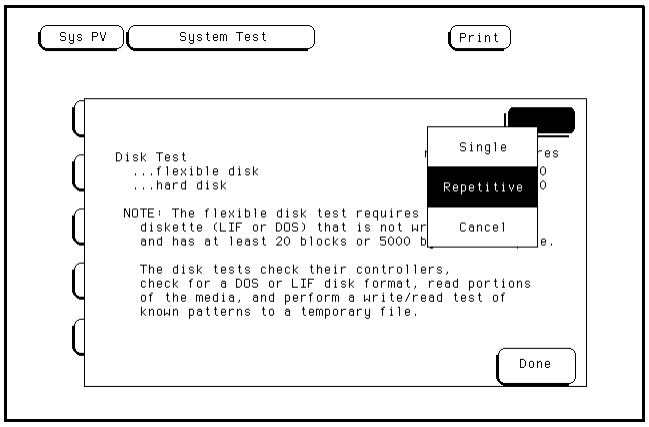
WARNING

This procedure is to be performed by service-trained personnel aware of the hazards involved, such as fire and electrical shock.

Equipment Required

Equipment	Critical Specification	Recommended Model/Part
Digitizing Oscilloscope	> 100 MHz Bandwidth	HP 54600B

1. Turn off the instrument, then remove the power cable. Remove the instrument cover and the disk drive assembly.
2. Reconnect the disk drive cable to the rear of the flexible disk drive. Turn the disk drive assembly over so that the solder connections of the cable socket on the flexible drive are accessible.
3. Connect the power cable, then turn on the instrument.
4. Insert the disk that contains the functional performance verification software and enter the test operating system.
5. In the Sys PV menu select the Flexible Disk test. Insert a disk that has enough available bytes to run the test in the disk drive, then select Run-Repetitive.

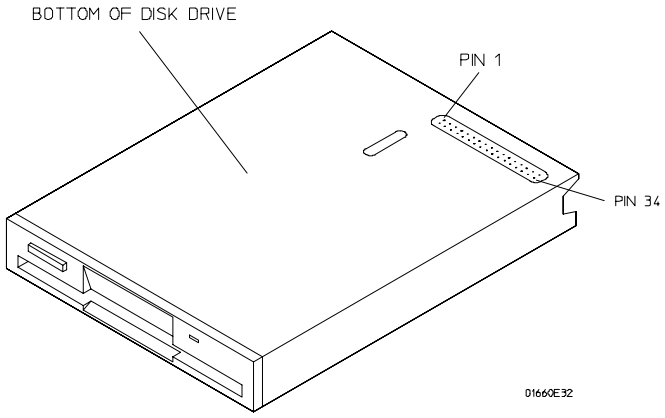


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6 Check for the following voltages and signals using an oscilloscope.

Disk Drive Voltages

Pin	Signal Description	Pin	Signal Description
1	NC	2	Disk Change
3	NC	4	High Density
5	NC	6	NC
7	+5 V	8	Index
9	+5 V	10	Drive Select
11	+5 V	12	NC
13	Ground	14	NC
15	Ground	16	Motor On
17	Ground	18	Direction
19	Ground	20	Step
21	Ground	22	Write Data
23	Ground	24	Write Gate
25	Ground	26	Track 00
27	Ground	28	Write Protect
29	Ground	30	Read Data
31	Ground	32	Side Select
33	Ground	34	Ready



7 Select Stop, and turn off the logic analyzer. Remove the power cable.

The test will not immediately stop when Stop is selected; it will continue until the current iteration of the disk test is completed and then stop.

8 Disconnect the disk drive cable and re-install the disk drive in the logic analyzer.

9 Reconnect the disk drive cable and install the cover on the logic analyzer.

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To test the hard disk drive voltages

Refer to chapter 6, "Replacing Assemblies," for instructions to remove or replace covers and assemblies.

WARNING

This procedure is to be performed by service-trained personnel aware of the hazards involved, such as fire and electrical shock.

Equipment Required

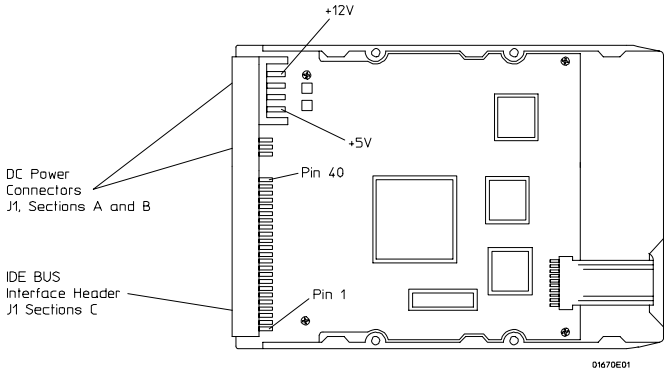
Equipment	Critical Specification	Recommended Model/Part
Digitizing Oscilloscope	> 100 MHz Bandwidth	HP 54600A

1. Turn off the instrument, then remove the power cable. Remove the instrument cover and the disk drive assembly.
2. Remove the hard disk drive from the disk drive assembly. Reconnect both hard disk drive cables to the rear of the disk drive. Turn the disk drive over so that the solder connections of the cable socket are accessible.
3. Connect the power cable, then turn on the instrument.
4. In the Sys PV menu select the Disk test. Select Run-Repetitive.
5. Check for the following voltages and signals using an oscilloscope.

Disk Drive Voltages

Pin No.	Signal	Voltage	Pin No.	Signal	Voltage	Pin No.	Signal	Voltage
1	RESET		27	IORDY		34	PDIAG	
3 - 18	DATA		28	CABLE SELECT		35	DAO	
20	KEYPIN		29	DMACK		36	ADDR2	
21	DMARQ		31	INTRQ		37	CS1FX	
23	DIOW		32	IOCS16		38	CS3FX	
25	DIOR		33	ADDR1		39	DASP	

Pins 2, 19, 22, 24, 26, 30, 40 are GROUND



6. Select Stop, and turn off the logic analyzer. Remove the power cable.

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The test will not immediately stop when Stop is selected; it will continue until the current iteration of the disk test is completed and then stop.

7 Disconnect the disk drive cables. Re-install the hard disk drive onto the disk drive assembly, and then re-install the disk drive assembly in the logic analyzer.

8 Reconnect the disk drive cables and install the cover on the logic analyzer.

To perform the BNC test

Equipment Required

Equipment	Critical Specification	Recommended Model/Part
Digitizing Oscilloscope	100 MHz Bandwidth	HP 54600B
BNC Shorting Cap		1250-0074
BNC Cable		HP 10503A
BNC-Banana Adapter		1251-2277

1 Press the Config key.

2 Assign pods 1 and 2 to Machine 1.

To assign the pod field, select the pods 1 and 2 field, then select Machine 1 in the pop-up menu.

3 In the Analyzer 1 box, select the Type field. Select Timing in the pop-up menu.

4 Set up the trigger menu.

a Press the Trig key. Select Clear Trigger All.

b Select Arming Control. In the Arming Control pop-up menu, select the field labeled Run, then select Port In. Press the Done key.

5 Attach a BNC shorting cap to the External Trigger Input on the rear panel of the logic analyzer.

6 Using a BNC cable, connect the External Trigger Output to the oscilloscope channel 1 input. Set the oscilloscope to Trigger On and measure TTL voltage levels.

7 Press the RUN front panel key.

The warning "MACHINE 1 Waiting on level 1" will appear.

8 Remove the shorting cap from the rear panel External Trigger input BNC.

9 The warning will go away and the oscilloscope will display a positive-going TTL pulse.

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To test the logic analyzer probe cables

This test allows you to functionally verify the probe cable and probe tip assembly of any of the logic analyzer pods. Only one probe cable can be tested at a time. Repeat this test for each probe cable to be tested.

Equipment Required

Equipment	Critical Specification	Recommended Model/Part
Pulse Generator	100 MHz, 3.5 ns pulse width, < 600 ps rise time	HP 8131A Option 020
Adapter (Qty 4)	SMA (m) - BNC (f)	HP 1250-1200
Coupler (Qty 4)	BNC (m)(m)	HP 1250-0216
6x2 Test Connectors (Qty 4)		

1 Turn on the equipment required and the logic analyzer.

2 Set up the pulse generator according to the following table.

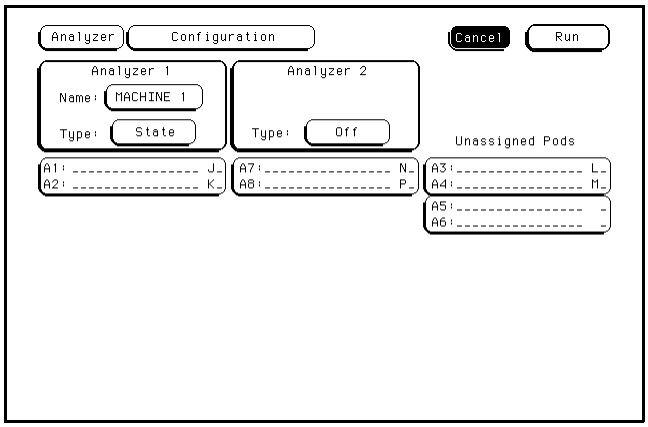
Pulse Generator Setup

Timebase	Channel 2	Period	Channel 1
Mode: Int	Mode: Pulse	Divide: Divide ÷ 1	Mode: Pulse
Period: 20.000 ns	Divide: PULSE ÷ 1	Ampl: 0.50 V	Delay: 0.000 ns
	Width: 3.500 ns	Offs: 0.00 V	Width: 3.500 ns
	High: –0.90 V		High: –0.90 V
	Low: –1.70 V		Low: –1.70 V
	COMP: Disabled (LED Off)		COMP: Disabled (LED Off)

3 Set up the logic analyzer Configuration menu.

a Press the Config key.

b In the Analyzer 1 box, select the field to the right of Type, then select State.

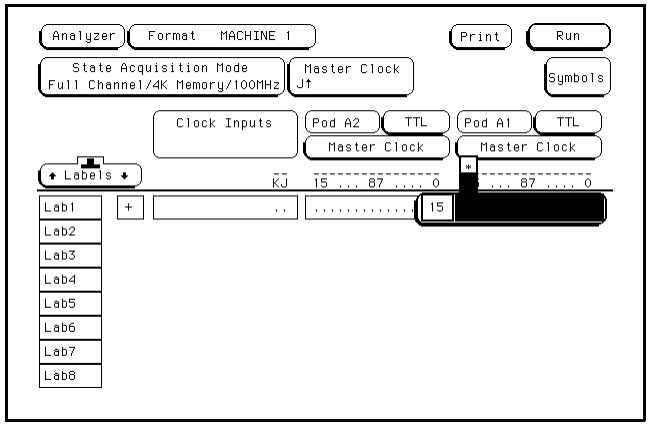


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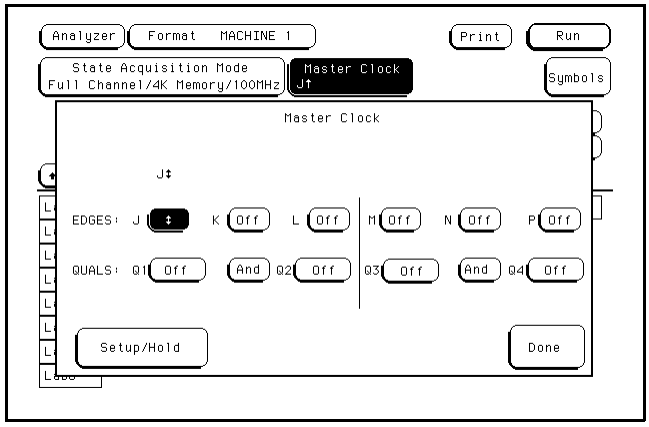
4 Set up the Format menu.

a Press the Format key.

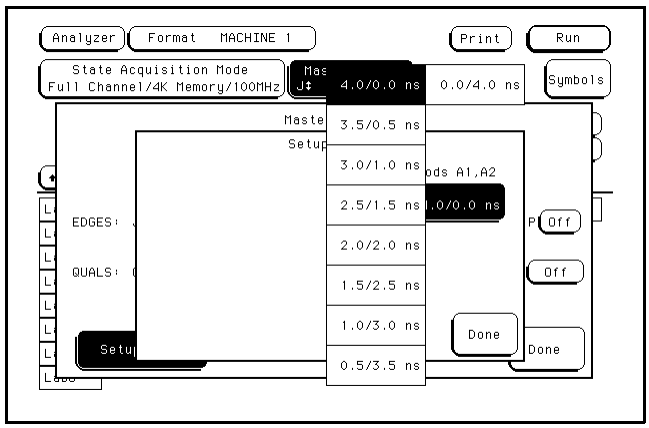
b Move the cursor to the field showing the channel assignments for the pod under test. Press the Clear Entry key until the pod channels are all assigned (all asterisks (*)). Press the Done key.



c Select Master Clock, then select a double edge for the clock of the pod under test. Turn off the other clocks.

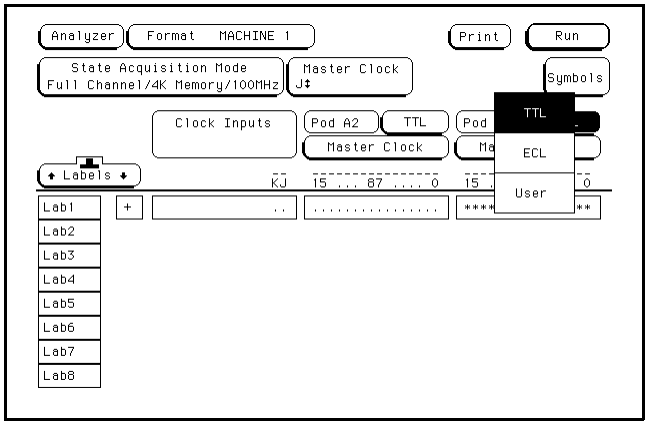


d In the Master Clock menu, select Setup/Hold, then select 4.0/0.0 ns for the pod being tested. Select Done. Select Done again to exit the Master Clock menu.



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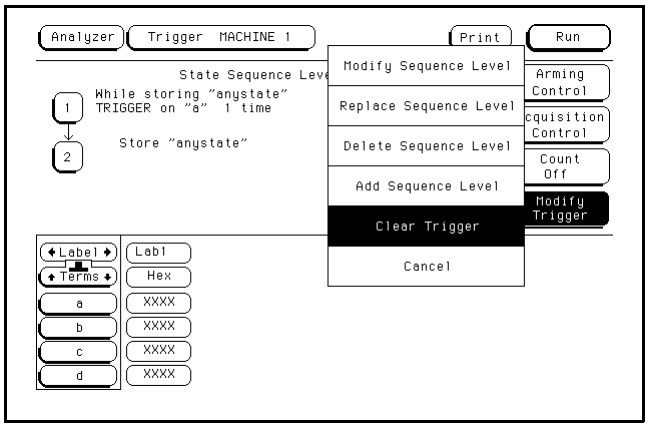
e Select the field to the right of the pod being tested, then select TTL.



5 Set up the Trigger menu.

a Press the Trigger key.

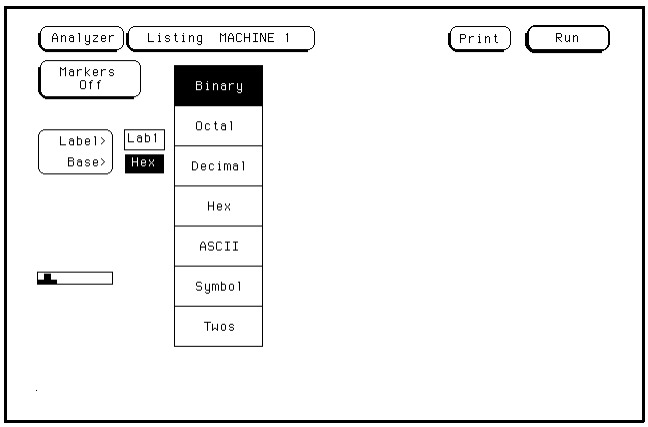
b Select Modify Trigger, then select Clear Trigger, then select All.



6 Set up the Listing menu.

a Press the List key.

b Select the field to the right of Base, then select Binary.



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7 Using four 6-by-2 test connectors, four BNC Couplers, and four SMA (m) - BNC (f) Adapters, connect the logic analyzer to the pulse generator channel outputs. To make the test connectors, see chapter 3, "Testing Performance."

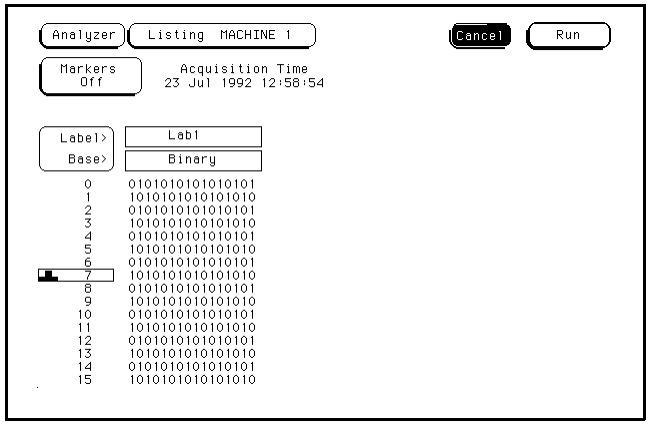
a Connect the even-numbered channels of the lower byte of the pod under test to the pulse generator channel 1 Output and J-clock.

b Connect the odd-numbered channels of the lower byte of the pod under test to the pulse generator channel 1 $\overline{\text{Output}}$.

c Connect the even-numbered channels of the upper byte of the pod under test and the clock channel to the pulse generator channel 2 Output.

d Connect the odd-numbered channels of the upper byte of the pod under test to the pulse generator channel 2 $\overline{\text{Output}}$.

8 On the logic analyzer, press Run. The display should look similar to the figure below.



9 If the display looks like the figure, then the cable passed the test.

If the display does not look similar to the figure, then there is a possible problem with the cable or probe tip assembly. Causes for cable test failures include the following:

- open channel
- channel shorted to a neighboring channel
- channel shorted to either ground or a supply voltage

Return to the troubleshooting flowchart.

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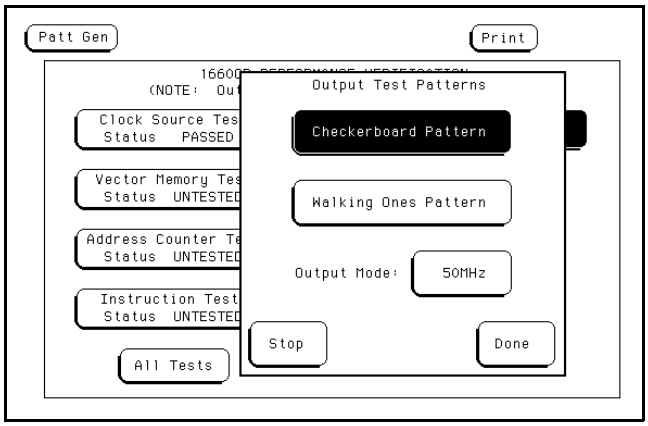
To verify pattern output (HP 1660CP-Series only)

Equipment Required

Equipment	Critical Specification	Recommended Model/Part
Oscilloscope	≥ 500 MHz Bandwidth	HP 54522A
Probe	500 MHz Bandwidth	HP 10441A
Output Data Pod	no substitute	10460A - series

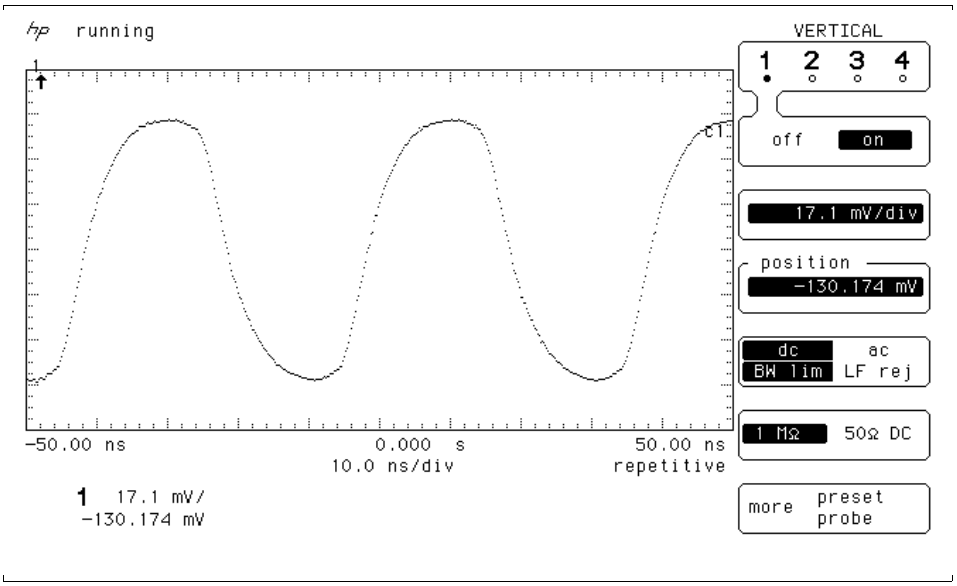
1 Connect one of the 10460-series data pods to the end of the pattern generator Pod 1 cable.

2 Touch Output Patterns. In the pop-up menu, touch Checkerboard Pattern.



3 Using an oscilloscope, verify the existence of logic-level transitions by touching the oscilloscope probe to each channel of Data Pod 1 and doing an Autoscale. The signal levels that appear on the oscilloscope display should correspond with the logic levels represented by the 10460-series pod being used.

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4 Repeat step 3 for each of the remaining four data pods.

5 Connect one of the 10460-series clock pods to the end of the pattern generator clock cable.

6 Using the oscilloscope as in step 3, verify the existence of logic-level transitions by touching the oscilloscope probe to each clock output of the clock pod.

7 In the pattern generator Output Patterns menu, touch Stop, then touch Done to exit the menu.

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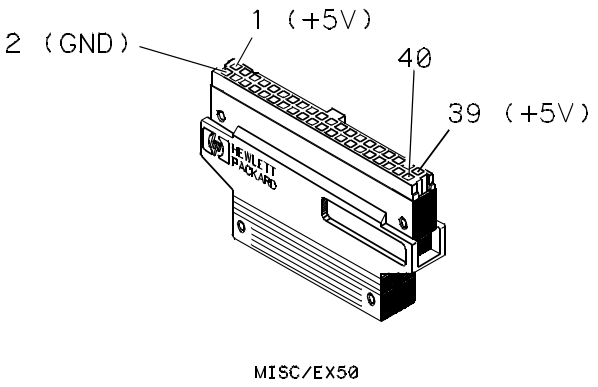
To test the auxiliary power

The +5 V auxiliary power is protected by a current overload protection device. If the current on pins 1 and 39 exceed 0.33 amps, the circuit will open. When the short is removed, the circuit will reset in approximately 1 minute. There should be +5 V after the 1 minute reset time.

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part
Digital Multimeter	0.1 mV resolution, better than 0.005% accuracy	HP 3478A

- Using the multimeter, verify the +5 V on pins 1 and 39 of the probe cables.



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6

To remove and replace the
- Handle 6–5
- Feet and tilt stand 6–5
- Cover 6–5
- Disk drive assembly 6–6
- Power supply 6–7
- CPU board 6–7
- SIMM memory 6–8
- Switch actuator assembly 6–9
- Rear panel assembly 6–10
- HP 1660C-series acquisition board 6–11
- HP 1660CS-series oscilloscope board 6–12
- HP 1660CP-series pattern generator board 6–13
- Front panel and keyboard 6–14
- Intensity adjustment 6–14
- Monitor 6–15
- Handle plate 6–15
- Fan 6–16
- Line filter 6–16
- HP 1660CP-series pattern generator cables 6–17
- HP-IB and RS-232-C cables 6–17
- I/O board 6–18

To return assemblies 6–18

Replacing Assemblies

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Replacing Assemblies

This chapter contains the instructions for removing and replacing the assemblies of the logic analyzer. Also in this chapter are instructions for returning assemblies.

WARNING

Hazardous voltages exist on the power supply, the CRT, and the CRT driver board. To avoid electrical shock, disconnect the power from the instrument before performing the following procedures. After disconnecting the power, wait at least three minutes for the capacitors on the power supply board and the CRT driver board to discharge before servicing the instrument.

CAUTION

Damage can occur to electronic components if you remove or replace assemblies when the instrument is on or when the power cable is connected. Never attempt to remove or install any assembly with the instrument on or with the power cable connected.

Replacement Strategy

These replacement procedures are organized as if disassembling the complete instrument, from the first assembly to be removed to the last. Some procedures say to remove other assemblies of the instrument, but do not give complete instructions. Refer to the procedure for that specific assembly for the instructions. Use the exploded view of the instrument on the next page as a reference during the replacement procedures.

CAUTION

Electrostatic discharge can damage electronic components. Use grounded wriststraps and mats when performing any service to this logic analyzer.

Tools Required

#10 TORX screwdriver
#15 TORX screwdriver
#1 Posidrive screwdriver
3/16 inch (5 mm) nut driver
9/32 inch (7 mm) nut driver
5/8 inch (16 mm) nut driver (HP 1660CS series only)

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Exploded View

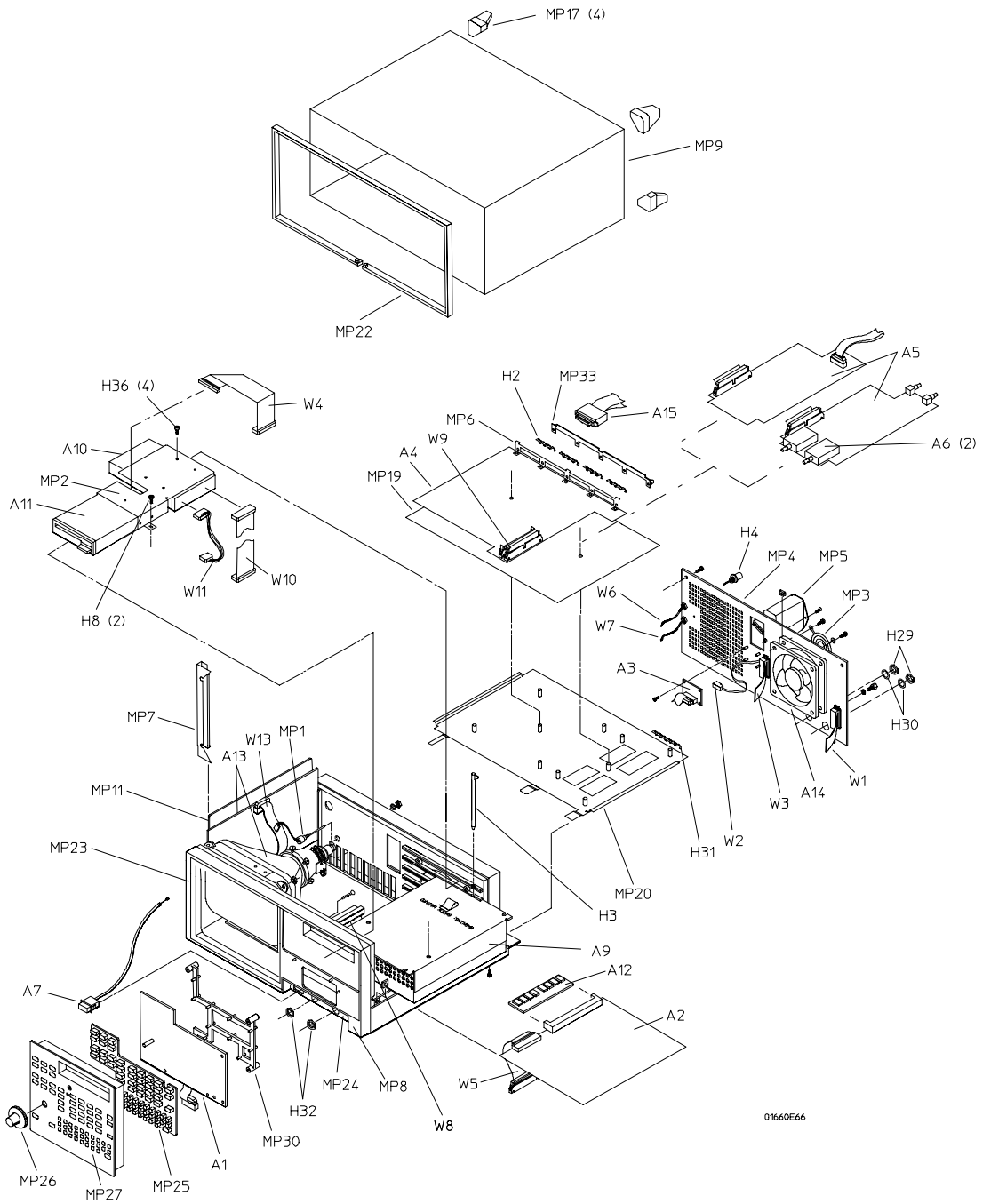
Listing

A1	Keyboard	MP1	Intensity adjustment	W1	HP-IB cable
A2	CPU board	MP2	Disk drive bracket	W2	Fan cable
A3	I/O Board	MP3	Fan guard	W3	RS-232-C cable
A4	Acquisition board	MP4	Rear panel	W4	Flexible disk drive cable
A5	Oscilloscope board *	MP5	Line filter	W5	Cable-60 conductor
A5	Pattern Generator board*	MP6	Ground bracket	W6	Jumper cable-orange
A6	Attenuator **	MP7	Ground bracket	W7	Jumper cable-white
A7	Switch actuator	MP8	Cabinet	W8	Power supply cable
A9	Power supply	MP11	Handle plate	W9	Cable - 60-conductor *
A10	Hard disk drive	MP19	Insulator	W10	Hard disk drive data cable
A11	Flexible disk drive	MP20	Mounting plate	W11	Hard disk drive power cable
A12	SIMM	MP23	Label	W12	I/O Board Cable
A13	Monitor assembly	MP24	Label	W13	Sweep cables
A14	Fan	MP25	Elastomeric keypad		
H3	Locking pin	MP26	RPG knob		
H4	BNC connector	MP27	Keyboard panel		
H29	Hex nut **	MP29	Front panel spacer		
H30	Lock washer **	MP30	Keyboard spacer		
H32	Hex nut **				

* The HP 1660CP series has a pattern generator board, and the HP 1660CS series has an oscilloscope board.

** HP 1660CS series only

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Exploded View of the HP 1660C

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To remove and replace the handle

- Remove the two screws in the endcaps, then lift off the handle.

To remove and replace the feet and tilt stand

1. Remove the screws connecting the four rear feet to the instrument.
2. Separate the rear feet from the instrument to remove them.
3. Press the locking tab on the bottom feet, then remove them.
4. Remove the tilt stand from the bottom front feet by lifting the stand up and out of the foot.
5. Reverse this procedure to install the feet and tilt stand.

To remove and replace the cover

1. Turn off the power and unplug the logic analyzer.
2. Remove the probe plate and disconnect the logic analyzer cables from the rear panel.
3. Using the previous procedures, remove the handle and the four rear feet.
4. Remove the seven screws from the front molding, then slide the molding forward to remove it.
5. Remove the cover.

   To remove the cover, set the instrument upright and facing toward you. Slide the chassis toward the front, out of the cover, and set it on a static-safe work area.
6. Reverse this procedure to install the cover.

   Check that all assemblies are properly installed before installing the cover.

   When installing the chassis in the cover, check that the tabs located at the bottom, rear of the cover align with the holes in the rear panel.

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To remove and replace the disk drive assembly

1. Using previous procedures, remove the following assemblies:
   - Handle
   - Rear Feet
   - Cover
2. Disconnect the two disk drive ribbon cables from the rear of both disk drives. Peel the cables away from the double-sided tape used to secure the cables to the disk drive bracket.
3. Disconnect the power cable from the rear of the hard disk drive.
4. Remove the two screws that attach the disk drive bracket to the power supply.
5. Slide the disk drive assembly toward the front of the instrument about 1/2 in. (1.25 cm). Angle the rear of the bracket up and out of the chassis, then remove the disk drive assembly completely out of the chassis by sliding the assembly toward the rear of the instrument.
6. To remove the flexible disk drive from the bracket, remove the four screws that attach the flexible drive to the bracket, two on each side.
7. To remove the hard disk drive, remove the four screws on top of the bracket that attach the hard drive to the bracket. If a new hard disk drive is being installed, then two rubber feet must be installed on the hard drive between the hard drive and the power supply.
8. Reverse this procedure to install the disk drive assembly.

   Check that the following assemblies are properly installed before installing the disk drive:
   - Monitor
   - Front Panel
   - Switch Actuator
   - CPU Board
   - Power Supply

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To remove and replace the power supply

1 Using previous procedures, remove the following assemblies:

- Handle
- Rear Feet
- Cover
- Disk Drive Assembly

WARNING

Hazardous voltages exist on the power supply. To avoid electrical shock, disconnect the power from the instrument before performing the following procedures. After disconnecting the power, wait at least three minutes for the capacitors to discharge before continuing.

2 Lift the PCB locking pins out of the chassis.

3 Slide the power supply out far enough to reach the power supply cables, then disconnect them from the power supply.

4 Slide the power supply the rest of the way out the side of the instrument.

5 Reverse this procedure to install the power supply.

Check that the following assemblies are properly installed before installing the power supply:

- Monitor
- Front Panel
- Switch Actuator
- CPU Board

To remove and replace the CPU board

1 Using previous procedures, remove the following assemblies:

- Handle
- Rear Feet
- Cover
- Disk Drive Assembly
- Power Supply

2 Disconnect the CPU board interface cable from the acquisition board by pressing down on the cable release tabs on the cable socket located on the acquisition board.

3 Disconnect the HP-IB and Input/Output cables from the CPU board.

4 Disconnect the front panel cable from the CPU board.

5 Disconnect the I\O board cable from the CPU board.

6 Slide the board out the side of the instrument.

7 Reverse this procedure to install the CPU board.

Check that the following assemblies are properly installed before installing the CPU board:

- Monitor
- Front Panel
- Switch Actuator

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To remove and replace SIMM memory

1 Using previous procedures, remove the following assemblies:

- Handle
- Rear Feet
- Cover
- Disk Drive Assembly
- Power Supply
- CPU Board

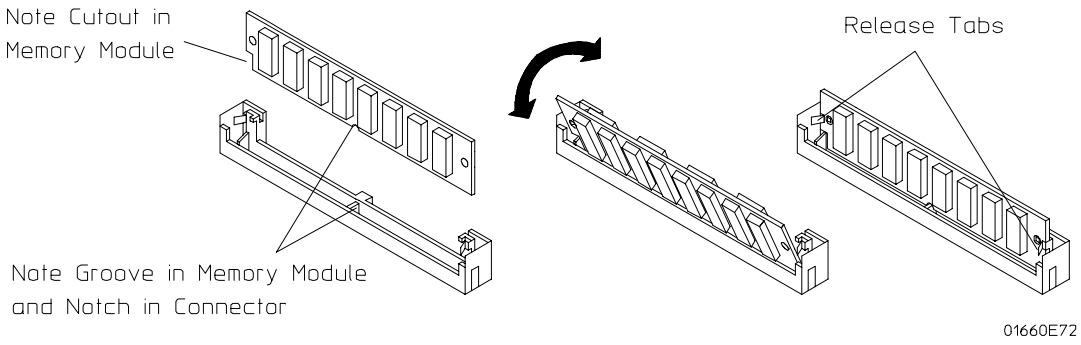
WARNING

Hazardous voltages exist on the power supply. To avoid electrical shock, disconnect the power from the instrument before performing the following procedures. After disconnecting the power, wait at least three minutes for the capacitors to discharge before servicing the instrument.

2 Hold the release tabs away from the SIMM (single inline memory module), then pull the module out.

3 Reverse this procedure to install a replacement SIMM.

Slide the SIMM module into the connector at an angle, then push it down parallel to the CPU board.



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To remove and replace the switch actuator assembly

1 Using previous procedures, remove the following assemblies:

- Handle
- Rear Feet
- Cover
- Disk Drive Assembly
- Power Supply
- CPU Board

2 Make sure the power switch is in the off position.

3 Disconnect the switch actuator from the line filter.

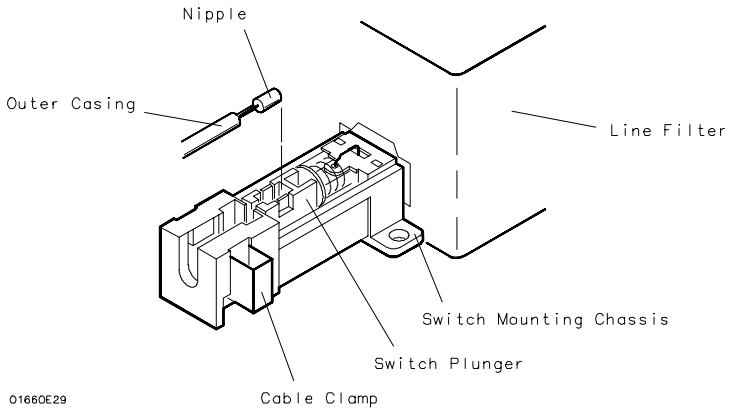
a Slide the clamp off of the outer casing far enough to release the switch actuator assembly.

CAUTION

If the wire in the switch actuator is bent, the complete assembly must be replaced. Refer to chapter 7, "Replaceable Parts" for the part number.

b Without bending the wire, gently pry the nipple out of the switch plunger.

c Slide the cable out of the switch assembly.



4 Remove the switch actuator assembly from the front of the cabinet.

To remove, depress the retaining ears on both sides of the assembly next to the front panel and push the assembly out the front.

5 Install the new switch actuator assembly. Make sure that the line filter switch is in the off position.

a Route the cable through the front panel, then snap the pushbutton into the front panel.

b Snap the nipple into the switch plunger.

c Position the free end of the outer casing into the switch mounting chassis. The edge of the outer casing should be all the way against the inner edge of the switch mounting chassis.

d Close the clamp by pushing it into the switch assembly until the clamp is seated.

6 Verify the push-on, push-off action of the assembly.

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To remove and replace the rear panel assembly

1. Using previous procedures, remove the following assemblies:
   - Handle
   - Rear Feet
   - Cover
   - Disk Drive Assembly
   - Power Supply
2. Remove the switch actuator cable from the line filter according to "To remove and replace the switch actuator assembly."
3. Disconnect the BNC In/Out and fan cables on the acquisition board.
4. Disconnect the RS-232-C and HP-IB cables from the CPU board.
5. Disconnect the I/O cable from the I/O board on the rear panel.
   a. For the HP 1660CS-series Logic Analyzers, remove the hex nut and lock washer from both BNC Cal ports.
   b. For the HP 1660CP-series Logic Analyzers, disconnect the pattern generator cable from the pattern generator board.
6. Remove the six rear panel screws.
7. Lift the rear panel away from the chassis.
8. Reverse this procedure to install the rear panel.

   Check that the following assemblies are properly installed before installing the rear panel:
   - Monitor
   - Acquisition Board
   - Oscilloscope Board (HP 1660CS-series only)
   - Pattern Generator Board (HP 1660CP-series only)

   When installing the rear panel, check that the alignment tabs on the acquisition board are lined up with the corresponding holes in the rear panel. Also, for the HP 1660CP-series Logic Analyzers ensure the ground springs are installed on the acquisition board and on the pattern generator board before installing the rear panel.

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To remove and replace the HP 1660C-series acquisition board

1. Using previous procedures, remove the following assemblies:
   - Handle
   - Rear Feet
   - Cover
   - Rear Panel
   - Disk Drive Assembly
   - Power Supply
2. Disconnect the sweep cable from acquisition board.
3. Disconnect the CPU board interface cable by pressing down on the cable release tabs on the cable socket located on the board.
4. Disconnect the power supply cable.
5. Slide the mounting plate out the rear of the instrument.

   Verify that the cable release tabs are down to slide the mounting plate out, then slide the mounting plate toward the rear out of the chassis.
6. Separate the acquisition board from the mounting plate by removing the screw at the center of the board.
7. Reverse this procedure to install the acquisition board.

   Check that the following assemblies are properly installed before installing the acquisition board:
   - Monitor

   When installing the mounting plate, check that the alignment tabs on the mounting plate are installed in the alignment holes in the inside bottom, front of the chassis.

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To remove and replace the HP 1660CS-series oscilloscope board

1. Using previous procedures, remove the following assemblies:
   - Handle
   - Rear Feet
   - Cover
   - Rear Panel
   - Disk Drive Assembly
   - Power Supply
2. Disconnect the sweep cable from acquisition board.
3. Disconnect the CPU board interface cable by pressing down on the cable release tabs on the cable socket located on the board.
4. Disconnect the power supply cable.
5. Remove the hex nut from the oscilloscope input attenuators on the lower front panel.
6. Slide the mounting plate out the rear of the instrument.

   Verify that the cable release tabs are down to slide the mounting plate out, then slide the mounting plate toward the rear out of the chassis.
7. Separate the oscilloscope board from the mounting plate by removing the screw at the center of the board. Remove the oscilloscope-to-acquisition board cable.
8. Remove the attenuators from the oscilloscope board by removing the mounting screws (two per attenuator) from the underside of the board. Then carefully lift the attenuator straight off of the board.
9. Reverse this procedure to install the oscilloscope board.

   Ensure that the monitor is properly installed before installing the oscilloscope board.

   When installing the mounting plate, check that the alignment tabs on the mounting plate are installed in the alignment holes in the inside bottom, front of the chassis.

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To remove and replace the HP 1660CP-series pattern generator board

1. Using previous procedures, remove the following assemblies:
   - Handle
   - Rear Feet
   - Cover
   - Rear Panel
   - Disk Drive Assembly
   - Power Supply
2. Disconnect the sweep cable from acquisition board.
3. Disconnect the CPU board interface cable by pressing down on the cable release tabs on the cable socket located on the board.
4. Disconnect the power supply cable.
5. Slide the mounting plate out the rear of the instrument.

   Verify that the cable release tabs are down to slide the mounting plate out, then slide the mounting plate toward the rear out of the chassis.
6. Separate the pattern generator board from the mounting plate by removing the screw at the center of the board. Remove the pattern generator-to-acquisition board cable.
7. Reverse this procedure to install the pattern generator board.

   Ensure that the monitor is properly installed before installing the pattern generator board.

   When installing the mounting plate, check that the alignment tabs on the mounting plate are installed in the alignment holes in the inside bottom, front of the chassis.

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To remove and replace the front panel and keyboard

1. Using previous procedures, remove the following assemblies:
   - Handle
   - Rear Feet
   - Cover
   - Disk Drive Assembly
   - Power Supply
   - CPU Board
2. Remove the four screws connecting the front panel.
3. Slide the front panel assembly out the front of the instrument.
4. Slide the spacers out the front of the instrument to remove them.

   Be careful not to lose the copper ground strips on the spacer.

   When installing the spacer, insert the pins of the spacer in the appropriate holes in the chassis. You can hold the spacer in place while installing the front panel by holding it with your finger through the disk drive mounting slot in the chassis.
5. Remove the RPG knob by pulling the knob off the RPG shaft.
6. Disassemble the front panel assembly by lifting the keyboard circuit board away from the front panel.
7. Lift the elastomeric keypad out of the front panel.
8. Reverse this procedure to assemble and install the front panel assembly.

   When assembling the front panel, check that the holes in the elastomeric keypad and the keyboard circuit board align with the pins on the front panel.

To remove and replace the intensity adjustment

1. Using previous procedures, remove the following assemblies:
   - Handle
   - Rear Feet
   - Cover
   - Disk Drive Assembly
   - Power Supply
   - Rear Panel
2. Disconnect the intensity adjustment cable from the CRT driver board.
3. Using a nut driver, remove the hex nut attaching the intensity adjustment to the chassis.
4. Slide the intensity adjustment assembly toward the front and up out of the instrument.
5. Reverse this procedure to install the intensity adjustment.

   When installing the intensity adjustment, check that the keying tab on the adjustment aligns with the keying hole in the chassis.

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To remove and replace the monitor

1 Using previous procedures, remove the following assemblies:

- Handle
- Rear Feet
- Cover
- Disk Drive Assembly
- Power Supply
- CPU Board
- Rear Panel
- Acquisition Board
- Oscilloscope Board (HP 1660CS-series only)
- Pattern Generator Board (HP 1660CP-series only)
- Intensity Adjustment

WARNING

Hazardous voltages exist on the CRT and the CRT driver board. To avoid electrical shock, disconnect the power from the instrument before performing the following procedures. After disconnecting the power, wait at least three minutes for the capacitors to discharge before servicing the instrument.

2 Disconnect the cable from the rear of the CRT.

3 Disconnect the yoke cable from the CRT driver board.

4 Disconnect the high voltage lead from the bell of the CRT.

5 Slide the CRT driver board up out of the chassis.

6 Using a nut driver, remove the three hex nuts attaching the monitor and ground bracket to the chassis, then remove the screw.

7 Slide the monitor assembly and ground bracket to the rear and up out of the chassis.

8 Reverse this procedure to install the monitor.

When installing the CRT driver board, check that the board is properly inserted in the circuit board tracks.

To remove and replace the handle plate

1 Using previous procedures, remove the following assemblies:

- Handle
- Rear Feet
- Cover

2 Remove the four screens that attach the handle plate to the chassis.

3 Remove the handle plate.

To remove the handle plate, align the plate toward the front of the instrument, then move it up and out of the instrument.

4 Reverse this procedure to install the handle plate.

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To remove and replace the fan

1 Using previous procedures, remove the following assemblies:

- Handle
- Rear Feet
- Cover
- Disk Drive Assembly
- Power Supply
- Rear Panel

2 Remove the four fan screws.

3 Lift the fan away from the rear panel.

4 Lift the fan guard away from the rear panel.

5 Reverse this procedure to install the fan.

When installing the fan, verify the correct orientation of the fan. If you mount the fan backwards, the instrument will overheat. Also, check the correct polarity of the fan cable.

To remove and replace the line filter

1 Using previous procedures, remove the following assemblies:

- Handle
- Rear Feet
- Cover
- Disk Drive Assembly
- Power Supply
- Rear Panel

2 Unsolder the ground wire from the lug on the rear panel.

3 Disconnect the line filter cable from the power supply.

4 Remove the two screws attaching the line filter to the rear panel.

5 Slide the line filter assembly out toward the rear.

6 Reverse this procedure to install the line filter.

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To remove and replace the HP 1660CP-series pattern generator cables

1. Using previous procedures, remove the following assemblies:
   - Handle
   - Rear Feet
   - Cover
   - Disk Drive Assembly
   - Power Supply
   - CPU Board
2. Remove the two screws securing the pattern generator cable clamp to the rear panel and remove the cable clamp.
3. Disconnect the faulty cable from the pattern generator board and feed the cable through the rear panel.
4. Reverse this procedure to install the replacement cable.

To remove and replace the HP-IB and RS-232-C cables

1. Using previous procedures, remove the following assemblies:
   - Handle
   - Rear Feet
   - Cover
   - Disk Drive Assembly
   - Power Supply
   - Rear Panel
2. Remove the two hex standoffs connecting the HP-IB cable, then slide the HP-IB cable forward and out of the rear panel.
3. Remove the two hex standoffs connecting the RS-232-C cable, then slide the RS-232-C cable forward and out of the rear panel.
4. Reverse this procedure to install the HP-IB and RS-232-C cables.

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To remove and replace the I/O board

1. Using previous procedures, remove the following assemblies:
   - Handle
   - Rear Feet
   - Cover
   - Disk Drive Assembly
   - Power Supply
   - Rear Panel
2. Remove the two jackscrews that attach the parallel printer (Centronics) port to the rear panel.
3. Remove four screws that secure the I/O board to the rear panel.
4. If LAN capability was not factory installed in an instrument and is being added to the instrument, then the cover plate must be removed from the rear panel. Remove two screws that secure the cover plate to the rear panel, and remove the cover plate.
5. Reverse this procedure to install the I/O board onto the rear panel.

To return assemblies

Before shipping the logic analyzer or assemblies to Hewlett-Packard, contact your nearest Hewlett-Packard Sales Office for additional details.

1. Write the following information on a tag and attach it to the part to be returned.
   - Name and address of owner
   - Model number
   - Serial number
   - Description of service required or failure indications
2. Remove accessories from the logic analyzer.

   Only return accessories to Hewlett-Packard if they are associated with the failure symptoms.
3. Package the logic analyzer.

   You can use either the original shipping containers, or order materials from an HP Sales Office.

CAUTION For protection against electrostatic discharge, package the logic analyzer in electrostatic material.

4. Seal the shipping container securely, and mark it FRAGILE.

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Replaceable Parts

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Replaceable Parts

This chapter contains information for identifying and ordering replaceable parts for your logic analyzer.

Replaceable Parts Ordering

Parts listed

To order a part on the list of replaceable parts, quote the Hewlett-Packard part number, indicate the quantity desired, and address the order to the nearest Hewlett-Packard Sales Office.

Parts not listed

To order a part not on the list of replaceable parts, include the model number and serial number of the module, a description of the part (including its function), and the number of parts required. Address the order to your nearest Hewlett-Packard Sales Office.

Direct mail order system

To order using the direct mail order system, contact your nearest Hewlett-Packard Sales Office.

Within the USA, Hewlett-Packard can supply parts through a direct mail order system. The advantages to the system are direct ordering and shipment from the HP Part Center in Mountain View, California. There is no maximum or minimum on any mail order. (There is a minimum amount for parts ordered through a local Hewlett-Packard Sales Office when the orders require billing and invoicing.) Transportation costs are prepaid (there is a small handling charge for each order) and no invoices.

In order for Hewlett-Packard to provide these advantages, a check or money order must accompany each order. Mail order forms and specific ordering information are available through your local Hewlett-Packard Sales Office. Addresses and telephone numbers are located in a separate document at the back of the service guide.

Exchange Assemblies

Some assemblies are part of an exchange program with Hewlett-Packard.

The exchange program allows you to exchange a faulty assembly with one that has been repaired and performance verified by Hewlett-Packard.

After you receive the exchange assembly, return the defective assembly to Hewlett-Packard. A United States customer has 30 days to return the defective assembly. If you do not return the defective assembly within the 30 days, Hewlett-Packard will charge you an additional amount. This amount is the difference in price between a new assembly and that of the exchange assembly. For orders not originating in the United States, contact your nearest Hewlett-Packard Sales Office for information.

See Also "To return assemblies" in chapter 6.

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Replaceable Parts List

The replaceable parts list is organized by reference designation and shows exchange assemblies, electrical assemblies, then other parts.

The exploded view does not show all of the parts in the replaceable parts list.

Information included for each part on the list consists of the following:

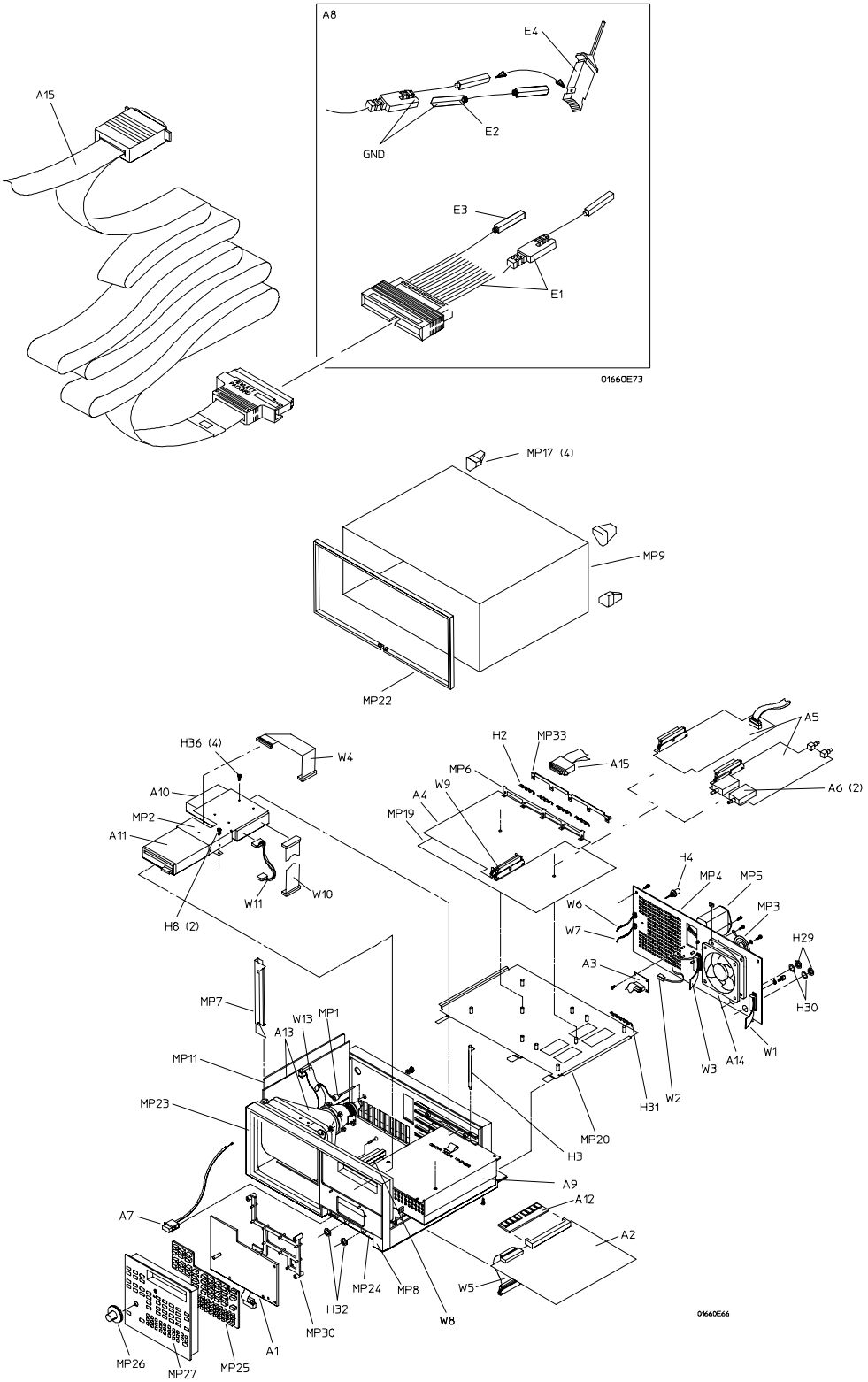
- Reference designator
- Hewlett-Packard part number
- Total quantity included with the instrument (Qty)
- Description of the part

Reference designators used in the parts list are as follows:

- A Assembly
- E Miscellaneous Electrical Part
- F Fuse
- H Hardware
- MP Mechanical Part
- W Cable

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Exploded View



Exploded view of the HP 1660 logic analyzer.

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HP 1660 Series Replaceable Parts

Ref. Des.	HP Part Number	QTY	Description
			Exchange Board Assembly
	01660-69528		Exchange Board Assembly - CPU
	01660-69517		Exchange Board Assembly-ACQ 128 CH (HP 1660C/CS/CP)
	01660-69518		Exchange Board Assembly-ACQ 96 CH (HP 1661C/CS/CP)
	01660-69519		Exchange Board Assembly-ACQ 64 CH (HP 1662C/CS/CP)
	01660-69521		Exchange Board Assembly-ACQ 32 CH (HP 1663C/CS/CP)
	01660-69520		Exchange Board Assembly-Oscilloscope (HP 1660CS-series only)
	01660-69526		Exchange Board Assembly-Pattern Generator (HP 1660CP-series only)
			HP 1660 Series
A1	01660-66502	1	Board assembly-keyboard
A2	01660-66528	1	Board assembly - CPU
A3	01660-66515	1	Board Assembly - I/O
A3	01660-66516	1	Board Assembly - I/O (required with LAN option)
A4	01660-66517	1	Board assembly-ACQ 128 CH (HP 1660C/CS/CP)
A4	01660-66518	1	Board assembly-ACQ 96 CH (HP 1661C/CS/CP)
A4	01660-66519	1	Board assembly-ACQ 64 CH (HP 1662C/CS/CP)
A4	01660-66521	1	Board assembly-ACQ 32 CH (HP 1663C/CS/CP)
A5	01660-66520	1	Board Assembly-Oscilloscope (HP 1660CS-series only)
A5	01660-66526	1	Board Assembly-Pattern Generator (HP 1660CP-series only)
A6	54512-63402	2	Attenuator (HP 1660CS-series only)
A7	01660-61901	1	Switch Actuator
A8	01650-61608	4	Probe tip assembly (HP 1660C/CS/CP)
A8	01650-61608	3	Probe tip assembly (HP 1661C/CS/CP)
A8	01650-61608	2	Probe tip assembly (HP 1662C/CS/CP)
A8	01650-61608	1	Probe tip assembly (HP 1663C/CS/CP)
A9	0950-2261	1	Power supply
A10	0950-2740	1	Hard Disk Drive
A11	5042-1713	1	Flexible Disk drive
A12	1818-5624	1	1024K x 32 SIMM (factory default)
A12	1818-5623	1	2048K x 32 SIMM (required with LAN option)
A13	2090-0304	1	Monitor assembly
A14	3160-1013	1	Fan-tubeaxial
A15	16550-61605	4	Probe cable (HP 1660C/CS/CP)
A15	16550-61605	3	Probe cable (HP 1661C/CS/CP)
A15	16550-61605	2	Probe cable (HP 1662C/CS/CP)
A15	16550-61605	1	Probe cable (HP 1663C/CS/CP)
A16	A2839B	1	Mouse
E1	5959-9333		Replacement probe leads (5 per package)
E2	5959-9334		Replacement probe grounds (5 per package)
E3	5959-9335		Replacement pod ground (2 per package)
E4	5090-4356		Grabber kit assembly (20 grabbers per package)
F1	2110-0003	1	Fuse, 250V, 3A, non-time-delay
H1	1400-0611	1	Clamp-cable
H2	01660-09101	5	Ground spring (HP 1660CP)
H2	01660-09101	4	Ground spring (HP 1660C/CS)
H2	01660-09101	3	Ground spring (HP 1661C/CS/CP)
H2	01660-09101	2	Ground spring (HP 1662C/CS/CP)
H2	01660-09101	1	Ground spring (HP 1663C/CS/CP)
H3	01650-46101	2	Locking pin PCB
H4	01660-67601	2	BNC connector assembly
H5	6960-0149	2	Plug-D hole 0.500" (HP 1660C-series only)
H8	0515-1363	10	MS 3.0 5 TH T10 (flexible disk drive, disk drive assembly, handle plate)
H10	0515-0430	12	MS M3 .0X0 .5X6MM PH T10 (acquisition board, rear panel to chassis, oscilloscope board on the HP 1660CS series, I/O board to rear panel)
H11	0515-2349	5	MS M3.0 X 0.50 - 14MM LG (trim strip cover to cabinet)
H12	0515-1035	2	MSFH M3 8 T10 (line filter)

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HP 1660 Series Replaceable Parts

Ref. Des.	HP Part Number	QTY	Description
H13	0515-1103	2	MSFH M3 10 T10 (trim strip cover to cabinet)
H14	0515-0664	4	MSPH M3 12 SMS10 (rear feet to cabinet)
H15	2950-0072	1	NUTH 1/4-32 .062 (intensity adjustment)
H16	2950-0001	2	NUTH 3/8-32 .093 (BNC trigger ports)
H17	0535-0056	3	NUT-HEX (monitor assembly)
H20	0515-0382	3	SM assembly M4 X 0.7 12MM-LG (monitor assembly, handle)
H21	0515-1349	4	SM M3 X 0.5 30MM-LG (front panel assembly)
H22	0380-1482	2	STDF-HEX .34-IN (HP-IB cable)
H23	3050-0010	4	WFL.147 .312 .03 (rear feet)
H24	2190-0009	2	WIL.168 .340 .02 (HP-IB cable)
H25	2190-0027	1	WIL.256 .478 .02 (intensity adjustment)
H26	2190-0016	2	WIL.377 .507 .02 (BNC connectors)
H28	0515-1031	4	MSF M3 6 T10 (accessory pouch)
H29	2950-0054	2	NUTH 1/2-28 .125 (BNC cal ports, HP 1660CS series only)
H30	2190-0068	2	WIL .505 .630 .02 (BNC cal ports, HP 1660CS series only)
H31	01650-29101	1	Ground Spring (HP 1660CS series only)
H32	54503-25701	2	Hex Nut (attenuator, HP 1660CS series only)
H33	0515-1246	4	MS M3 x 0.5 T10 (attenuator, HP 1660CS series only)
H34	0403-0179	2	Bumper-adhesive back (hard disk drive)
H35	0380-1858	4	Jackscrew with lock (RS-232, Centronics port to rear panel)
H36	2360-0462	4	MSPH 6-32 .25in (hard disk drive)
MP1	01660-61606	1	Intensity adjustment assembly
MP2	01660-01208	1	Bracket-disk drive
MP3	3160-0092	1	Fan guard
MP4	01660-00202	1	Rear panel
MP5	54501-62702	1	Line filter assembly
MP6	01660-01205	1	Ground bracket
MP7	01650-01202	1	Ground bracket
MP8	01660-60001	1	Cabinet assembly
MP9	01660-04102	1	Cover assembly
MP10	01660-44901	1	Handle vinyl grip
MP11	01660-01202	1	Handle plate
MP13	35672-21703	2	Strap retainer
MP14	35672-45004	2	Handle end cap
MP15	5041-8801	2	Foot
MP16	1460-1345	2	Tilt stand
MP17	01660-40501	4	Rear foot
MP18	5041-8822	2	Non-skid foot
MP19	01660-45401	1	Circuit board insulator
MP20	01660-01201	1	Circuit board mounting plate
MP21	01660-84501	1	Accessory pouch
MP22	01660-40502	1	Trim strip
MP23	01660-94312	1	ID label (HP 1660C)
MP23	01661-94303	1	ID label (HP 1661C)
MP23	01662-94303	1	ID label (HP 1662C)
MP23	01663-94303	1	ID label (HP 1663C)
MP23	01660-94313	1	ID label (HP 1660CS)
MP23	01661-94304	1	ID label (HP 1661CS)
MP23	01662-94304	1	ID label (HP 1662CS)
MP23	01663-94304	1	ID label (HP 1663CS)
MP23	01660-94316	1	ID label (HP 1660CP)
MP23	01661-94317	1	ID label (HP 1661CP)
MP23	01662-94318	1	ID label (HP 1662CP)
MP23	01663-94319	1	ID label (HP 1663CP)
MP24	01660-94302	1	Line switch label (HP 1660C series only)
MP24	01660-94307	1	Line switch label (HP 1660CS series only)
MP25	01660-41901	1	Elastomeric keypad (HP 1660C series only)
MP25	01660-41902	1	Elastomeric keypad (HP 1660CS series only)
MP26	01660-47401	1	RPG knob
MP27	01660-60002	1	Assembled keyboard panel and label
	01660-94303	0	Keyboard label-replacement
	01660-45201	0	Keyboard panel-replacement

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HP 1660 Series Replaceable Parts

Ref. Des.	HP Part Number	QTY	Description
MP29	01660-44703	1	Front panel spacer
MP30	01660-44702	1	Keyboard spacer
MP33	01660-04101	1	Probe mounting plate (HP 1660C/CS/CP)
MP33	01661-04101	1	Probe mounting plate (HP 1661C/CS/CP)
MP33	01662-04101	1	Probe mounting plate (HP 1662C/CS/CP)
MP33	01663-04101	1	Probe mounting plate (HP 1663C/CS/CP)
MP34	01660-04105	1	Cover Plate (1660C-series only)
MP35	01660-94304		Label-pods and cable
MP36	0361-1272	4	Plastic Push Fastener
MP37	1252-2218	2	20 pos. clip retainer (sweep cable)
MP38	1252-2220	1	34 pos. clip retainer (flexible disk to CPU board)
MP39	8160-0780	1	Ground spring (acquisition board cable connectors)
MP40	01660-61201	1	Cable Clamp (HP 1660CP-series only)
W1	01650-61613	1	HP-IB cable
W2	01660-61613	1	Fan cable
W3	01660-61601	1	RS-232-C cable
W4	01660-61614	1	Flexible disk drive cable
W5	01660-61604	1	Cable - 60 Conductor
W6	01660-61607	1	Jumper cable assembly-orange
W7	01660-61608	1	Jumper cable assembly-wht
W8	54503-61606	1	Power supply cable
W9	01660-61604	1	Cable - 60 Conductor (HP 1660CS and 1660CP series only)
W10	01660-61609		Hard disk drive data cable
W11	01660-61610		Hard disk drive power cable
W12	01660-61611		I/O board cable
W13	01650-61601		Sweep cable (monitor assembly)
W14	16542-61607		Double probe adapter
W15	8120-1521	1	Power cord - United States (7.5 ft)
W15	8120-1703	1	Power cord (Option 900-UK)
W15	8120-0696	1	Power cord (Option 901-Austl)
W15	8120-1692	1	Power cord (Option 902-Eur)
W15	8120-2296	1	Power cord (Option 906-Swit)
W15	8120-2957	1	Power cord (Option 912-Den)
W15	8120-4600	1	Power cord (Option 917-Africa)
W15	8120-4754	1	Power cord (Option 918-Japan)
			Pattern Generator
W16	16522-61601	4	Output Cable (HP 1660CP-series only)
W17	16522-61602	1	Pattern Generator Clock Cable (HP 1660CP-series only)

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Power Cables and Plug Configurations

This instrument is equipped with a three-wire power cable. The type of power cable plug shipped with the instrument depends on the country of destination. The W15 reference designators (table, previous page) show option numbers of available power cables and plug configurations.

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Theory of Operation

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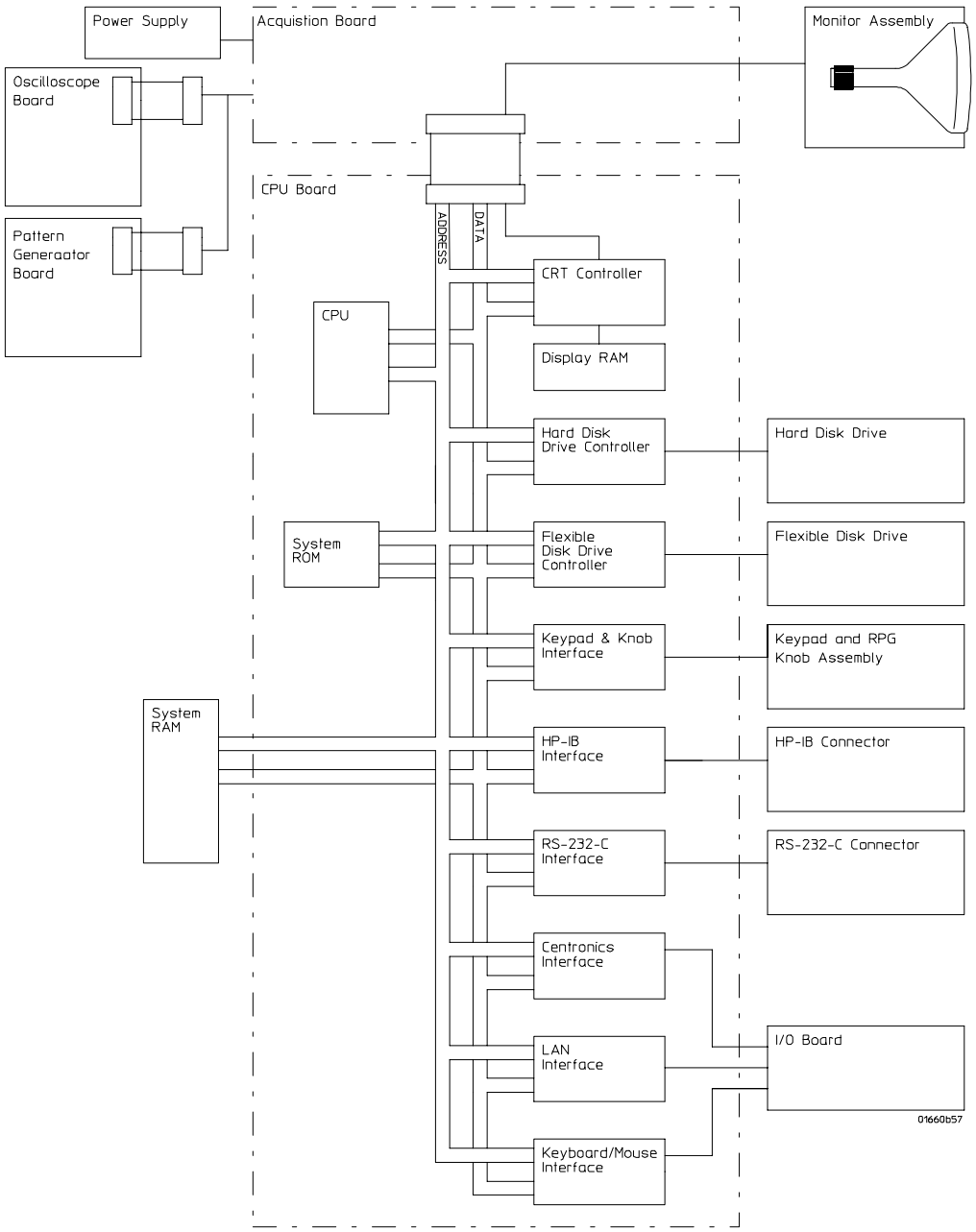
Theory of Operation

This chapter tells the theory of operation for the logic analyzer and describes the self-tests. The information in this chapter is to help you understand how the logic analyzer operates and what the self-tests are testing. This information is not intended for component-level repair.

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The block-level theory is divided into two parts: theory for the logic analyzer and theory for the acquisition boards. A block diagram is shown with each theory.

The HP 1660C/CS/CP Series Logic Analyzer



The HP 1660C/CS/CP Logic Analyzer

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HP 1660C/CS/CP Series Theory

CPU Board

The microprocessor is a Motorola 68EC020 running at 25 MHz. The microprocessor controls all of the functions of the logic analyzer including processing and storing data, displaying data, and configuring the acquisition ICs to obtain and store data.

System Memory

The system memory is made up of both read-only memory (ROM) and random access memory (RAM). Two types of ROM are used. A single 128Kx8 EPROM is used as a boot ROM, and four 512Kx8 Flash ROMS are configured to provide a 512Kx32 Flash ROM space. One SIMM socket supports 2-MB, 4-MB, or 8-MB SIMM.

On power-up, instructions in the boot ROM command the instrument to execute its boot routine. The boot routine includes power-up operation verification of the instrument subsystems and entering the operating system. The CPU searches for the operating system on Flash ROM. Then, if the operating system is in Flash ROM, the instrument will be initialized with the default configuration and await front panel instructions from you. If the operating system is not in Flash ROM, the CPU accesses the disk drives to see if the operating system is on the disks.

The DRAM stores the instrument configuration, acquired data to be processed, and any inverse assembler loaded in the instrument by the user.

CRT Controller and Display RAM

A Brooktree BT475 RAMDAC color palette and a National Semiconductor LM1882CM video frame generator control the CRT. One of the RGB outputs of the color palette provides the eight-shade gray scale display. The video frame generator provides the horizontal and vertical synchronization timing signals.

The display RAM is a 256Kx8 video RAM and stores all of the pixel information used by the color palette. A serial address counter and an address multiplexer control the DRAM addressing. At the conclusion of each video frame the vertical sync signal from the video generator resets the serial address counter and a new frame is generated.

Disk Drive Controller

The disk drive controller consists of a single floppy drive controller IC. The floppy drive controller provides all signals to the disk drive including read and write data, read and write signals, write gate, and step signal. The floppy drive controller also reads status signals from the disk drive, including a track 00 signal, disk ready, and disk change signal.

Keypad and Knob Interface

The front panel keypad is scanned directly from the microprocessor address bus during the video blanking cycle of the CRT. When a front panel key is pressed the associated address bits are fed to the data bus through the pressed key and read by the microprocessor.

The rotary pulse generator (RPG) knob is part of the PS2 circuitry. Pulses and direction of rotation information are directed to an RPG interface IC and then to the PS2 loop. The microprocessor then reads and interprets the RPG signals and performs the desired tasks.

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HP-IB Interface

The instrument interfaces to HP-IB as defined by IEEE Standard 488.2. The interface consists of an HP-IB controller and two octal drivers/receivers. The microprocessor routes HP-IB data to the controller. The controller then buffers the 8-bit HP-IB data bits and generates the bus handshaking signals. The data and handshaking signals are then routed to the HP-IB bus through the octal line drivers/receivers. The drivers/receivers provide data and control signal transfer between the bus and controller.

RS-232-C Interface

The instrument RS-232-C interface is compatible with standard RS-232-C protocol. The interface consists of a controller and drivers/receivers. The controller serializes parallel data from the microprocessor for transmission. At the same time the controller also receives serial data and converts the data to parallel data characters for the microprocessor.

The controller contains a baud rate generator that can be programmed from the logic analyzer front panel for one of eight baud rates. Other RS-232-C communications parameters can also be programmed from the logic analyzer front panel.

The drivers/receivers interface the instrument with data communications equipment. Slew rate control is provided on the ICs eliminating the need for external capacitors.

CRT Monitor Assembly

The CRT Monitor Assembly consists of a monochrome CRT and a monitor driver board. The monitor driver board provides the biasing and control signals for the CRT. Pixel information is stored in the display RAM on the CPU board and is routed to the monitor driver board through the acquisition board and the sweep cable.

Flexible Disk Drive

The disk drive assembly is a high density disk drive that formats double-sided, double-density or high density disks in LIF or DOS format. A disk drive controller on the CPU board controls the disk drive. Signals are routed directly to the disk drive through the disk drive cable.

Power Supply

A low voltage power supply provides all DC voltages needed to operate the logic analyzer. The power supply also provides the +5 Vdc voltage to the probe cables to power logic analyzer accessories and preprocessors.

Unfiltered voltages of +12 V, -12 V, +5 V, -5.2 V, and +3.5 V are supplied to the acquisition board where they are filtered and distributed to the CPU board, CRT Monitor Assembly, and probe cables.

LAN Interface

The LAN interface is primarily a single LAN integrated circuit with supporting components. Isolation circuitry for the LAN port is included on the I/O board. The LAN interface circuitry is enabled only on the HP 1660C/CS-series products with LAN option installed. The 1660CP-series comes standard with the LAN interface.

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Keyboard/Mouse Interface

An 82C42PC PS2 controller makes up the PS2 Keyboard/Mouse interface. The PS2 controller interfaces the logic analyzer backplane with the keyboard and/or mouse devices.

I/O Board

The Input/Output (I/O) Board primarily includes a Centronics port and two mini-DIN (PS/2) ports for the HP 1660C/CS/CP-series products. On products ordered with the LAN interface, the I/O board also includes isolation circuitry and LAN connectors for the LAN.

Hard Disk Drive Interface

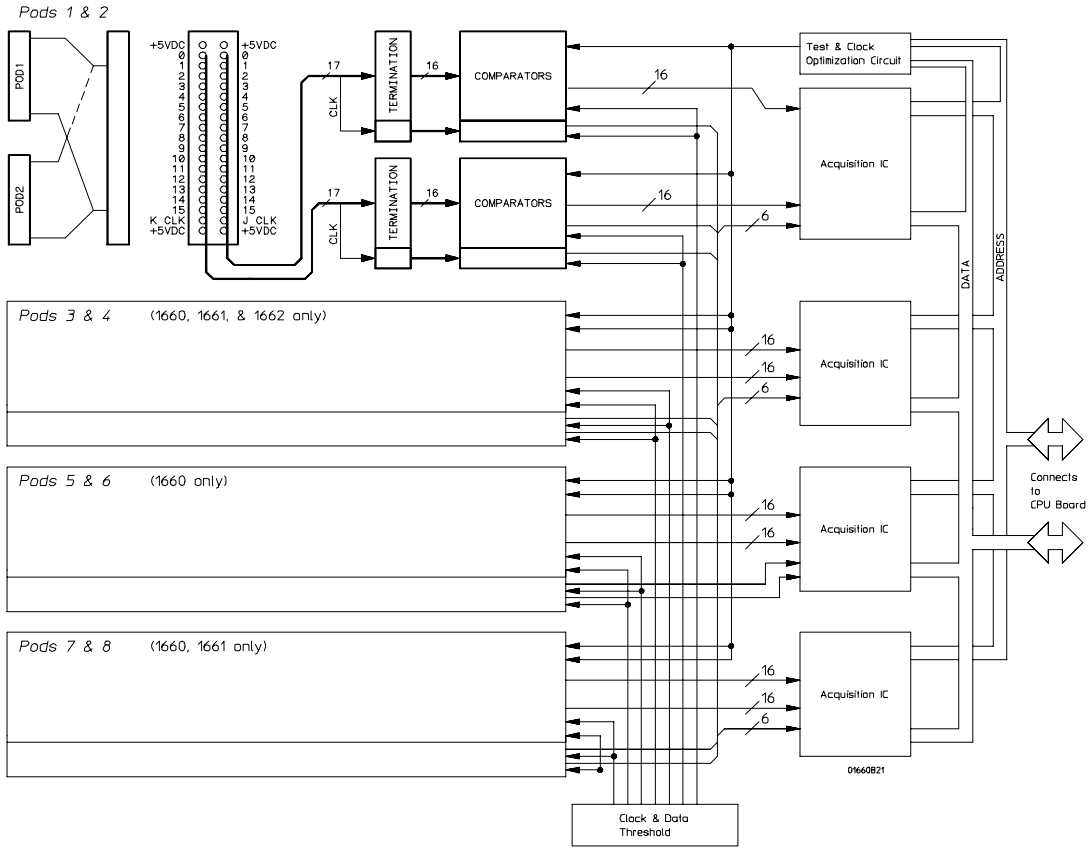
Buffers interface the hard disk drive with the logic analyzer backplane.

Hard Disk Drive

The Hard Disk Drive is an IDE-compatible disk drive. A 40-pin IDE connector allows the disk drive to interface with the logic analyzer backplane through the hard disk drive interface.

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The Logic Acquisition Board



The Logic Acquisition Board

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Logic Acquisition Board Theory

Probing

The probing circuit includes the probe cable and terminations. The probe cable consists of two 17-channel pods which are connected to the circuit board using a high-density connector. Sixteen single-ended data channels and one single-ended clock/data channel are passed to the circuit board per pod.

If the clock/data channel is not used as a state clock in state acquisition mode, it is available as a data channel. The clock/data channel is also available as a data channel in timing acquisition mode. Eight (HP 1660C/CS/CP), six (HP 1661C/CS/CP), four (HP 1662C/CS/CP), or two (1663C/CS/CP) clock/data channels are available as data channels, however only six clock/data channels can be assigned as clock channels in the HP 1660C/CS/CP and HP 1661C/CS/CP. All clock data channels available in the HP 1662C/CS/CP and HP 1663C/CS/CP can be assigned as clock channels.

The cables use nichrome wire woven in polyarmid yarn for reliability and durability. The pods also include one ground path per channel in addition to a pod ground. The channel grounds are configured such that their electrical distance is the same as the electrical distance of the channel.

The probe tip assemblies and termination modules connected at the end of the probe cables have a divide-by-10 RC network that reduces the amplitude of the data signals as seen by the circuit board. This adds flexibility to the types of signals the circuit board can read in addition to improving signal integrity.

The terminations on the circuit board are resistive terminations that reduce transmission line effects on the cable. The terminations also improve signal integrity to the comparators by matching the impedance of the probe cable channels with the impedance of the signal paths of the circuit board. All 17 channels of each pod are terminated in the same way. The signals are reduced by a factor of 10.

Comparators

Two proprietary 9-channel comparators per pod interpret the incoming data and clock signals as either high or low depending on where the user-programmable threshold is set. The threshold voltage of each pod is individually programmed, and the voltage selected applies to the clock channel as well as the data channels of each pod.

Each of the comparator ICs has a serial test input port used for testing purposes. A test bit pattern is sent from the Test and Clock Synchronization Circuit to the comparator. The comparators then propagate the test signal on each of the nine channels of the comparator. Consequently, all data and clock channel pipelines on the circuit board can be tested by the operating system software from the comparator.

Acquisition

The acquisition circuit is made up of a single HP proprietary ASIC. Each ASIC is a 34-channel state/timing analyzer, and one such ASIC is included for every two logic analyzer pods. All of the sequencing, pattern/range recognition, and event counting functions are performed on board the IC.

In addition to the storage qualification and counting functions, the acquisition ASICs also perform master clocking functions. All six state acquisition clocks are fed to each IC, and the ICs generate their own sample clocks. Every time you select RUN, the ICs individually perform a clock optimization before data is stored.

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Clock optimization involves using programmable delays on board the IC to position the master clock transition where valid data is captured. This procedure greatly reduces the effects of channel-to-channel skew and other propagation delays.

In the timing acquisition mode, an oscillator-driven clock circuit provides a four-phase, 100-MHz clock signal to each of the acquisition ICs. For high speed timing acquisition (100 MHz and faster), the sample period is determined by the four-phase, 100-MHz clock signal.

For slower sample rates, one of the acquisition ICs divides the 100-MHz clock signal to the appropriate sample rate. The sample clock is then fed to all acquisition ICs.

Threshold

A precision octal DAC and precision op amp drivers make up the threshold circuit. Each of the eight channels of the DAC is individually programmable which allows you to set the thresholds of the individual pods. The 16 data channels and the clock channel of each pod are all set to the same threshold voltage.

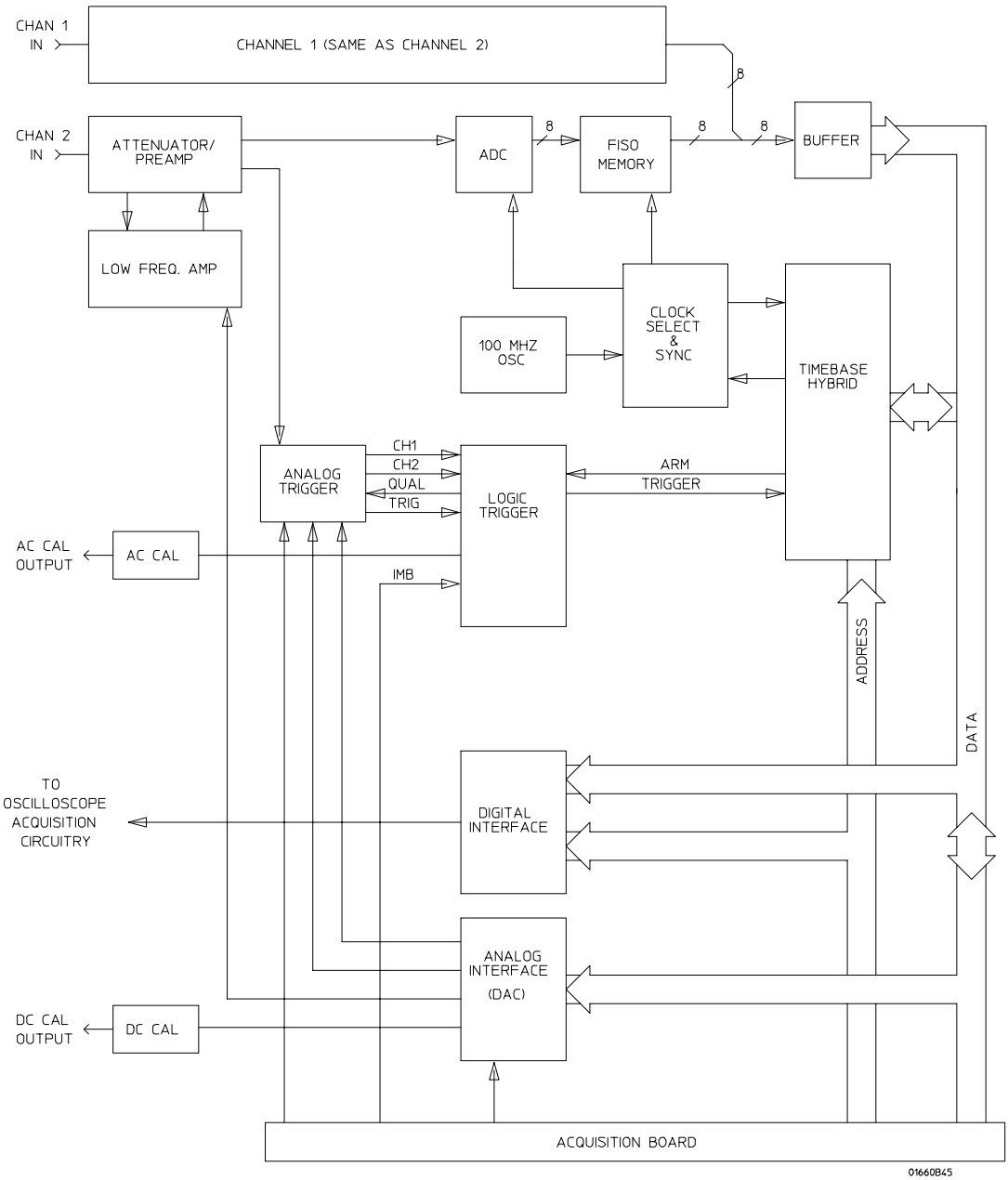
Test and Clock Synchronization Circuit

ECLinPS (TM) ICs are used in the Test and Clock Synchronization Circuit for reliability and low channel-to-channel skew. Test patterns are generated and sent to the comparators during software operation verification. The test patterns are propagated across all data and clock channels and read by the acquisition ASIC to ensure both the data and clock pipelines are operating correctly.

The Test and Clock Synchronization Circuit also generates a four-phase, 100-MHz sample/synchronization signal for the acquisition ICs operating in the timing acquisition mode. The synchronizing signal keeps the internal clocking of the individual acquisition ASICs locked in step with the other ASICs at fast sample rates. At slower sample rates, one of the acquisition ICs divides the 100-MHz clock signal to the appropriate sample rate. The slow speed sample clock is then used by all acquisition ICs.

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The Oscilloscope Board



The Oscilloscope Board

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Oscilloscope Board Theory (HP 1660CS series only)

Attenuator/Preamp Theory of Operation

The channel signals are conditioned by the attenuator/preamps, thick film hybrids containing passive attenuators, impedance converters, and a programmable amplifier. The channel sensitivity defaults to the standard 1-2-4 sequence (other sensitivities can be set also). However, the firmware uses passive attenuation of 1, 5, 25, and 125, with the programmable preamp, to cover the entire sensitivity range.

The input has a selectable 1 MΩ input impedance with ac or dc coupling or a 50Ω input impedance with dc coupling. Compensation for the passive attenuators is laser trimmed and is not adjustable. After the passive attenuators, the signal is split into high-frequency and low-frequency components. Low frequency components are amplified on the main assembly, where they are combined with the offset voltage. The ac coupling is implemented in the low frequency amplifier.

The high- and low-frequency components of the signal are recombined and applied to the input FET of the preamp. The FET provides a high input impedance for the preamp. The programmable preamp adjusts the gain to suit the required sensitivity and provides the output signal to the main assembly. The output signal is then sent to both the trigger circuitry and ADC.

Oscilloscope Acquisition

The acquisition circuitry provides the sampling, digitizing, and storing of the signals from the channel attenuators. The channels are identical. Trigger signals from each channel and the external triggers synchronize acquisition through the time base circuitry. A 100 MHz oscillator and a time base provide system timing and sample clocking. A voltage-controlled oscillator (VCO), frequency divider, and digital phase detector provide the sample clock for higher sample rates. After conditioning and sampling, the signals are digitized, then stored in a hybrid IC containing a FISO (fast in, slow out) memory.

ADC The eight-bit ADC digitizes the channel signal. Digitization is done by comparators in a flash converter. The sample clock latches the digitized value of the input to save it so that it can be sent to memory.

FISO Memory 8000 samples of the FISO (fast in, slow out) memory are used per measurement per channel. Memory positions are not addressed directly. The configuration is a ring which loops continuously as it is clocked. Memory position is tracked by counting clocks. The clocking rate is the same as the ADC, however the clock frequency is half that of the ADC since the FISO clocks on both transitions of the clock period. Data is buffered onto the CPU data bus for processing.

Triggering There are two main trigger circuits that control four trigger sources. The two trigger circuits are the analog trigger and the logic trigger. The analog trigger IC operates as a multichannel Schmidt trigger/comparator. A trigger signal (a copy of the analog input signal) from each of the inputs is directed to the analog trigger IC inputs. The trigger signal is continuously compared with the trigger reference level selected by the user. Once the trigger condition is met, the trigger TRUE signal is fed to the logic trigger, which begins the acquisition and store functions by way of the time base.

The four trigger sources are Channel 1, Channel 2, Intermodule Bus (IMB), and external BNC. The operation of the input channels was discussed previously. The IMB trigger signal is sent directly to the logic trigger. External triggering is provided by the BNC input of the HP 1660C/CS-series Logic Analyzer.

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Time Base The time base provides the sample clocks and timing necessary for data acquisition. It consists of the 100 MHz reference oscillator and time base hybrid.

The 100 MHz reference oscillator provides the base sample frequency.

The time base hybrid has programmable dividers to provide the rest of the sample frequencies appropriate for the time range selected. The time base uses the time-stretched output of the fine interpolator to time-reference the sampling to the trigger point. The time base has counters to control how much data is taken before (pre-trigger data) and after (post-trigger data) the trigger event. After the desired number of pre-trigger samples has occurred, the Time base hybrid sends a signal to the Logic Trigger (trigger arm) indicating it is ready for the trigger event. When the trigger condition is satisfied, the Logic Trigger sends a signal back to the time base hybrid. The time base hybrid then starts the post-trigger delay counter.

When the countdown reaches zero, the sample clocks are stopped and the CPU is signaled that the acquisition is complete. The Fine Interpolator is a dual-slope integrator that acts as a time-interval stretcher. When the logic trigger receives a signal that meets the programmed triggering requirements, it signals the time base. The time base then sends a pulse to the fine interpolator. The pulse is equal in width to the time between the trigger and the next sample clock. The fine interpolator stretches this time by a factor of approximately 500. Meanwhile, the time base hybrid runs a counter with a clock derived from the sample rate oscillator. When the interpolator indicates the stretch is complete, the counter is stopped. The count represents, with much higher accuracy, the time between the trigger and the first sample clock. The count is stored and used to place the recently acquired data in relationship with previous data.

AC Cal The AC Cal is a multiplexer circuit that can provide several signals to the Probe Compensation/AC Calibrator output on the rear panel. The signal provided depends on the mode of the instrument. It can be either a probe compensation signal, a pulse representing the trigger event, signals used for self-calibration, or the 100 MHz reference oscillator when sample period is 1 ns.

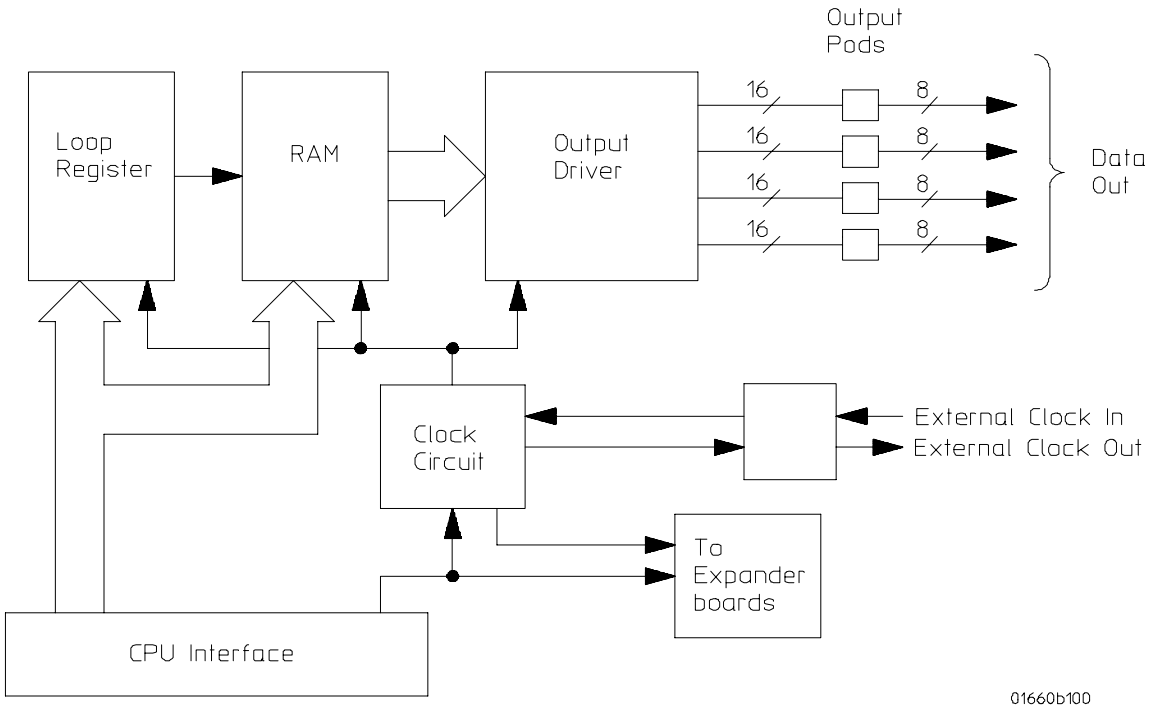
DC Cal The DC Cal output, a rear panel signal, is used for self-calibration. It is one output from the 16-channel DAC.

Digital Interface The Digital Interface provides control and interface between the system control and digital functions in the acquisition circuitry.

Analog Interface The Analog Interface provides control of analog functions in the acquisition circuitry. It is primarily a 16-channel DAC with an accurate reference and filters on the outputs. It controls channel offsets and trigger levels, and provides the DC Cal output.

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The Pattern Generator Board



The Pattern Generator Board

Pattern Generator Board Theory (HP 1660CP series only)

Loop Register

The loop register holds the programmable vector flow information. When the pattern generator reaches the end of the vector listing, the loop register is queried for the RAM address location of the next user-programmed vector. In many cases, the next vector address location would be the start of the vector listing. Consequently the vectors would continue to loop from the end of the listing back to the beginning until the user instructs the module to stop.

RAM

Consisting of six 256Kx16 VRAM ICs and RAM addressing circuitry, the RAM stores the desired patterns that appear at the output. The RAM addressing circuitry is merely a counter which addresses the pattern locations in RAM. When the end of the vector listing is reached, the addressing circuitry is loaded from the loop register with the address of the first vector of the listing to provide an uninterrupted vector loop. The RAM output is sent to the Output Driver circuit where the patterns are presented into a logic configuration usable by the output pods.

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Output Driver

The output driver circuit is made up of a series of latch/logic translators and multiplexers. The latch/translators convert the working-level TTL signals to output-level ECL signals for each channel. The ECL-level signals are then directed to the multiplexers.

The multiplexers, one per channel, direct the programmed data patterns to the output channels. The single-ended ECL-level signals are converted to differential signals which are routed to the output cables and to the pods. Note that the differential ECL output signal of the pattern generator module is not suitable to directly drive ECL circuitry.

Clock Circuit

The clock circuit paces the loop register, the RAM address circuitry, and the multiplexers in the output driver according to the desired data rate. A 200 MHz clock source is directed through a divider circuit which provides a 100MHz and 50MHz clock in addition to 200MHz. The 200MHz, 100MHz, 50MHz and external clock signals are routed to a clock select multiplexer. The output of the multiplexer, which represents the user-selected clocking rate, is distributed to the above listed subcircuits on both the master board and all expander boards that are configured with the master board.

The output of the clock select multiplexer is also distributed to an external clock out circuit. The clock signal is routed to a bank of external clock delays, and then to an external clock delay select multiplexer. The output of this multiplexer, which represents the desired clock delay, is directed to the external clock out pin on the clock pod. Consequently, either the internal clock or external clock is redirected to the clock out pin on the clock pod with a user-selected clock delay.

CPU Interface

The CPU interface is a single programmable-logic device which interprets the 1660CP-series CPU logic and translates the logic into signals to drive and program the pattern generator module.

Pod

The Clock or Data Pod converts the differential output ECL signal to the logic levels of interest. Because the output of the pattern generator module cannot directly drive ECL circuitry, the Clock and Data Pod is required to interface the pattern generator with the target system.

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Self-Tests Description

The self-tests identify the correct operation of major functional areas in the logic analyzer. The self-tests are not intended for component-level diagnostics.

Three types of tests are performed on the HP 1660C/CS/CP series logic analyzers: the power-up self-tests, the functional performance verification self-tests, and the parametric performance verification tests.

The power-up self-tests are performed when power is applied to the instrument.

The functional performance verification self-tests are run using a separate operating system, the performance verification (PV) operating system. The PV operating system resides on a separate disk that must be inserted in the disk drive when running the functional performance verification self-tests. The system and analyzer tests are functional performance verification tests.

Parametric performance verification requires the use of external test equipment that generates and monitors test data for the logic analyzer to read. The performance verification procedures in chapter 3 of this service guide make up the parametric performance verification for the logic analyzer. Refer to chapter 3, "Testing Performance," for further information about parametric performance verification.

Power-up Self-Tests

The power-up self-tests are divided into two parts. The first part is the system memory tests and the second part is the microprocessor interrupt test. The system memory tests are performed before the logic analyzer actually displays the power-up self-test screen. Both the system ROM and RAM are tested during power-up. The interrupt test is performed after the power-up self-test screen is displayed.

The following topics describe the power-up self-tests.

ROM Test

The ROM test performs several checksum tests on various read only memory elements, including the system ROM as well as the various software modules present in flash ROM.

Passing the ROM test implies that the microprocessor can access each ROM memory address and that each ROM segment provides checksums that match previously calculated values.

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RAM Test

The RAM test checks the video RAM (VRAM), system dynamic RAM (DRAM), and static RAM memory within the real time clock IC. The microprocessor first performs a write/read in each memory location of the VRAM. At each VRAM memory location a test pattern is written, read, and compared. An inverse test pattern is then written, read, and compared. After verifying correct operation of the VRAM, the System RAM and real time clock RAM are tested in a similar fashion.

Passing the RAM test implies that the microprocessor can access each VRAM memory location and that each VRAM memory location can store a logical "1" or a logical "0." If the VRAM is functioning properly, the logic analyzer can construct a correct, undistorted display. Passing the RAM test also implies that the memory locations of system RAM can be accessed by the microprocessor and the data in RAM is intact, and that the memory locations inside the real time clock IC can store a logical "1" or a logical "0."

Interrupt Test

The Interrupt Test checks the microprocessor interrupt circuitry. With all interrupts disabled from their source, the microprocessor waits for a short period of time to see if any of the interrupt lines are asserted. An asserted interrupt line during the wait period signifies incorrect functioning of the device generating the interrupt or the interrupt circuitry itself. Those interrupts that can be asserted under software control are exercised to verify functionality.

Passing the Interrupt Test implies that the interrupt circuitry is functioning properly. Passing the Interrupt Test also implies that the interrupt generating devices are functioning properly and not generating false interrupts. This means that the microprocessor can execute the operating system code and properly service interrupts generated by pressing a front panel key or receiving an HP-IB or RS-232-C command.

System Tests (System PV)

The system tests are functional performance verification tests. The following describes the system tests:

ROM Test

The ROM test performs several checksum tests on various read only memory elements, including the system ROM as well as the various software modules present in flash ROM.

Passing the ROM test implies that the microprocessor can access each ROM memory address and that each ROM segment provides checksums that match previously calculated values.

RAM Test

The RAM test performs a write/read operation in each memory location in system dynamic RAM (DRAM). The video RAM in the display subsystem and the acquisition RAM in the data acquisition subsystem are not tested as part of the RAM test and are tested elsewhere. At each DRAM memory location, the code that resides at that location is stored in a microprocessor register. A test pattern is then stored at the memory location, read, and compared. An inverse test pattern is then stored, read, and compared. The original code is then restored to the memory location. This continues until all DRAM memory locations have been tested. The static RAM in the real time clock chip is also tested in a similar fashion.

Passing the RAM test implies that all RAM memory locations can be accessed by the microprocessor and that each memory location can store a logical "1" or a logical "0."

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HP-IB Test

The HP-IB test performs a write/read operation to each of the registers of the HP-IB IC. A test pattern is written to each register in the HP-IB IC. The pattern is then read and compared with a known value.

Passing the HP-IB test implies that the read/write registers in the HP-IB IC can store a logical "1" or a logical "0," and that the HP-IB IC is functioning properly. Incoming and outgoing HP-IB information will not be corrupted by the HP-IB IC.

RS-232-C Test

This test checks the basic interface functions of the RS-232-C port. Both internal and external portions of the port circuitry are tested. In order for the RS-232-C test to pass, the RS-232-C loopback connector must be installed on the RS-232-C connector.

PS2 Test

The PS2 test exercises the PS2 interface between the logic analyzer and external keyboard, if an external keyboard is connected. First, a read/write operation is performed to each of the registers of the PS2 IC. A test pattern is written to each memory location, read, and compared with a known value. Second, if an external keyboard is connected to the PS2 port, the keyboard controller that resides in the keyboard is polled by the microprocessor. A test pattern is sent to the keyboard controller and returned to the microprocessor by the keyboard controller. The test pattern is then compared with a known value.

Passing the PS2 test implies that the read/write registers in the PS2 IC can store a logical "1" or a logical "0," and that the PS2 IC is functioning properly. Also, passing the PS2 test implies that the PS2 pathway to the external keyboard is functioning and that the keyboard controller can communicate with the microprocessor in the logic analyzer. Incoming PS2 information from the external keyboard will not be corrupted by the pathway between the keyboard controller and microprocessor.

Disk Test

The disk test verifies the operation of both the flexible disk drive and hard disk drive.

For the flexible disk drive, the disk test exercises the disk controller circuitry by performing a write/read on a disk. Either a LIF formatted disk with 20 sectors available space or DOS formatted disk with 5K available space is required and should be inserted in the disk drive. When the disk test is executed the disk is first checked sector by sector to find any bad sectors. If no bad sectors are found a test file will be created on the disk and test data will be written to the file. The file is then read and the test data compared with known values. The test file is then erased at the conclusion of the test.

For the hard disk drive, the disk test exercises the disk controller that is on the hard disk drive assembly. In addition, the buffers that make up the hard disk drive interface are tested. When the test is executed, the sectors of the hard disk are checked, and then write/read tested like the flexible disk drive.

Passing the disk test implies that the flexible disk controller circuitry in the logic analyzer and the disk read/write circuitry in the flexible disk drive are functioning properly. The flexible disk drive can read and write to a LIF or DOS formatted disk, and the data will not be corrupted by the flexible disk drive circuitry. Passing the disk test also implies that the hard disk drive controller circuitry, interface, and read/write circuitry are functioning properly, and that the data will not be corrupted by the hard disk drive circuitry.

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Perform Test All

Selecting Perform Test All will initiate all of the previous functional verification tests in the order they are listed. The failure of any or all of the tests will be reported in the test menu field of each of the tests. The Perform All Test will not initiate the Front Panel Test or the Display Test.

Front Panel Test

A mock-up of the logic analyzer front panel is displayed on the CRT when the Front Panel Test is initiated. The operator then pushes each front panel button and turns the RPG (rotary pulse generator) knob to toggle the corresponding fields from light to dark on the front panel mock-up. Successively pushing any front panel key will cause the corresponding field to toggle back and forth between light and dark. An exception is the Done key. Pressing the Done key a second time will cause an exit of this test.

The Front Panel Test passes when all of the key fields in the front panel mock-up on the CRT can be toggled by pressing the corresponding front panel key, and the two RPG fields can be toggled by turning the knob. The Front Panel Test is not called when Perform Test All is selected.

Display Test

When initiated, the display test will cause three test screens to be displayed sequentially. The first test screens is a test pattern used to align the CRT. The second two screens verify correct operation of the color palette by displaying first a full bright screen and then a half bright screen.

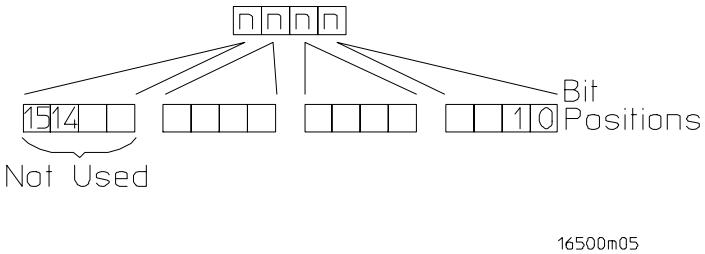
The pass or fail status of the display test is determined by the operator. The Display Test passes when all three test screens are displayed according to chapter 4, "Calibrating and Adjusting." The display test is not used when Perform Test All is selected.

LAN Test

The LAN test verifies the functionality of the LAN circuitry on the logic analyzer CPU board. When you run the LAN Test, the test menu reports a status number. The following figure shows the bit positions of the hexadecimal status reporting word.

A "1" in a bit position signifies that the bit is set and the test failed.

A "0" in a bit position signifies that the bit is not set and the test passed.



Status Reporting Message

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Status Bits

Bit 0	The internal registers of the LAN IC are loaded with known test values and then are read. If this bit is not set, it implies that the LAN IC is operating properly and that the microprocessor can communicate with the LAN IC. If this bit is set, then the LAN module is not operational and must be replaced.
Bit 1	The CAM (Content Addressable Memory) bit reports whether the LAN address can be written from the LAN module Static RAM (SRAM) to the internal memory of the LAN IC. Also, the CAM bit reports whether the LAN address can be written to SRAM from the LAN IC. If this bit is not set, it implies that both the SRAM and the LAN IC internal memory are able to recognize and store the LAN address. If this bit is set, then the LAN module is not operational and must be replaced.
Bit 2	If this bit is not set, then the self-test has detected that the LAN cable is properly connected to the logic analyzer. If this bit is set, then the physical connection of the LAN cable must be checked.
Bit 3	If the Termination bit is set, then the self-test has detected an excessive number of collisions. The most probable cause of excessive collisions is an improperly terminated LAN cable. Provide a proper termination of the LAN cable according to the LAN topology being used.
Bit 4	The MAC (Media Access Control) bit indicates whether the Media Access Control unit on the LAN IC is functioning. If this bit is not set, it implies that both the transmit functions and receive functions of the LAN IC are operating properly. If this bit is set, then the LAN module is not able to properly transmit and receive packets and must be replaced.
Bit 5	The ENDEC (Encoder/Decoder) bit indicates whether the encoder/decoder internal to the LAN IC is functioning. The encoder/decoder is the interface between the MAC and the Ethernet transceiver. If this bit is set, then the ENDEC is not operating properly and the LAN module must be replaced.
Bit 6	The TRANS (Transceiver, such as Ethernet transceiver) bit indicates whether the circuitry between the LAN IC and the LAN cable is functioning. If this bit is not set, then the path between the LAN cable and the LAN IC is operating properly. If this bit is set, then either the CPU board or the I/O board must be replaced.
Bit 7	Timeout bit. If this bit is set, then bits 4, 5, or 6 will also be set. Refer to the appropriate bit for a suggested course of action.
Bit 8	The Tx bit indicates whether the transmission portion of the MAC, ENDEC, or TRANS test failed. Therefore, the Tx bit is used in conjunction with bits 4, 5, and 6. Refer to the appropriate bit for the suggested course of action.
Bit 9	The Rx bit indicates whether the receive portion of the MAC, ENDEC, or TRANS test failed. The Rx bit is used in conjunction with bits 4, 5, and 6. Refer to the appropriate bit for the suggested course of action.
Bit 10	The Parameters bit indicates the integrity of the LAN module self-test parameters. If this bit is not set, then the parameters sent to the self-test routine are correct. If this bit is set, then contact your nearest HP Sales and Service Office.
Bit 11	The E2PROM that is used to hold the Ethernet address, IP address, and gateway address has been corrupted. If this bit is set, the LAN module must be replaced.
Bits 12–15	Not Used

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Analyzer Tests (Analy PV)

The analyzer tests are functional performance verification tests. There are three types of analyzer tests: the Board Test, the Chip Tests, and the Data Input Inspection. The following describes the analyzer self-tests:

Board Test

The Board Test functionally verifies the two oscillators and the 9-channel comparators on the circuit board. First, the oscillators are checked using the event counter on one of the acquisition ICs. The event counter will count the number of oscillator periods within a pre-determined time window. The count of oscillator periods is then compared with a known value.

The comparators are then checked by varying the threshold voltage and reading the state of the activity indicators. The outputs of the octal DAC are set to the upper voltage limit and the activity indicators for all of the pod channels are read to see if they are all in a low state.

The octal DAC outputs are then set to the lower voltage limit, and the activity indicators are read to see if they are in a high state. The DAC outputs are then set to 0.0 V, allowing the comparators to recognize the test signal being routed to the test input pin of all of the comparators. Consequently, the activity indicators are read to see if they show activity on all channels of all of the pods.

Chip Tests

During the Chip Tests, six tests are performed on the acquisition ICs. The tests are the Communications, Memory, Encoder, Resource, Sequencer, and Clock Generation Tests.

Communications Test The communications test verifies that communications pipeline between the various subsystems of the IC are operating. Checkerboard patterns of "1s" and "0s" are routed to the address and data buses and to the read/write registers of each chip. After verifying the communications pipelines, the acquisition clock synchronization signals that are routed from IC to IC are checked. Finally, the IC master clock optimization path is checked and verified.

Passing the communications test implies that the communications pipelines running from subsystem to subsystem on the acquisition IC are functioning and that the clock optimization circuit on the IC is functioning. Also, passing this test implies that the acquisition clock synchronization signals are functioning and appear at the synchronization signal output pins of the acquisition IC.

Memory Test Acquisition RAM is checked by filling the IC RAM with a checkerboard pattern of "1s" and "0s," then reading each memory location and comparing the test pattern with known values. Then, the IC RAM is filled with an inverse checkerboard pattern, read, and compared with known values.

Passing the memory test implies that the acquisition IC RAM is functioning and that each memory location bit can hold either a logical "1" or logical "0."

Encoder Test The encoder in the FISO front end is tested and verified using a walking "1" and walking "0" pattern. The walking "1" and "0" is used to stimulate all of the encoder output pins which connect directly to the FISO memory cells. Additionally, the post-store counter in each of the acquisition ICs is tested.

Passing the encoder test implies that the FISO encoder is functioning and can properly route the acquired data to the acquisition memory FISO RAM. Also, passing this test implies that the post-store counter on the acquisition ICs is functioning.

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Resource Test The pattern, range, edge, and glitch recognizers are tested and verified. First, the test register is verified for correct operation. Next, the pattern comparators are tested to ensure that each bit in the recognizer memory location as well as the logic driver/receiver are operating. The edge and glitch pattern detectors are then verified in a similar manner. The range detectors are verified with their combinational logic to ensure that the in- and out-of-range conditions are recognized.

Passing the resource test implies that all of the pattern, range, edge, and glitch resources are operating and that an occurrence of the pattern, edge, or glitch of interest is recognized. Also, passing this test implies that the range recognizers will detect and report in- and out-of-range acquisition data to the sequencer or storage qualifier. The drivers and receivers at the recognizer input and output pins of the acquisition IC are also checked to be sure they are functioning.

Sequencer Test The sequencer, the state machine that controls acquisition storage, is tested by first verifying that all of the sequencer registers are operating. After the registers are checked, the combinational logic of the storage qualification is verified. Then, both the occurrence counter and the sequencer level counter are checked.

Passing the sequencer test implies that all 12 available sequence levels are functioning and that all possible sequence level jumps can occur. Also, passing this test implies that user-defined ANDing and ORing of storage qualified data patterns will occur, and that the occurrence counter that appears at each sequence level is functioning.

Clock Generator Test The master clock generator on the acquisition ICs is tested by first checking the operation of the clock optimization circuit. The state acquisition clock paths are then checked to ensure that each state clock and clock qualifier are operating by themselves and in all possible clock and qualifier combinations. The timing acquisition optimization circuit is then operationally verified. Finally, the timing acquisition frequency divider (for slower timing sample rates) is checked.

Passing the clock generator test implies that each acquisition IC can generate its own master clock whether the clock is generated using a combination of external clocking signals (state mode) or internal sample clock signals (timing mode).

Data Input Inspection

The data input inspection allows a user to verify that all of the data and clock/data pipelines are operational. When the data input inspection test is selected, a test signal is fed to the test input pins of all 9-channel comparators. The test menu displays the activity indicators for all data and clock/data channels, which should show transitioning data signals on all channels.

The data input inspection is not an active part of the performance verification. However, the test is useful for identifying failed channels in order to temporarily work around the problem until the logic analyzer module can be sent to an HP service center for repair.

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Oscilloscope tests (Scope PV)

The following self-tests check the major components of the HP 1660CS-series oscilloscope board as well as all associated circuitry. When the self-tests have all been completed with a "PASS" status, the major data and control pipelines in the HP 1660CS-series oscilloscope board are functioning properly.

Data Memory Test This test verifies the correct operation of the FISO (fast-in/slow-out) data memory on the board. Test patterns are written into the memory and then read and compared with known values.

Timebase Test The pre-trigger and post-trigger delay modes are first tested by programming a predetermined time interval in the trigger counters. At the end of the time intervals, the arm, trigger, and run status bits are read and compared with known values. The coarse and fine interpolators are then checked by reading the values of the interpolator counters after a simulated acquisition. The counter values are then compared with a known value. Finally, the sample clock is checked by programming a sample clock frequency and then reading the status of the clock to detect when one clock period has elapsed. The clock period time interval is then compared with a known value.

A/D Test This test verifies the correct operation of the A/D converter on the board. A check of the trigger in Trigger Immediate mode is first made. The A/D converters are then exercised by setting the reference voltage and channel offset such that a simulated acquisition obtains data in the extremes and middle of the quantization range of the A/D converter. After each simulated acquisition, the data is compared with known values.

D/A Test This test verifies the correct operation of the D/A converter on the board. Both the offset and trigger level D/A converters for each channel are set to a reference level and then changed. The logic trigger IC is programmed to detect the changes. The detection of a correct trigger indicates that the D/A converter is operating normally.

Trigger Test This test verifies the correct operation of the trigger components on the board. First, the logic trigger memory is checked by writing and then reading known patterns. The logic qualifiers, logic trigger output, and trigger holdoff are then checked.

IMB Test This test verifies the correct operation of the oscilloscope board interface to the intermodule bus.

All Tests This will automatically execute each test, one at a time, until all tests are done.

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Pattern Generator tests (Patt Gen)

The following section contains a description of each of the the pattern generator self tests.

Clock Source Test

The Clock Source Test checks that the internal clock sources are functioning by verifying the presence of a given clock source. The test toggles each clock source in the following fashion. First the board is stopped and outputs are disabled. Module RAM is loaded with zeros, then the module is placed in the respective mode for the given clock and the clock source is selected. The module is then started and the main status checked to see that the pipeline is running. The board will then be stopped and the status checked to see that the pipeline did stop.

Passing the Clock Source Test implies that the internal clock sources are functioning properly, and that the other dependent subcircuits respond to the clock signal.

Diagnostic Integer Value: The integer returned will have the following bit format:

BIT #:	15, 14,13, 12	11, 10, 9, 8	7, 6, 5, 4	3, 2, 1, 0
	200M clk	100M clk	50M clk	PLD clk

Each nibble of the output corresponds to one of the clock sources. The bit pattern of each nibble has the following definition:

0 — passed
1 — failed to run
2 — failed to stop
3 — failed to both run and stop

Vector Memory Test

The Vector Memory Test does a first order check of the functionality of RAM. The first pass of the test will load the entire RAM with 0x0000. The software will step the clock enough times to output one page worth of data. At each clock a test read port for each RAM IC will be checked and verified for all 0s.

The second pass of the test will load all the RAMS with 0xFFFF and then check using the same technique as in the first pass, verifying for all Fs.

The third pass loads memory with an alternating 0x5555 and 0xAAAA checkerboard pattern. Again the test checks the data in the same fashion as in the first pass.

Passing the Vector Memory Test implies that each memory location in RAM can store a logic 1 or 0. Passing the test also implies that the CPU interface is functioning and can properly affect control over the memory and memory addressing.

Diagnostic Integer Value: This test checks the RAM of the entire board. The returned integer for a particular card has the following format:

BIT #:	15, 14	13, 12, 11, 10, 9, 8, 7, 6	5, 4, 3, 2, 1, 0
	Test 1	Fail row	Failed test

Bits 14,15 contain the test that failed where the value is the following:

1— failed all zeros test
2— failed all ones test
3— failed alternating test

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Bits 6-13 contain the row of the page that failed.
Bits 0-5 contain the failure code for the six RAM ICs on the board. Bits 0-4 contain the failure code for the RAMs for pod 1-5, and bit 5 contains the failure code for the RAM used for instructions. A one in the bit position indicates that that RAM provided incorrect information.

Address Counter Test

The Address Counter Test contains four subtests that check the functionality of the column and row address counters for board RAM. The four subtests use each of the four loop registers to perform the test.

The first step of the test is to load memory using the current loop register with a specific pattern for the address counter. Memory is loaded with 0x0000 except at predetermined RAM row and column positions, which are loaded with 0xFFFF.

The current loop register is used to set the address for the 0xFFFF loading. The loop register is also used to reset the addresses back to zero for starting the stepping process.

After memory has been loaded the clock is stepped through all possible RAM addresses checking for the correct data at each address.

Passing the Address Counter Test implies that each RAM memory location can be accessed by the RAM addressing circuitry while under control of the clocking circuit. Passing the test also implies that the loop registers are operating correctly.

Diagnostic Integer Value: This test checks the counters of the entire board. The returned integer has the following format:

BIT #:	15	14, 13, 12, 11, 10, 9, 8, 7, 6	5, 4, 3, 2, 1, 0
	Row/Col	Fail row	Failed RAM

Bit 15 is used to flag where the value of the fail row bits (6-14) came from. If the failing row value was less than 511 bit 15 is set to zero. If the failing row was greater than 511 bit 15 is set to one. The failed row bits (6-14) contain a value from 0 to 255.

Bits 0-5 contain the failure code for the six RAMs on the board. Bits 0-4 contain the failure code for the RAM for pods 1-5, and bit 5 contains the failure code for the RAM used for instructions. A one in the bit position indicates that that ram provided incorrect information.

Instruction Tests

This test contains three subtests that have unique descriptions. Each subtest is described below.

Passing the Instruction Tests implies that CPU addressing, RAM addressing, and the instruction decoder of the board responds properly to user commands.

Subtest #1 — Instruction Interface Test This test checks the functionality of the break command in the instruction memory and the status register that reads the break.

On the first pass of this test, instruction memory is loaded with zeros (NOP). The board is run and the main status register polled to see that the hardware is running. If the hardware is stopped the test fails.

The second pass of the test places the break instruction on the next to last vector in memory. Again the hardware is started and the status is read. This time the board should stop or the test fails.

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Diagnostic Integer Value: This test is only valid for signals on the master board of the configuration. The values returned from any expansion cards will be zero. The integer returned will have the following bit format:

BIT #:	15 ,14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4	3, 2, 1, 0
	unused	Test Mode

The Test Mode bit positions have the following meaning:

0 — passed
1 — stopped without break
2 — failed to stop from software
4 — failed to stop with break
8 — stopped by something other than break

Subtest #2 — Wait Instruction Test This test checks the functionality of the wait command in the instruction memory and the status register that reads the wait. The test is performed on each of the four event registers. The current wait event being tested is loaded on the first page of memory and a break instruction is loaded on the third page of memory.

The first pass of the test places a wait on no event in the event register. The hardware is started and a wait is begun for the vectors to hit the break instruction on the third page. The main status is checked to see that the hardware is stopped by the break instruction.

The second pass of the test places a wait on any condition in the event register. Again the hardware is started wait is begun. On this pass the hardware should be stopped by the wait condition and not by the break condition.

The final pass clears the current wait condition using the hardware wait clear command. The board should run from the current wait to the break condition and once again stop.

Diagnostic Integer Value: The integer returned will have the following bit format:

BIT #:	15, 14,13, 12	11, 10, 9, 8	7, 6, 5, 4	3, 2, 1, 0
	Event D	Event C	Event B	Event A

Each nibble corresponds to the event register being tested. The value of the nibble for the event register has the following definition:

0 — passed
1 — failed to stop on break with no event wait
2 — stopped on wait with setting of no event
3 — failed to stop on break or wait with wait any event
4 — failed to stop on wait with wait any event
5 — failed to clear wait
6 — stopped on false break condition

It should be noted that the value returned will be the last error encountered.

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Subtest #3 — If Instruction Test This test checks the functionality of the if branching.

Instruction memory is loaded with a wait on event 'a' instruction in the non-if branch of memory and a break instruction in the if branch.

The first pass of the test sets the branch pattern to a never branch condition. The board is started and a wait is begun for the vectors to get to the wait instruction. The hardware should stop on the wait instruction, not the break. The main status is checked to verify this stop condition.

The second pass of the test sets the branch pattern to always branch. Again the board is started and a wait is begun. In this case the break instruction should be the stop condition.

Diagnostic Integer Value: The integer returned will have the following bit format:

BIT #:	15 ,14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4	3, 2, 1, 0
	unused	Test Mode

The Test Mode bit positions have the following meaning:

0 — passed
1 — failed to stop on wait in non-if branch
2 — took if branch on no branch event
4 — failed to stop on break in if branch
8 — took non-if branch on any branch event

Output Patterns for testing with an external logic analyzer or oscilloscope

The performance test will set up two predefined patterns for examining the board from an external analyzer or scope. This allows the user to check the output pipeline for functionality and also helps to perform a quick check of all bit locations in the data VRAMS.

The data is output based on the frequency mode chosen by the user:

50MHz Mode — 20 ns period

100MHz Mode — 10 ns period

200MHz Mode — 5 ns period

Either a checkerboard pattern (alternating 1s and 0s across the output channels) or a walking ones pattern are available.

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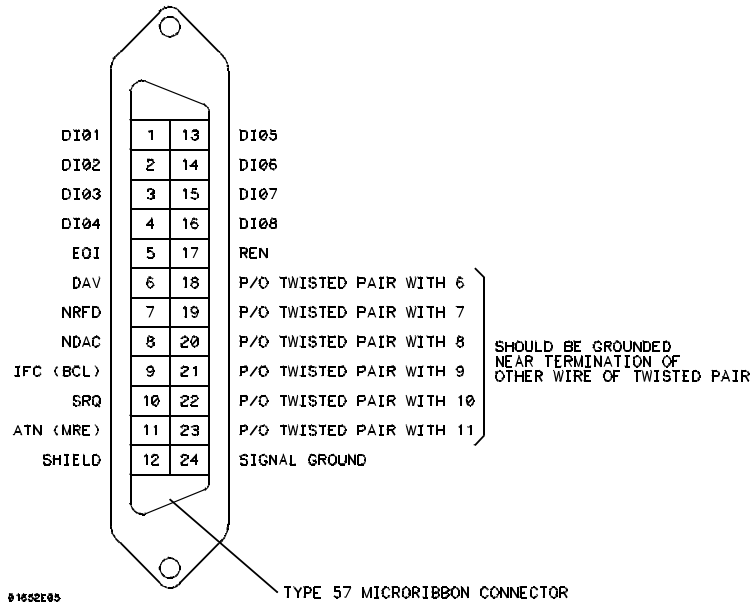
The Hewlett-Packard Interface bus (HP-IB) is Hewlett-Packard's implementation of IEEE Standard 488-1978, "Standard Digital Interface for Programming Instrumentation." HP-IB is a carefully defined interface that simplifies the integration of various instruments and computers into systems. The interface makes it possible to transfer messages between two or more HP-IB compatible devices. HP-IB is a parallel bus of 16 active signal lines divided into three functional groups according to function.

Eight signal lines, called data lines, are in the first functional group. The data lines are used to transmit data in coded messages. These messages are used to program the instrument function, transfer measurement data, and coordinate instrument operation. Input and output of all messages, in bit parallel-byte serial form, are also transferred on the data lines. A 7-bit ASCII code normally represents each piece of data.

Data is transferred by means of an interlocking "Handshake" technique which permits data transfer (asynchronously) at the rate of the slowest active device used in that transfer. The data byte control lines coordinate the handshaking and form the second functional group.

The remaining five general interface management lines (third functional group) are used to manage the devices connected to the HP-IB. This includes activating all connected devices at once, clearing the interface, and other operations.

The following figure shows the connections to the HP-IB connector located on the rear panel.



HP-IB Interface Connector

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The logic analyzer interfaces with RS-232-C communication lines through a standard 25 pin D connector. The logic analyzer is compatible with RS-232-C protocol. When a hardwire handshake method is used, the Data Terminal Ready (DTR) line, pin 20 on the connector, is used to signal if space is available for more data in the logical I/O buffer. Pin outs of the RS-232-C connectors are listed in the following table.

RS-232-C Signal Definitions

Pin Number	Function	RS-232-C Standard	Signal Direction and Level
1	Protective Ground	AA	Not applicable
2	Transmitted Data (TD)	BA	Data from Mainframe High = Space = "0" = +12 V Low = Mark = "1" = –12 V
3	Received Data (RD)	BB	Data to Mainframe High = Space = "0" = +3 V to +25 V Low = Mark = "1" = –3 V to –25 V
4	Request to Send (RTS)	CA	Signal from Mainframe High = ON = +12 V Low = OFF = –12 V
5	Clear to Send (CTS)	CB	Signal to Mainframe High = ON = +3 V to +12 V Low = OFF = –3 V to –25 V
6	Data Set Ready (DSR)	CC	Signal to Mainframe High = ON = +3 V to +25 V Low = OFF = –3 V to –25 V
7	Signal Ground	AB	Not applicable
8	Data Carrier Detect (DCD)	CF	Signal to Mainframe High = ON = +3 V to +25 V Low = OFF = –3 V to –25 V
20	Data Terminal Ready (DTR)	CD	Signal from Mainframe High = ON = +12 V Low = OFF = –12 V
23	Data Signal Rate Selector	CH/CI	Signal from Mainframe Always High = ON = +12 V

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- Before turning on the instrument, you must connect the protective earth terminal of the instrument to the protective conductor of the (mains) power cord. The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. You must not negate the protective action by using an extension cord (power cable) without a protective conductor (grounding). Grounding one conductor of a two-conductor outlet is not sufficient protection.
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- Do not install substitute parts or perform any unauthorized modification to the instrument.
- Capacitors inside the instrument may retain a charge even if the instrument is disconnected from its source of supply.
- Use caution when exposing or handling the CRT. Handling or replacing the CRT shall be done only by qualified maintenance personnel.

Safety Symbols



Instruction manual symbol: the product is marked with this symbol when it is necessary for you to refer to the instruction manual in order to protect against damage to the product.



Hazardous voltage symbol.



Earth terminal symbol: Used to indicate a circuit common connected to grounded chassis.

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New editions are complete revisions of the manual. Many product updates do not require manual changes; and, conversely, manual corrections may be done without accompanying product changes. Therefore, do not expect a one-to-one correspondence between product updates and manual updates.

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