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Errata

Title & Document Type: 16510A Front Panel Reference

Manual Part Number: 16510-90902

Revision Date: January 1988

HP References in this Manual

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Front-Panel Operation Reference

HP 16510A
Logic Analyzer Module

for the HP 16500A Logic Analysis System



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Manual Set Part Number 16510-90902
Microfiche Part Number 16510-90802

Printed in U.S.A January 1988

Printing History First Edition - January 1988 Printed in U.S.A.

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Introduction

About this manual...

Welcome to the new generation of HP logic analyzers! The HP 16500A Logic Analysis System has been designed to be easier to use than any Hewlett-Packard logic analyzer before. In addition, because of its configurable architecture, it can easily be tailored to your specific logic design and debug needs.

The user interface of the HP 16500A was designed for the most intuitive operation possible. Pop-up windows and color graphics help lead you through setups and measurements so you won't have to memorize a lot of steps. As you read this manual and the other manuals about the mainframe and acquisition modules, you will see just how easy the HP 16500A is to use.

This logic analyzer reference manual is divided as follows:

- Chapters 1 through 4 contain introductory information about the logic analyzer and the accessories supplied with the HP 16510A. They contain information that will familiarize you with the user-interface and menus.
- Chapters 5 and 6 describe all the menus of the logic analyzer.
- Chapters 7 through Appendix C discuss other logic analyzer functions such as making basic measurements, printing, specifications, etc.

If you aren't familiar with the HP 16510A Logic Analyzer, we suggest you read the *HP 16510A Getting Started Guide*. This guide contains tutorial examples on the basic functions of the logic analyzer.

If you're new to logic analyzers...or just need a refresher, we think you'll find *Feeling Comfortable with Logic Analyzers* valuable reading. It will eliminate any misconceptions or confusion you may have about their application, and will show you how to get the most out of your new logic analyzer.

1 General Information

Logic Analyzer Description

The HP 16510A logic analyzer is part of a new generation of general purpose logic analyzers with improved features to accommodate next generation design tasks.

The 80-channel HP 16510A logic analyzer is capable of 100 MHz timing and 25 MHz state analysis on all channels.

This analyzer is designed as a stand alone instrument for use by digital and microprocessor hardware designers. The HP 16500A mainframe has HP-IB and RS-232C interfaces for hardcopy printouts and control by a host computer.

User Interface

The user interface is easier to use than in previous generations for first- time and casual users as well as experienced logic analyzer users.

The HP 16500A has three user interface devices: the knob on the front panel, the touchscreen, and the optional mouse.

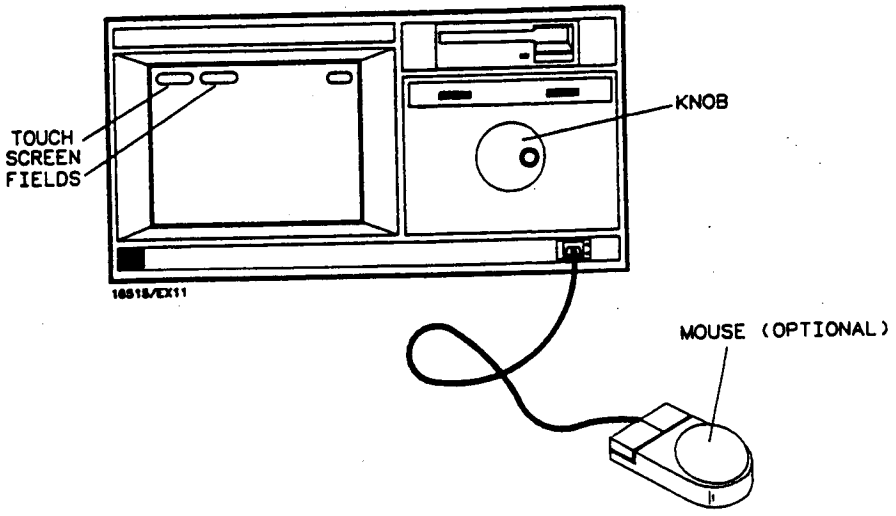


Figure 1-1. HP 16500A User Interfaces

The knob on the front panel is used to move the cursor on certain menus, increment or decrement numeric fields, and to roll the display.

The touchscreen fields can be selected by touch or with the optional mouse. To activate a touchscreen field by touch, touch or press the field (the dark blue box) on the display with your finger until the field changes color. Then remove your finger from the screen to activate your selection.

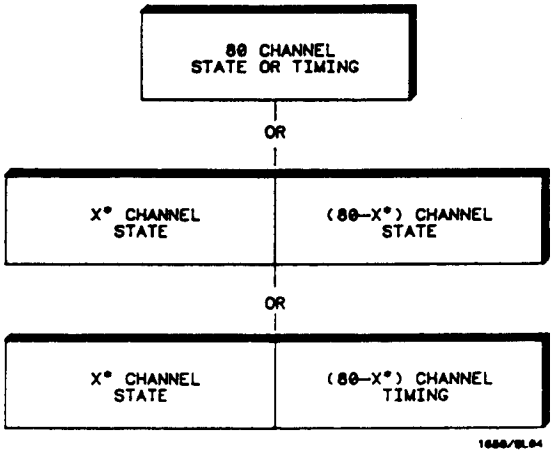
To activate a field with the optional mouse, position the cursor (+) of the mouse over the desired field and press the button on the upper-left corner of the mouse.

The user interfaces are discussed in more detail in the *HP 16500A Reference* manual.

Configuration Capabilities

The HP 16510A can be configured as two independent machines (analyzers) maximum at one time or two machines interactively. The combinations are:

- Up to 80 channels state
- Up to 80 channels timing
- Two state machines with multiples of 16 channels per machine with a combined maximum of 80 channels
- One state and one timing machine with multiples of 16 channels per machine with a combined maximum of 80 channels



* multiples of 16 channels

Figure 1-1. HP 16510A Configuration Capabilities

Key Features

Two 3.5-inch disc drives are integral to the instrument for storing logic analyzer configurations and acquired data. The disc drive also provides a way of loading inverse assembly configuration files into the logic analyzer for configuring ease.

Additional key features of both models include:

- Transitional timing for extended timing analyzer memory
- Lightweight passive probes for easy hook-up
- All channels can be used for state or timing at the maximum sample rate
- HP-IB and RS-232C interface for programming and printer dumps
- An external trigger BNC connector
- Efficient package size
- Transitional or glitch timing modes
- 1k-deep memory on all channels
- Glitch detection
- Marker measurements
- Triggering and pattern qualification
- Overlapping of timing waveforms
- Eight sequence levels
- Eight pattern recognizers
- One range recognizer
- Time and number-of-states tagging
- Pre-store
- Auto-scale
- Programmability
- Cross-domain triggering
- Interactive measurements
- Mixed-mode display
- Oscilloscope type controls in the timing analyzer

Accessories Supplied

Table 1 lists the accessories supplied with your HP16510A. If any of these accessories were missing when you received the logic analyzer from the factory, contact your nearest Hewlett-Packard office. If you need additional accessories, refer to the *Accessories for the HP 1650A/HP 1651A and HP 16500A Logic Analyzers* data sheet.

Table 1-1. Accessories

Accessory	HP Part No.	Quantity
Probe assemblies	01650-61608	5
Probe Cables (25MHz State)	16510-61601	3
Probe cables	16510-61602	2
Grabbers (Note 1)	5959-0288	100
Ground leads (long)	01650-82102	5
Ground leads (short)	01650-82103	10
RS-232C Loop back adapter	01650-63202	1
Probe and probe cable numbering label card	01650-94303	1
Operating system disc	16510-13501	2
Operating and Programming manual set	16510-90902	1
Service manual	16510-90901	1

Notes:

1. Package of 20 per part number.

Available Accessories

In addition to the accessories supplied, there are a number of accessories available that will make your measurement tasks easier and more accurate. You will find these listed in the *Accessories for the HP 1650A/ HP 1651A and HP 16510A Logic Analyzers.*

2 Probing

Introduction

This chapter contains a description of the probing system of the HP 16510A logic analyzer. It also contains the information you need to connect the probe system components to each other, to the logic analyzer, and to the system under test.

Probing Options

You can connect the HP 16510A logic analyzers to your system under test in one of four ways:

- HP 10320C User-definable Interface (optional)
- HP 10269C with microprocessor specific modules (optional)
- the standard HP 16510A probes (general purpose probing)
- direct connection to a 20-pin 3M® Series type header connector using the optional termination adapter (HP Part No. 01650-63201).

The HP 10320C User-Definable Interface

The optional HP 10320C User-definable Interface module combined with the HP 10269C General Purpose Probe Interface (optional) allows you to connect the HP 16510A logic analyzer to your target system. The HP 10320C includes a breadboard (HP 64651B) which you custom wire for your system.

Also available as an option that you can use with the HP 10320C is the HP 10321A Microprocessor Interface Kit. This kit includes sockets, bypass capacitors, a fuse for power distribution, and wire-wrap headers to simplify wiring of your interface when you need active devices to support the connection requirements of your system.

The HP 10269C General Purpose Probe Interface

Instead of connecting the probe tips directly to the signal lines, you may use the HP 10269C General Purpose Probe Interface (optional). This allows you to connect the probe cables (without the probes) to connectors on the interface. When the appropriate preprocessor is installed in the interface, you will have a direct connection between the logic analyzer and the microprocessor under test.

There are a number of microprocessor specific preprocessors available as optional accessories which are listed in the *Accessories for the HP 1650/HP1651A and HP 16500A Logic Analyzers* data sheet. Chapter 11 of this manual also introduces you to preprocessors and inverse assemblers.

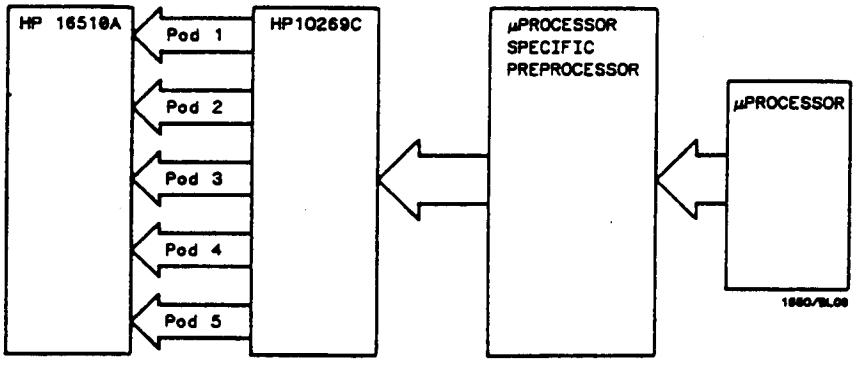


Figure 2-1. HP 10269C with Preprocessor

General Purpose Probing

General purpose probing involves connecting the probes directly to your target system without using the interface. General purpose probing does not limit you to specific hook-up schemes as the probe interface does.

The Termination Adapter

The optional termination adapter (HP Part No. 01650-63201) allows you to connect the probe cables directly to test ports on your target system without the probes. However, since the probes contain the proper termination for the logic analyzer inputs, a termination must be provided when you aren't using the probes. The termination adapter provides this termination.

The termination adapter is designed to connect to a 20 (2x10) position, 4-wall, low profile header connector, 3M® Series 3592 or equivalent.

You connect the termination adapter to the probe cable in place of the pod connector and connect the other end of the adapter directly to your test port.

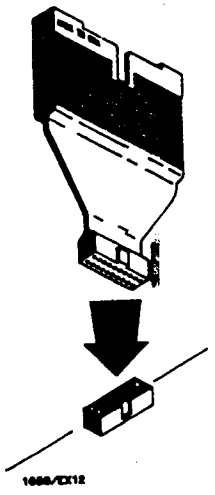


Figure 2-2. Termination Adapter

The HP 16510A Probing System

The standard HP 16510A probing system consists of probes, pods, probe cable and grabbers. This system is passive (has no active circuits at the outer end of the cable). This means that the pods and probes are smaller and lighter, making them easier to use.

The passive probe system is similar to the probe system used with high frequency oscilloscopes. It consists of a series R-C network (90.9 kΩ in parallel with 8 pF) at the probe tip, and a shielded resistive transmission line.

The advantages of this system are:

- 2 ns risetime with ± 5% perturbations
- 8 pF input capacitance at the probe tip
- signal ground at the probe tip for higher speed timing signals
- inexpensive removable probe tip assemblies

Probes and Probe Pods

Probes and probe pods allow you to connect the logic analyzer to your system under test without the HP 10269C Probe Interface. This general purpose probing is useful for discrete digital circuits. Each probe and pod assembly contains 16 data channels, one clock channel, and pod ground.

Probe Pod Assembly

The pods, as they will be referred to for consistency, are the probe housings (as shown below) that group 16 data, one clock line, and grounds, corresponding to a logic analyzer pod.

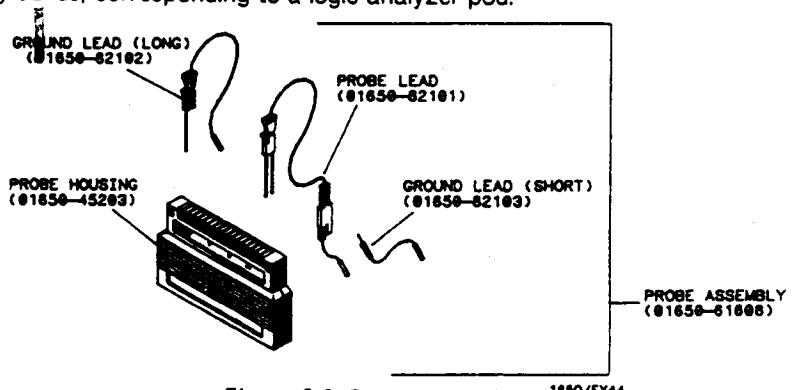


Figure 2-3. Probe Assembly

Probe Cable The probe pod cable contains 17 signal lines, 34 chassis ground lines and two power lines that is woven together. It is 4.5 feet long.

CAUTION

The probe grounds are chassis (earth) grounds, not "floating" grounds.

Each cable is capable of carrying 0.60 amps for preprocessor power. DO NOT exceed this 0.60 amps per cable or the cable will be damaged. Also, the maximum power available from the logic analyzer (all cables) is 2 amps at 5 volts.

Note

The preprocessor power source is fused. The fuse is located inside the HP 16500A on the logic analyzer card. If a preprocessor appears to be malfunctioning, refer to the HP 16510A service manual for instructions on checking this fuse.

The probe cable connects the logic analyzer to the pods, termination adapter, or the HP 10269C General Purpose Probe Interface.

Probes Each probe is a 12-inch twisted pair cable and is connected to the probe cable at the pod. One end of each probe has a probe tip assembly where the input R-C network is housed and a lead that connects to the target system. The other end of the probe has a two-pin connector that connects to the probe cable.

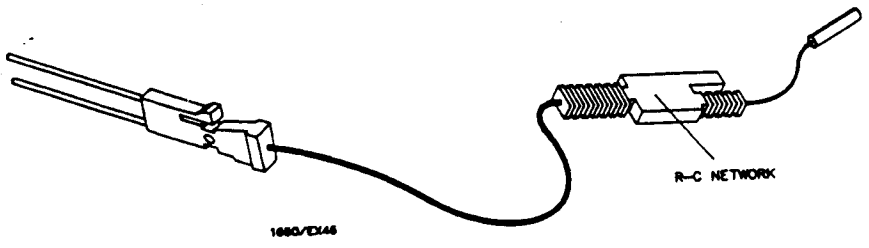


Figure 2-4. Probe Cable

You can connect the probe directly to the test pins on your target system. To do so, the pins must be 0.63 mm (0.025 in.) square pins or round pins with a diameter of between 0.66 mm (0.026 in.) and 0.84 mm (0.33 in.).

Each probe has an input impedance of 100 kΩ in parallel with approximately 8 pF.

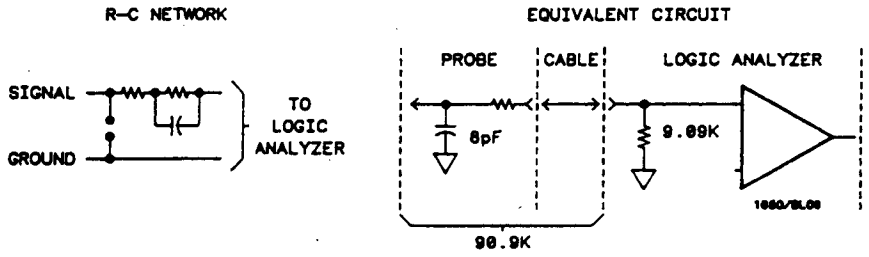


Figure 2-5. Probe Input Circuit

Probes can be grounded in one of two ways: a common pod ground and a probe ground for each probe.

Grabbers The grabbers have a hook that fits around IC pins and component leads and connects to the probes and the ground leads. The grabbers have been designed to fit on adjacent IC pins.

Pod Grounds Each pod is grounded by a pod ground lead that should always be used. You can connect the ground lead directly to a ground pin on your target system or use a grabber. The grabber connects to the ground lead the same way it connects to the probe lead.

To connect the ground lead to grounded pins on your target system, the pins must be 0.63 mm (0.025 in.) square pins or round pins with a diameter of 0.66 mm (0.026 in.) to 0.84 (0.033 in.).

Probe Grounds You can ground the probes in one of two ways. You can ground the probes with the pod ground only; however, the ground path won't be the same length as the signal path through the probe. If your probe ground path must be the same as your signal path, use the short ground lead (probe ground). The probe ground lead connects to the molded probe body via a pin and socket. You can then use a grabber or grounded pins on your target system the same way as the pod ground.

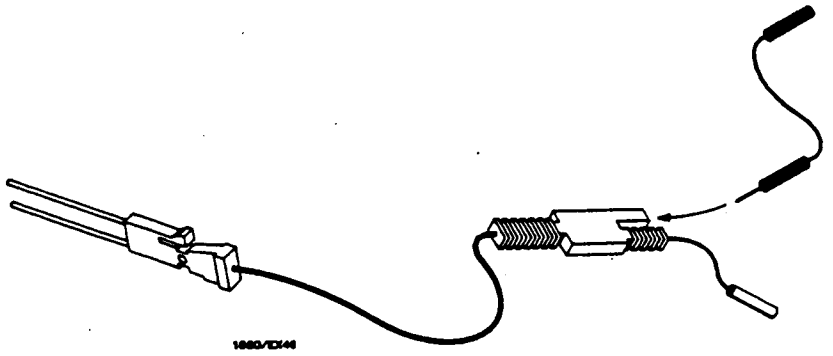


Figure 2-6. Probe Grounds

Note

For improved signal fidelity, use a probe ground for every four probes in addition to the pod ground.

If you need additional probe ground leads, order HP part number 01650-82103 from your nearest Hewlett Packard sales office.

Signal Line Loading

Any signal line you intend to probe must be able to supply a minimum of 600 mV to the probe tip, which has an input impedance of 100 kΩ shunted by 8 pF. If the signal line is incapable of this, you will not only have an incorrect measurement but the system under test may also malfunction.

Maximum Probe Input Voltage

The maximum input voltage of each probe is ± 40 volts peak.

Pod Thresholds

There are two preset thresholds and a user-definable pod threshold for each pod. The two preset thresholds are ECL (-1.3 V) and TTL (+1.6 V). The user-definable threshold can be set anywhere between - 9.9 volts and +9.9 volts in 0.1 volt increments.

The pod thresholds of pods 1, 2, and 3 can be set independently. The pod thresholds of pods 4 and 5 are slaved together; therefore, when you set the threshold on either pod 4 or 5, both thresholds will be the same.

Connecting the Logic Analyzer to the Target System

There are four ways you can connect the logic analyzer to your target system as previously mentioned at the beginning of this chapter: the probes (general purpose probing); the HP 10320C User-definable Interface; the HP 10269C with microprocessor specific preprocessor modules; and direct connection to a 20 pin 3M® Series type header connector using the optional termination adapter (HP Part No. 01650-63201).

Since the probe interface hook-ups are microprocessor specific, they will be explained in their respective operating notes. The rest of this chapter is dedicated to general purpose probing with the HP 16510A probes.

Connecting the Probe Cables to the Logic Analyzer

The probe cables are installed in the Logic Analyzer module at the factory. The cable for pod 1 is the far left cable (rear view). Cables 2 through 5 follow cable 1 consecutively from left to right. If there is a need to install or replace the cables refer the *HP 16510A Service Manual*, Section VI.

Connecting the Pods to the Probe Cable

The pods of the HP 16510A differ from other logic analyzers in that they are passive (have no active circuits at the outer end of the cable). The pods, as they will be referred to for consistency, are the connector bodies (as shown below) that the probes are installed in when you receive your logic analyzer.

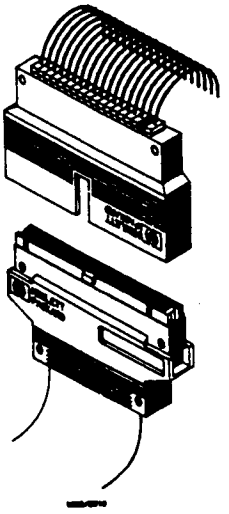


Figure 2-7. Connecting Pods to Probe Cables

To connect a pod to a cable, you align the key on the cable connector with the slot on the pod connector and push them together.

Disconnecting the Probes from the Pods

The probes are shipped already installed in the pods. However, you can disconnect any un-used probes from any of the pods. This keeps the un-used probes from getting in your way.

To disconnect a probe, insert the tip of a ball-point pen in the latch opening and push while gently pulling the probe out of the pod connector as shown below.

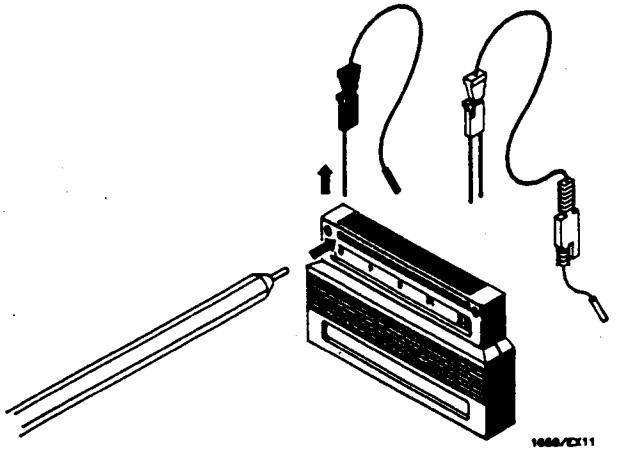


Figure 2-8. Disconnecting Probes from Pods

You connect the probes to the pods by inserting the double pin end of the probe into the pod. The probes and pod connector body are both keyed (beveled) so that they will fit together only one way.

Connecting the Grabbers to the Probes

You connect the grabbers to the probes by slipping the connector at the end of the probe onto the recessed pin in the side of the grabber. If you need to use grabbers for either the pod or the probe grounds, connect them to the ground leads the same way you connect them to the probes.

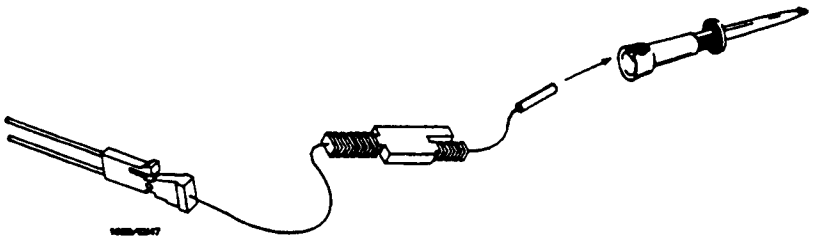


Figure 2-9. Connecting Grabbers to Probes

Connecting the Grabbers to the Test Points

The grabbers have a hook that fits around IC pins and component leads. You connect the grabber by pushing the rear of the grabber to expose the hook, hooking the lead and releasing your thumb as shown below.

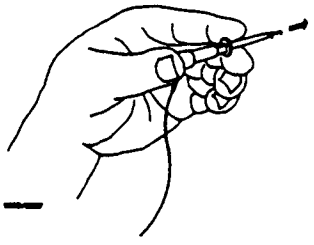


Figure 2-10. Connecting Grabbers to Test Points

Labeling Pods, Probes, and Cables

So you can find the pods and probes you want to connect to your target system, you need to be able to quickly identify them. Included with your logic analyzer are self-adhesive labels for each pod, cable and probe.

They come in sets. Each set has labels for the end of the cable-- a label for the pod connector body, a label for the clock probe and 16 labels for each of the channels.

One end of each cable is already connected to the HP 16510A logic analyzer module. The cable for pod 1 is the far left cable (rear view). Cables 2 through 5 follow cable 1 consecutively from left to right.

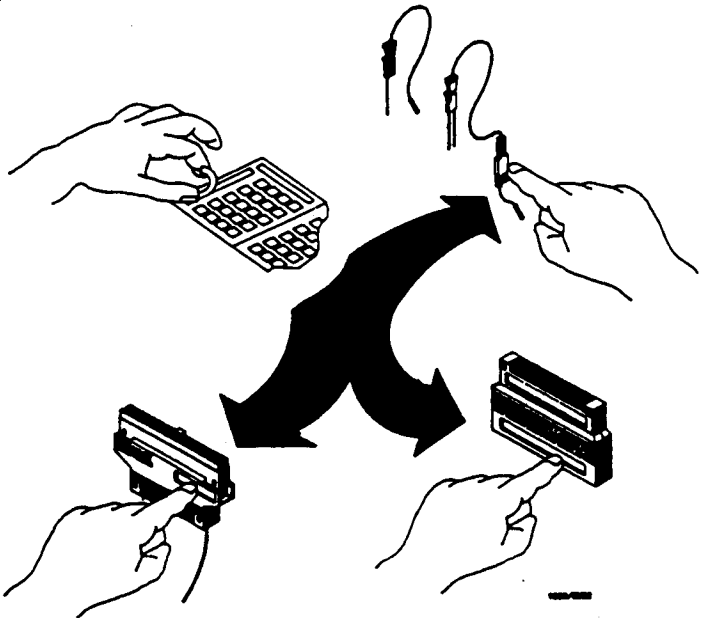


Figure 2-11. Labeling Pods, Probes, and Cables

3 Using the Front-Panel Interface

Introduction

This chapter gives you an overview of how to use the front-panel interface.

The front-panel user interface is merely accessing the many menus and using the convenient touch-screen to move around the menu tree. The front panel itself consists of a disc drive, the knob, power switch, display, and receptacle for connecting the optional mouse.

The user interface allows you to configure the logic analyzer and each analyzer (machine) within the logic analyzer. It also displays acquired data and measurement results.

Using the front-panel interface is a basic process of:

- Selecting the desired menu
- Selecting a desired field within a menu
- Displaying the options or current variable data associated with the desired field
- Selecting the desired option or entering new data (editing current data) in the field
- Starting and Stopping data acquisition when the logic analyzer is connected and configured

Using the Mouse

Everything that can be done with the touch screen and knob on the HP 16500A can also be done with the optional mouse. The mouse plugs into the connector in the lower right of the front panel. As soon as the mouse is plugged in, it is active.

When the mouse is plugged in, a white cursor (cross) appears on the screen. Moving the mouse causes the cursor to move. To "touch" a field with the mouse, move the cursor to the field and press the left button on the mouse.

To use the mouse to perform the functions of the front-panel knob, hold down the right button and move the mouse. When you release this button, the function returns to the cursor.

How to Select Menus

Before you try to select one of the main menus, make sure the field in the upper left-hand corner is set to **State/Timing E**. If the HP 16500A is in **System** or **Intermodule**, touch that field and select **State/Timing E** when the pop-up appears.

Note

*The field containing **State/Timing (x)** may have a different letter following State/Timing. Don't be alarmed. This letter merely tells you what card slot the State/Timing module is in.*

To select the main menus touch the second field from the left at the top of the screen. A pop-up appears showing you the active menus. The menus are:

- Configuration
- Format 1, 2, or both
- Trace 1, 2, or both
- Waveform (Timing analyzer only)
- Listing (State analyzer only)

When the menu is displayed you can access the fields within the menus. The second field from the left in the upper left-hand corner always displays the current menu. To move around in the menu tree, you must always touch the field displaying the current menu and select a new menu when the pop-up appears.

The Configuration, Format, Trace, Waveform, and Listing menu fields provide access to their respective menus. All menus, subsystems, and fields in the entire logic analyzer are pop-ups that appear on top of the currently displayed menu.

If more than one analyzer (machine) is on, you see the selected menu of either analyzer 1 or analyzer 2 depending on what analyzer menu was last displayed or what you did in the **State/Timing E Configuration** menu.

To switch from one of these menus to another menu within the same analyzer (machine) touch the current field (i.e. Waveform), which is displayed in the field second from the left in the upper left corner and make a new selection.

How to Switch Between Analyzers

You can switch between analyzers in any main menu by touching the field (second from the left in the upper left-hand corner). When the pop-up appears you can select the desired menu in the desired analyzer when both analyzers are on. One example of the options available when both analyzers (one state and one timing) are on are:

- Format 1
- Format 2
- Trace 1
- Trace 2
- Waveform (for Timing analyzer)
- Listing (for State analyzer)

Touch the field in the pop-up to enter the desired menu. You will immediately go to that menu.

Returning to the System Configuration Menu

You can return to the System Configuration menu from any main logic analyzer menu. To return to the System Configuration menu, touch **State/Timing E**. When the pop-up appears, touch **System**. When the pop-up closes, System will be displayed in the upper left corner. If **Configuration** is not displayed in the field second from the left in the upper left corner, touch this field. When the pop-up appears, touch **Configuration**. You will now be in the **System Configuration** menu.

Pop-up Menus

The pop-up menu is used exclusively in this logic analyzer. This gives you more flexibility to move through the menu tree and faster access to the individual subsystems.

To use the pop-ups when they appear, simply touch the field in the pop-up you want. The pop-up will immediately close and the menu you select will appear.

How to Close Pop-up Menus

Some pop-up menus automatically close when you touch a desired field. After closing, the logic analyzer places your choice in the main menu field from which you opened the pop-up.

Other pop-up menus don't automatically close when you make your selection (i.e. alphanumeric keyboard). These menus have a **Done** option. To close the pop-up all you have to do is touch the **Done** field.

Toggle Fields

Some fields will toggle between two options (i.e., off and on). When you touch one of these fields, the displayed option toggles to the other choice and no additional pop-up appears.

How to Select Options

How to select options depends on what type of pop-up menu appears when you touch the field. When the pop-up appears, you will see a list of options. You select the option by touching the option field. In most cases the pop-up menu closes when you touch an option and the selected option will be displayed. However, in some pop-ups, selecting the option does not automatically close the pop-up. In this case the option **Done** is present.

There are also pop-up menus where each option within the pop-up menu has more than one option available. In these cases, when you touch that field, another pop-up, with options, will be superimposed on the original pop-up.

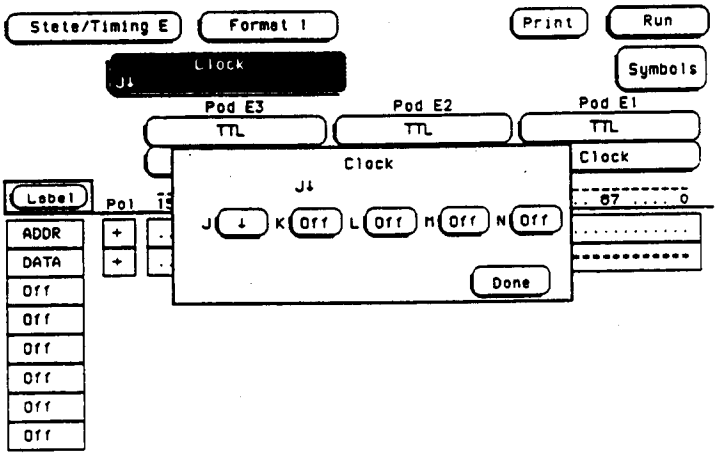


Figure 3-1. State Clock Pop-up Menu

An example of one of these is the clock field in the State Format Specification menu. When you select the clock field in this menu it will pop-up and show you all five clocks (**J**, **K**, **L**, **M**, and **N**). When you select one of the five clocks, another pop-up appears showing you the available choices of clock specifications.

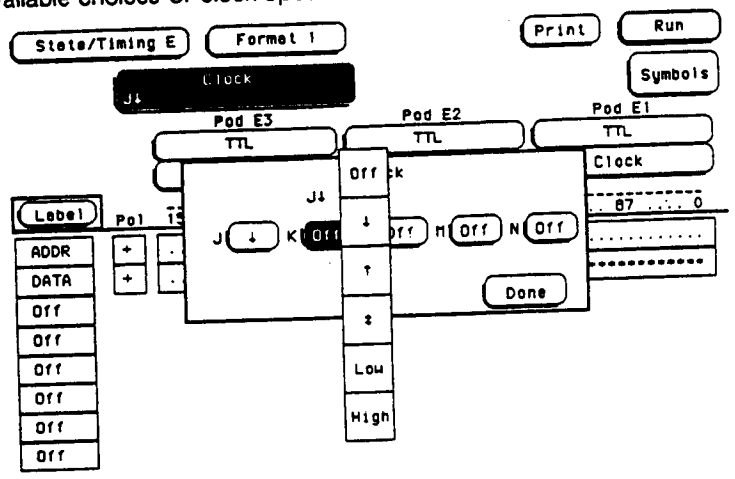


Figure 3-2. State Clock Pop-up with K Pop-up Open

When you touch one of these the pop-up will close, however, the original clock pop-up still remains open. When you are finished specifying the choices for the clocks, you close the original pop-up menu by touching **Done**.

How to Enter Numeric Data

There are a number of pop-up menus in which you enter numeric data. The two major types are:

- Numeric entry with fixed units
- Numeric entry with variable units (i.e. μs, ms, etc.)

There are several numeric entry menus where you enter only the value, the units being pre-determined. There are other numeric entry menus for which you will be required to specify the units. One such type of numeric entry pop-up that you enter the units is the pod threshold pop-up.

Besides being able to set the pod thresholds to either of the preset thresholds (TTL or ECL), you can set the thresholds to a specific voltage from - 9.9 V to + 9.9V.

To set pod thresholds to a specific voltage, you enter either Format menu and touch a pod field. When the pop-up appears you can choose **TTL**, **ECL**, or **User**.

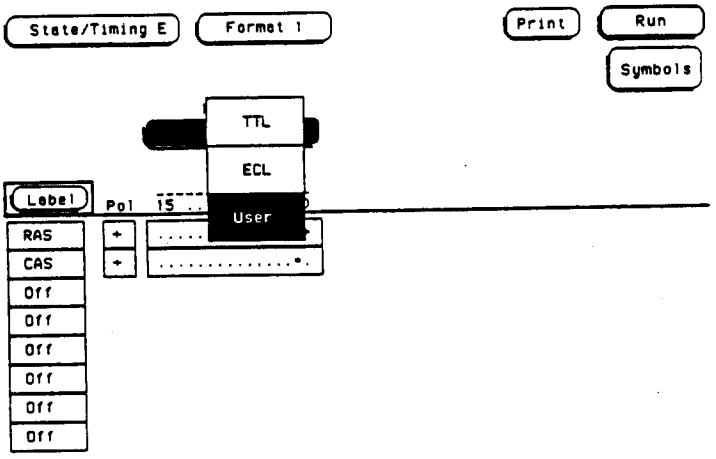


Figure 3-3. Pod Threshold

If you select the **User** option, a numeric keypad pop-up appears where you enter the desired threshold voltage. After selecting the value, you select the units (i.e., mV or V). Touch **Done** when you have finished specifying the pod threshold.

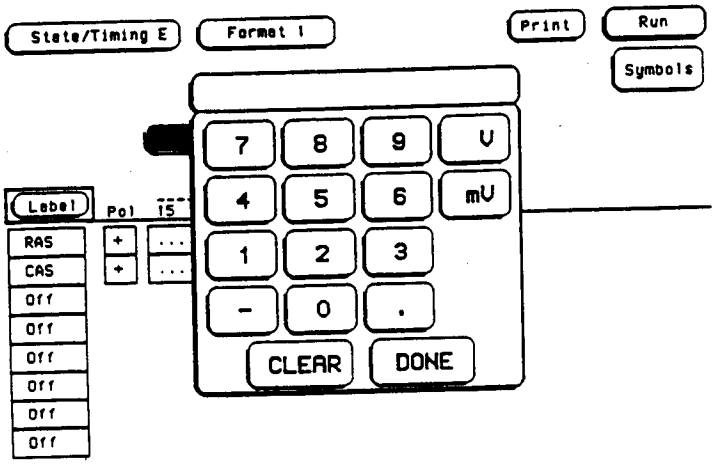


Figure 3-4. Numeric Entry Keypad

If you want a negative voltage for the threshold, press the - (minus sign) in the pop-up. Entering the - (minus sign) can be done either before or after the voltage level has been entered.

How to Enter Alpha Data

You can give specific names to several items. These names can represent your measurement specifically. For example, you might choose the name 68000STATE for the state analyzer configuration you are using on a 68000 microprocessor measurement.

The two major examples of items that can be named are:

- The name of each analyzer
- Labels
- Symbols
- Filenames
- File descriptions

For example, you can name each analyzer with a name that is representative of your measurement. The default names for the analyzers within the logic analyzer are MACHINE 1 and MACHINE 2. To rename an analyzer, touch the field to the right of **Name:**_____ in the **State/Timing E Configuration** menu. When the alphanumeric pop-up menu appears, enter the name you desire.

The line above the alphanumeric keyboard contains the current name. When you first enter the pop-up, the cursor in the name field is at the left. You can enter the name you wish by overwriting the existing name. If only a few changes need to be made, you can move the cursor using the knob to a character needing changed and select a new character. You can also clear the entire field by touching **Clear**. When you have entered the desired name, touch **Done** and the pop-up will close. The new name will appear in the field to the right of **Name:**_____.

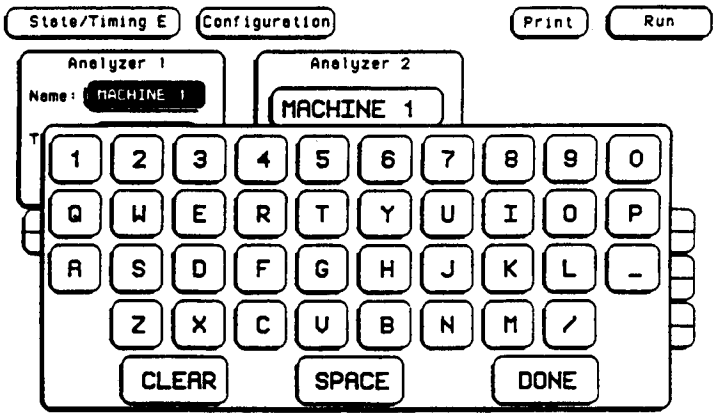


Figure 3-5. Alphanumeric Keypad

How to Roll Data

The roll feature is available in all menus that contain off-screen data. This allows you to roll data for viewing. Data can be off-screen both above and below or left and right of what you see on screen.

One example of a menu having off-screen data above and below the screen is the State Listing. The state listing is normally a list 1024 lines long, however, the display is only capable of showing you 16 lines at a time. To roll data in the state Listing (when the box in the left center of the listing area is light blue) simply turn the knob. If this box is not light blue, touch this box and then turn the knob. If you touch this box when it is light blue, a keypad will appear with which you can enter a state location. This allows you to effectively roll the displayed listing in large increments.

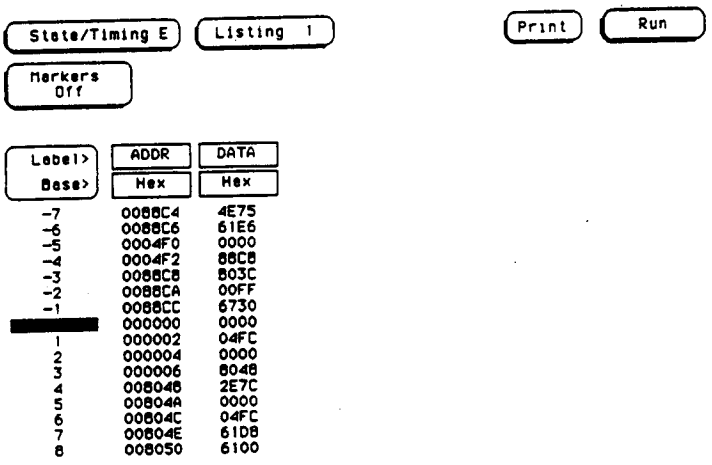


Figure 3-6. State Listing Menu with Off-screen Data

An example of off-screen data left and right can also be shown in figures 3-7 and 3-8. Figure 3-7 illustrates a timing Trace menu with labels off screen. In this case only six of the eight labels can be displayed at a time. Whenever there is data off screen to the left or right, an additional field exists in the menu as shown in figure 3-7. This is called a field because it is enclosed in a box and will turn light blue when touched.

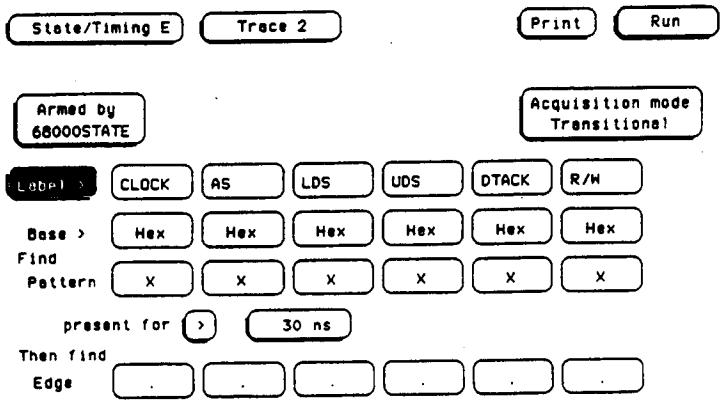


Figure 3-7. Additional Field indicating Off-screen Data

If data does not exist off screen, the term **Label >** will not be enclosed in a box (see figure 3-8).

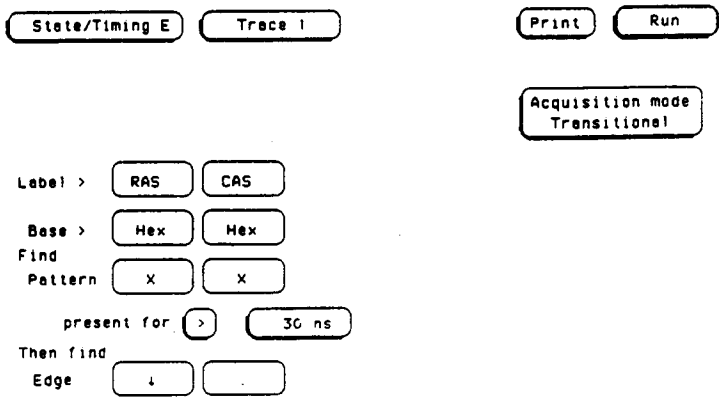


Figure 3-8. No Off-screen Data Left or Right

Assignment/ Specification Menus

There are a number of pop-up menus in which you can assign or specify what you want the logic analyzer to do. The basic menus of this type consist of:

- Assigning bits to pods
- Specifying patterns
- Specifying edges

Assigning Pod Bits to Labels

The bit assignment fields in both state and timing analyzers work identically. The convention for bit assignment is:

* (asterisk) indicates assigned bits.
. (period) indicates un-assigned bits.

An example of assigning bits is in either the Timing or State Format menu.

Note

If you don't see any bit assignment fields, it merely means you don't have any pods assigned to this analyzer. Either switch analyzers or assign a pod to the analyzer you are working with.

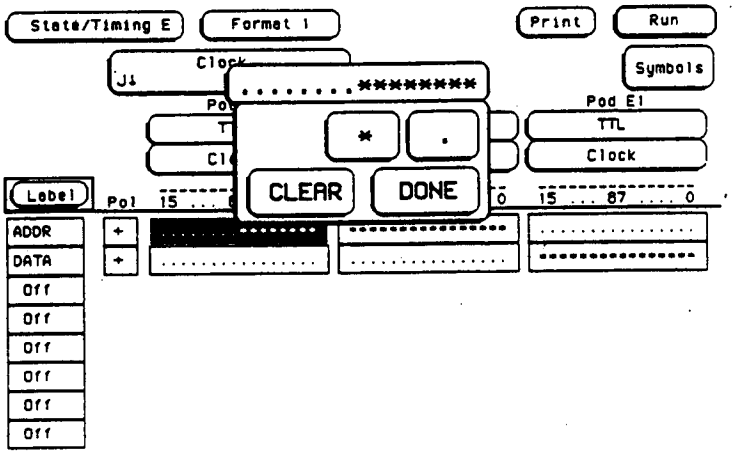


Figure 3-9. Bit Assignment Pod

To assign bits to either Analyzer 1 or Analyzer 2 there must be at least one pod assigned to the desired analyzer. If ther are no pods assigned to the analyzer you wish to use follow steps 1 and 2. If there is a pod assigned to the desired analyzer go to step 3 where you access the Format menu.

1. Enter the State/Timing E Configuration menu.

2. Touch a Pod field. When the pop-up appears, assign the pod to the analyzer of your choice.

3. Touch the field second from left in the top left corner. When the pop-up appears, touch Format 1 (or 2).

4. Before you can select a bit pattern at least one label must be on. To turn a label on, touch the label field and when the pop-up appears, touch **Turn Label On**.

5. Touch the bit assignemnt field to access the bit assignment pop-up.

6. When the pop-up appears, using the KNOB, place the cursor on the desired bit and touch the asterisk to assign a bit or the period to unassign a bit. Touch **Done** when bit assignment is complete.

When the pop-up closes the bit assignment field is again displayed, however, now it is displayed with the assigned pattern.

Specifying Patterns

The Pattern field appears in several menus. Patterns can be specified in one of the available number bases. Patterns can be viewed in ASCII, but cannot be selected in ASCII.

The convention for "don't care" in these menus is an X except in the decimal base. If the base is set to decimal after a "don't care" is specified, a $ will be displayed.

To select a pattern, enter the Trace menu and follow these steps:

1. Touch the field to the right of Pattern. You will see a keypad pop-up (see figure 3-10).

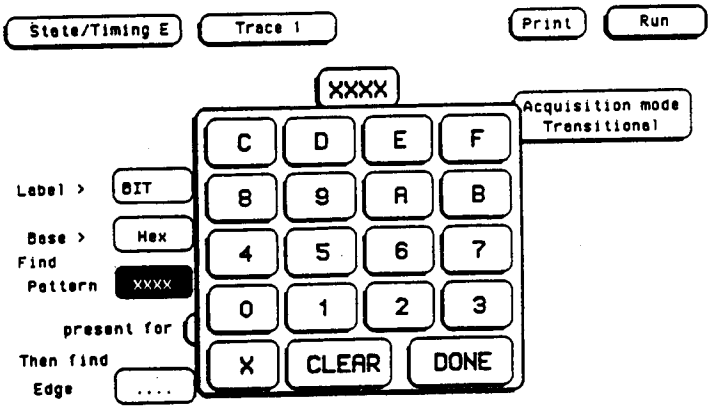


Figure 3-10. Specifying Patterns Keypad Pop-up Menu

2. Using the alphanumeric keyboard, enter the desired pattern.

Note

Notice that the ***Base >*** *field and the* ***Find Pattern*** field are interactive. Only a keypad pop-up will appear that is compatible with the base selected. Since ASCII patterns cannot be entered directly, a keypad will not appear for data entry if the base is set to ASCII.

When the pop-up is open, you enter your desired pattern from the keypad (including don't cares). When you finish entering your pattern, close the pop-up by touching Done.

Specifying Edges

You can select a positve-going (↑), negative-going (↓), and either edge (↕) for your trigger.

To specify edges, enter the Trace menu and follow these steps:

1. Touch the field in the bottom left corner of the display. This field is labeled **Edge**. You will see the following pop-up.

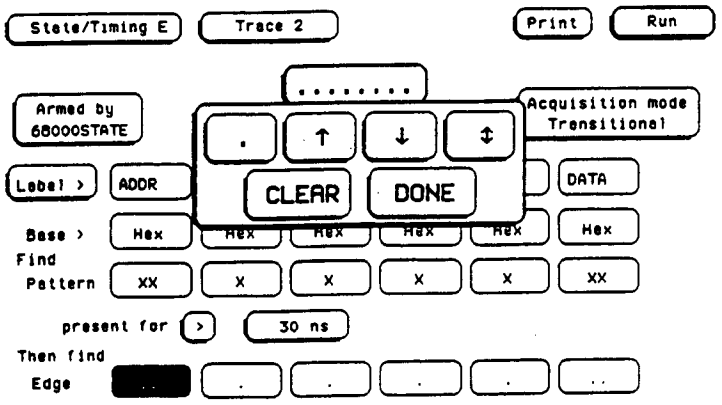


Figure 3-11. Specifying Edges Pop-up Menu

2. When the pop-up appears you can make your edge selection for any bit by placing the cursor, using the KNOB, on the desired bit and touching the period, either edge, or both edges field. 3. After you have made your edge selection, touch **Done**.

Note

*When you close the pop-up after specifying edges, you will see dollar signs (**$$.**) in the **Then find Edge** field if the logic analyzer can't display the edge correctly. This indicates the logic analyzer can't display the data correctly in the number base you have selected.*

4 Using the Menus

Introduction

This chapter contains menu maps of the HP 16510A logic analyzer. Since the front-panel user interface consists mainly of menus that you access to configure the logic analyzer, the menu maps provide quick reference to the menus, menu options, and ultimately the functions of the logic analyzer.

Menu Maps

The following pages show the menu maps of all functions of the logic analyzer. The State/Timing Configuration menu is the logic analyzer's system level menu. The rest of the menus are the subsystem level menus of the logic analyzer.

State/Timing Configuration Menu Map

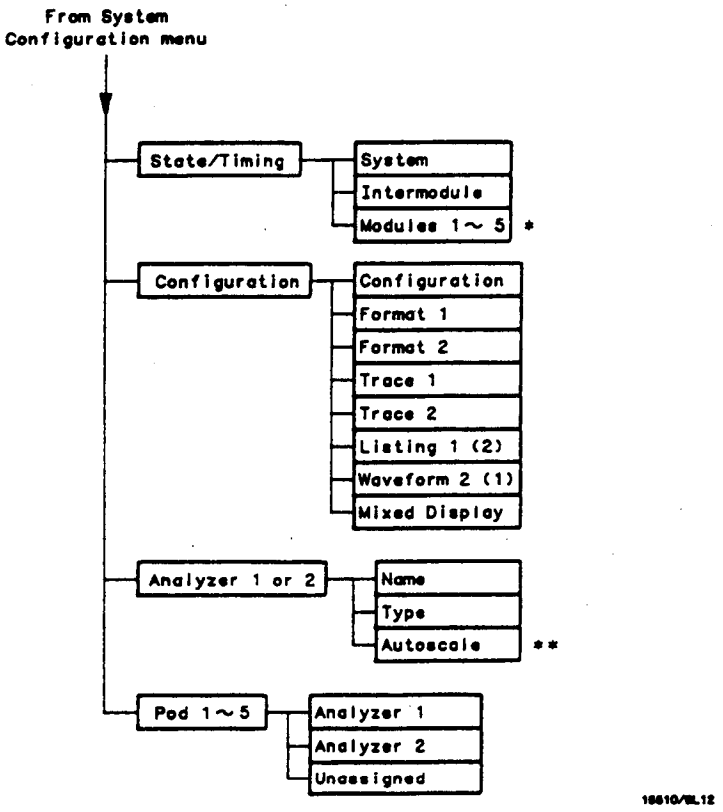


Figure 4-1. State/Timing Configuration Menu Map

Timing Format Menu Map

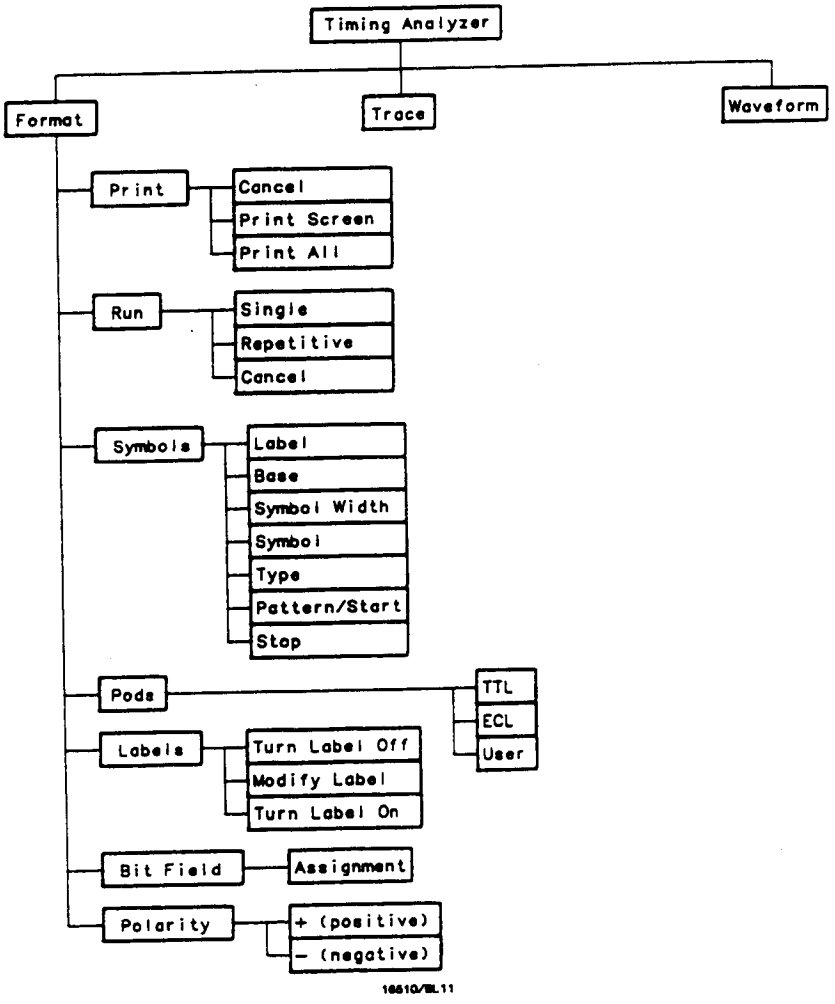
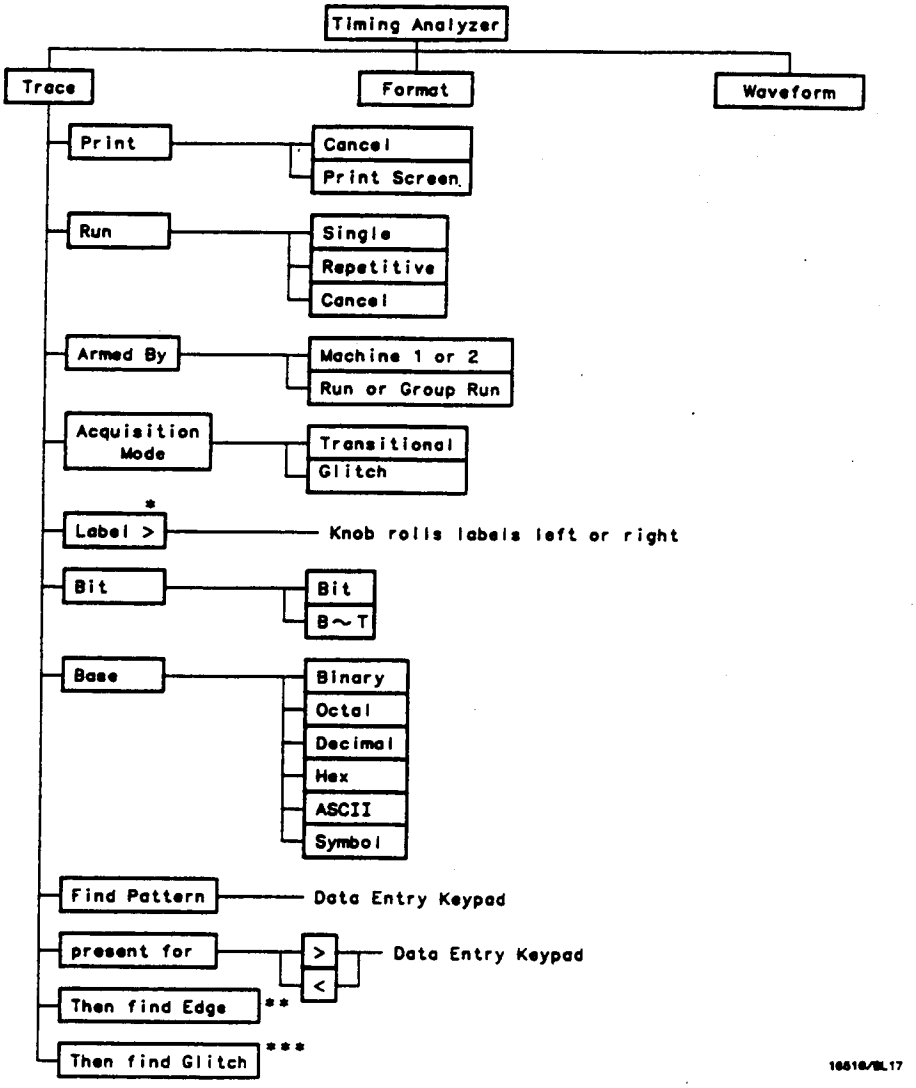


Figure 4-2. Timing Format Menu Map

Timing Trace Menu Map



* Only appears when off-screen labels exist
** Only available when "greater than" is specified in "present for" field
*** Only available when "then find edge" is present and in Glitch mode

Figure 4-3. Timing Trace Menu Map

Timing Waveform Menu Map

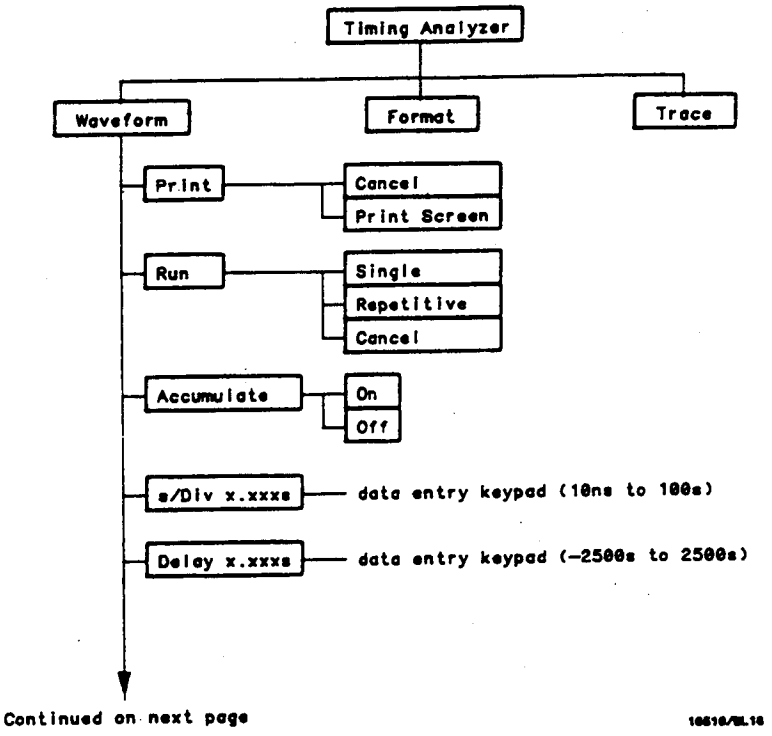


Figure 4-4a. P/O Timing Waveform Menu Map

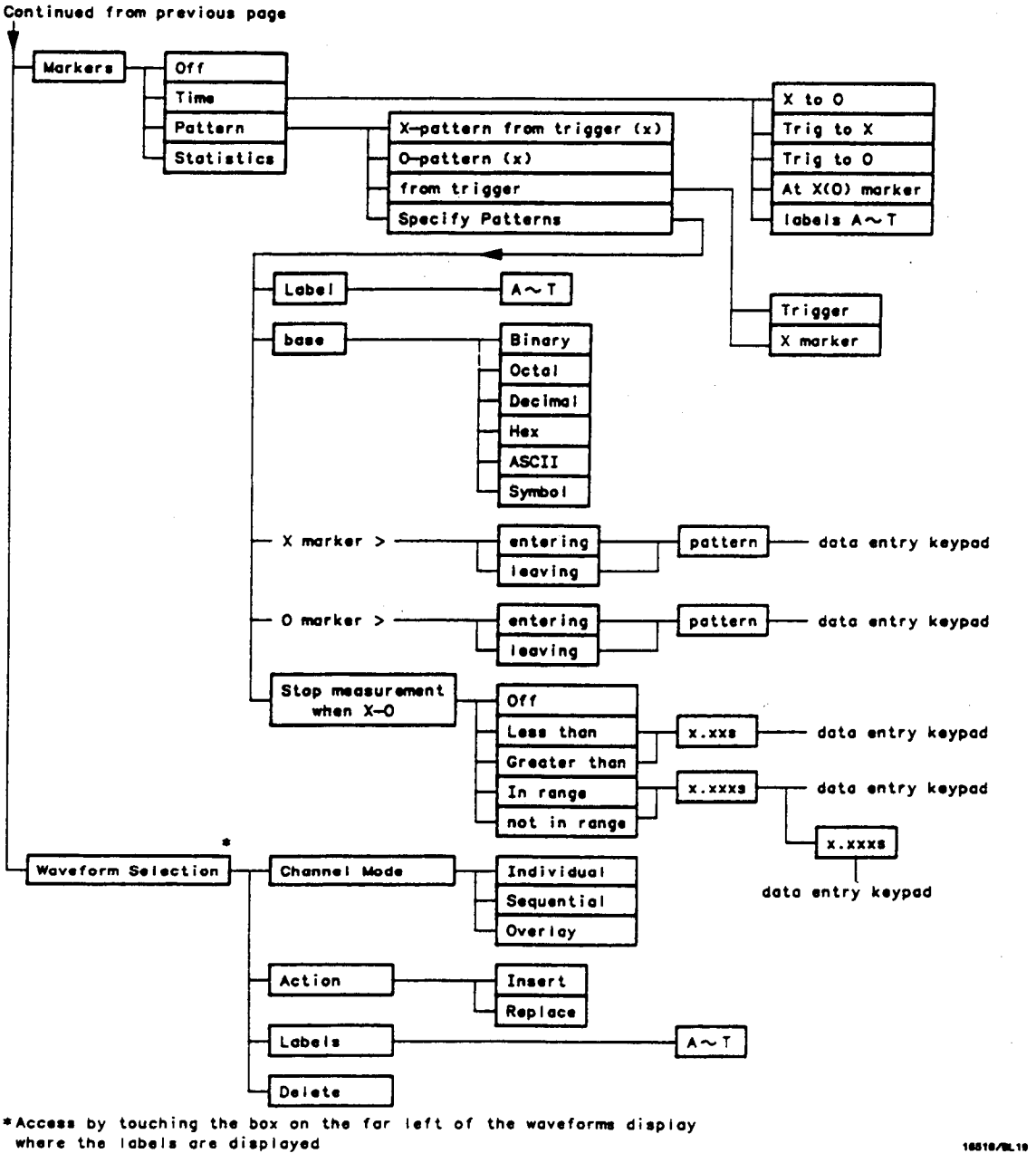


Figure 4-4b. P/O Timing Waveform Menu Map

State Format Menu Map

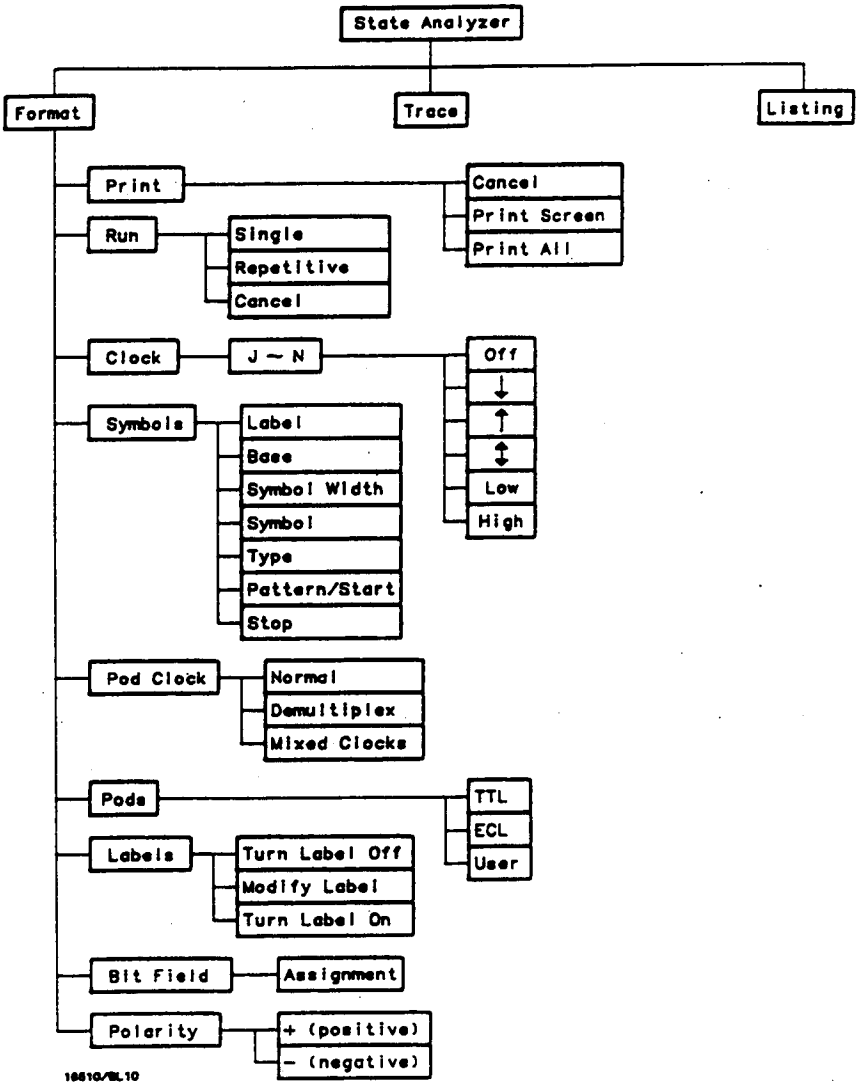


Figure 4-5. State Format Menu Map

State Trace Menu Map

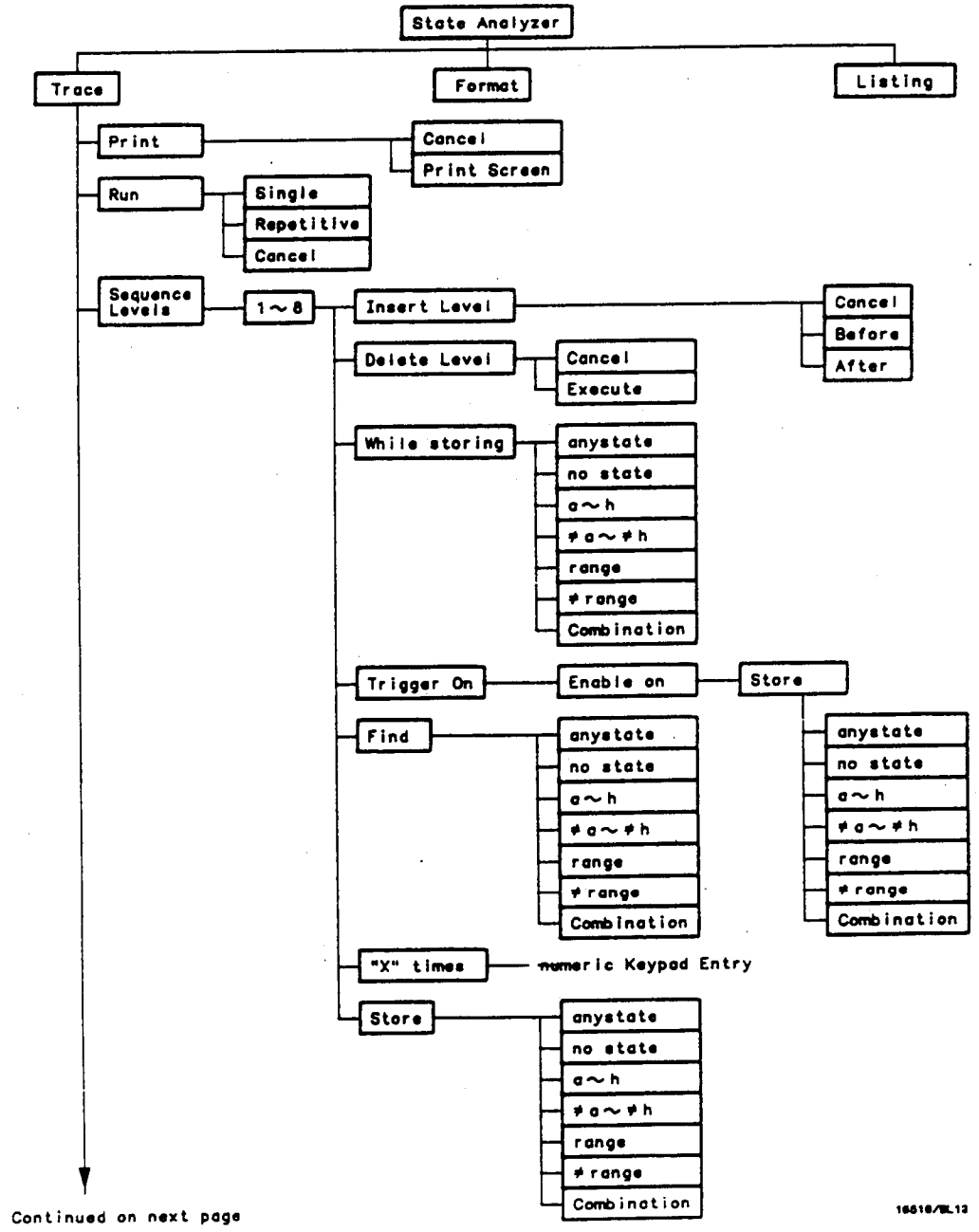


Figure 4-6a. P/O State Trace Menu Map

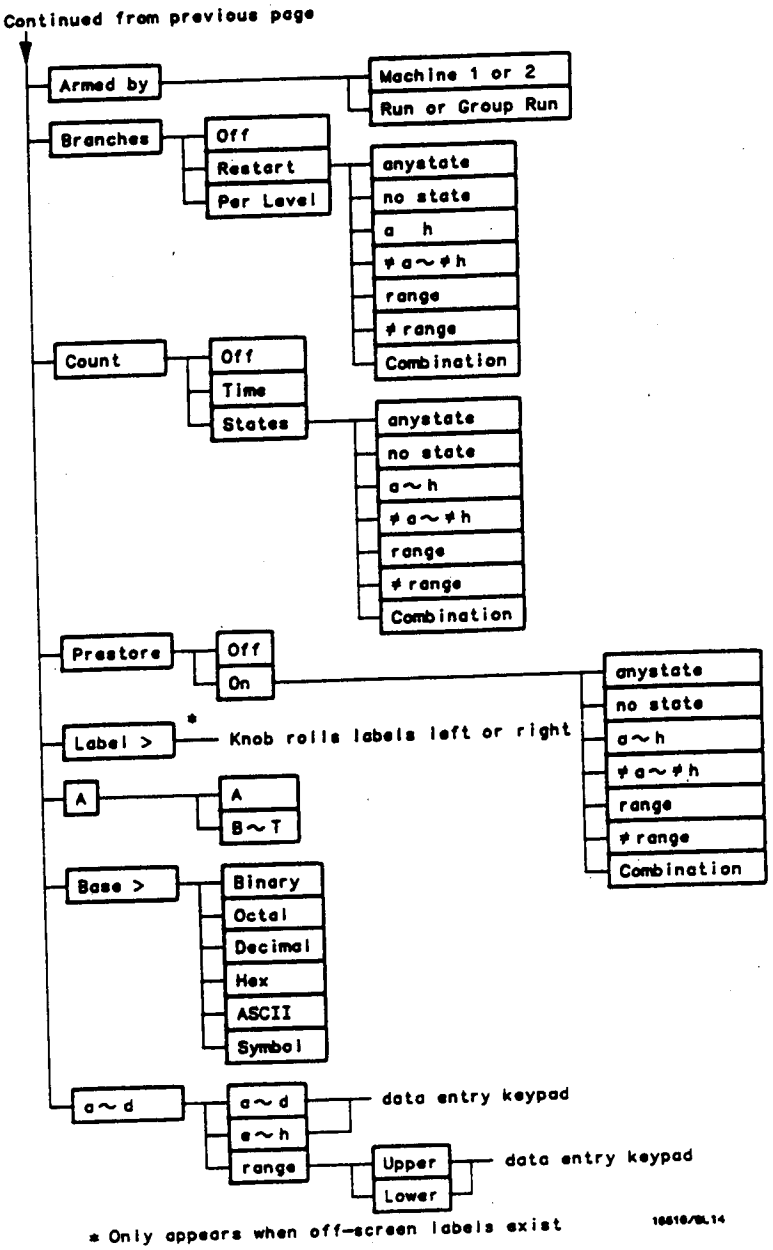


Figure 4-6b. P/O State Trace Menu Map

State Listing Menu Map

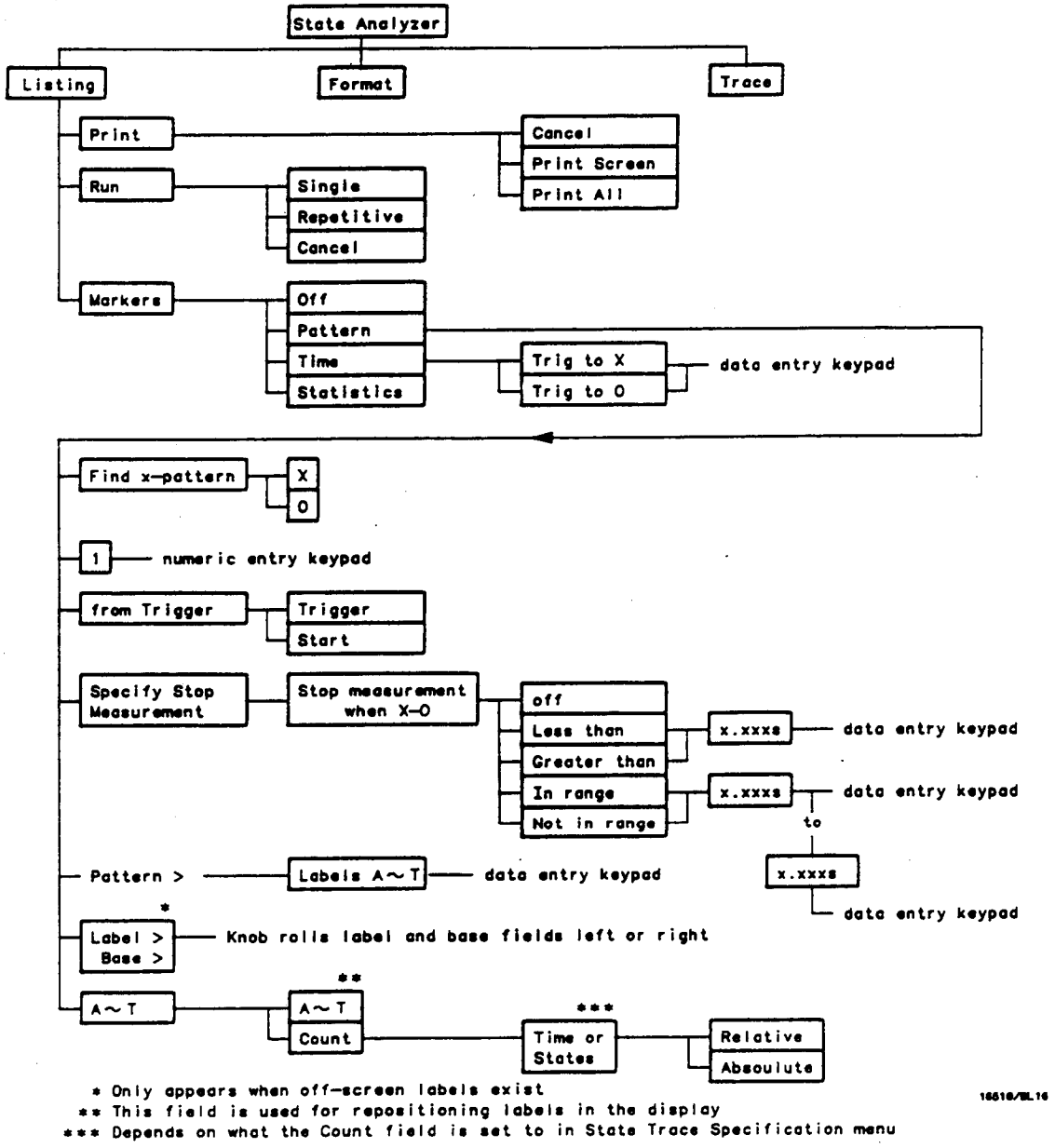
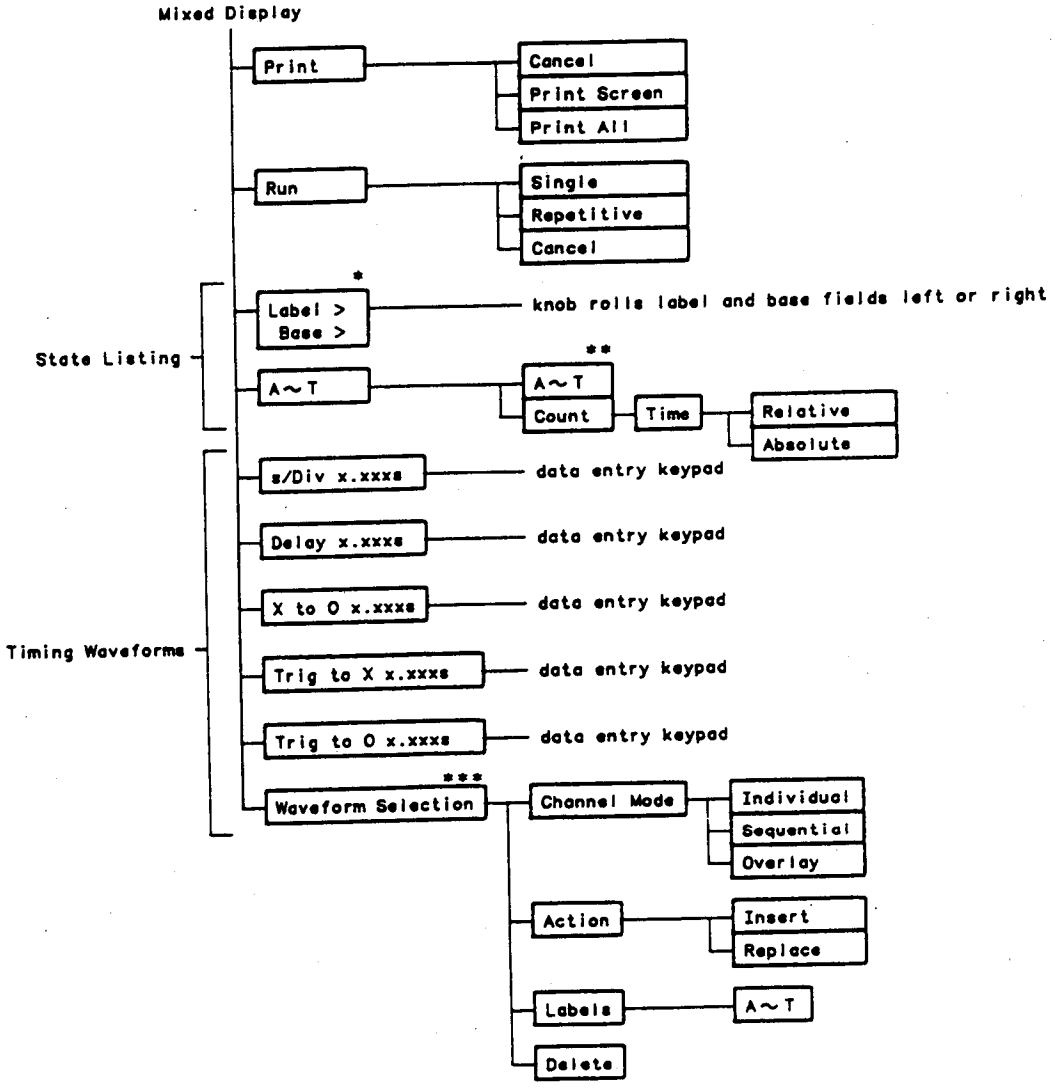


Figure 4-7. State Listing Menu Map

Mixed Display Menu Map



* Only appears when off-screen labels exist
** This field is used for repositioning labels in the display
*** Access by touching the box on the far left of the waveforms display where the labels are displayed

Figure 4-8. Mixed Display Menu Map

5 Menus

Introduction

This chapter describes the menus and pop-up menus that you will use on your logic analyzer. The purpose and functions of each menu are explained in detail, and we have included many illustrations and examples to make the explanations clearer.

The main menus of the logic analyzer are grouped into two categories: System Level Menus and Subsystem Level Menus. The System Level Menu is:

- State/Timing Configuration Menu

The Subsystem Level Menus are:

- Format (timing and state)
- Trace (timing and state)
- Timing Waveforms
- State Listing

An illustration of each main menu is given at the beginning of the section that describes the menu. In the illustration, the fields are numbered according to the order in which they are discussed to make them easy to reference.

System Level Menu

When the logic analyzer is selected from the System Configuration menu, the State/Timing Configuration menu is displayed. It is in this menu that you configure your logic analyzer in one of four ways: timing analyzer only, state analyzer only, two state analyzers, or one timing analyzer and one state analyzer. You can also name each internal analyzer and assign pods to them.

State/Timing Configuration Menu

The State/Timing Configuration menu for the HP 16510A Logic Analyzer is shown below. The fields in the menu that are numbered in the figure are described in this section.

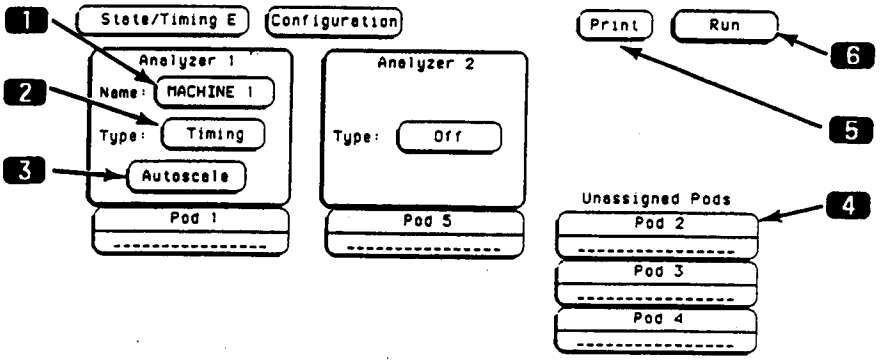


Figure 5-1. State/Timing Configuration Menu

1 Name You name an analyzer by selecting the Name field under it. An alphanumeric pop-up menu will appear. The keypad is similar to a computer keyboard.

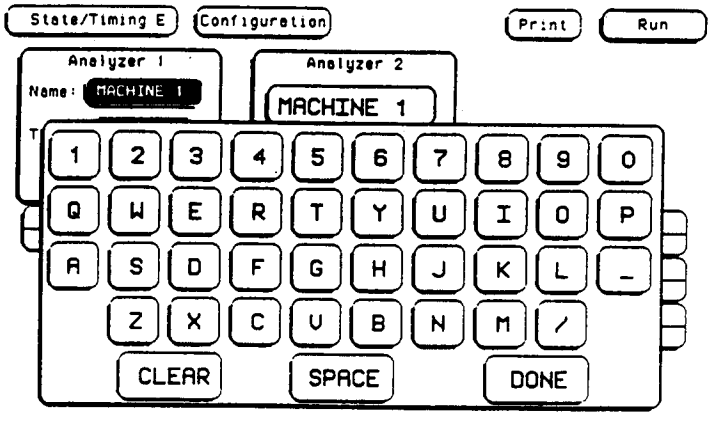


Figure 5-2. Alphanumeric Keypad Pop-up

At the top of the keypad pop-up, is a box where the current name appears when the pop-up opens, and where the new name will appear when you touch keys on the keypad. In the name box is a cursor which indicates in what space your next selection will be placed.

You can name the analyzer in one of two ways. The first way is to position the cursor over the character to be replaced in the pop-up using the KNOB, then touching the new character. The new character appears in the name box.

The second way is to touch **CLEAR**. This clears the entire name from the box and places the cursor at the beginning of the name box in the pop-up.

When you have entered the correct name, touch **DONE**.

2 Type The Type field defines the machine as either a state analyzer or a timing analyzer or indicates that a system performance analysis (SPA) can be done on that analyzer (optional). When this field is touched, a pop-up menu appears. You touch the machine type to make your selection.

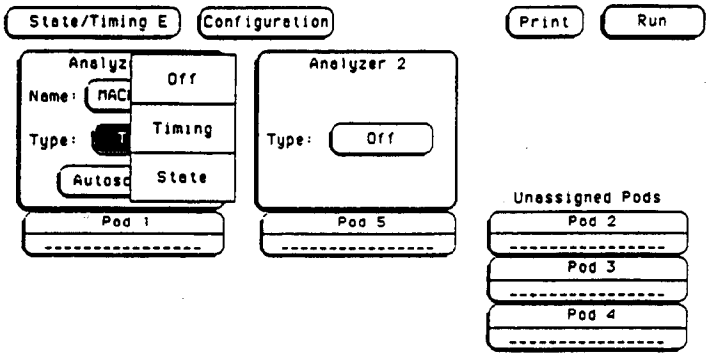


Figure 5-3. Type Pop-up Menu

3 Autoscale The purpose of **Autoscale** is to provide a starting point for setting up a measurement. The Autoscale field only appears on a timing analyzer. When you touch Autoscale, you will see a pop-up with two options: **Cancel** and **Execute**. If you select Cancel, the autoscale is cancelled and control is returned to the State/Timing Configuration menu.

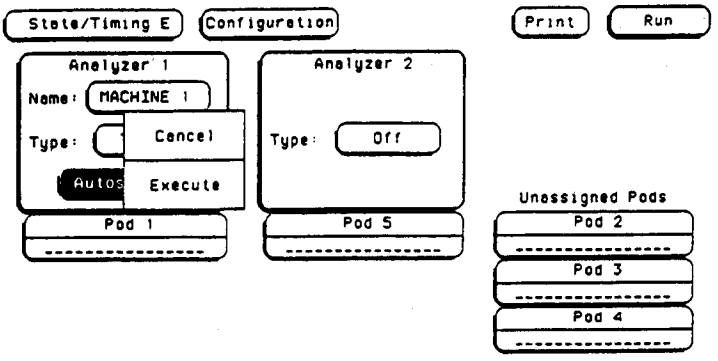


Figure 5-4. Autoscale Pop-up Menu

If you choose Execute, autoscale configures the timing Format and Trace Specification menus and the timing Waveforms menu. Any configurations that you have done will be lost. Autoscale searches for channels with activity on the pods assigned to the timing analyzer and displays them in the Waveforms menu.

Note

Executing autoscale erases all previous configurations for your timing analyzer and turns the other analyzer off. If you don't want this to happen, touch Cancel in the pop-up.

4 Pods Each pod can be assigned to one of the analyzers. When the HP 16510A Logic Analyzer is powered up, Pod 1 is assigned to Analyzer 1 and Pod 5 is assigned to Analyzer 2.

To assign a pod, touch the pod field. With the pop-up that appears, you can assign the pod to Analyzer 1, Analyzer 2, or Unassign it. Making a selection closes the pop-up and moves the pod field to the analyzer to which the pod is assigned.

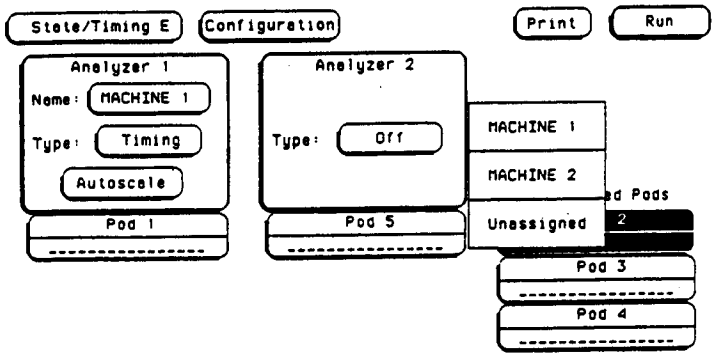


Figure 5-5. Pod Assignment Pop-up Menu

5 Print The Print field allows you to print what is displayed on the screen at the time you initiate the printout. When you touch the Print field, a pop-up appears showing you the print options **Cancel, Print Screen,** and in some menus, **Print All.**

You start a print by touching the **Print** field. When the pop-up appears, you touch either **Print Screen** or **Print All** . The information on the screen is frozen, and the **Print** field changes to **Cancel** and turns red. While the data is being transferred to the printer, the logic analyzer's user-interface is not usable with the exception of the **Cancel** field. When the logic analyzer has completed the data transfer to the printer, the advisory "Print Completed" is displayed and the user-interface is usable again.

If you wish to stop a printout before it is completed, touch **Cancel**. This stops the print, and the message "Print Cancelled" appears in red.

Print Screen. In the Print Screen mode, the printer uses its graphics capabilities so that the printout will look just like the logic analyzer screen.

Print All. The Print All option prints not only what is displayed on screen but what is below, and, in the Format Specification, what is to the right of the screen at the time you initiate the printout.

Note

Make sure the first line you wish to print is in the light blue box at the center of the listing area when you touch ***Print All.*** *Lines above this box will not print.*

Use this option when you want to print all the data in menus like:

- Timing Format Specifications
- State Format Specifications
- State Trace Specifications
- State Listing
- Symbols

If there is information below the screen, as in the State Listing, the information will be printed on multiple pages. In Timing and State Format Specifications, the print will be compressed when necessary to print data that is off-screen to the right.

When you select the **Print All** option, the information on the screen is frozen, and the message "Printing All" appears at the top of the display. Don't worry, this message will not appear in your printout. While the data is being transferred to the printer, the logic analyzer's user-interface is not usable. When the logic analyzer has completed the data transfer to the printer, the advisory "Print Completed" appears and the user-interface is again usable.

If you wish to stop a printout before it is completed, touch **Cancel**. This stops the print and the message "Print Cancelled" appears at the top of the display.

6 Run The **Run** field allows you to start data acquisition. The pop-up that appears when you touch this field contains the trace mode options **Single**, **Repetitive**, and **Cancel**. This field is explained in detail in "Run/Trace Mode" in both the Timing and State Trace specification menus sections of this chapter.

Sub-System Level Menus

The HP 16510A logic analyzer is configured for measurements in the Timing and State Format and Trace Specification menus. The Format menus can be accessed by touching **Format 1** or **2**, and the Trace menus by touching **Trace 1** or **2**.

The **Format Specification** menus let you specify how the logic analyzer groups the input channels from your microprocessor. You can set the threshold levels of the pods assigned to the analyzer, assign labels and channels, specify symbols, and, in the case of the state analyzer, set clocks for triggering.

The **Trace Specification** menus allow you to configure the logic analyzer to capture only the data of interest in your measurement. The logic analyzer acquires data until it triggers at a location that you specify by setting certain parameters for the data. In the timing analyzer you can configure the analyzer to trigger on specific patterns, edges, or glitches. In the state analyzer you can configure the analyzer to trigger on a sequence of states.

At power up, the logic analyzer is configured with a default setting. You can use this default setting to make a test measurement on your system. It can give you an idea of where to start your measurement.

Each of the format and trace specification menus will be covered in this chapter. For examples on setting up configurations for measurements with the timing and state analyzers, refer to your *HP 16510A Getting Started Guide* or chapters 7 through 9 in this manual.

Timing and State Format Specification Menus

At power up the Timing and State Format Specification menus look basically the same, with a few exceptions in the state analyzer. The Timing Format Specification menu looks like that shown below:

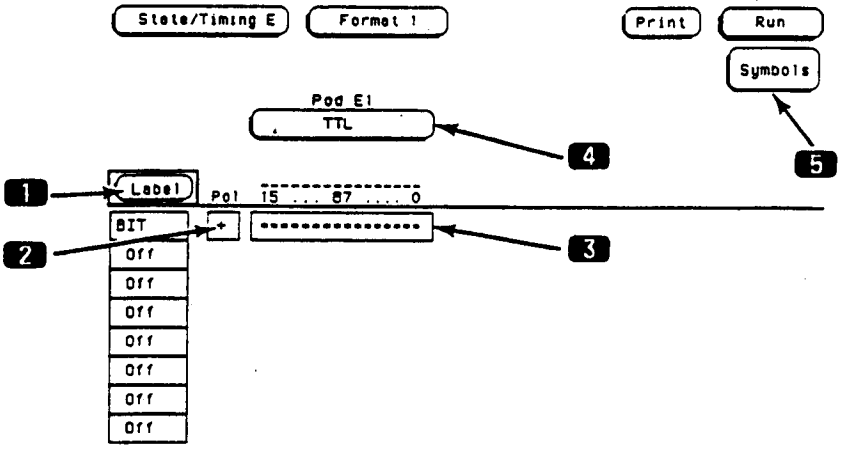


Figure 5-6. Timing Format Specification Menu

The State Format Specification menu for the HP 16510A looks like the following:

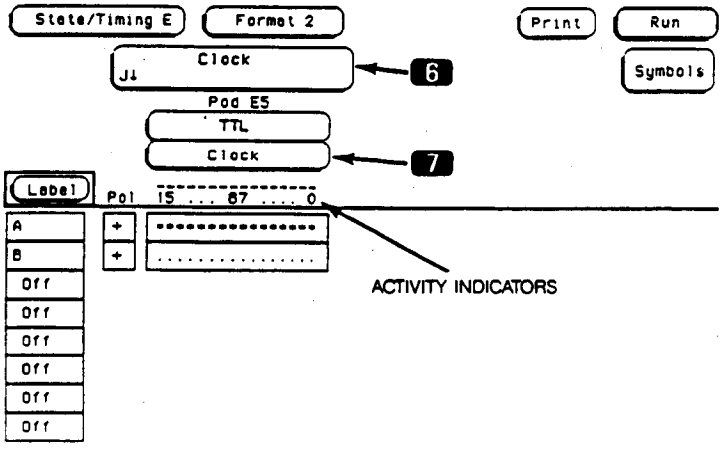


Figure 5-7. State Format Specification Menu

These menus show only one pod assigned to each analyzer at power up. Any number of pods can be assigned to one analyzer, from none to all five. In the **Format** menus, only three pods appear at a time in the display. If there are any pods off screen, an additional field will be present. This field is labeled **Pods** ↔. To view off-screen pods, touch the **Pods** ↔ field and rotate the KNOB. The pods are always positioned so that the lowest numbered pod is on the right and the highest numbered pod is on the left.

Timing and State Format Specification Menu Fields

Seven types of fields are present in the menus. They are:

1) Label
2) Polarity (Pol)
3) Bit assignments
4) Pod threshold
5) Specify Symbols
6) Clock (state analyzer only)
7) Pod Clock (state analyzer only)

A portion of the menu that is not a field is the Activity Indicators display. The indicators appear above the bit numbers of each pod. When the logic analyzer is connected to your target system and the system is running, you will see ↕ in the Activity Indicators display for each channel that has activity. These tell you that the signals on the channels are transitioning.

The fields in the Format menus are described in the following sections. The descriptions apply to both the timing and state analyzers unless noted otherwise.

1 Label

The label column contains 20 Label fields that you can define. Of the 20 labels, the logic analyzer displays only 8 at one time. To view the labels that are off screen, rotate the KNOB. The labels roll up and down.

To access one of the Label fields, touch the desired field. You will see a pop-up menu like that shown below.

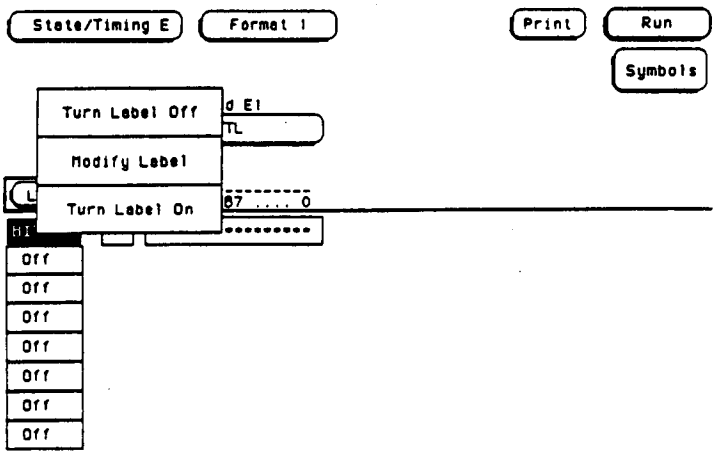


Figure 5-8. Label Pop-up Menu

Turn Label On. Selecting this option turns the label on and gives it a default letter name. If you turned all the labels on they would be named **POD 1** through **T** from top to bottom in the timing analyzer and **A** throughT in the state analyzer. When a label is turned on, bit assignment fields for the label appear to the right of the label under the pods.

Modify Label. If you want to change the name of a label, or want to turn a label on and give it a specific name, you would select the **Modify Label** option. When you do, an alphanumeric keypad pop-up menu appears. You use the pop-up keypad to name the label. A label name can be a maximum of six characters.

Turn Label Off. Selecting this option turns the label off. When a label is turned off, the bit assignments are saved by the logic analyzer. This gives you the option of turning the label back on and still having the bit assignments if you need them. The timing waveforms and state listings are also saved.

You can give the same name to a label in the state analyzer as in the timing analyzer without causing an error. The logic analyzer distinguishes between them. An example of this appears in chapter 7 of the *HP 16510A Getting Started Guide* and chapter 9 of this manual.

2 Polarity (Pol)

Each label has a polarity assigned to it. The default for all the labels is positive (+) polarity. You can change the polarity of a label by touching the the polarity field. This toggles the polarity between positive (+) and negative (-).

In the state analyzer, negative polarity inverts all the data. In the timing analyzer, negative polarity inverts all the data, but doesn't change the actual waveforms in the Timing Waveforms Menu.

3 Bit Assignment

The bit assignment fields allow you to assign bits (channels) to labels. Above each column of the bit assignment fields is a line that tells you the bit numbers from 0 to 15, with the left bit numbered 15 and the right bit numbered 0. This line helps you know exactly which bits you are assigning.

The convention for bit assignment is:

- * (asterisk) indicates assigned bit
- . (period) indicates unassigned bit

At power up the 16 bits of Pod 1 are assigned to the timing analyzer, and the 16 bits of Pod 5 are assigned to the state analyzer.

To change a bit assignment configuration, touch a bit assignment field. You will see the following pop-up menu.

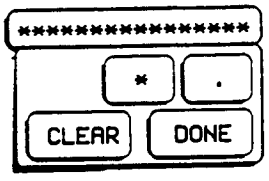


Figure 5-9. Bit Assignment Pop-up Menu

Use the KNOB to move the cursor to an asterisk or a period you wish to change. Touch the desired state (asterisk or period) in the pop-up. When the bits (channels) are assigned as desired, touch **DONE**. This closes the pop-up and displays the new bit assignment in the Format Specification menu.

Assigning one channel per label may be handy in some applications. This is illustrated in chapter 7 of the *HP 16510A Getting Started Guide*. Also, you can assign a channel to more than one label, but this usually isn't desired.

Labels may have from 1 to 32 channels assigned to them. If you try to assign more than 32 channels to a label, the logic analyzer will beep, indicating an error, and a message will appear at the top of the screen telling you that 32 channels per label is maximum.

Channels assigned to a label are numbered from right to left by the logic analyzer. The least significant assigned bit (LSB) on the far right is numbered 0, the next assigned bit is numbered 1, and so on. Since the maximun of 32 channels can be assigned to one label, the highest number that can be given to a channel is 31. Although labels can contain split fields, assigned channels are always numbered consecutively within a label. The numbering of channels is illustrated with the figure below.

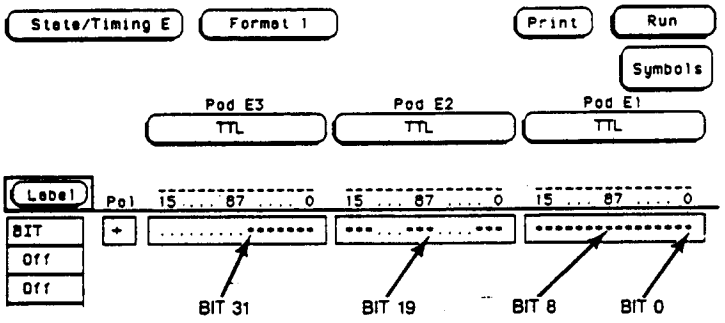


Figure 5-10. Numbering of Assigned Bits

4 Pod Threshold Each pod has a threshold level assigned to it. Threshold levels may be defined for Pods 1, 2 and 3 individually, and one threshold for Pods 4 and 5. It doesn't matter if Pods 4 and 5 are assigned to different analyzers. Changing the threshold of either pod 4 or 5 changes the threshold of the other.

If you touch the pod threshold fields you will see the following pop-up menu.

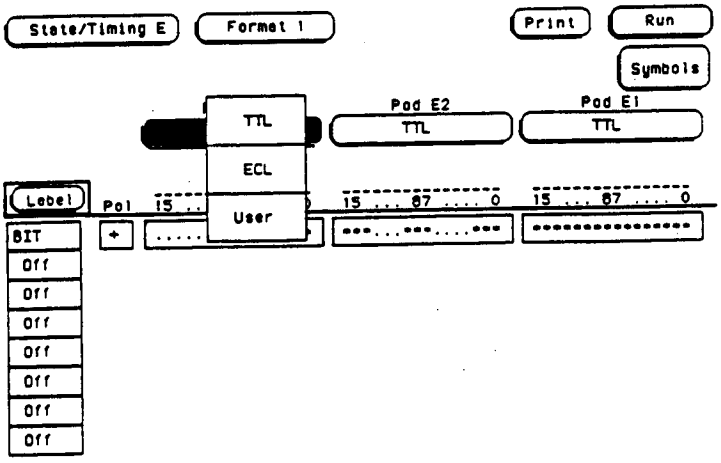


Figure 5-11. Pod Threshold Pop-up Menu

TTL sets the threshold at +1.6 volts, and ECL sets the threshold at -1.3 volts.

The **User** option lets you set the threshold to a specific voltage between -9.9 V and +9.9 V. If you select this option you will see a numeric entry keypad pop-up menu as shown.

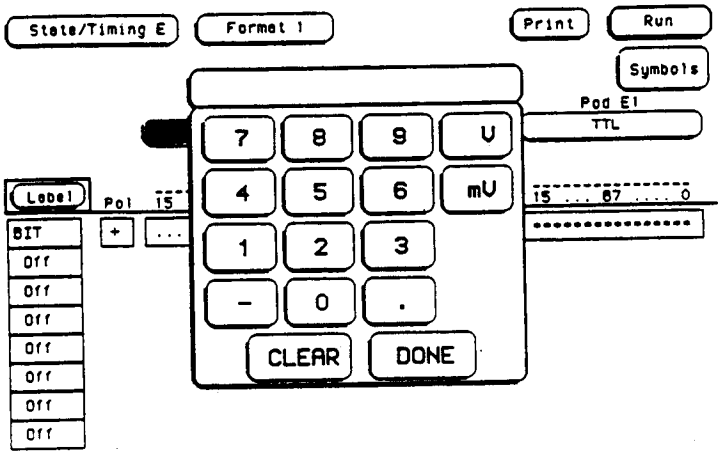


Figure 5-12. Numeric Entry Keypad Pop-up Menu

You enter a threshold in the pop-up with the keypad by touching the desired value, units and polarity. When the correct threshold voltage is displayed, touch **DONE**. The pop-up will close and the new threshold will be placed in the pod threshold field.

In the state analyzer, the same threshold level applies to a pod's clock as to its 16 data bits.

5 Specify Symbols

The logic analyzer supplies **Timing** and **State Symbol Tables** in which you can define a mnemonic for a specific bit pattern of a label. When measurements are made by the logic analyzer, the mnemonic is displayed where the bit pattern occurs if the **Symbol** base is selected.

It is possible for you to specify up to 200 symbols in the logic analyzer. If you have only one of the internal analyzers on, all 200 symbols can be defined in it. If both analyzers are on, the 200 symbols are split between the two. For example, analyzer 1 may have 150, leaving 50 available for analyzer 2.

To access the **Symbol Table** in either the State or Timing **Format** Specification menus, touch the **Symbols** field. You will see a new menu as shown. This is the default setting for the **Symbol Table** in both the timing and state analyzers.

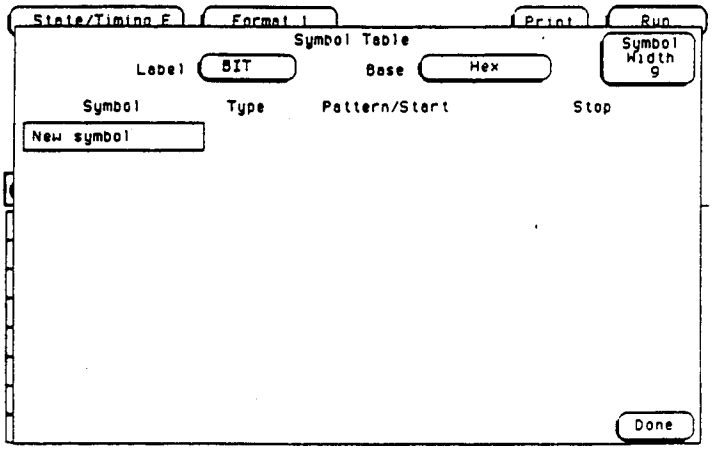


Figure 5-13. Symbol Table Menu

There are four fields in the Symbol Table menu. They are:

- Label
- Base
- Symbol Width
- Symbol name

Label. The Label field identifies the label for which you are specifying the symbols. If you select this field you will get a pop-up that lists all the labels that are turned on in that analyzer.

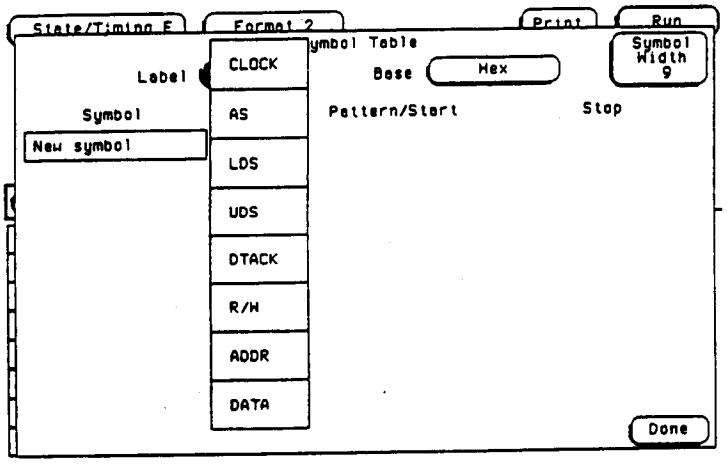


Figure 5-14. Label Pop-up Menu

Each label has a separate symbol table. This allows you to give the same name to symbols defined under different labels. In the Label pop-up touch the label for which you wish to specify symbols.

Base. The Base field tells you the number base in which the pattern will be specified. The base you choose here will appear in the **Find Pattern** field of the Timing Trace Specification menu in the timing analyzer, or the pattern field of the State Trace Specification menu in the state analyzer. These are covered later in this chapter.

To change the base, touch the current base. You will see the following pop-up menu.

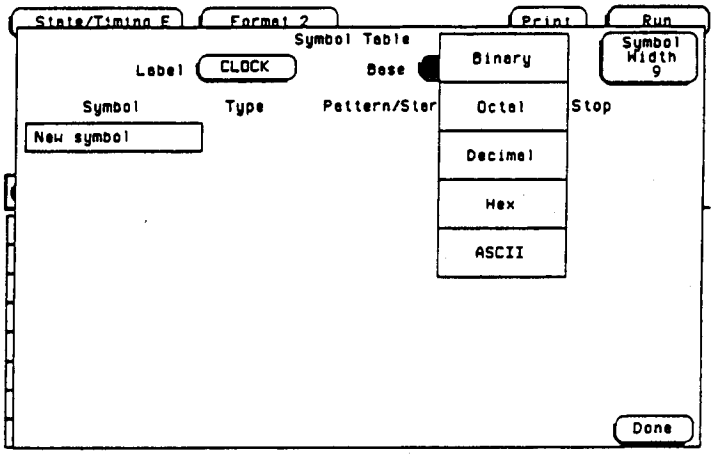


Figure 5-15. Base Pop-up Menu

If more than 20 channels are assigned to a label, the **Binary** option is not offered in the pop-up. The reason for this is that when a symbol is specified as a range, there is only enough room for 20 bits to be displayed on the screen.

When you decide which base you want to work in, choose that option from the number **Base** pop-up menu.

If you choose the **ASCII** option, you can see what ASCII characters the pattern and ranges defined by your symbols represent. ASCII characters represented by the decimal numbers 0 to 127 (hex 00 to 7F) are offered on your logic analyzer. Specifying patterns and ranges for symbols is discussed in the next section.

Note

You cannot specify a pattern or range when the base is ASCII. First define the pattern or range in one of the other bases, then switch to ***ASCII*** *to see the ASCII characters.*

Symbol Width. The Symbol Width field lets you specify how many characters of the symbol name will be displayed when the symbol is referenced in the Timing and State Trace Specification menus, the Timing Waveforms menu, or the State Listing menu. Selecting this field gives you the following pop-up.

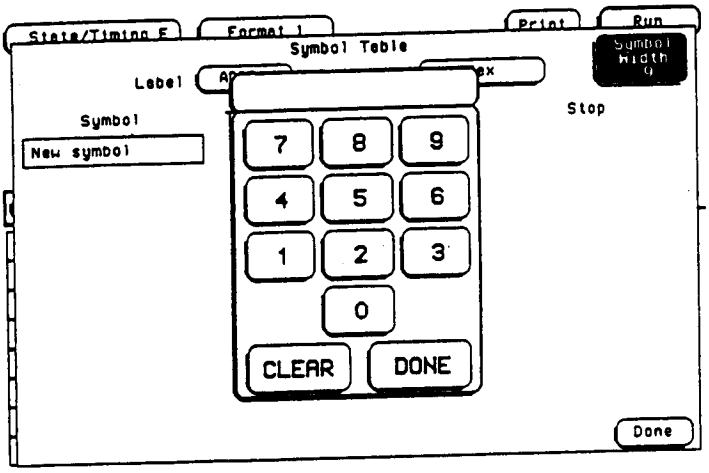


Figure 5-16. Symbol Width Pop-up Menu

You can have the logic analyzer display from 1 to all 16 of the characters in the symbol name. This is covered more in the sections on the Trace menus, the Waveforms menu, and the State Listing menu later in this chapter.

Symbol Name. When you first access the Symbol Table, there are no symbols specified. The symbol name field reads **New Symbol.** If you select this field an alphanumeric keypad pop-up menu appears. Use the keypad to enter the name of your symbol. A maximum of 16 characters can be used in the name of a symbol.

When you touch **DONE** field in the keypad pop-up menu, the name of the symbol appears in the symbol name field, and two more fields appear in the display to the right of the symbol name.

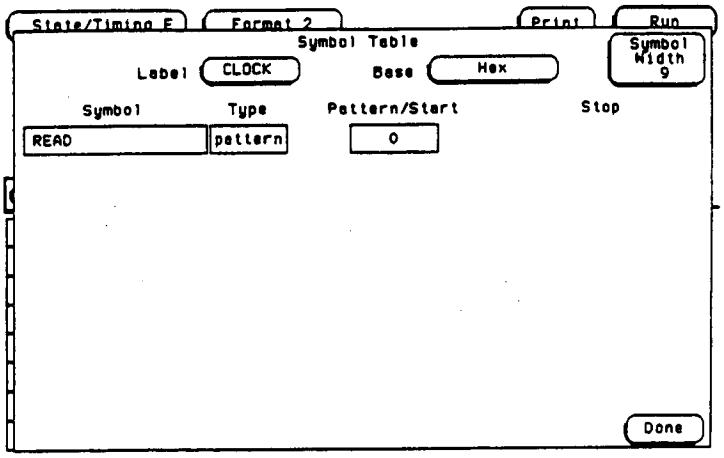


Figure 5-17. Symbol Defined as a Pattern

The first of these fields defines the symbol as either a pattern or a range. If you touch this field, it will toggle between **pattern** and **range**.

When the symbol is defined as a pattern, one field **(Pattern/start)** appears to specify what the pattern is. Touching this field displays a pop-up with which you can specify the pattern. Use the keypad and the **X** (Don't Care) key to enter the pattern.

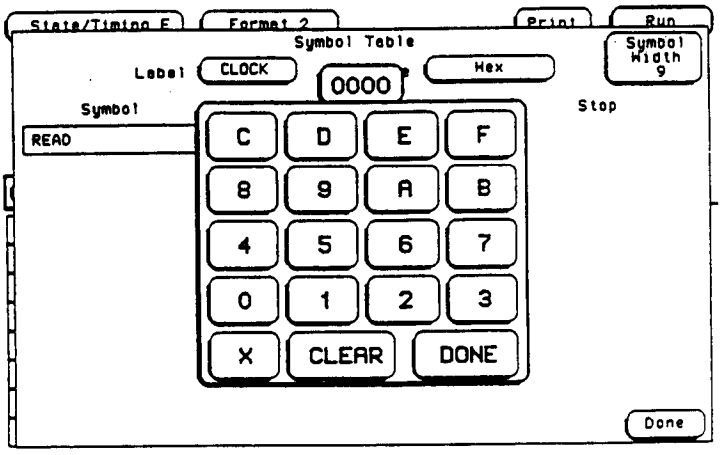


Figure 5-18. Specify Pattern Pop-up

If the symbol is defined as a range, two fields appear in which you specify the upper and lower boundaries of the range. The fields are **Pattern/Start** and **Stop**.

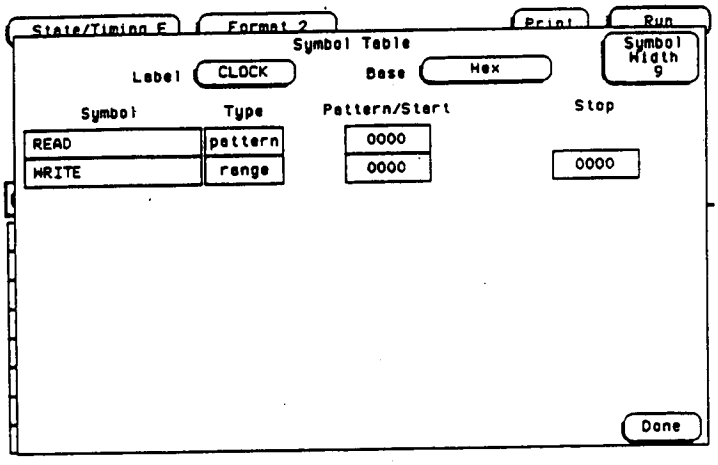


Figure 5-19. Symbol Defined as a Range

Touching either of these fields gives you a pop-up with which you can specify the boundary of the range.

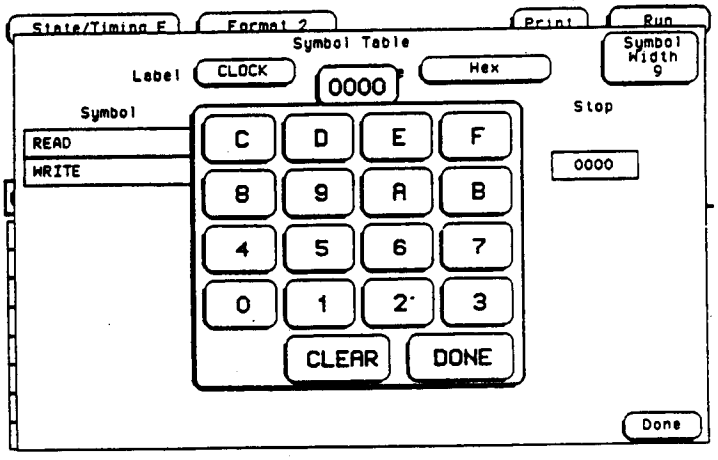


Figure 5-20. Specify Range Pop-up

You can specify ranges that overlap or are nested within each other. They must be specific. Don't cares are not allowed.

The logic analyzer gives patterns priority over ranges when displaying measurements. This will be covered in more detail in the sections "Timing Waveforms Menus" and "State Listing Menus" later in this chapter. To add more symbols to your symbol table, touch the field of the last symbol defined. A pop-up menu appears as shown.

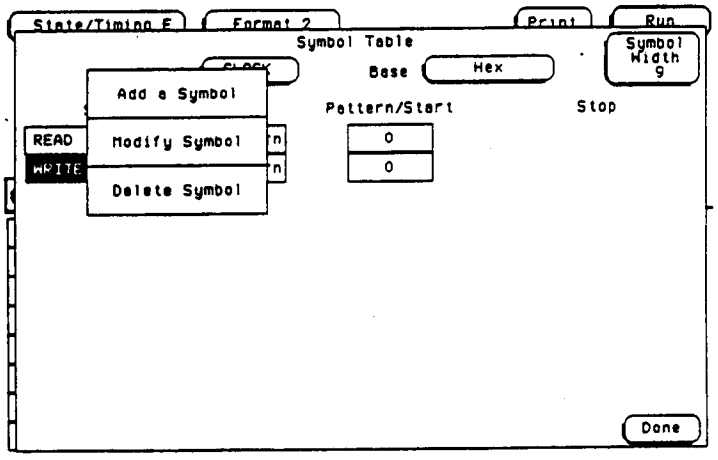


Figure 5-21. Symbol Pop-up Menu

The first option in the pop-up is **Add a Symbol**. It allows you to add another symbol. When you select it, you will see an alphanumeric pop-up menu. Use the keypad to enter the name of your new symbol. When you select Done, your new symbol will appear in the Symbol Table.

The second option in the pop-up is **Modify symbol**. If you select this option, you will see an alphanumeric pop-up menu with which you can change the name of the symbol.

The third option in the pop-up is **Delete Symbol**. If you select this option, the symbol will be deleted from the Symbol Table.

Leaving the Symbol Table Menu. When you have specified all your symbols, you can leave the Symbol Table menu by touching **Done**. This puts you back in the Format Specification menu that you were in before entering the Symbol Table.

6 Clock The Clock field is present in the Format Specification menu only in the state analyzer. This field displays the clocks that are to be used to clock the logic analyzer. The display will be referred to as the "clocking arrangement."

The HP 16510A Logic Analyzer has five clock channels, each of which is on a pod. The clocks are connected through the pods simply for convenience. The clock channels are labeled J, K, L, M, and N and are on pods 1 through 5, respectively. The clocking of the state analyzer is synchronous with your system because the analyzer uses the clocks present in your system that assure valid data.

When you select the Clock field, you will see the following pop-up menu with which you specify the clock.

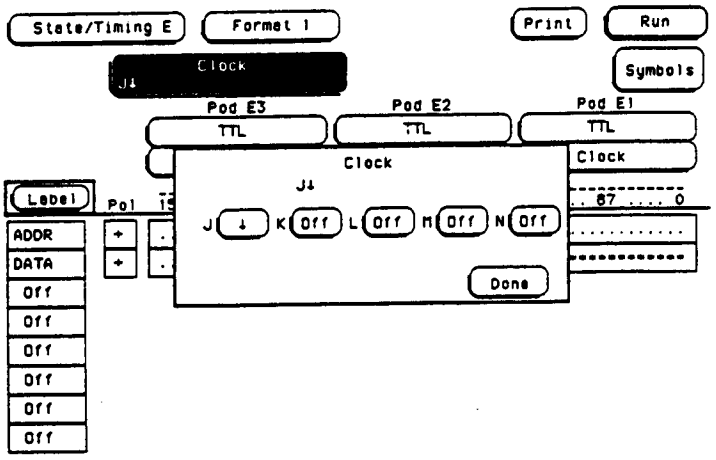


Figure 5-22. Clock Pop-up Menu

You can use one of the clocks alone or combine them to build one clocking arrangement.

If you select a field to the right of one of the clocks in the pop-up, you will see another pop-up menu:

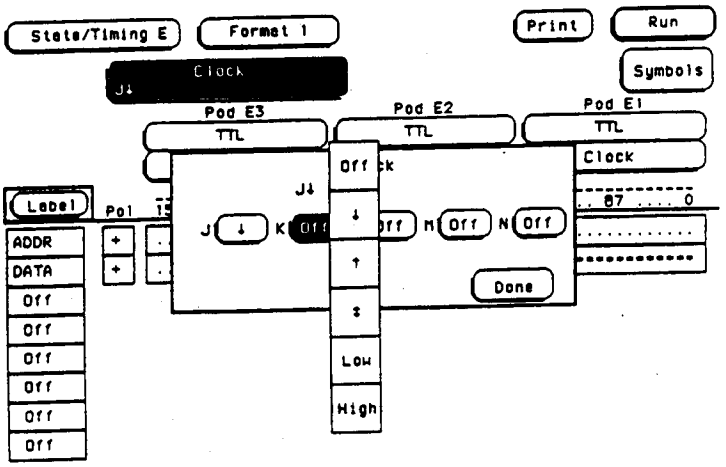


Figure 5-23. Single Clock Pop-up Menu

With this menu you set the condition needed by each clock. You can specify that the logic analyzer looks for the negative edge of the clock, the positive edge, either edge, a high level, or a low level, or you can turn the clock off.

The clocks are combined by ORing and ANDing them. Clock edges are ORed to clock edges, clock levels are ORed to clock levels, and clock edges are ANDed to clock levels.

For example, if you select ↓ for the J clock, ↑ for the K clock, **High** for the M clock, and **Low** for the N clock, the resulting clocking arrangement will appear in the display as:

```
Clock
(J↓+K↑)•(M=1+N=0)
```

Figure 5-24. Example of a Clocking Arrangement

With this arrangement, the logic analyzer will clock the data when there is a negative edge of the J clock OR a positive edge of the K clock, AND when there is a high level on the M clock OR a low level on the N clock.

You must always specify at least one clock edge. If you try to use only clock levels, the logic analyzer will display a message telling you that at least one edge is required.

7 Pod Clock Your logic analyzer has the capability of clocking data in three different ways. The pod **Clock** fields in the **State Format Specification** menu allow you to specify which of the three ways you want to clock the data.

Each pod assigned to the state analyzer has a pod **Clock** field associated with it. As with the Clock field discussed in the previous section, the pod Clock fields are present only in the state analyzer. Selecting one of the pod **Clock** fields gives you the following pop-up menu:

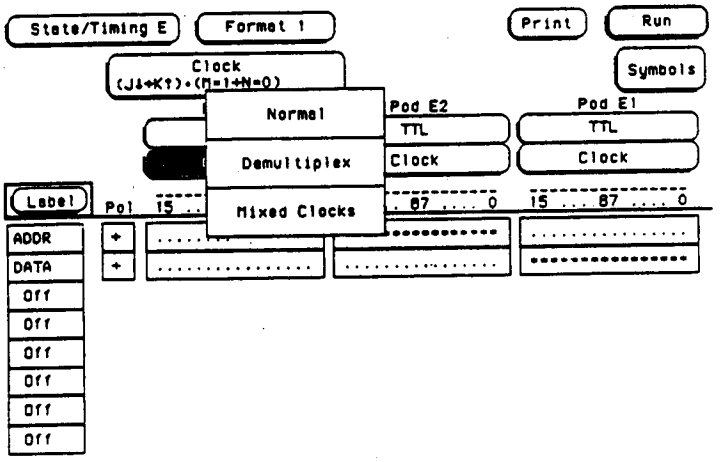


Figure 5-25. Pod Clock Field Pop-up Menu

Normal. This option specifies that clocking will be done in single phase. That is, the clocking arrangement located in the Clock field above the pods in the State Format Specification menu will be used to clock all data (pods) assigned to this machine.

For example, suppose that the Clock field looks like the following:



Figure 5-26. Example of a Clocking Arrangement

In Normal mode the state analyzer will sample data present on all pods assigned to this machine on a negative edge of the J clock OR on a positive edge of the K clock.

Demultiplex. With the HP 16510A Logic Analyzer, you can clock two different types of data that occur on the same lines. For instance, lines that transfer both address and data information need to be clocked at different times in order to get the right information at the right time. The Demultiplex option provides the means to do this.

When you select the Demultiplex option, the pod Clock field changes to **Master | Slave**, and two clock fields appear above the pods where just one Clock field used to be. These fields are the **Master Clock** and **Slave Clock**, as shown:

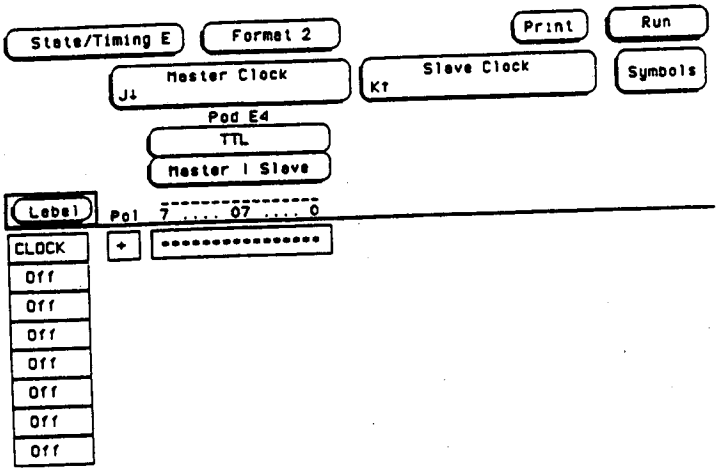


Figure 5-27. Master Clock and Slave Clock

Demultiplexing is done on the data lines of the specified pod to read only the lower eight bits. This is two phase clocking, with the **Master Clock** following the **Slave Clock**. The analyzer first looks for the clocking arrangement that you specify in the **Slave Clock**. When it sees that, the analyzer clocks the data present on bits 0-7 of the pod, then waits for the clocking arrangement that you specify in the **Master Clock**. When it sees that clocking arrangement, it again clocks the data present on bits 0-7 of the pod. The upper eight bits of the pod are ignored and don't need to be connected to your system.

Notice that the bit numbers that appear above the bit assignment field have changed. The bits are now numbered **7....07....0** instead of **15....87....0**. This helps you set up the analyzer to clock the right information at the right time.

The address/data lines AD0-AD7 on the 8085 microprocessor are an example for **Demultiplex**. During part of the operating time the lines have an address on them, and during other times they have data on them. Hook the lower eight bits of one of the pods to these eight lines and set the Slave and Master Clocks for the pod such that they clock the data and the address at the proper time.

In this example, you may choose to assign the bits in the State Format Specification menu similar to that shown in the following figure. In this case you would want to clock the address with the Slave Clock and the data with the Master Clock.

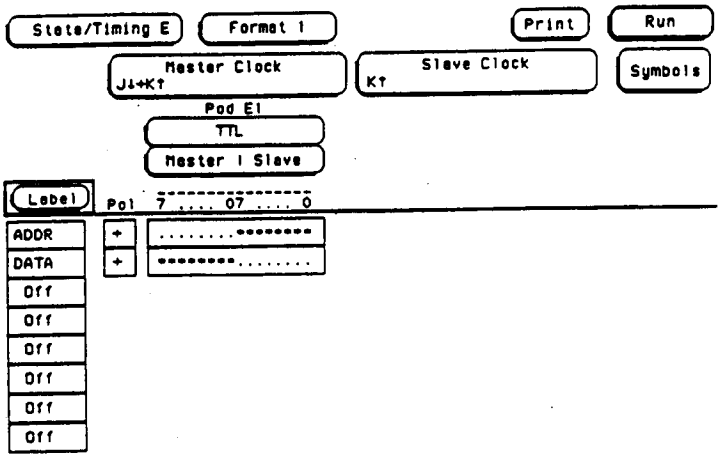


Figure 5-28. Bit Assignments for Master and Slave Clocks

The Master and Slave Clocks can have the same clocking arrangements. The clocking is still done the same way, with the lower eight bits being clocked first on the Slave Clock, then on the Master Clock.

Mixed Clocks. The **Mixed Clocks** option allows you to clock the lower eight bits of a pod separately from the upper eight bits. The state analyzer uses Master and Slave Clocks to do this. If you select this option in the pod Clock pop-up, the pod Clock field changes to **Master | Slave**, and two Clock fields, **Master** and **Slave**, appear above the pods.

As in Demultiplex, the Master Clock follows the Slave Clock. The state analyzer looks for the clocking arrangement given by Slave Clock and clocks the lower eight bits. Then it looks for the clock arrangement given by the Master Clock and clocks the upper eight bits. Unlike Demultiplex, all 16 bits of a pod are sampled.

The Master and Slave Clocks can have the same clocking arrangements. The clocking is still done the same way, with the lower eight bits clocked on the Slave Clock and the upper eight bits clocked on the Master Clock.

Timing Trace Specification Menu

The Timing Trace Specification menu lets you specify the trigger point for the logic analyzer to start capturing data and the manner in which the analyzer will capture data. You configure the timing analyzer to find a pattern first and then a transition in the signal or signals.

The menu looks like that shown below. This is the default setting for the menu.

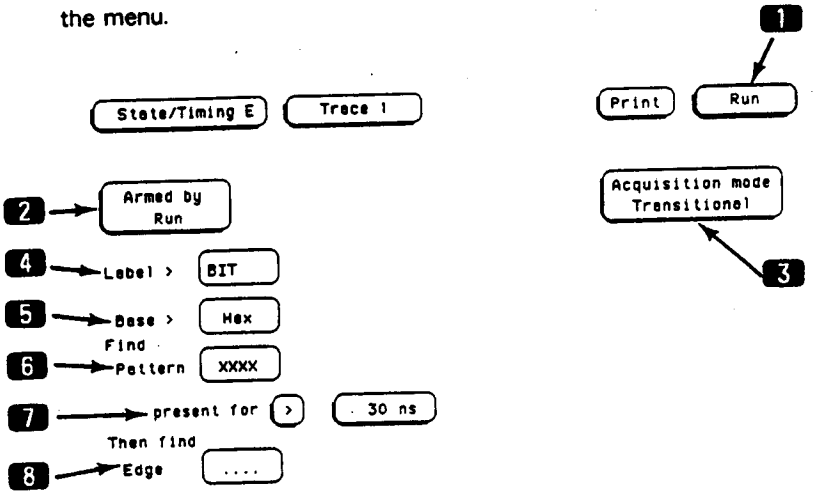


Figure 5-29. Timing Trace Specification Menu

Timing Trace Specification Menu Fields

The fields in the Timing Trace Specification menu are:

1) Run/Trace Mode
2) Armed by
3) Acquisition mode
4) Label
5) Base
6) Find Pattern
7) Pattern Duration (present for _____)
8) Then find Edge

These are described in the following sections.

1 Run/Trace Mode

You specify the mode in which the timing analyzer will trace data when you touch **Run**. You have two choices for trace mode: Single and Repetitive. When you touch **Run** and hold your finger on the field, you will see the following pop-up menu:

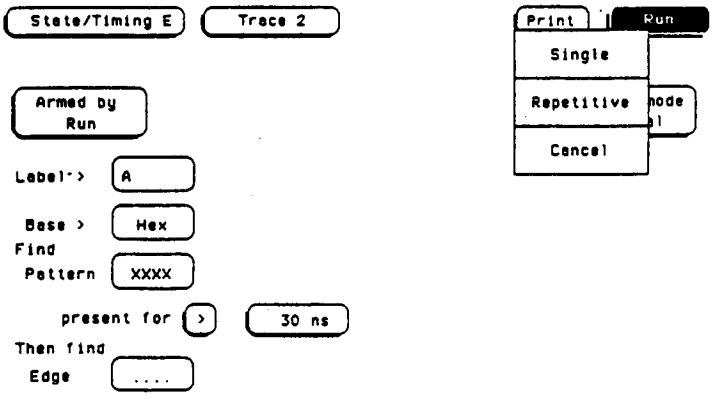


Figure 5-30. Run field pop-up Menu

You select the trace mode by touching the **Run** field, and, without lifting your finger from the screen, move it to the desired trace mode. When you lift your finger, the logic analyzer traces data in the mode you specify. If you wish to abort the trace after you touch **Run** but before the trace starts, move your finger to **Cancel** before lifting your finger.

Single Trace mode acquires data once per trace. **Repetitive Trace** mode repeats single acquisitions until **Stop** is touched, or until the time interval between two specified patterns is less than or greater than a specified value, or within or not within a specified range. The **Stop Measurement** feature is explained in detail in "Markers Pattern" in both the "Timing Waveforms" and "State Listing" sections of Chapter 6 of this manual.

2 Armed By The **Armed By** field is present when more than one analyzer is on at the same time. The Armed by field lets you specify how your timing analyzer is to be armed. The analyzer can be armed by **Run**, the other analyzer, or an external arm from the IMB (Intermodule Bus). "Intermodule Measurements" are covered in chapter 10 of the *HP 16500A Reference Manual*.

When you select the Armed by field, a pop-up menu appears like that shown below. Use this menu to select the arming option for your analyzer.

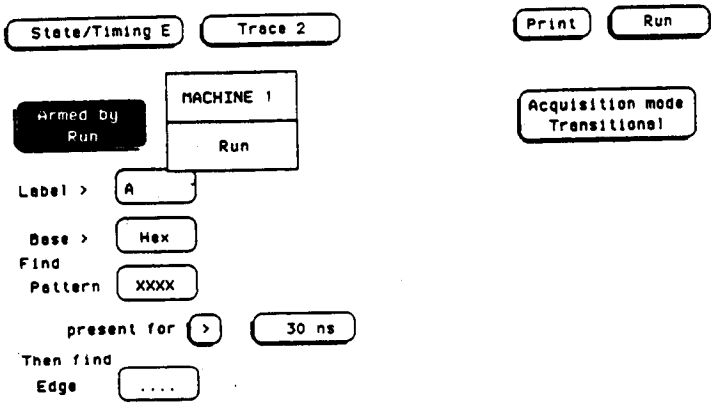


Figure 5-31. Armed By Pop-up Menu

3 Acquisition Mode The Acquisition mode field allows you to specify the mode in which you want the timing analyzer to acquire data. You are given two choices for the mode of acquisition: Transitional and Glitch. When you touch this field, the field toggles from one mode to the other.

Transitional Acquisition Mode. When the logic analyzer is operating in the Transitional Acquisition mode, it samples the data at regular intervals, but it stores data in memory only when there have been transitions in the signals since the last data sample was stored. A time tag that is stored with each sample allows reconstruction of the samples in the Timing Waveforms display.

Transitional timing always samples at a rate of 100 MHz (10 ns/sample). This provides maximum timing resolution even in records that span long time windows. Time covered by a full memory acquisition varies with the number of pattern changes in the data. If there are many transitions, the data may end prior to the end of the time window desired because the memory is full. However, a prestore qualification in your logic analyzer insures that data will be captured and displayed between the left side of the screen and the trigger point.

The figure below illustrates Transitional acquisition, comparing it to Traditional acquisition.

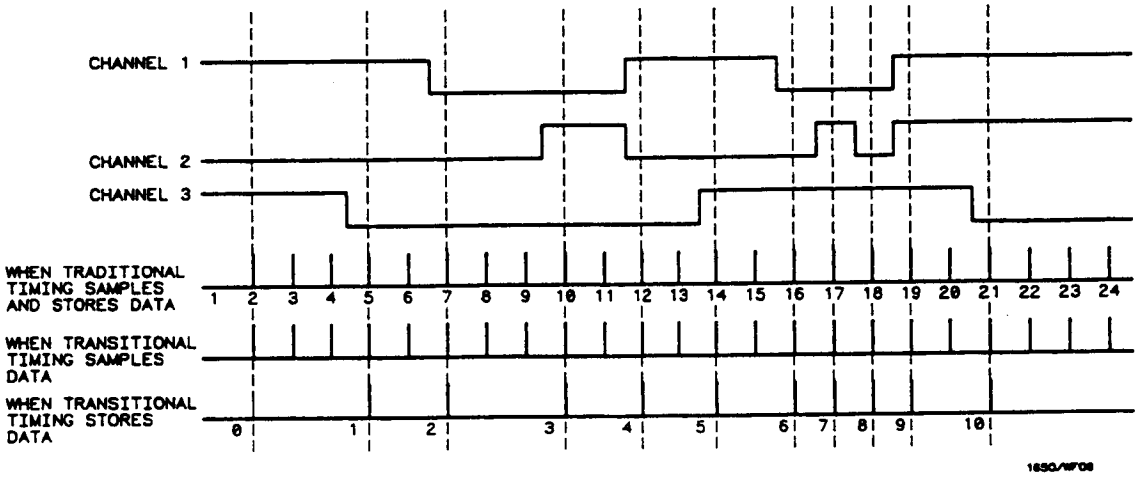


Figure 5-32. Transitional Timing vs. Traditional Timing

Traditional timing samples and stores data at regular intervals. Transitional timing samples data at regular intervals but stores a sample only when there has been a transition on one or more of the channels. This makes it possible for Transitional timing to store more information in the same amount of memory.

Glitch Acquisition Mode. A glitch is defined as any transition that crosses the logic threshold more than once between samples. It can be caused by capacitive coupling between traces, power supply ripple, or a number of other events. The glitch, in turn, can cause major problems in your system.

Your logic analyzer has the capability of triggering on a glitch and capturing all the data that occurred before it. The glitch must have a width of at least 5 ns at threshold in order for the analyzer to detect it.

If you want your timing analyzer to trigger on a glitch in the data, set the Acquisition mode to Glitch. This causes several changes in the analyzer. One change is that a field for glitch detection in each label is added to the Timing Trace Specification menu, as shown:

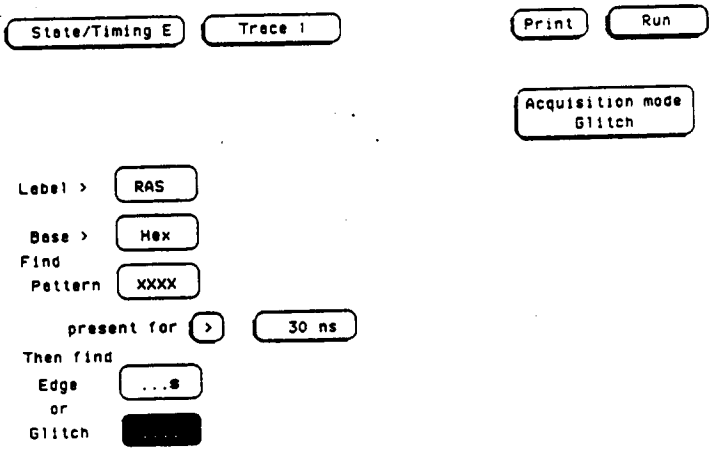


Figure 5-33. Glitch Specification Field

With these glitch detection fields you specify on which channel or channels you want the analyzer to look for a glitch. These fields are discussed in more detail in the "Then Find Edge" section later in this chapter.

Glitch Acquisition mode causes the storage memory to be cut in half, from 1k to 512. Half of the memory (512) is allocated for storing the data sample, and the other half for storing the second transition of a glitch in a sample. Every sample is stored. The sample rate varies from 20 Hz to 50 MHz (50 ms/sample to 20 ns/sample) and is automatically selected by the timing analyzer to insure complete data in the window of interest.

When your timing analyzer triggers on a glitch and displays the data, the glitch appears in the waveform display as shown below.

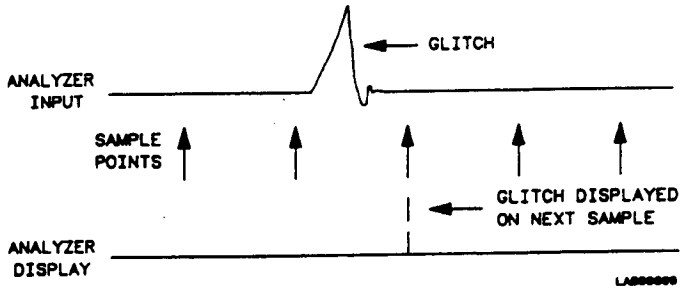


Figure 5-34. Glitch in Timing Waveform

4 Label The Label fields contain the labels that you define in the Timing Format Specification menu. If there are more labels than can fit on screen, use the KNOB to view those that aren't displayed.

5 Base The Base fields allow you to specify the number base in which you want to define a pattern for a label. The Base fields also let you use a symbol that was specified in the Timing Symbol Table for the pattern. Each label has its own base defined separately from the other labels. If you select one of the Base fields, you will see the following pop-up menu. Decide which base you want to define your pattern in and select that option.

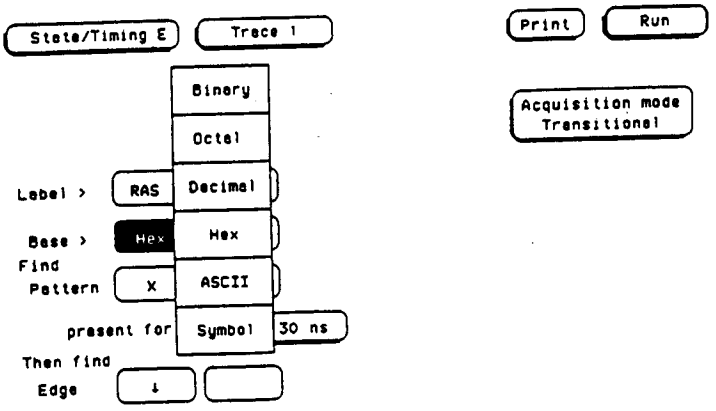


Figure 5-35. Base Pop-up Menu

One of the options in the Base pop-up is ASCII. It allows you to see the ASCII characters that are represented by the pattern you specified in the Find Pattern field.

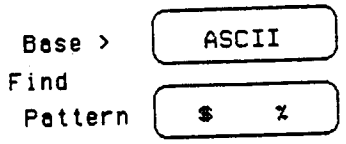


Figure 5-36. ASCII Defined as Numeric Base

In the figure above, the **Find Pattern** field is no longer a selectable field when the base is **ASCII**. If you touch this field, the message "ASCII entry not available" appears. You cannot enter ASCII characters directly. You must specify a pattern in one of the other bases; then switch the base to ASCII and to see what characters the pattern represents.

The **Symbol** option in the **Base** pop-up allows you to use a symbol that has been specified in the Timing **Symbol Tables** as a pattern, or specify absolute and enter another pattern. You specify the symbol you want to use in the **Find Pattern** field.

6 Find Pattern

With the Find Pattern fields, you configure your timing analyzer to look for a certain pattern in the data. Each label has its own pattern field that you use to specify a pattern for that label.

During a run, the logic analyzer looks for a pattern in your data generated by the logical AND of all the labels' patterns. That is, it looks for a simultaneous occurrence of the specified patterns. When it finds the pattern, it triggers at the point that you specified in the **Then find Edge** fields. See the "Then Find Edge" section later in this chapter for more information about edge triggering.

You specify a pattern by touching the **Find Pattern** field. A keypad pop-up appears with which you enter the desired pattern. The pop-up will vary depending on the base you choose and the number of channels you assign to that label.

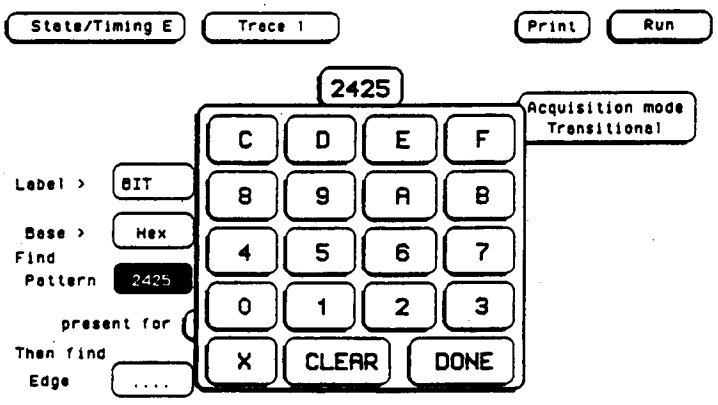


Figure 5-37. Specify Pattern Pop-up for Find Pattern Field (HEX)

Enter your pattern in the pop-up and touch **DONE**. The pattern appears under the label in the **Find Pattern** field.

As mentioned in the previous section on the Base field, if you specify ASCII as the base for the label, you won't be able to enter a pattern. You must specify one of the other number bases to enter the pattern, then you can switch the base to ASCII and see what ASCII characters the pattern represents.

If you choose **Symbols** in the **Base** field, you can use one of the symbols specified in the Timing Symbol Tables as the pattern. The **Find Pattern** field looks similar to that below:

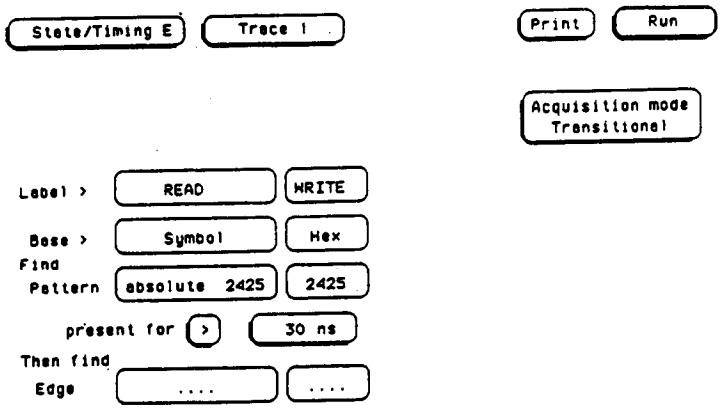


Figure 5-38. Symbol Defined in Base Field

If you select this field you get a pop-up similar to that shown:

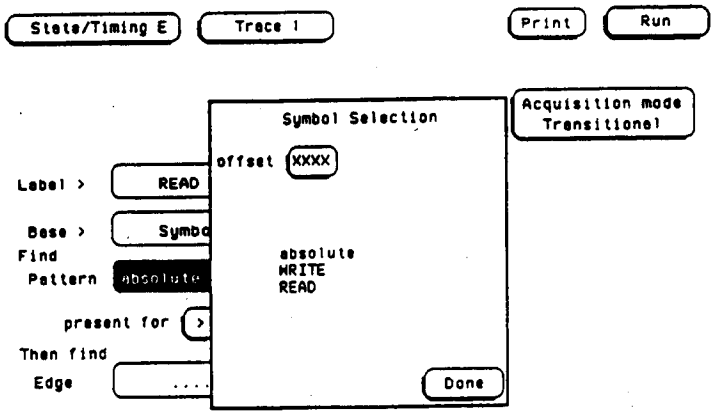


Figure 5-39. Symbol Selection Pop-up Menu for Find Pattern Field

The pop-up lists all the symbols defined for that label. It also contains an option **absolute**. Placing the blue bar on this option causes another field within the pop-up to appear. This field is labeled **offset** _____. The offset field lets you specify a pattern not given by one of your symbols.

To select an option from the pop-up, use the KNOB to roll the symbols up and down until the desired symbol is highlighted by the blue bar. Touch **Done** to close the pop-up and place the symbol name in the **Find Pattern** field under the label.

When you specify symbols in the Timing **Symbol Tables**, you also specify the number of characters in the symbol name that are to be displayed. If you specify to display only three characters of a symbol name, only REA of READ and WRI of WRITE would be displayed in the **Find Pattern** field. In addition, only the first three letters of absolute would be displayed.

7 Pattern Duration (present for _____)

There are two fields with which you specify the Pattern Duration. They are located next to **present for** _____ in the Timing **Trace Specification** menu. You use these fields to tell the timing analyzer to trigger before or after the specified pattern has occurred for a given length of time.

The first field can be set to > (greater than) or < (less than). When you touch this field, it toggles between > and <. The second field specifies the duration of the pattern. If you select > in the first field, you can set the duration to a value between 30 ns and 10 ms. If you select < in the first field, you can set the duration to a value between 40 ns and 10 ms. If you attempt to set the duration to a value outside the given range, the analyzer will automatically set it to the nearest limit.

To change the value of the pattern duration, touch the second field to get a pop-up keypad similar to the one shown:

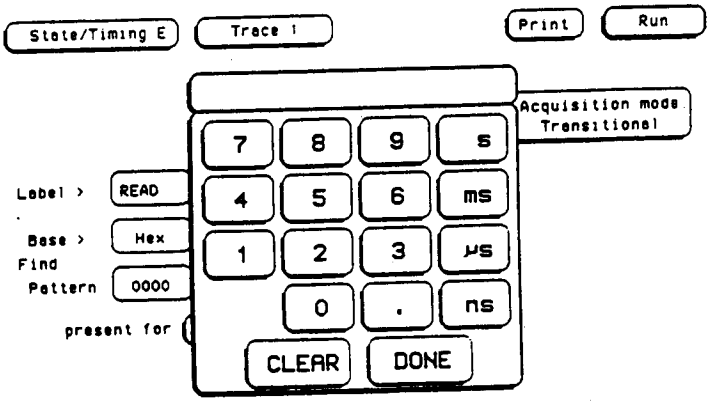


Figure 5-40. Pattern Duration (present for) Pop-up Menu

With the keypad enter the desired value and units for pattern duration, then touch **DONE**. Your value for pattern duration will appear in the field.

As an example, suppose you configure the **present for field** as shown:

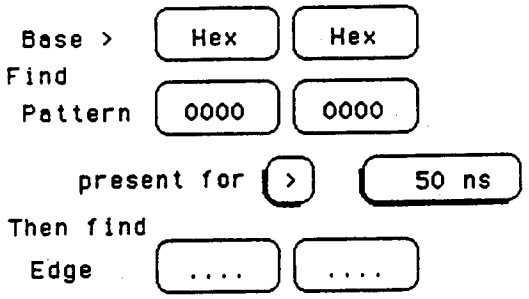


Figure 5-41. Example of Pattern Duration > 50 ns

This configuration tells the timing analyzer to look for a certain pattern specified by you that has a duration of greater than 50 ns. Once the timing analyzer has found the pattern, it can look for the trigger.

Choosing < (less than) forces glitch and edge triggering off, and the timing analyzer triggers immediately at the end of the pattern that meets the duration requirements. The fields with which you specify edges and glitches don't appear in the menu. For instance, if you configure the present for field as shown:

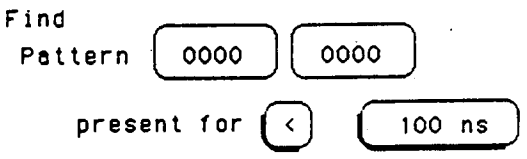


Figure 5-42. Example of Pattern Duration < 100 ns

The analyzer will trigger when the specified pattern has a duration less than 100 ns. The pattern must also be valid for at least 20 ns.

8 Then Find Edge

With the **Then find Edge** fields you can specify the edges (transitions) of your data on which your timing analyzer triggers. You can specify a positive edge, a negative edge, or either edge. Each label has its own edge trigger specification field so that you can specify an edge on any channel.

When you specify an edge on more than one channel, the timing analyzer logically ORs them together to look for the trigger point. That is, it triggers when it sees any one of the edges you specified. It also ANDs the edges with the pattern you specified in the **Find Pattern** fields. The logic analyzer triggers on an edge following the valid duration of the pattern while the pattern is still present.

To specify an edge, touch one of the **Then find Edge** fields. You will see a pop-up similar to that shown below.

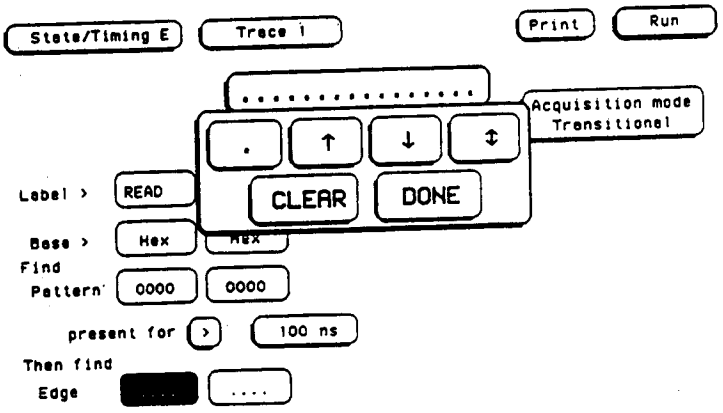


Figure 5-43. Specify Edge Pop-up for Then Find Edge Field

The top row of periods and arrows in your pop-up may look different than this depending on the number of channels you assigned to the label. Each period in the pop-up indicates that no edge is specified for that channel. To specify a negative edge, place the cursor on one of the periods in the pop-up and touch the ↓. The period changes to ↓. To specify a positive edge, touch the ↑. The period changes to ↑.

If you want the analyzer to trigger on either a positive or a negative edge, touch the ↕. The period changes to ↕.

If you want to delete an edge specification, place the cursor on the arrow for that channel and touch the . (period). To clear an entire label, touch CLEAR in the pop-up.

When you have finished specifying edges, touch **Done** to close the pop-up.

An example of a positive, negative, and either edge specification is shown below.

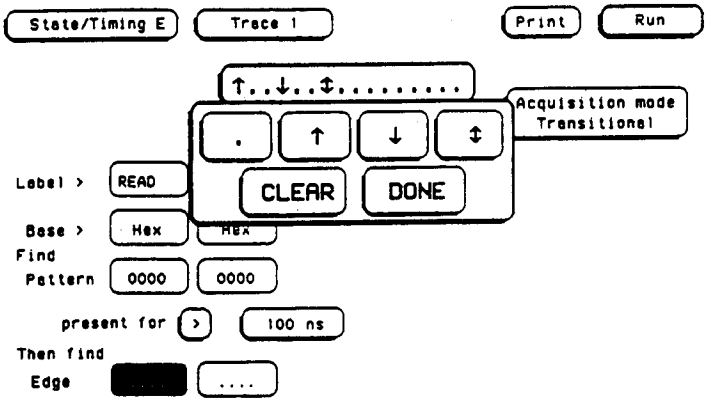


Figure 5-44. Combination of Edges Specified

Note

*When you close the pop-up after specifying edges, you will see **($$..)** in the Then find Edge field. These indicate edges have been specified; however, the logic analyzer can't display them correctly unless you have selected Binary for the base.*

Glitch Triggering. When you set the Acquisition mode on Glitch, a glitch detection field for each label is added to the screen. These fields allow you to specify glitch triggering on your timing analyzer. Selecting one of these fields brings up the following pop-up menu.

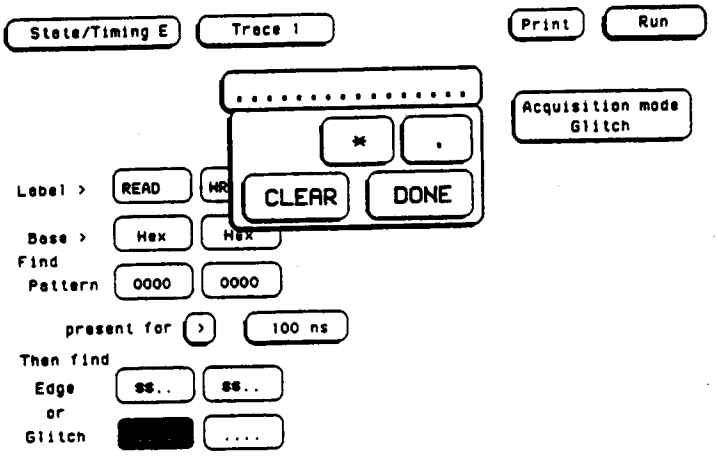


Figure 5-45. Specify Glitch Pop-up for Then Find Glitch Field

Your pop-up may look different depending on the number of channels you have assigned to the label. Each period indicates that the channel has not been specified for glitch triggering.

To specify a channel for glitch triggering, place the cursor on one of the periods and touch the asterisk. The period is replaced with an asterisk, indicating that the logic analyzer will trigger on a glitch on this channel.

Note

If you select < (less than) in the present for field, edge and glitch triggering are turned off. The Then find Edge or Glitch fields no longer appear on the screen. The logic analyzer triggers on only the pattern specified in the Find Pattern fields.

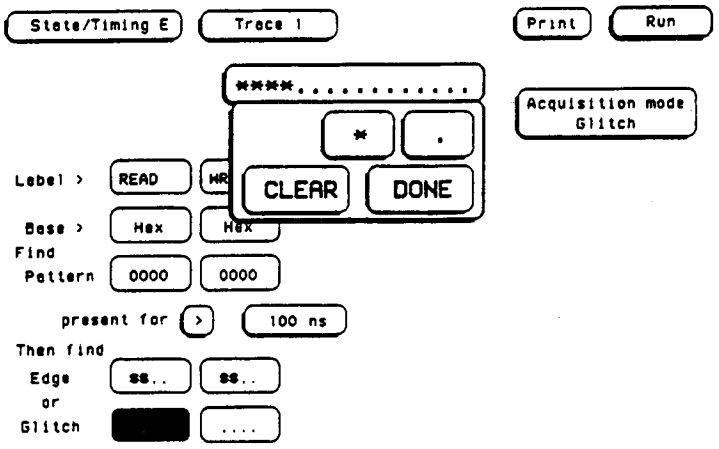


Figure 5-46. Glitches Specified

If you want to delete a glitch specification, place the cursor on the asterisk and touch the period. The asterisk is replaced with a period.

Note

When you close the pop-up after specifying glitches, you will see dollar signs ($$_) in the Glitch field. These indicate that glitches have been specified; however, the logic analyzer can't display them correctly unless you have selected Binary for the base.

When you specify a glitch on more than one channel, the logic analyzer logically ORs them together. In addition, the logic analyzer ORs the glitch specifications with the edge specifications, then ANDs the result with the pattern you specified in the Find Pattern fields in order to find the trigger point. An equation illustrating this is:

(glitch + glitch + edge + edge) • pattern

State Trace Specification Menu

The State Trace Specification menu allows you to specify a sequence of states required for trigger. The default setting for the menu looks like that shown below.

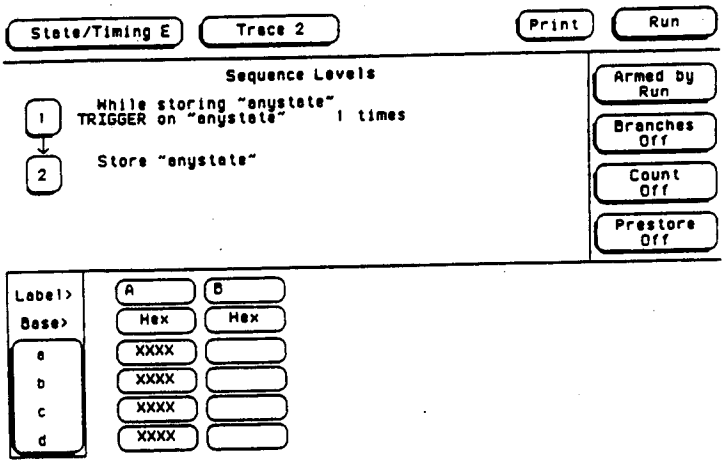


Figure 5-47. State Trace Specification Menu

The menu is divided into three sections: the Sequence Levels in the large center box, the acquisition fields at the right of the screen, and the qualifier and pattern fields at the bottom of the screen.

Before describing the fields in the menu, we need to define a few terms. These terms will be used in the discussions on the fields, so understanding their meanings is essential.

Pattern Recognizers: a pattern of bits (0, 1, or X) in each label. There are eight recognizers available when one state analyzer is on. Four are available to each analyzer when two state analyzers are on. The pattern recognizers are given the names a through h and are partitioned into groups of four, **a-d** and **e-h**.

Range Recognizer: recognizes data which is numerically between or on two specified patterns. One range term is available and is assigned to the first state analyzer that you turn on or if only one analyzer is on, then the range term is assigned to it.

Qualifier: a term you specify that can be anystate, nostate, a single pattern recognizer, a range recognizer, the complement of a pattern or range recognizer, or a logical combination of pattern and range recognizers. When you select a field to specify a qualifier, you will see the following qualifier pop-up menu.

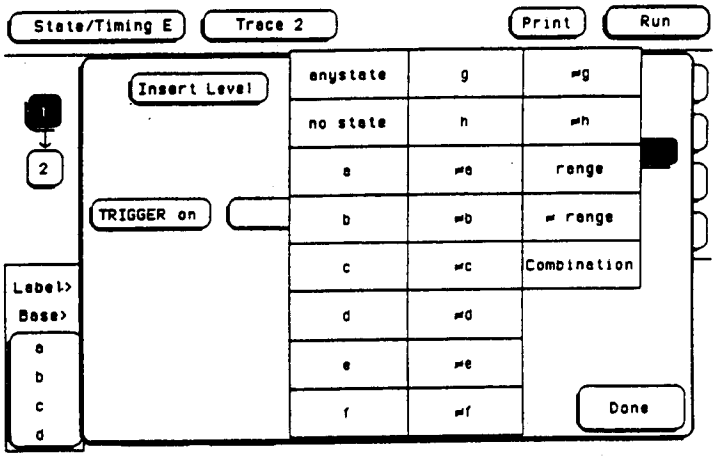


Figure 5-48. Qualifier Pop-up Menu

If you select the **Combination** option in the pop-up, you will see a pop-up similar to that shown below.

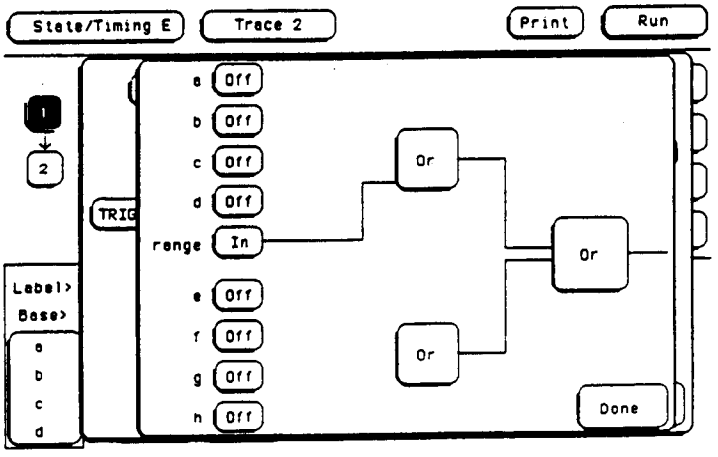


Figure 5-49. Full Qualifier Specification Pop-up

Note

If two multi-pod state analyzers are on, the qualifier pop-up menu will show that only four pattern recognizers are available to each analyzer. Pattern recognizers a-d and the range recognizer go with the first analyzer created, and pattern recognizers e-h go with the second analyzer. In the ***Full Qualifier Specification*** *pop-up, there will be only one OR gate and one set of pattern recognizers.*

With this **Full Qualifier Specification** pop-up, you specify a logical combination of patterns or a range as the qualifier. The pattern recognizers are always partitioned into the groups of four as shown. Only one operator is allowed between the patterns in a group. Patterns in uncomplemented form (a, b, etc.) can only be ORed. The complements of patterns (≠a, ≠b, etc.) can only be ANDed. For example, if the first OR field (gate) is changed to AND, all the patterns for that gate are complemented, as shown below.

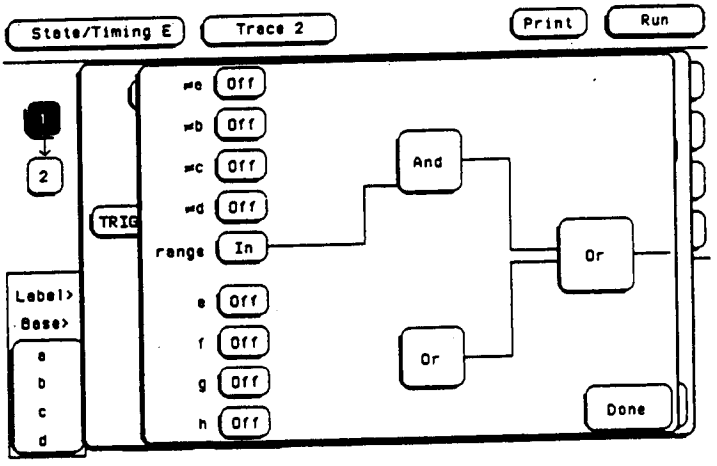


Figure 5-50. Complemented Patterns

To specify a pattern to be used in the combination, touch the pattern recognizer field. The field toggles from **Off** to **On** and a connection is drawn from the pattern field to the gate. In figure 5-51, patterns b, c and d and the range are ORed together, and ≠e and ≠g are ANDed together.

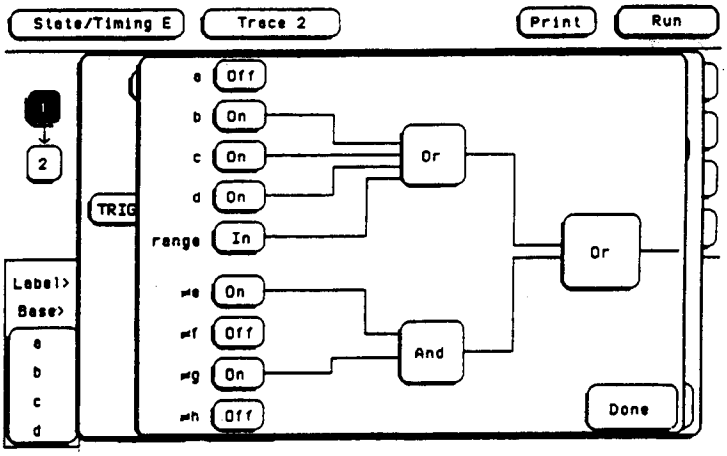


Figure 5-51. Patterns Assigned for Logical Combinations

As shown in the previous figures, the range is included with the first group of patterns (a-d). If you select the range field, you will see the following pop-up menu.

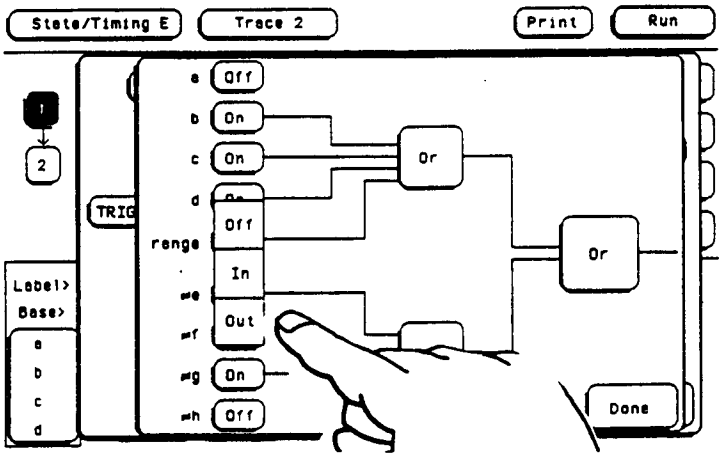


Figure 5-52. Range Specification Pop-up Menu

Off disconnects the range from the qualifier specification. **In** indicates that the contents of the range are to be in the qualifier specification, and **Out** indicates that the complement of the range is to be in the qualifier specification, or in other words, "not-in-range."

When you have specified your combination qualifier, select **Done**. The Full Qualifier Specification pop-up closes and the Boolean expression for your qualifier appears in the field for which you specified it.

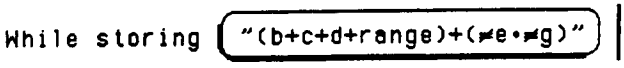


Figure 5-53. Boolean Expression for Qualifier

Sequence Levels

There are eight trigger sequence levels available in the state analyzer. You can add and delete levels so that you have from two to eight levels at a time. Only three levels appear in the Sequence Levels display at one time. To display other levels so that they can be accessed, rotate the KNOB.

If you select level 1 shown in figure 5-47, you will see the following pop-up menu:

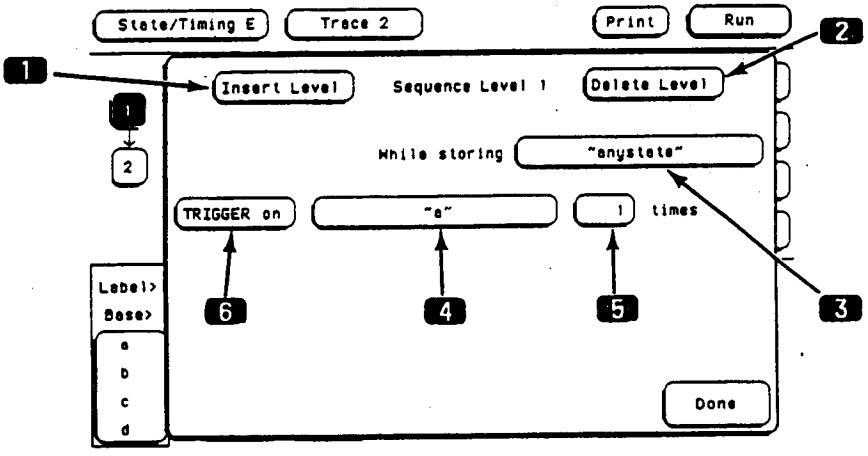


Figure 5-54. Sequence Level Pop-up Menu

Not all sequence level pop-up menus look like this one. This happens to be the trigger sequence level in which you specify the state on which the analyzer is to trigger. The trigger term can occur in any of the first seven levels, and it is not necessarily a selectable field. The fields in the menu of figure 5-54 are described on the following pages.

1 Insert Level To insert a level, touch the field labeled **Insert Level**. You will see the following pop-up menu.

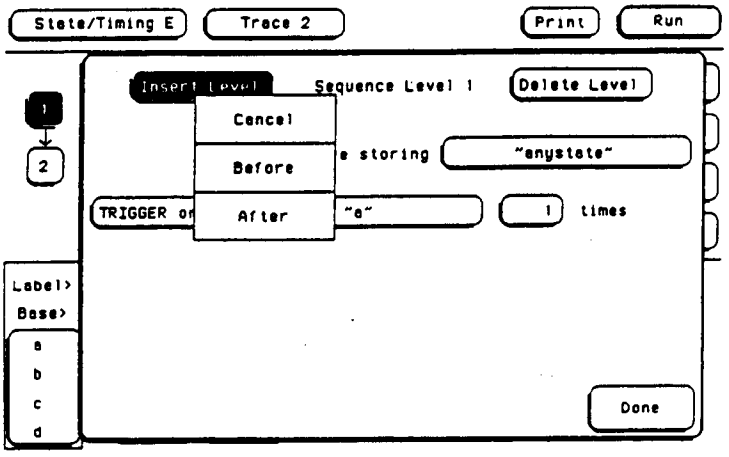


Figure 5-55. Insert Level Pop-up Menu

Cancel returns you to the sequence level pop-up without inserting a level. **Before** inserts a level before the present level. **After** inserts a level after the present level. If there are eight levels, the **Insert Level** field doesn't appear in the sequence level pop-ups.

2 Delete Level If you want to delete the present level, touch the field labeled **Delete Level**. You will see a pop-up menu with the choices **Cancel** and **Execute**. **Cancel** returns you to the sequence level pop-up without deleting the level. **Execute** deletes the present level and returns you to the State Trace Specification menu.

Note

If there are only two levels, neither field can be deleted even though the Delete Level field still appears in the menu. There will always be a trigger term level and a store term level in Sequence Levels. Therefore, if you try to delete either of these, all terms you have specified in these levels will be set to default terms, and, the trigger and store term levels will remain.

3 Storage Qualifier Each sequence level has a storage qualifier. The storage qualifier specifies the states that are to be stored and displayed in the State Listing. Selecting this field gives you the qualifier pop-up menu shown in figure 5-48, with which you specify the qualifier.

As an example, suppose you specify the storage qualifier in a sequence level as shown below.

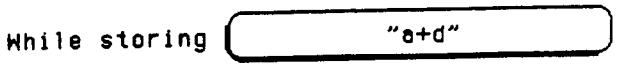


Figure 5-56. Storage Qualifier Example

The only states that will be stored and displayed are the states given by pattern recognizers a and d.

4 Branching Qualifier Every sequence level except the last has a primary branching qualifier. With the branching qualifier, you tell the analyzer to look for a specific state or states. The primary branching qualifier advances the sequencer to the next level if its qualifier is satisfied.

In the example of figure 5-54, the branching qualifier tells the analyzer when to trigger. In other sequence levels, the qualifier may simply specify a state that the analyzer is to look for before continuing to the next level.

Some sequence levels also have a secondary branching qualifier. The secondary branch will, if satisfied, route the sequencer to a level that you define. This is covered in more detail in "Branches" later in this chapter.

5 Occurrence Counter

The primary branching qualifier has an occurrence counter. With the occurrence counter field you specify the number of times the branching qualifier is to occur before moving to the next level.

To change the value of the occurrence counter, touch the field. You will see a pop-up similar to that shown below.

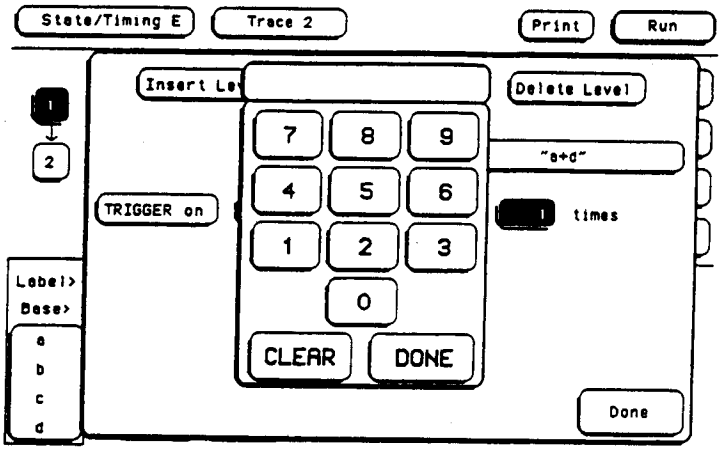


Figure 5-57. Occurrence Counter Pop-up

You can enter the value by touching the appropriate numeric keys. The qualifier can be specified to occur from one to 65535 times.

6 Storage Macro

Your logic analyzer has the capability of post-trigger storage through a storage macro. The storage macro is available only in the second to last level, and it consumes both that level and the last level. The field in figure 5-54 allows you to configure the state analyzer for post-trigger storage. This field does not always say Trigger on. If the sequence level is not a trigger level, the field will say **Then find**, as shown below.



Figure 5-58. Then Find Branching Qualifier

Selecting the field gives you a pop-up with two options. One option is what the field said previously. The other option is **Enable** on. If you select this option, the Sequence Level pop-up changes to look similar to that shown below.

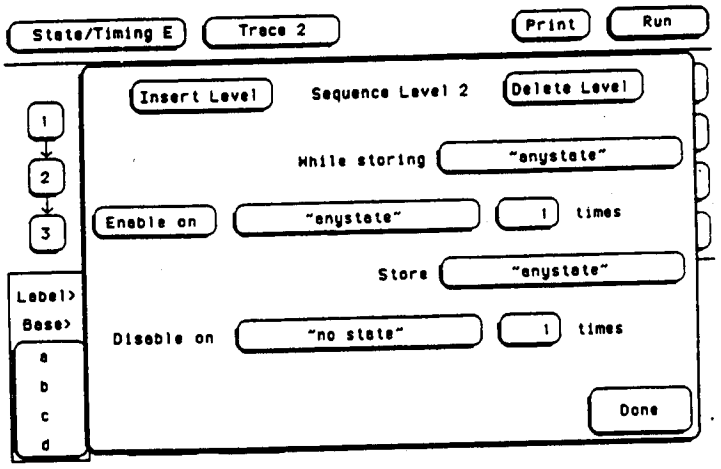


Figure 5-59. Sequence Level Pop-up Menu with Storage Macro On

Note

***Enable on** can only be the next to the last term, and when on, the last term is combined with the Enable term. For example, when you close the pop-up in figure 5-59, levels 2 and 3 will be combined.*

You specify qualifiers for the states on which you want the macro to enable, the states you want to store, and the states on which you want the macro to disable. The storage macro is a loop that keeps repeating itself until memory is full. The loop is repeated when the disable qualifier is satisfied.

As an example, suppose you configure the sequence level of figure 5-59 to look like that shown below.

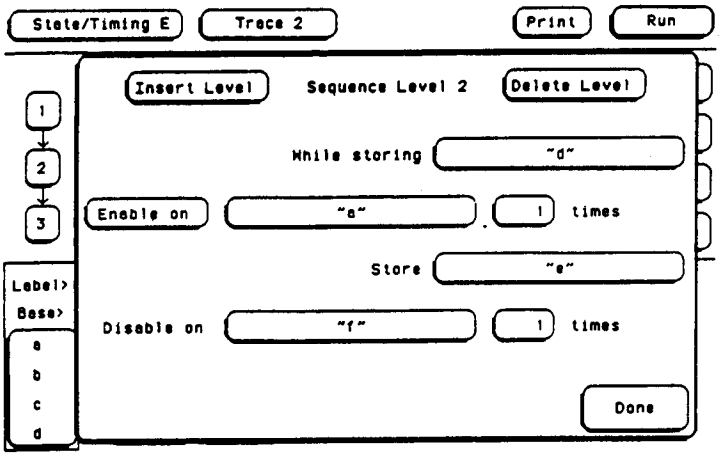


Figure 5-60. Storage Macro Sequence Level Example

The logic analyzer will store the state given by pattern recognizer d until it comes across the state given by a. When it sees state a, the logic analyzer starts to store the state given by pattern recognizer e. It stores that state until it sees the state given by f, at which time it disables and starts the process all over again. The analyzer repeats this process until its memory is full.

Reading the Sequence Level Display

Reading the display is fairly straightforward. For example, suppose your display looks like that shown below.

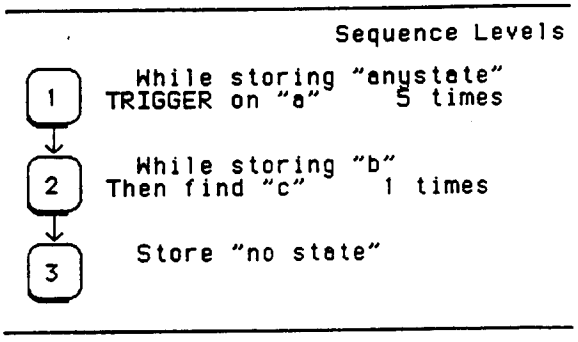


Figure 5-61. Sequence Level Display Example

In level 1 **anystate** is stored while the logic analyzer searches for five occurrences of the pattern given by pattern recognizer a. When the five occurrences are found, the sequencer moves on to level 2. In level 2 the state given by pattern recognizer b is stored until one occurrence of the pattern given by pattern recognizer c is found and the logic analyzer triggers. In level 3 **nostate** is stored, so the last state stored is the trigger state.

An example of a state listing for the previous State Trace configuration is shown below. The state patterns specified are:

a = B03C
b = 0000
c = 8930

```
 MACHINE 2    -   STATE LISTING

Label    >  A
Base     >   Hex

 -0028        4E75
 -0027        61E6
 -0026        0000
 -0025        88C8
 -0024        B03C
 -0023        00FF
 -0022        6730
 -0021        48E7
 -0020        4E75
 -0019        3000
 -0018        0000
 -0017        8930
 -0016        B03C
 -0015        00FF
 -0014        67F8
 -0013        B03C
 -0012        61FA
 -0011        B03C
 -0010        0000
 -0009        8930
 -0008        4EFA
 -0007        FF9A
 -0006        61E6
 -0005        B03C
 -0004        0000
 -0003        0000
 -0002        0000
 -0001        0000
 +0000        8930
```

Figure 5-62. State Listing Example

Anystate was stored while the analyzer looked for five occurrences of the state B03C. After the fifth occurrence was found, only state 0000 was stored until state 8930 was found, and the analyzer triggered. After the trigger, no states were stored.

Acquisition Fields

The acquisition fields are comprised of the Trace mode, Armed by, Branches, Count, and Prestore fields, as shown below.

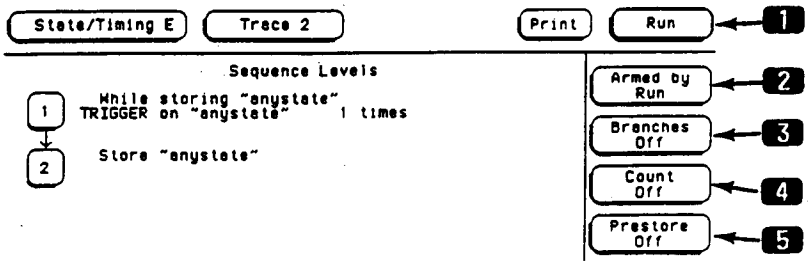


Figure 5-63. State Trace Specification Acquisition Fields

1 Run/Trace Mode You specify the mode in which the timing analyzer will trace when you touch **Run**. You have two choices for trace mode: **Single** and **Repetitive**. When you touch **Run** and hold your finger on the field, you will see the following pop-up menu:

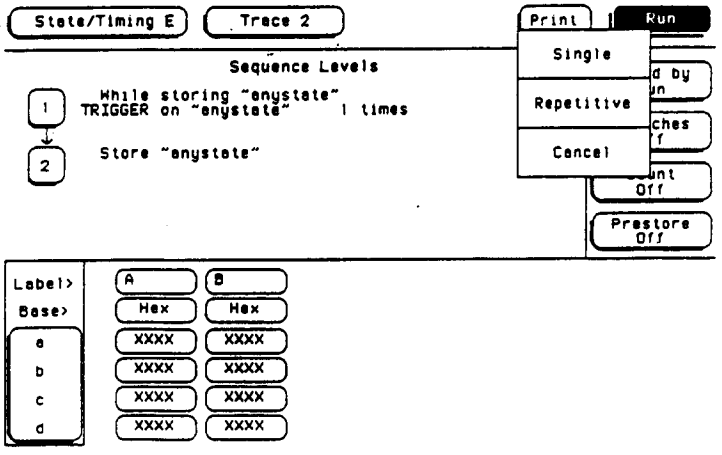


Figure 5-64. Run field pop-up Menu

You select the trace mode by touching the **Run** field, and, without lifting your finger from the screen, move it to the desired trace mode. When you lift your finger, the logic analyzer traces data in the mode you specify. If you wish to abort the trace after you touch **Run** but before the trace starts, move your finger to **Cancel** before lifting your finger.

Single Trace mode acquires data once per trace. Repetitive Trace mode repeats single acquisitions until **Stop** key is touched, or until conditions specified with the X and O markers in the State Listing menu are met.

2 Armed By The Armed By field is present when more than one analyzer is on at the same time. The Armed by field lets you specify how your state analyzer is to be armed. The analyzer can be armed by **Run**, the other analyzer, or an external arm from the IMB (Intermodule Bus). "Intermodule Measurements" are covered in chapter 10 of the *HP 16500A Reference Manual*.

When you select the Armed by field, a pop-up menu appears like that shown below. Use this menu to select the arming option for your analyzer. With the menu, select the arming option for your analyzer.

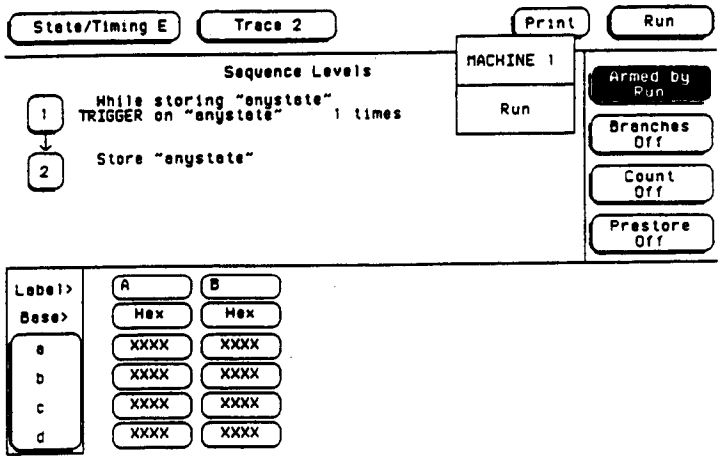


Figure 5-65. Armed By Pop-up Menu

3 Branches The Branches field allows you to configure the sequencer of your state analyzer to branch from one sequence level to another with secondary branching qualifiers, or to restart when a certain condition is met. Selecting this field gives you the following pop-up menu.

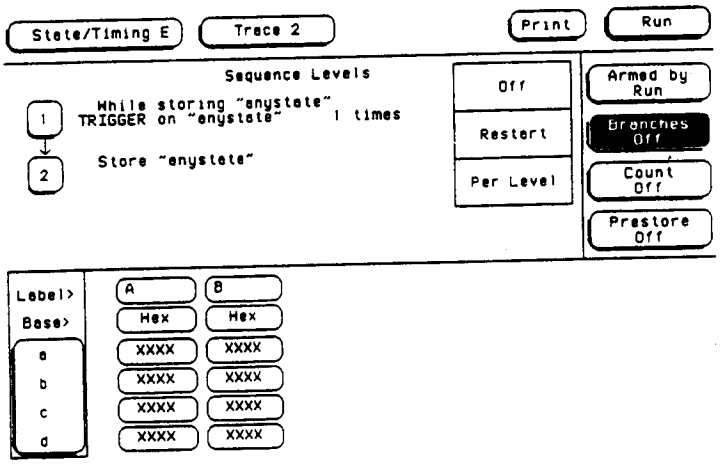


Figure 5-66. Branches Pop-up Menu

Off. If you select Off, all secondary branching qualifiers are deleted from the sequence levels. Only the primary branches remain.

Restart. The Restart option allows you to start over from sequence level 1 when a specified condition is met. This can be handy if you have code that branches off in several paths and you want the analyzer to follow one certain path. If the analyzer goes off on an undesired path, you would want the analyzer to stop and go back to the beginning and take the correct path.

If you select the **Restart** option, you will see a qualifier pop-up menu like that shown in figure 5-48. With the pop-up you select the qualifier for the pattern on which you want your analyzer to start over.

When your state analyzer is reading data it proceeds through the sequence. If a term doesn't match the branching qualifier, it is then checked against **Restart**. If the term matches, the state analyzer jumps back the sequence level 1.

Per Level. Selecting the Per level option allows you to define a secondary branching qualifier for each sequence level. A statement is added in each level so that you can configure the analyzer to move to a different level when a secified condition is met. An example of a sequence level with a secondary branching qualifier is shown in the following figure.

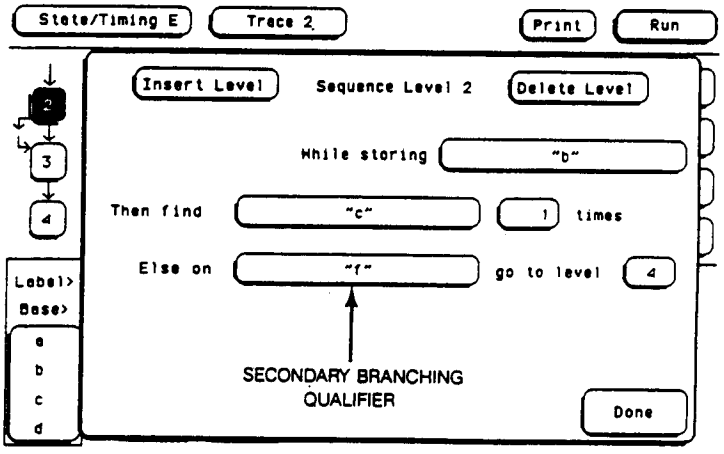


Figure 5-67. Secondary Branching

With this configuration, the state analyzer will store the state given by pattern recognizer **b** until it finds the state given by **c**. If it finds the state given by **f** before it finds **c**, it will branch to sequence level 4. If you have specified a storage macro in the next to last sequence level, the **Else on** statement will not appear in that level since a secondary branching qualifier already exists for that level.

In the last sequence level, which only specifies states that are to be stored, the secondary branching qualifier statement looks like that shown in the following figure.

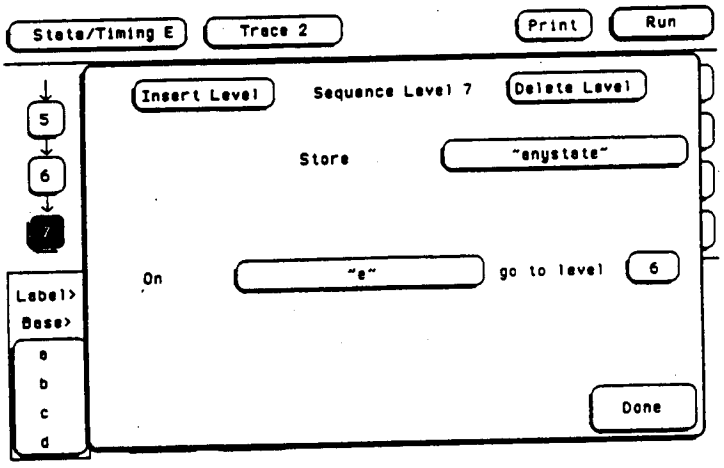


Figure 5-68. Secondary Branch Qualifier in Last Sequence Level

In this example, as the state analyzer stores **anystate**, it will branch to sequence level 6 if it finds the state given by qualifier **e**.

The trigger sequence level is used as a boundary for branching between levels. This level and the levels that occur before it cannot branch to levels that occur after the trigger level, and vice versa. Therefore, if there are eight sequence levels and level 5 is the trigger sequence level, then levels 1 through 5 can branch to levels 1 through 5 only, and levels 6 through 8 can branch to levels 6 through 8 only.

You can tell if secondary branch qualifiers have been specified by looking at the **Sequence Levels** display. Figure 5-69 shows how the display looks with the configuration that was given in Figure 5-67. An arrow is drawn out of level 2 to indicate that branching originates from that level, and an arrow is drawn into level 4 to indicate that a branch is going into that level.

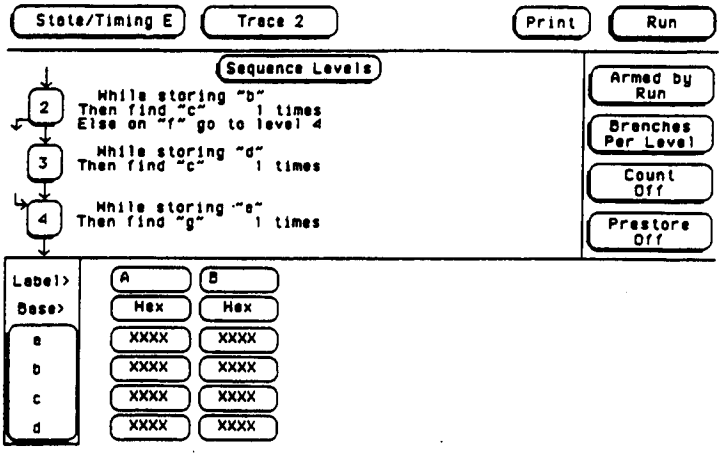


Figure 5-69. Branching Between Sequence Levels

Each sequence level can branch to only one level through a secondary branching qualifier. However, the number of times tc which a level can be branched is limited only by the number of levels present. A level can have only one arrow pointing away from it, but it can have two pointing to it if more than one other level is branching to it. An example of this is shown in the figure below. The arrow with two tails indicates that a level above and a level below branch to that level.

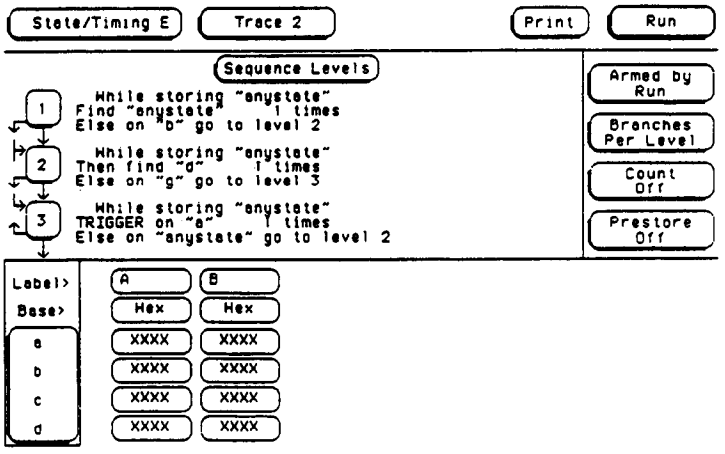


Figure 5-70. Multiple Branching Between Levels

4 Count The Count field allows you to place tags on states so you can count them. Counting cuts the acquisition memory in half from 1k to 512, and the maximum clock rate is reduced to 16.67 MHz.

Selecting this field gives you the following pop-up menu.

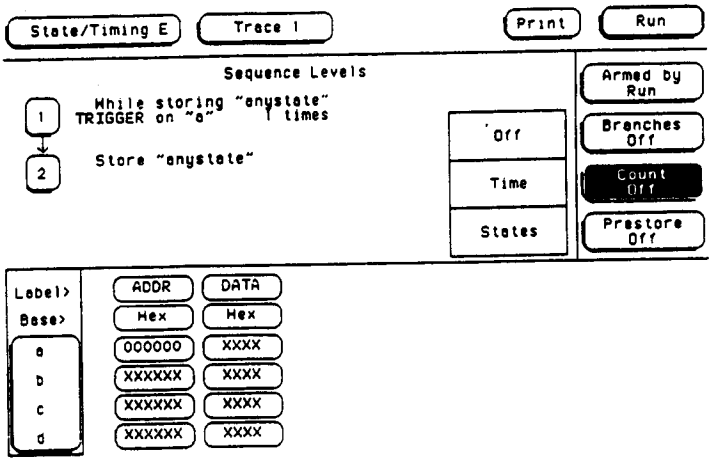


Figure 5-71. Count Pop-up Menu

Off. If you select **Off**, the states are not counted in the next measurement.

Time. If you select **Time** counting, the time between stored states is measured and displayed in the State Listing under the label Time. The time displayed can be either relative to the previous state or to the trigger. The maximum time between states is 48 hours.

An example of a state listing with time tagging relative to the previous state is shown below.

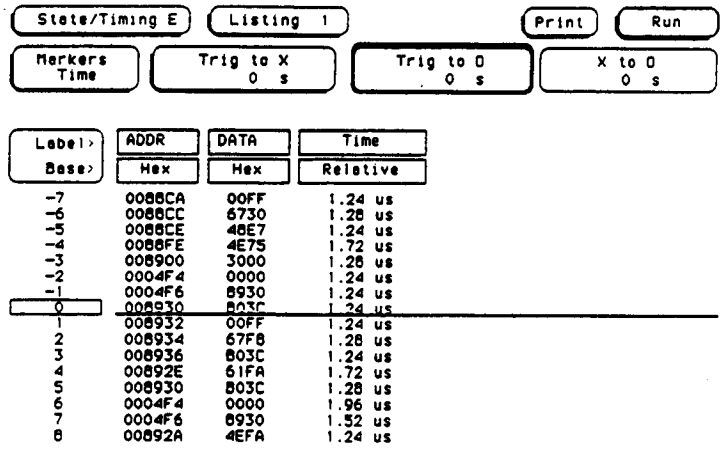


Figure 5-72. Relative Time Tagging

An example of a state listing with time tagging relative to the trigger is shown below.

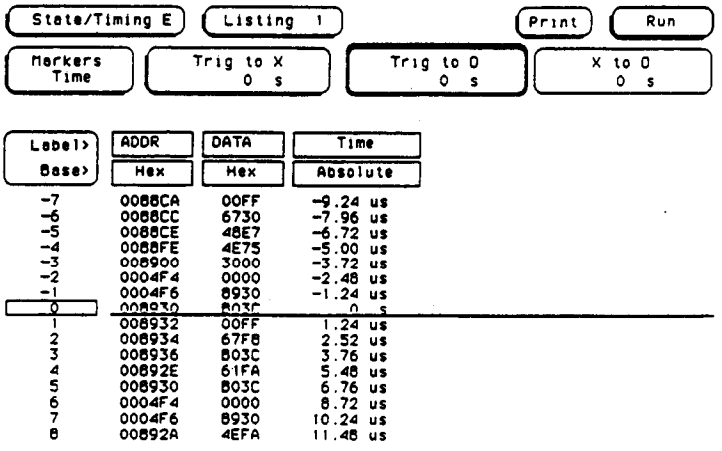


Figure 5-73. Absolute Time Tagging

States. State tagging counts the number of qualified states between each stored state. If you select this option, you will see a qualifier pop-up menu like that shown in figure 5-48. You select the qualifier for the state that you want to count.

In the State Listing, the state count is displayed under the label States. The count can be relative to the previous stored state or to the trigger. The maximum count is 4.4 X 10^{12}.

An example of a state listing with state tagging relative to the previous state is shown below.

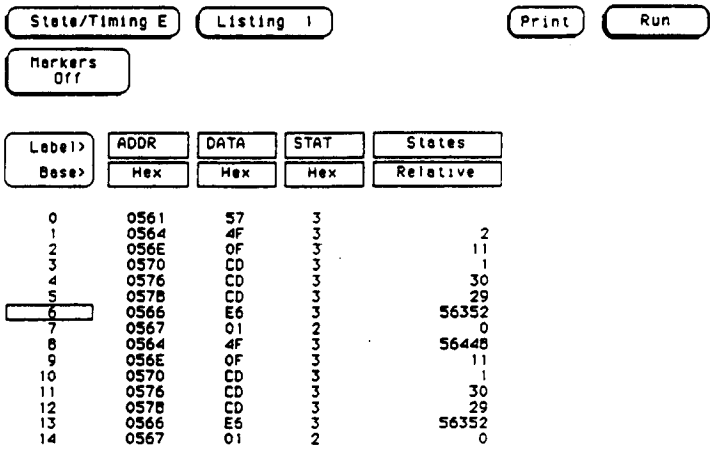


Figure 5-74. Relative State Tagging

An example of a state listing with state tagging relative to the trigger is shown below.

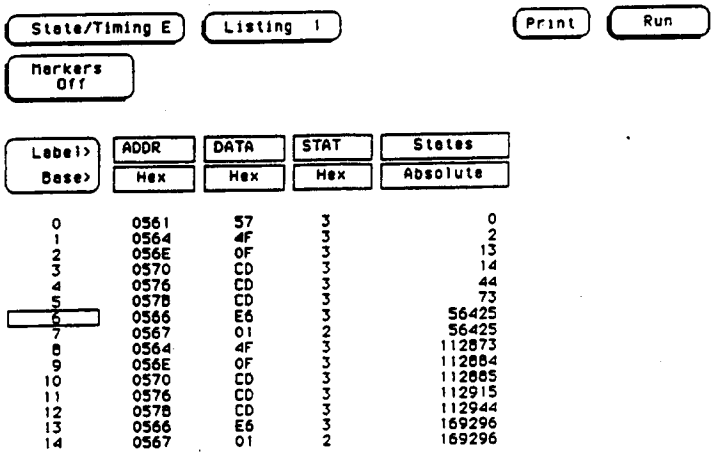


Figure 5-75. Absolute State Tagging

5 Prestore

Prestore allows you to store two qualified states before each state that is stored. There is only one qualifier that enables prestore for each sequence level. If you select this field, you will see a pop-up with the options **Off** and **On**. Selecting On gives you a qualifier pop-up menu like that in figure 5-48, from which you choose the pattern, range or combination of patterns and ranges that you want to prestore.

During a measurement, the state analyzer stores in prestore memory occurrences of the states you specify for prestore. A maximum of two occurrences can be stored. If there are more than two occurrences, previous ones are pushed out. When the analyzer finds a state that has been specified for storage, the prestore states are pushed on top of the stored state in memory and are displayed in the State Listing.

Qualifier and Pattern Fields

The qualifier and pattern fields appear at the bottom of the State Trace Specification menu. They allow you to specify patterns for the qualifiers that are used in the sequence levels.

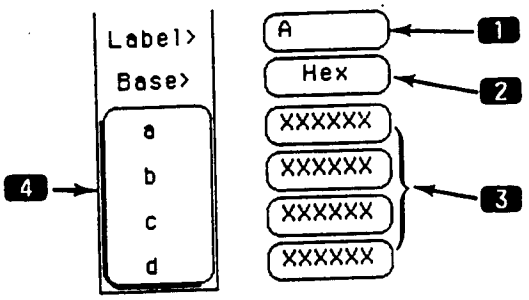


Figure 5-76. Qualifier and Pattern Fields

1 Label The Label fields display the labels that you specified in the State Format Specification menu. The labels appear in the order that you specified them; however, you can change the order. Select one of the label fields and you will see a pop-up menu with all the labels. Decide which label you want to appear in the label field and select that label. The label that was there previously switches positions with the label you selected from the pop-up.

2 Base The Base fields allow you to specify the number base in which you want to define a pattern for a label. The base fields also let you use a symbol that was specified in the State Symbol Table for the pattern. Each label has its own base defined separately from the other labels. If you select one of the base fields, you will see the following pop-up menu. When you decide which base you want to define your pattern in, select that option.

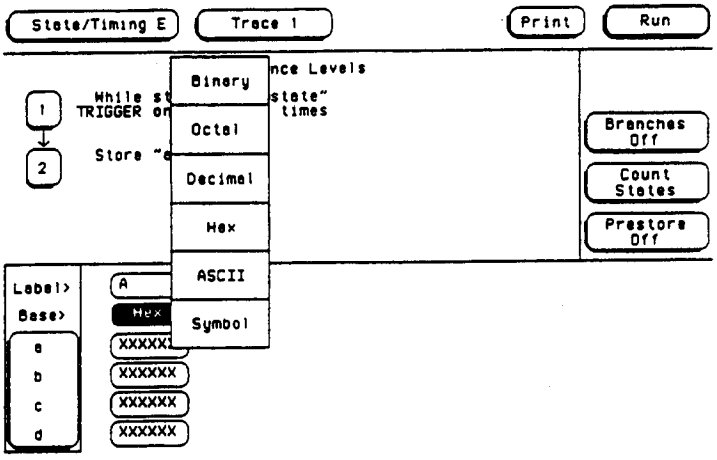


Figure 5-77. Numeric Base Pop-up Menu

One of the options in the Base pop-up is **ASCII**. It allows you to see the ASCII characters that are represented by the pattern you specify in the pattern fields.

Note

You cannot define ASCII characters directly. You must first define the pattern in one of the other number bases; then you can switch the base to ***ASCII*** *to see the ASCII characters.*

The **Symbol** option in the Base pop-up allows you to use a symbol that has been specified in the State Symbol Tables as a pattern. In the pattern fields you specify the symbols you want to use.

3 Qualifier Field If you select the qualifier field, you will see the following pop-up menu.

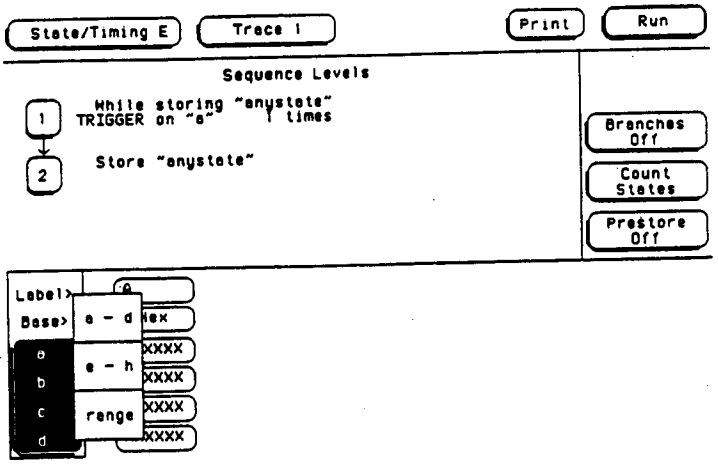


Figure 5-78. Qualifier Field Pop-up Menu

Patterns. The pattern recognizers are in two groups of four: **a-d** and **e-h**. If you select one of these two options, the qualifier field will contain only those pattern recognizers. For instance, the qualifier field in figure 5-76 contains only the recognizers **a-d**.

Ranges. If you select the **range** option, the qualifier and pattern fields look similar to that shown below.

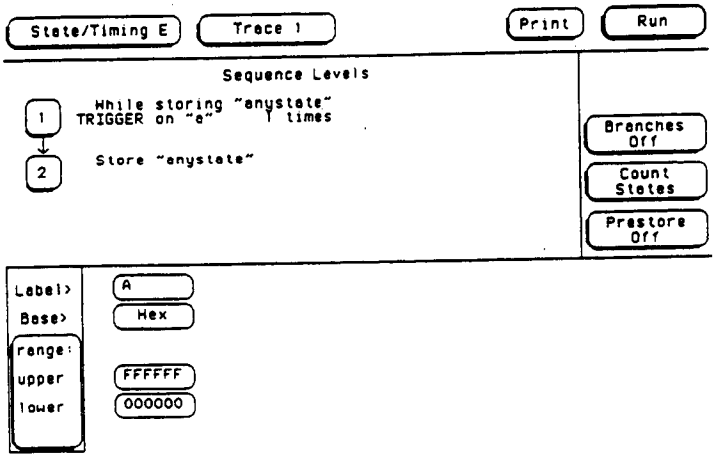


Figure 5-79. Range Qualifier and Pattern Fields

Only one range can be defined, and it can be defined over only one label, hence over only 32 channels. The channels don't have to be adjacent to each other. The logic analyzer selects the label over which the range will be defined by looking at the labels in order and choosing the first one that has channels assigned under only two pods. A label that contains channels from more than two pods cannot be selected for range definition. If all the labels have channels assigned under more than two pods, the range option is not offered in the qualifier field pop-up menu.

4 Pattern Fields

The pattern fields allow you to specify the states that you want the state analyzer to search for and store. Each label has its own pattern field that you use to specify a pattern for that label (if you are defining a pattern for a pattern recognizer).

During a run, the state analyzer looks for a specified pattern in the data. When it finds the pattern, it either stores the state or states, or it triggers, depending on the step that the sequencer is on.

6 Interpreting the Display

Introduction

This chapter describes the Timing Waveforms and State Listing menus and how to interpret them. It also tells you how to use the fields in each of these menus to manipulate the displayed data so you can find your measurement answers.

The Timing Waveforms Menu

The Timing Waveforms menu is the display menu of the timing analyzer. It is accessed by selecting Waveform 1(2) in the pop-up that appears when the field second from the left at the top of the screen is touched. It will automatically be displayed when RUN is selected.

There are two different areas of the timing waveforms display, the menu area and the waveforms area. The menu area is in the top one-fourth of the screen and the waveforms area is the bottom three-fourths of the screen.

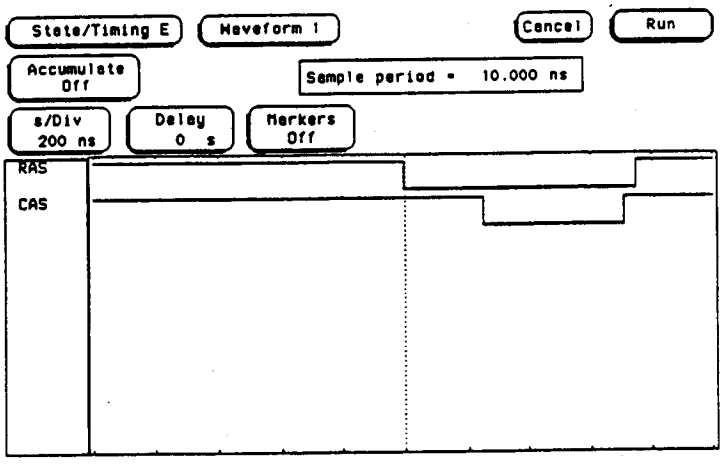


Figure 6-1. Timing Waveform Menu and Display

The waveforms area displays the data the timing analyzer acquires. The data is displayed in a format similar to an oscilloscope with the horizontal axis representing time and the vertical axis representing amplitude. The basic difference between an oscilloscope display and the timing waveforms are: the vertical axis only displays highs (above threshold) and lows (below threshold); lows are represented by a darker line for easy differentiation.

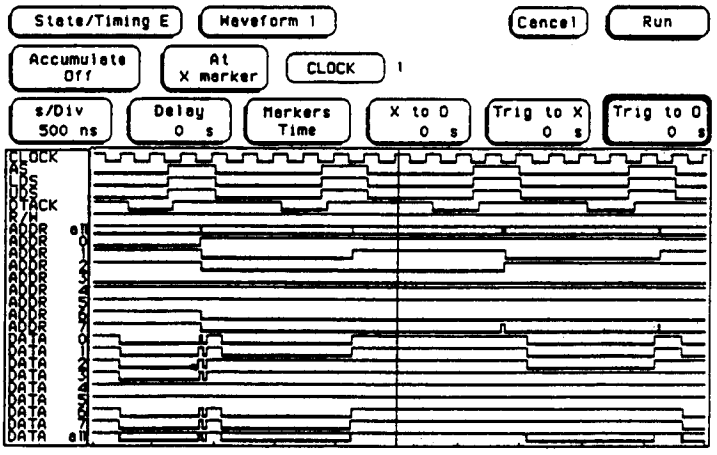


Figure 6-2. Timing Waveforms Menu with 24 Waveforms

Timing Waveforms Menu Fields

The menu area contains fields that allow you to change the display parameters, place markers, and display waveform measurement parameters.

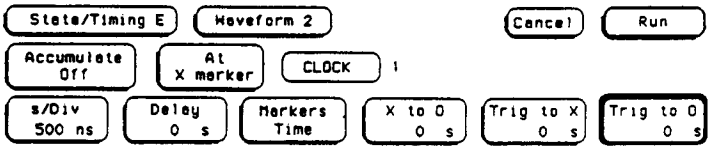


Figure 6-3. Timing Waveforms Menu Fields

Markers (Timing)

The Markers field allows you to specify how the X and O markers will be positioned on the timing data. The options are:

- Off
- Time
- Patterns
- Statistics

Markers Off/ Sample Period

When the markers are off they are not visible and the sample rate is displayed. In transitional timing mode, the sample rate will always be 10 ns. In Glitch, the sample period is controlled by the s/Div setting and can be monitored by turning the markers off.

Note

The sample period displayed is the sample period of the last acquisition. If you change the s/Div setting, you must touch Run to initiate another acquisition before the sample period is updated.

Although the markers are off, the logic analyzer still performs statistics, so if you have specified a stop measurement condition the measurement will stop if the pattern specified for the markers is found.

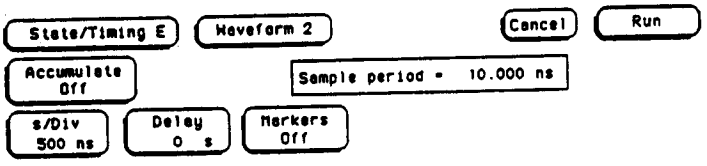


Figure 6-4. Markers Off

Markers Time

When the markers are set to Time, you can place the markers on the waveforms at events of interest and the logic analyzer will tell you:

- Time Trig(ger) to X
- Time Trig(ger) to O
- Time X to O

To position the markers, touch the appropriate field for marker selection. The field will turn light blue and can then be set using the knob. The Trig to X field controls the green marker and the Trig to O field controls the yellow marker. The trigger point is displayed with the red marker. To set the markers at a predetermined time relationship, touch the field a second time, the field will turn white and a numeric keypad will appear. Set the desired time reference, including the time units on the right column of the keypad, and touch done to close the pop-up.

When the X to O field is light blue, both markers can be moved with the knob, but the relative placement between them will not change.

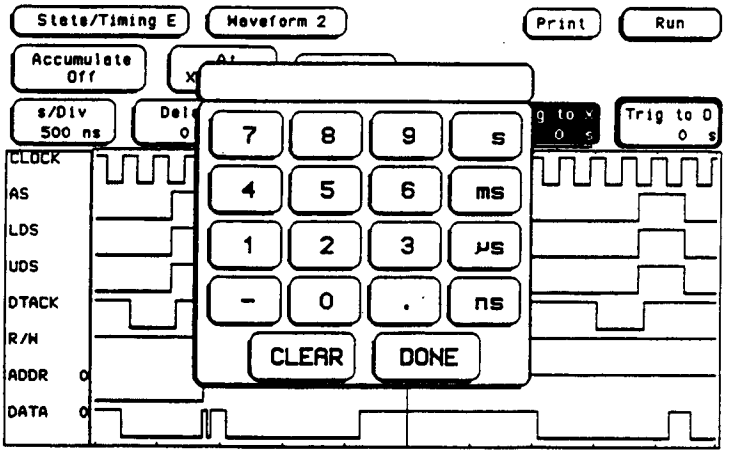


Figure 6-5. Time Reference Pop-up

Markers Pattern

When the markers are set to pattern you can specify patterns that the logic analyzer will place the markers on. You can also specify how many occurrences of each marker pattern the logic analyzer looks for. This use of the markers allows you to find time between specific patterns in the acquired data.

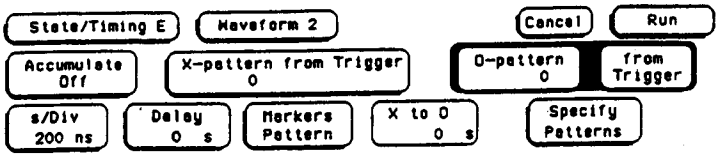


Figure 6-6. Markers Patterns Menu

Patterns for each marker (X and O) can be specified. Patterns can be specified for both markers in each label, however, the logic analyzer can only search one label at a time. You can also specify whether the marker is placed on the pattern at the beginning of its occurrence (entering) or end of its occurrence (leaving).

Another feature of markers set to patterns is the **Stop measurement when X-O ____**, which is in the pop-up that appears when you select **Specify Patterns**. The options are:

- Off
- Less than
- Greater than
- In range
- Not in range

With this feature you can use the logic analyzer to look for a specified time or range of time between the marked patterns and have it stop acquiring data when it sees this time between markers (The X marker must precede the O marker).

Note

The upper and lower range boundaries must not be the same value. For example, if you want to stop a measurement when the X and O markers are in range of 200 ns, you should set the range values to 190 ns and 210 ns. This eliminates erroneous measurement termination.

Markers Statistics

When statistics are specified for markers, the logic analyzer displays:

- Number of total runs
- Number of valid runs (runs where markers were able to be placed on specified patterns)
- Minimum time between the X and O markers
- Maximum time between the X and O markers
- Average time between the X and O markers

Statistics are based on the time between markers which are placed on specific patterns. If a marker pattern is not specified, the marker will be placed on the trigger point by the logic analyzer. In this case, the statistical measurement will be the time from the trigger to the specified marker.

How the statistics will be updated depends on the timing trace mode (single or repetitive).

In repetitive, statistics will be updated each time a valid run occurs until you press Stop. When you touch Run after Stop, the statistics will be cleared and will restart from zero.

In single, each time you touch Run an additional valid run will be added to the data and the statistics will be updated. This will continue unless you change the placement of the X and O markers between runs.

Accumulate Mode

Accumulate mode is selected by toggling the Accumulate On/Off field. When accumulate is on, the timing analyzer displays the data from a current acquisition on top of the previously acquired data.

When the old data is cleared depends on whether the trace mode is in single or repetitive. In single, new data will be displayed on top of the old each time Run is selected as long you stay in the Timing Waveforms menu between runs. Leaving the Timing Waveforms menu always clears the accumulated data. In repetitive mode, data is cleared from the screen only when you start a run after stopping acquistion with the Stop key or when changing menus.

At __ marker The At X (or O) marker _____ fields allow you to select either the X or O markers. You can place these markers on the waveforms of any label and have the logic analyzer tell you what the pattern is. For example, in the following timing waveforms display, the number 35 to the right of the field containing ADDR is the pattern in hexadecimal that is marked by the X marker. The base of the displayed field is determined by the base of the specified label you selected in the timing Trace menu. You can toggle the At__ marker field between the X an O markers.

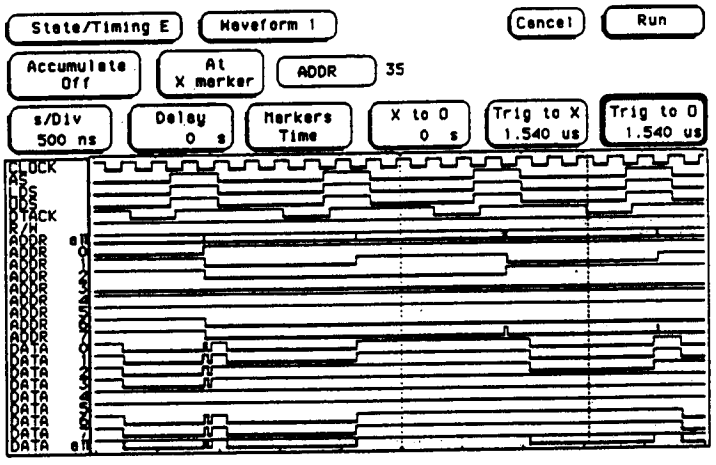


Figure 6-7. At X Marker ADDR fields

This display tells you that the pattern on the lines in the address label where the X marker is located is 35H.

The next field to the right of the At__ marker field will pop up when selected and show you all the labels assigned to the timing analyzer as shown below.

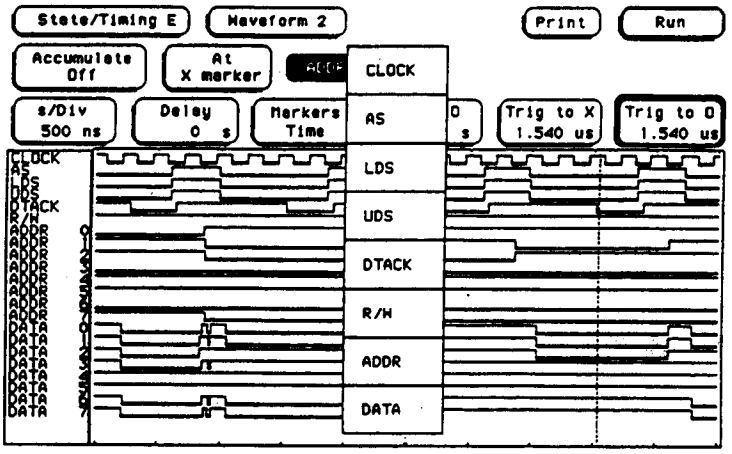


Figure 6-8. Label Option Pop-up

s/Div (seconds-per-division) Field

The seconds-per-division field allows you to change the time window of the Timing Waveforms menu.

To activate the s/Div field you must touch the field. The field will turn light blue indicating it can be controlled by the knob. The knob can increment or decrement the s/Div setting in a 1-2-5 sequence. If you touch the field again, a pop-up appears. Using the keypad on the pop-up you can change the seconds-per-division by entering integers and units. The range for the s/Div field is 10 ns/div to 100 s/div.

When you enter a value from the keypad, the seconds-per-division does not have to be a 1-2-5 sequence.

Note

Sample period is fixed at 10 ns in the Transitional acquisition mode. In Glitch mode, changing the s/Div setting changes the sample period for the next run. To view the sample period after the next run, turn the markers off if they are on and touch Run.

Delay Field

The delay field allows you to enter a delay. The delay can be either positive or negative. Delay allows you to place the time window (selected by s/Div) of the acquired data at center screen.

The center tic mark at the horizontal center and top of the waveforms area represents trigger + delay. The red vertical dotted line represents the trigger point (see figure 6-9).

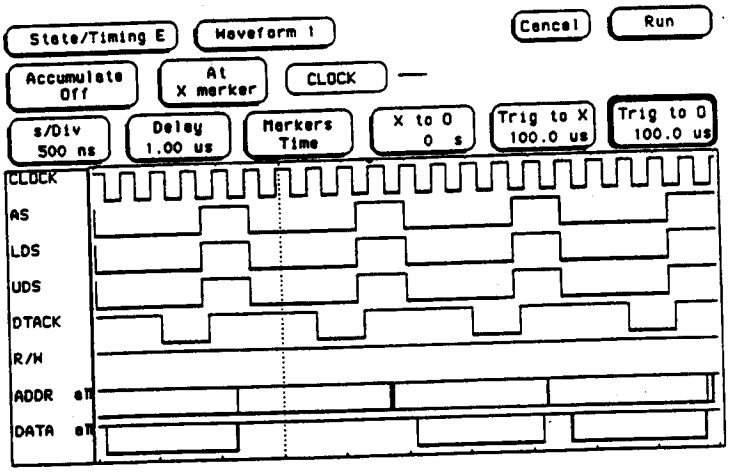


Figure 6-9. Trigger and Trace Points

If you want to trace after the trigger point, enter a positive delay. If you want to trace before the trigger point (similar to negative time), enter a negative delay. The logic analyzer is capable of maximum delays of -2500 seconds to +2500 seconds. In transitional mode the maximum delay is determined by the number of transitions of the incoming data. Data may not be displayed at all settings of s/Div and Delay.

In Glitch mode the maximum delay is 25 seconds, which is controlled by memory and sample period (512 X 50 ms). The sample rate is also dependent on the delay setting. It is represented by the following formula:

```
if delay < 20 ns
     Hwdelay = 20 ns (this is an instrument constant)
if delay > 10 ms
     Hwdelay = 10 ms
else Hwdelay = delay (delay setting in waveforms menu)

Sample period = larger of:
  s/Div - 25 or
  absolute value [(delay - Hwdelay) - 256]
If sample period > 50 ms
Then sample period = 50 ms
```

The State Listing Menu

The State Listing menu is the display menu of the state analyzer. It is accessed when the state analyzer is on. It will automatically be displayed when you press RUN.

There are two different areas of the state listing display, the menu area and the listing area. The menu area is in the top one-fourth of the screen and the listing area is the bottom three-fourths of the screen.

The listing area shows the data the state analyzer acquires. The data is displayed in a listing format as shown below.

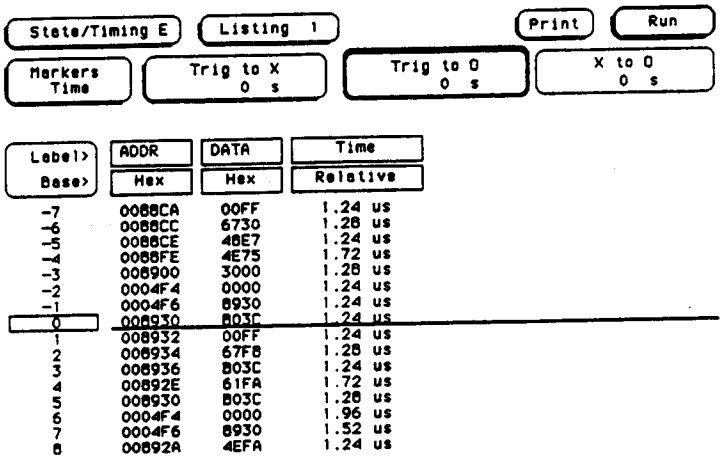


Figure 6-10. State Listing Menu

This listing display shows you 16 of the possible 1024 lines of data at one time. You can use the knob to roll the listing to the lines of interest.

The column of numbers at the far left represent the location of the acquired data in the state analyzer's memory. The trigger state is always 0. At the vertical center of this column you will see a box containing a number. The box is used to quickly select another location in the state listing.

The rest of the columns (except the Time/States column) represent the data acquired by the state analyzer. The data is grouped by label and displayed in the number base you have selected (hexadecimal is the default base). The Time or States column is on when you select either of these in the Count field of the Trace Menu.

The Time column displays either the Relative time (time from one state to the next) or Absolute time (time from each state to the trigger). The States column displays the number of qualified states Relative to the previously stored state or the trigger (absolute).

State Listing Menu Fields

The menu area contains fields that allow you to change the display parameters, place markers, and display listing measurement parameters.



Figure 6-11. State Listing Menu Fields

Markers (State)

The two markers (X & O) are horizontal lines that appear crossing the data area of the display when they are turned on. Each marker has a unique color and the border of its respective marker field is the same color. The default color for the X marker color is green and the default color for the O marker color is yellow. The Markers field allows you to specify how the X and O markers will be positioned. The marker options are:

If Count is off (as specified in the Trace menu):
- Off
- Pattern

If Count is on Time (as specified in the Trace menu):
- Off
- Pattern
- Time
- Statistics

If Count is on States (as specified in the Trace menu):
- Off
- Pattern
- States

Markers Off When the markers are off they are not displayed, but are still placed at the specified points in the data. If Stop measurement is on and the Stop measurement criteria are present in the data, the measurement will stop even though the markers are off.

Markers Pattern When the markers are set to patterns, you can specify patterns on which the logic analyzer will place the markers. You can also specify how many occurrences of each marker pattern the logic analyzer looks for. This use of the markers allows you to find a specific pattern for each label in the acquired data.

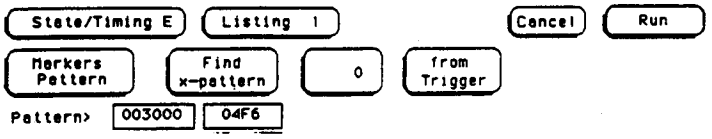


Figure 6-12. Markers Pattern

Patterns for each marker (X and O) can be specified. Patterns can be specified for both markers in each label. The logic analyzer searches for the logical "and" of patterns in up to 20 labels.

In the X (O)-pattern from Trigger field you specify how many occurrences of the marked pattern from a reference point you want the logic analyzer to search for. The reference points are:

- Trigger
- Start (of a trace)
- X Marker (only available when searching for the O marker).

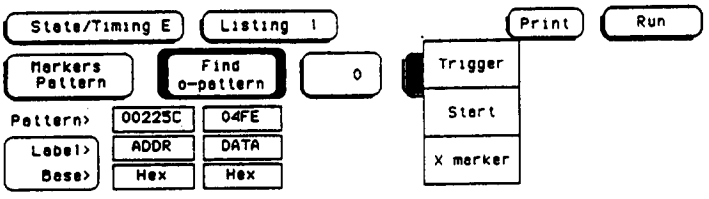


Figure 6-13. Search Reference Pop-up

Another feature of markers set to patterns is the Stop measurement when X-O ____. which is found in the Specify Patterns field. The options are:

- Off
- Less than
- Greater than
- In range
- Not in range

This feature is only available when Count is set to Time in the Trace menu. With this feature you can use the logic analyzer to look for a specified time or range of time between the marked patterns and to stop acquiring data when it finds this time between markers. The X marker must precede the O marker.

Note

The upper and lower range boundaries must not be the same value. For example, if you want to stop a measurement when the X and O markers are in range of 200 ns, you should set the range values to 190 ns and 210 ns. This eliminates erroneous measurement termination.

Markers Time

When the markers are set to Time, you can place the markers on states in the listing of interest and the logic analyzer will tell you:

- Trig(ger) to X
- Trig(ger) to O
- Time X to O

To position the markers, touch the field of the marker you wish to position.

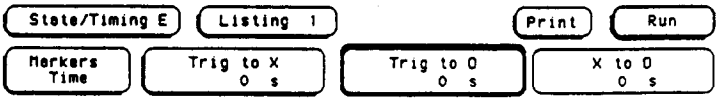


Figure 6-14. Markers Time

The Time X to O field will change according to the position of the X and O markers. It displays the total time between the states marked by the X and O markers.

Markers Statistics

When statistics are specified for markers, the logic analyzer will display the:

- Total runs
- Number of valid runs (runs where markers were able to be placed on specified patterns)
- Minimum time between the X and O markers
- Maximum time between the X and O markers
- Average time between the X and O markers

How the statistics will be updated depends on the state trace mode (single or repetitive).

In repetitive, statistics will be updated each time a valid run occurs until you touch Stop. When you touch Run after Stop, the statistics will be cleared and will restart from zero.

In single, each time you touch Run an additional valid run will be added to the data and the statistics will be updated. This will continue unless you change the placement of the X and O markers between runs.

Markers States

When the Count is set to State in the State Trace Specification menu, you have the option of placing the X and O markers on states of interest in the listing and the logic analyzer will tell you:

- Trig(ger) to X
- Trig(ger) to O
- X to O (x)

This feature is similar to "Markers Time" except the number of states are displayed instead of time.

Timing/State Mixed Mode Display

When both timing and state analyzers are on, you can display both the State Listing and the Timing Waveforms simultaneously as shown.

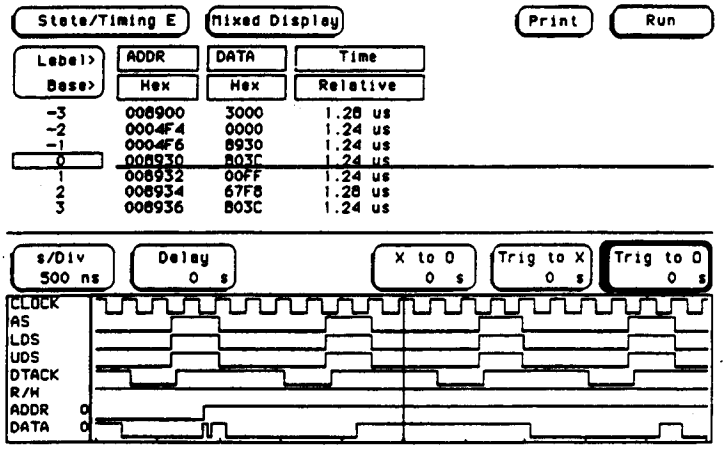


Figure 6-15. Timing/State Mixed Mode Display

The data in both parts of the display can be time correlated as long as Count (State Trace menu) is set to Time.

The markers for the State Listing and the Timing Waveform in time-correlated Mixed Mode are different from the markers in the individual displays. You will need to place the markers on your points of interest in the time-correlated Mixed Mode even though you have placed them in the individual displays.

State/State Mixed Mode Display

When two state analyzers are on, the logic analyzer can display both state listings as shown in figure 6-16. The acquired data of both machines is interlaced.

The State/State mixed mode can be set up in either Listing 1 or Listing 2. For example, the mixed display in figure 6-16 is in Listing 1. The data acquired by machine 1 is displayed with the state location numbers centered in the far left column. The data acquired by machine 2 is displayed with the state location numbers offset to the right of this column.

To time correlate data from two state machines, the Count (State Trace Menu) for both machines must be set to Time.

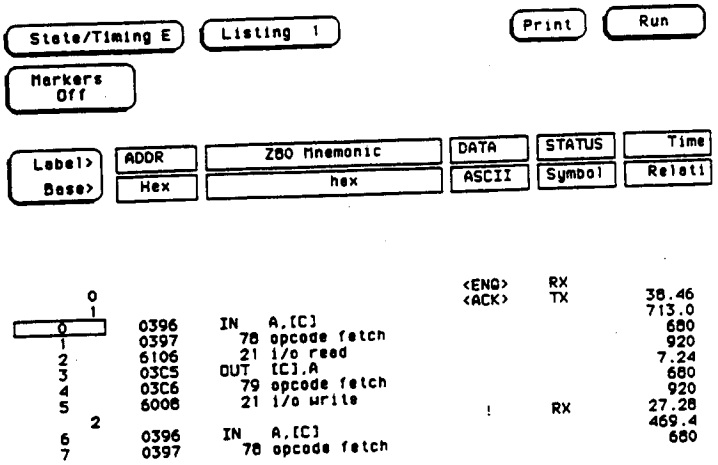


Figure 6-16. State/State Mixed Mode Display

The markers for a State/State time-correlated Mixed Mode will be the same as the markers placed in each of the individual State Listings.

To display a two state mixed mode listing you must start with a single state listing. In this example, Listing 1 is the starting point. The desired display is:

- addresses of machine 1
- inverse assembled data of machine 1
- data on the data bus of machine 2
- status of machine 2

Start with the Listing 1 display by touching the STAT field. The following pop-up appears:

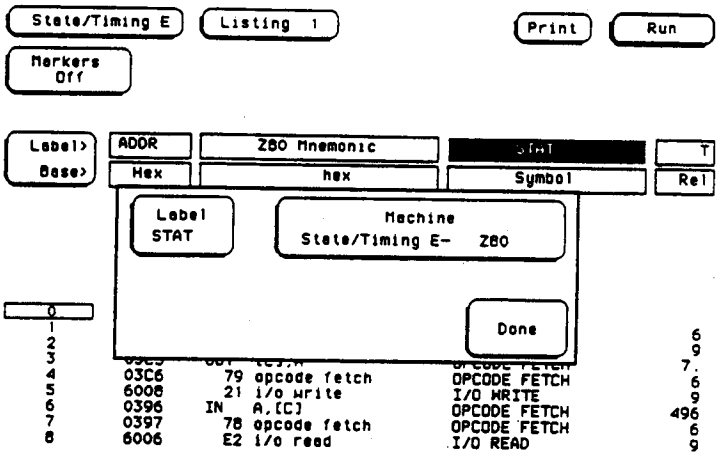


Figure 6-17. Machine and Label Pop-up

With this pop-up you can select a label from either machine to be displayed where the label "STAT" is now displayed. In this example, you want the data from machine 2. Touch the "Machine - State/TimingE- Z80" field.

When the pop-up appears, choose the machine that will supply data for the display. Since you want to see the data from the data bus of the other state analyzer (State/Timing E-RS232 PORT), touch this field in the pop-up.

The pop-up will close and machine 2 will supply data for this label location on screen.

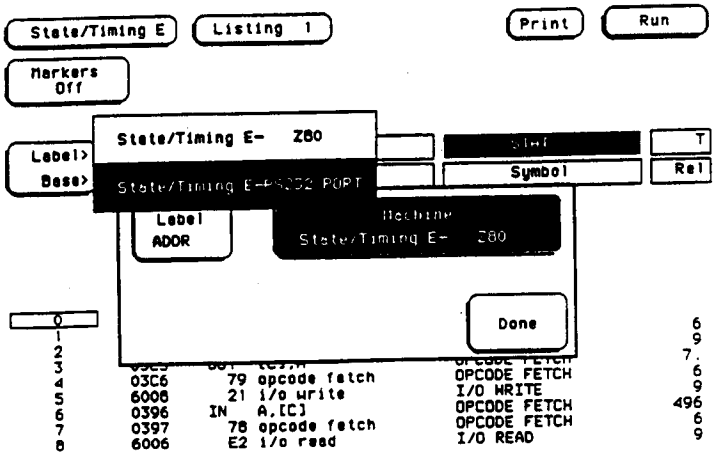


Figure 6-18. Machine Selection Pop-up

You now must specify what label you want from machine 2. The field to the left of the machine pop-up allows you to select a label from the labels assigned to machine 2. Touch this field to view the labels assigned to machine 2.

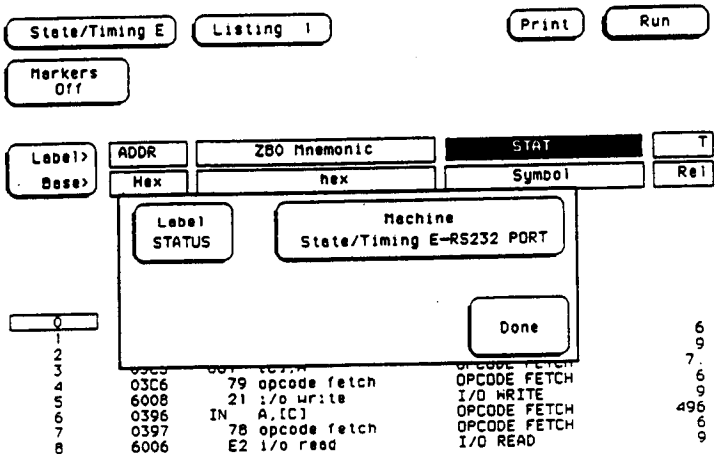


Figure 6-19. Machine 2 Label Field

When the pop-up appears, touch the "DATA" field.

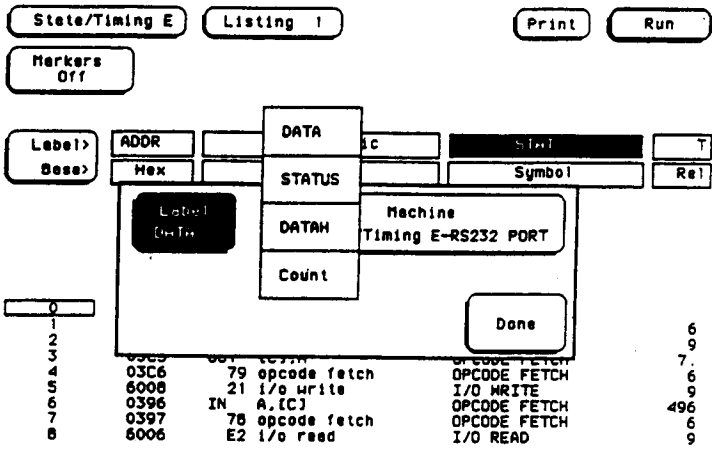


Figure 6-20. Machine 2 Labels Pop-up

When you are finished selecting the machine and the label, touch Done to close the original pop-up. The data from machine 2 replaces STAT in Listing 1.

Time-Correlated Displays

The HP 16510A Logic Analyzer can time-correlate data between the timing analyzer and the state analyzer and between two state analyzers.

The logic analyzer uses a counter to keep track of the time between the triggering of one analyzer and the triggering of the second. It uses this count in the mixed mode displays to reconstruct time-correlated data.

7 Using The Timing Analyzer

Introduction

In this chapter you will learn how to use the timing analyzer by setting up the logic analyzer to make a simple measurement. We give you the measurement results as actually measured by the logic analyzer, since you may not have the same circuit available.

The exercise in this chapter is organized in a task format. The tasks are ordered in the same way you will most likely use them once you become an experienced user. The steps in this format are both numbered and lettered. The numbered steps state the step objective. The lettered steps explain how to accomplish each step objective. There is also an example of each menu after it has been properly set up.

How you use the steps depends on how much you remember from chapters 1 through 5. If you can set up each menu by just looking at the menu picture, go ahead and do so. If you need a reminder of what steps you need to perform, follow the numbered steps. If you still need more information about "how," use the lettered steps.

Problem Solving with the Timing Analyzer

In this exercise, assume you are designing a dynamic RAM memory (DRAM) controller and you must verify the timing of the row address strobe (RAS) and the column address strobe (CAS). You are using a 4116 dynamic ram and the data book specifies that the minimum time from when LRAS is asserted (goes low) to when LCAS is no longer asserted (goes high) is 250 ns. You could use an oscilloscope but you have an HP 16500A/510A on your bench. Since the timing analyzer will do just fine when you don't need voltage parametrics, you decide to go ahead and use the logic analyzer.

What Am I Going to Measure?

After configuring the logic analyzer and hooking it up to your circuit under test, you will be measuring the time (x) from when the RAS goes low to when the CAS goes high, as shown below.

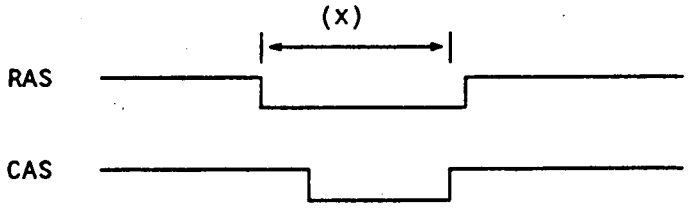


Figure 7-1. RAS and CAS Signals

How Do I Configure the Logic Analyzer?

In order to make this timing measurement, you must configure the logic analyzer as a timing analyzer. By following these steps you will configure Analyzer 1 as the timing analyzer.

If you are in the **State/Timing E Configuration** menu you are in the right place and you can start with step 2; otherwise, start with step 1.

1. Touch the field in the upper left corner of the display and select **State/Timing E**.

2. In the **State/Timing E Configuration** menu, change Analyzer 1 type to **Timing**. If Analyzer 1 is already a timing analyzer, go on to step 3.

   a. Touch the field **Type:** _____ .

   b. When the pop-up appears, touch **Timing**.

3. Name Analyzer 1 "DRAM TEST" (optional)

   a. Touch the field to the right of **Name:**_____ of Analyzer 1.

   b. Using the alphanumeric keyboard pop-up, change the name of Analyzer 1 to "DRAM TEST."

4. Assign pod 1 to the timing analyzer.

   a. Touch the **Pod 1** field.

   b. When the pop-up appears, touch DRAM TEST (or Machine 1) to assign pod 1 to Analyzer 1.

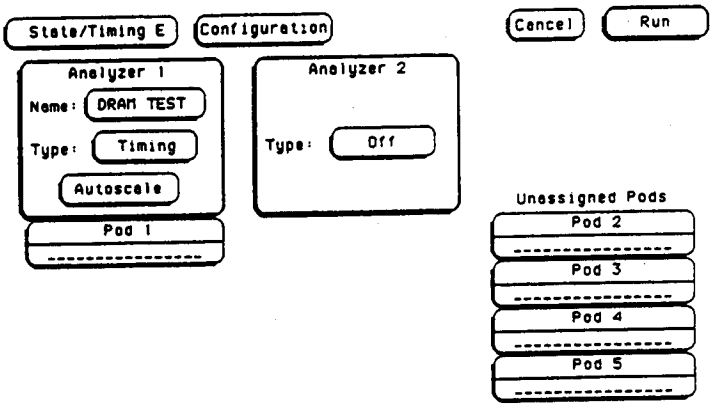


Figure 7-2. State/Timing E Configuration Menu

Connecting the Probes

At this point, if you had a target system with a 4116 DRAM memory IC, you would connect the logic analyzer to your system.

Since you will be assigning Pod 1 bit 0 to the RAS label, you hook Pod 1 bit 0 to the memory IC pin connected to the RAS signal. You hook Pod 1 bit 1 to the IC pin connected to the CAS signal.

Activity Indicators

When the logic analyzer is connected and your target system is running, you will see two ↕ at the right-most end (least significant bits) of the Pod 1 field in the **State/Timing E Configuration** menu. This indicates the RAS and CAS signals are transitioning.

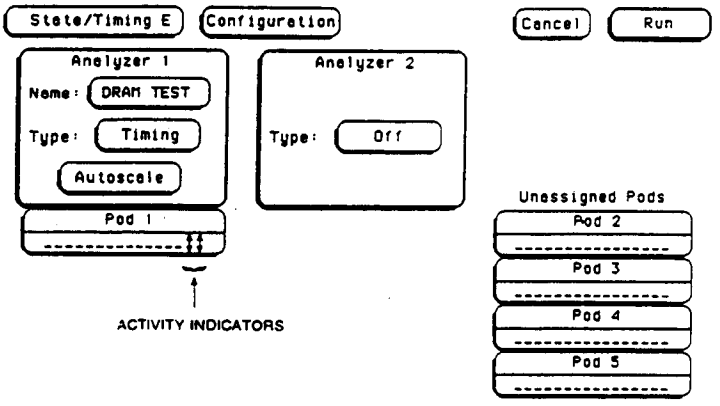


Figure 7-3. Activity Indicators

Configuring the Timing Analyzer

Now that you have configured the system, you are ready to configure the timing analyzer. You will be:

- Creating two names (labels) for the input signals
- Assigning the channels connected to the input signals
- Specifying a trigger condition

1. Display the Timing Format Specification menu.

   a. Touch the field second from the left in the upper left corner.

   b. When the pop-up appears, touch the **Format 1** field.

2. Name two labels, one RAS and one CAS.

   a. Touch the top field in the label column.

   b. When the pop-up appears, touch **Modify Label**.

   c. Using the alphanumeric keyboard, enter the label RAS and touch **DONE**.

   d. Touch the next field down from the RAS label and repeat steps b and c for the CAS label.

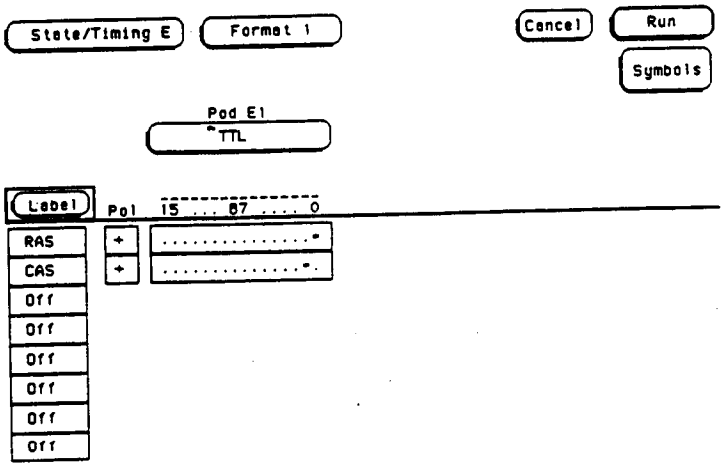


Figure 7-4. Timing Format Specification Menu

3. Assign the channels connected to the input signals (Pod 1 bits 0 and 1) to the labels RAS and CAS respectively.

   a. Touch the bit assignment field below Pod 1 and to the right of RAS.

   b. Any combination of bits may be assigned to this pod; however, you will want only bit 0 assigned to the RAS label. The easiest way to assign bits is to touch **CLEAR** to un-assign any assigned bits before you start.

   c. Use the knob to position the cursor on bit 0 (right most bit) in the bit assignment pop-up and touch the asterisk field. This will place an asterisk in the 0 bit. Touch **DONE** when the asterisk is in place.

   d. Assign Pod 1 bit 1 to the CAS label by touching the CAS bit assignment field and placing the cursor on bit one and touching the asterisk. Touch **DONE** when complete.

Specifying a Trigger Condition

To capture the data and then place the data of interest in the center of the display of the timing waveform menu, you need to tell the logic analyzer when to trigger. Since the first event of interest is when the LRAS is asserted (negative- going edge of RAS), you need to tell the logic analyzer to trigger on a negative-going edge of the RAS signal.

1. Display the Timing Trace Specification menu.

   a. Touch the field second from the left in the upper left corner.

   b. When the pop-up appears, touch the **Trace 1** field.

2. Set the trigger so that the logic analyzer triggers on the negative-going edge of the RAS.

   a. Touch the **Then find Edge** field under the label RAS.

   b. When the pop-up appears, touch the field with the arrow pointing down. This selects a negative-going edge. Touch **DONE** when your selection is complete.

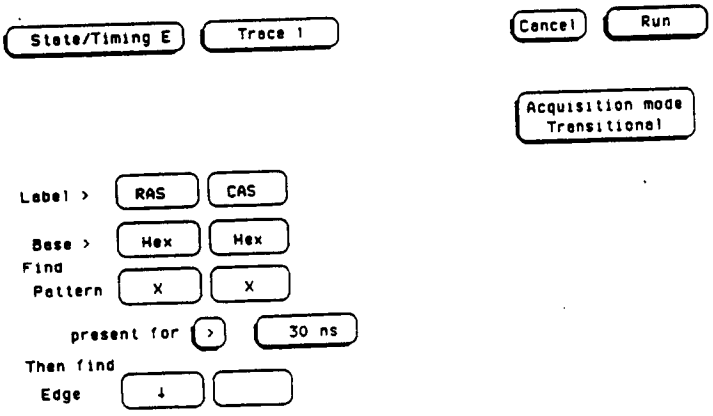


Figure 7-5. Timing Trace Specification Menu

Acquiring the Data

Now that you have configured and connected the logic analyzer, you acquire the data for your measurement by touching the **Run** field. The display switches to the Timing Waveforms menu when the logic analyzer starts acquiring data. The logic analyzer will look for a negative edge on the RAS signal and trigger if it sees one.

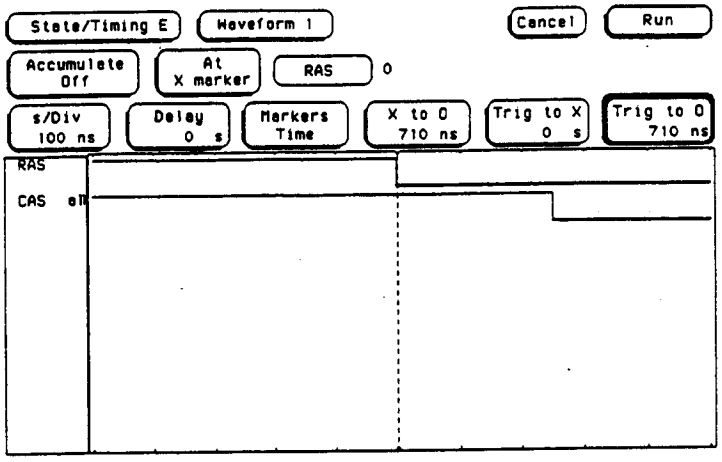


Figure 7-6. Timing Waveforms Menu

If this is the first time you acquire data and you have not previously set up the Timing Waveforms menu, you will see a label named "RAS" and a label named "CAS all." The "CAS all" indicates all bits assigned to the CAS label will be displayed. In this example, "CAS" and "CAS all" will be the same since only one bit has been assigned to the CAS label. To turn on just the "CAS" label and delete the "CAS all" label, follow these steps:

1. Touch the large blue field where the "CAS all" label resides.
2. When the pop-up appears, place the cursor on the "CAS all" label and touch the **Delete** field.
3. Touch the "CAS" field and the "CAS" label will appear below the "RAS" label.
4. Touch **Done** when you are finished.

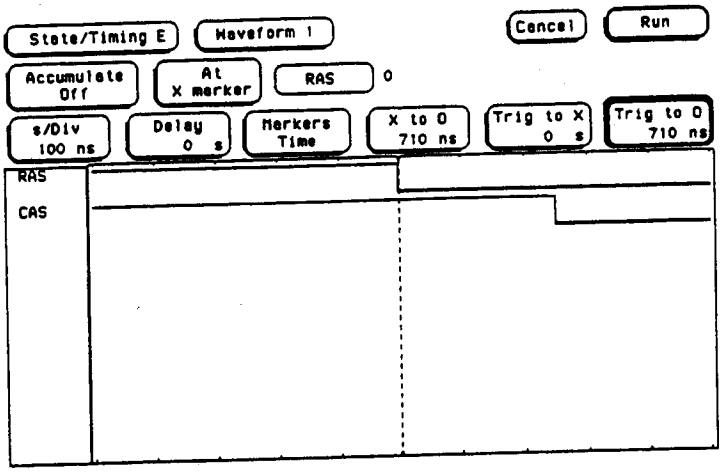


Figure 7-7. RAS and CAS labels

The RAS label shows you the RAS signal and the CAS label shows you the CAS signal. Notice the RAS signal goes low at or near the center of the waveform display area (horizontal center).

The Timing Waveform Menu

The timing waveform menu differs from the other menus you have used so far in this exercise. Besides displaying the acquired data, it has menu fields that you use to change the way the acquired data is displayed and fields that give you timing answers. Before you can use this menu to find answers, you need to know some of the special symbols and their functions. The symbols are:

- The green and yellow dotted lines
- The red dotted line

The Green and Yellow Dotted Lines

The X and O are markers are green and yellow vertical dotted lines respectively. You can use them to find your answer. You place them on the points of interest on your waveforms and the logic analyzer displays the time between the markers. The X and O markers will be in the center of the display when X to trig(ger) and O to trig(ger) are both 0.000 s (see example below).

The X marker displayed is green and the O marker displayed is yellow. The trigger marker is red.

The Red Dotted Line

The red vertical dotted line indicates the trigger point you specified in the Timing Trace Specification menu. The red dotted line is at center screen and is superimposed on the negative-going edge of the RAS signal.

Configuring the Display

Now that you have acquired the RAS and CAS waveforms, you need to configure the Timing Waveforms menu for best resolution and to obtain your answer.

Display Resolution

You get the best resolution by changing the seconds per division (s/Div) to a value that displays one negative-going edge of both the RAS and CAS waveforms. Set the **s/Div** by following these steps.



Figure 7-8. RAS and CAS Signals

1. Touch the **s/Div** field one time (the field will turn light blue) to allow you to adjust the horizontal scaling with the front-panel knob. Touch the **s/Div** field one more time (the field will turn white) and use the keypad pop-up to select any scaling you desire.

2. While the field is light blue, rotate the knob until your waveform shows you only one negative-going edge of the RAS and one positive-going edge of the CAS waveform (see above). In this example 200 ns is best.

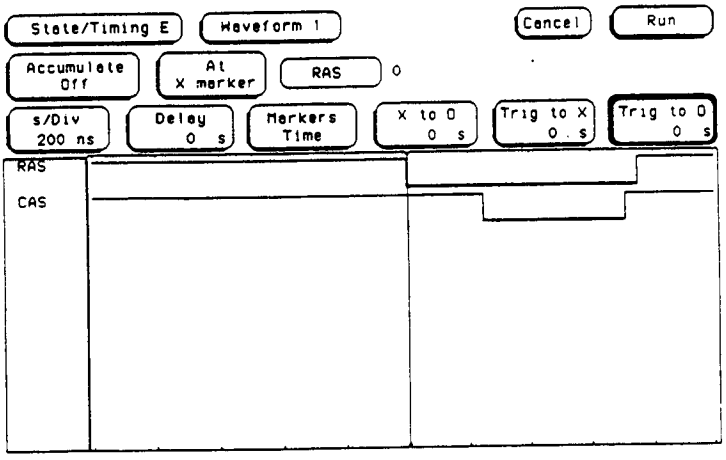


Figure 7-9. Waveform at 200 ns/Div

Making The Measurement

What you want to know is how much time elapses between the time RAS goes low and the time CAS goes high again. You will use the X and O markers to quickly find the answer. Remember you specified the negative-going edge of the RAS to be your trigger point, therefore the X marker (green) should be on this edge if the X to Trig field = 0. If not, follow steps 1 and 2.

1. Touch the **Trig to X** field. The field will turn light blue. At this time you can either adjust the X to trigger time using the front-panel knob, or touch the field again and use the keypad to set the time to 0. Notice that this step has superimposed the X marker (green) over the trigger marker (red).

2. Touch the **Trig to O** field. The field will turn light blue. At this time you should use the front-panel knob to set O marker (yellow) on the positive going edge of the CAS waveform. It is possible to touch the field again and use the keypad pop-up to set the desired time, however, you do not know the time to set it to. The knob allows you to place the marker wherever you want it to be.

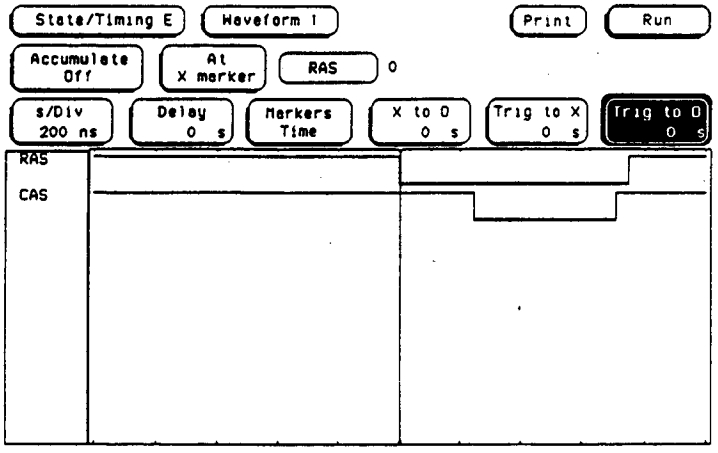


Figure 7-10. Marker Placement

Finding the Answer

Your answer could be calculated by adding the **Trig to X** and **Trig to O** times, but you don't have to. The logic analyzer has already calculated this answer and displays it in the **X to O** field on the display.

This example indicates the time is 710 ns. Since the data book specifies a minimum of 250 ns, it appears your DRAM controller circuit is designed properly.

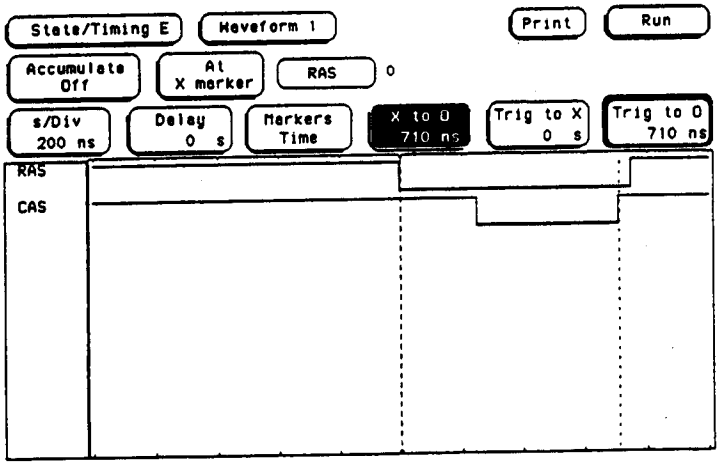


Figure 7-11. Time X to O

Summary

You have just learned how to make a simple timing measurement with the HP 16510A logic analyzer. You have:

- specified a timing analyzer
- assigned pod 1
- assigned bits
- assigned labels
- specifed a trigger condition
- learned which probes to connect
- acquired the data
- configured the display
- set the s/Div for best resolution
- positioned the markers for the measurement answer

You have seen how easy it is to use the timing analyzer to make timing measurements which you could have made with a scope. You can use the timing analyzer for any timing measurement that doesn't require voltage parametrics or doesn't go beyond the accuracy of the timing analyzer.

The next chapter teaches you how to use the state analyzer. You will go through a simple state measurement in the same way you did the timing measurement in this chapter.

8 Using The State Analyzer

Introduction

In this chapter you will learn how to use the state analyzer by setting up the logic analyzer to make a simple state measurement. We give you the measurement results as actually measured by the logic analyzer, since you may not have the same circuit available.

The exercise in this chapter is organized in a task format. The tasks are ordered in the same way you will most likely use once you become an experienced user. The steps in this format are both numbered and lettered. The numbered steps state the step objective. The lettered steps explain how to accomplish each step objective. There is also an example of each menu after it has been properly set up.

How you use the steps depends on how much you remember from the *Getting Started Guide*. If you can set up each menu by just looking at the menu picture, go ahead and do so. If you need a reminder of what steps you need to perform, follow the numbered steps. If you still need more information about "how," use the lettered steps.

Problem Solving with the State Analyzer

In this example assume you have designed a microprocessor controlled circuit. You have completed the hardware, and the software designer has completed the software and programmed the ROM (read-only memory). When you turn your circuit on for the first time, it doesn't work properly. You have checked the power supply voltages and the system clock and they are working properly.

Since the circuit has never worked before, you and the software engineer aren't sure if it is a hardware or software problem. You need to do some testing to find a solution.

What Am I Going to Measure?

You decide to start where the microprocessor starts when power is applied. We will describe a 68000 microprocessor; however, every processor has similiar start-up routines.

When you power up a 68000 microprocessor it is held in reset for a specific length of time before it starts doing anything to stabilize the power supplies. The time the microprocessor is held in reset ensures stable levels (states) on all the devices and buses in your circuit. When this reset period has ended, the 68000 performs a specific routine called "fetching the reset vector."

The first thing you check is the time the microprocessor is held in reset. You find the time is correct. The next thing to check is whether the microprocessor fetches the reset vector properly.

The steps of the 68000 reset vector fetch are:

1. Set the stack pointer to a location you specify which is in ROM at address locations 0 and 2.

2. Find the first address location in memory where the microprocessor fetches its first instruction. This is also specified by you and stored in ROM at address locations 4 and 6. What you decide to find out is:

    1. What ROM address does the microprocessor look at for the location of the stack pointer, and what is the stack pointer location stored in ROM?

    2. What ROM address does the microprocessor look at for the address where its first instruction is stored in ROM, and is the instruction correct?

    3. Does the microprocessor then go to the address where its first instruction is stored?

    4. Is the executable instruction stored in the first instruction location correct?

Your measurement, then, requires verification of the sequential addresses the microprocessor looks to and of the data in ROM at these addresses. If the reset vector fetch is correct (in this example), you will see the following list of numbers in HEX (default base) when your measurement results are displayed.

```
+0000  000000  0000
+0001  000002  04FC
+0002  000004  0000
+0003  000006  8048
+0004  008048  3E7C
```

This list of numbers will be explained in detail later in this chapter in "The State Listing."

How Do I Configure the Logic Analyzer?

In order to make this state measurement, you must configure the logic analyzer as a state analyzer. By following these steps you will configure Analyzer 1 as the state analyzer.

If you are in the **State/Timing E Configuration** menu you are in the right place and you can start with step 2; otherwise, start with step 1.

1. Using the field in the upper left corner and the field second from the left of the display, get the **State/Timing E Configuration** menu on screen.

   a. Touch the field on the left and when the pop-up appears, touch the field labeled **State/Timing E**.

   b. Touch the field second from the left. When the pop-up appears, touch **Configuration**.

2. In the **State/Timing E Configuration** menu, change the Analyzer 1 type to **State**. If Analyzer 1 is already a state analyzer, go on to step 3.

   a. Touch the field to the right of **Type:** _____.

   b. Touch the field labeled **State**.

3. Name Analyzer 1 **68000STATE** (optional)

   a. Touch the field to the right of **Name:** _____.

   b. When the alphanumeric keyboard pop-up appears, touch the appropriate keys to change the name to **68000STATE**.

   c. Touch **DONE** when you finish entering the name.

4. Assign pods 1, 2, and 3 to the state analyzer.

   a. Touch **Pod 1** field if it is not already assigned to the state analyzer.

   b. In the Pod 1 pop-up, touch the field labeled **68000STATE**.

   c. Repeat steps a and b for pods 2 and 3.

The display should reflect the configuration shown below:

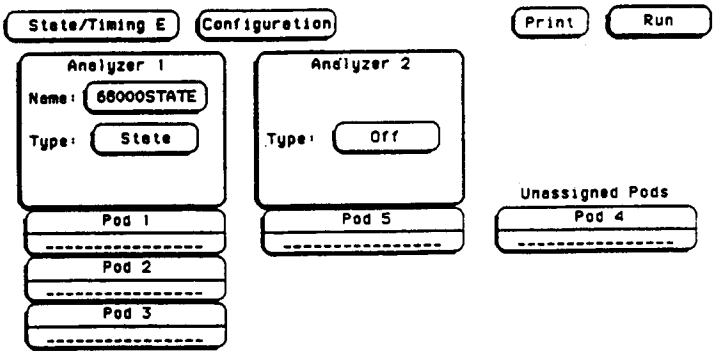


Figure 8-1. State/Timing E Configuration Menu

Connecting the Probes

At this point, if you had a target system with a 68000 microprocessor, you would connect the logic analyzer to your system. Since you have assigned labels ADDR and DATA, you would hook the probes to your system accordingly.

- Pod 1 probes 0 through 15 to the data bus lines D0 through D15.
- Pod 2 probes 0 through 15 to the address bus lines A0 through A15.
- Pod 3 probes 0 through 7 to the address bus lines A16 through A23.
- Pod 1, CLK (J clock) to the address strobe (LAS).

Activity Indicators

When the logic analyzer is connected and your target system is running, you will see ↕ in the Pod 1, 2, and 3 fields of the **State/Timing E Configuration** menu. This indicates which signal lines are transitioning.

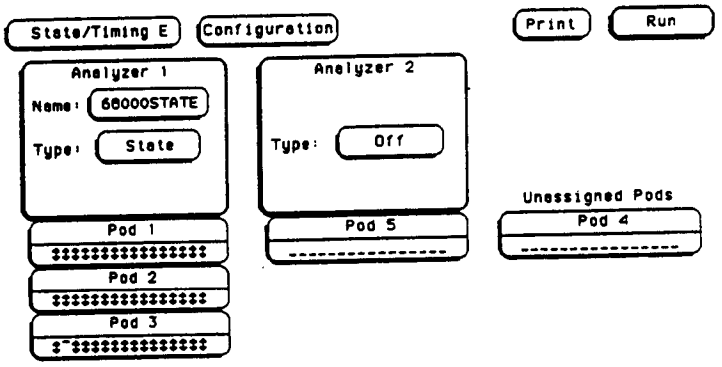


Figure 8-2. Activity Indicators

Configuring the State Analyzer

Now that you have configured the system, you are ready to configure the state analyzer. You will be:

- Creating two names (labels) for the input signals
- Assigning the channels connected to the input signals
- Specifying the State (J) clock
- Specifying a trigger condition

1. Display the State Format Specification menu.

   a. Touch the field second from the left at the top of the screen.

   b. When the pop-up appears, touch the field labeled **Format 1**.

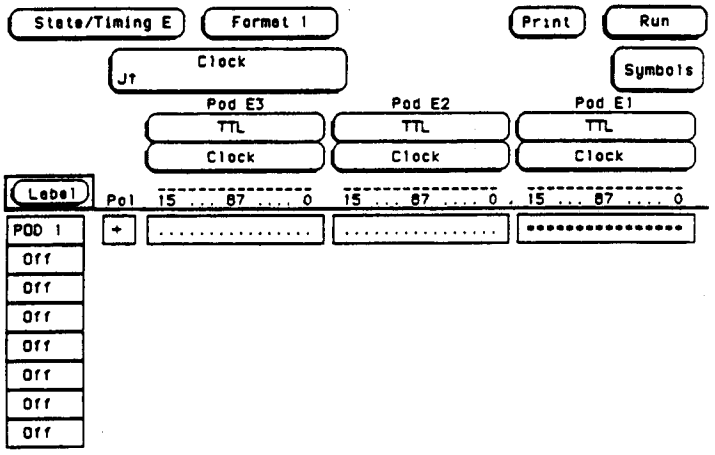


Figure 8-3. State Format Specification Menu

2. Name two labels, one ADDR and one DATA.

   a. Touch the top field in the label column.

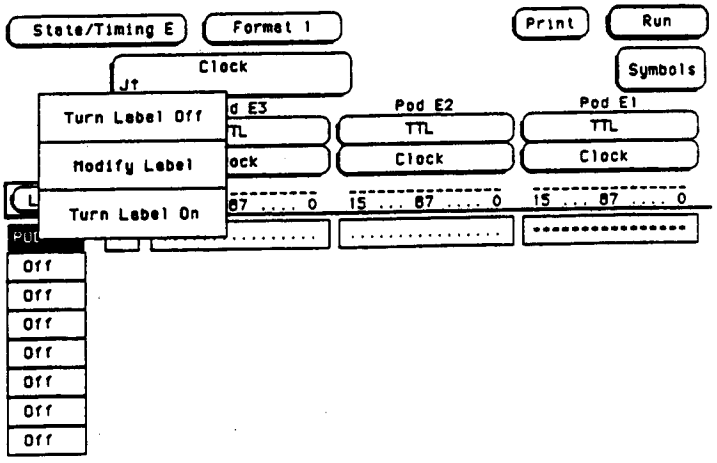


Figure 8-4. Label Selection

b. When the pop-up appears, touch **Modify Label**.

c. With the alphaneumeric keypad, change the name of the label to ADDR.

d. Touch **DONE** to close pop-up.

e. Name the second label DATA.

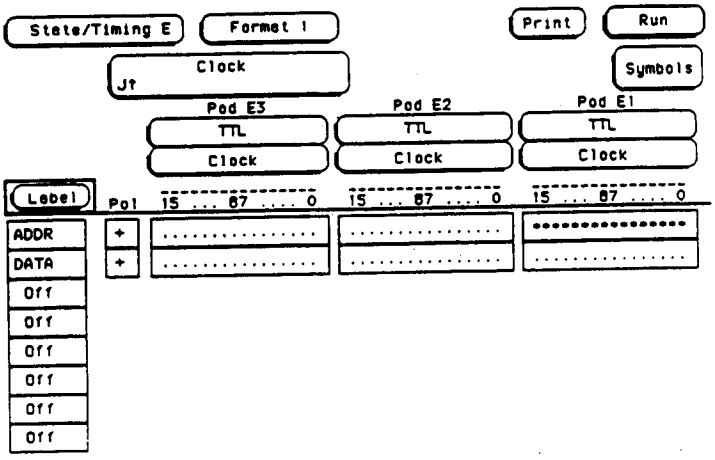


Figure 8-5. State Format Specification with Labels Assigned

3. Assign Pod 1 bits 0 through 15 to the label DATA.

   a. Touch the the bit assignment field below Pod E1 and to the right of DATA. You will see the following pop-up.

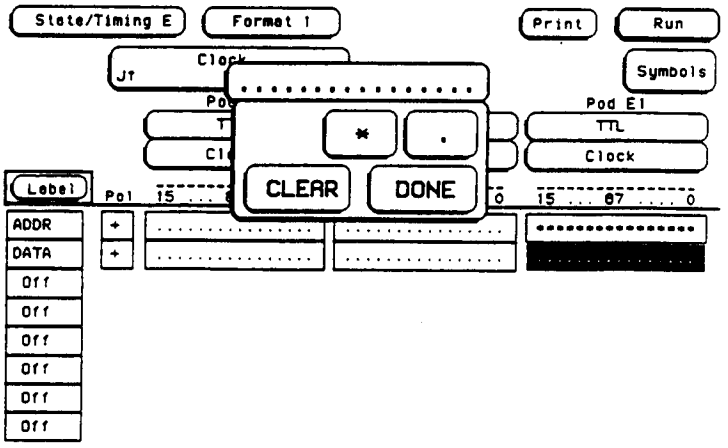


Figure 8-6. Bit Assignment Field

Any combination of bits may already be assigned to this pod; however, you will want all 16 bits assigned to the DATA label.

   b. Using the knob, place the cursor on each un-assigned bit one at a time and touch the asterisk (*) field. When all 16 bits are assigned, touch **DONE** to close the pop-up.

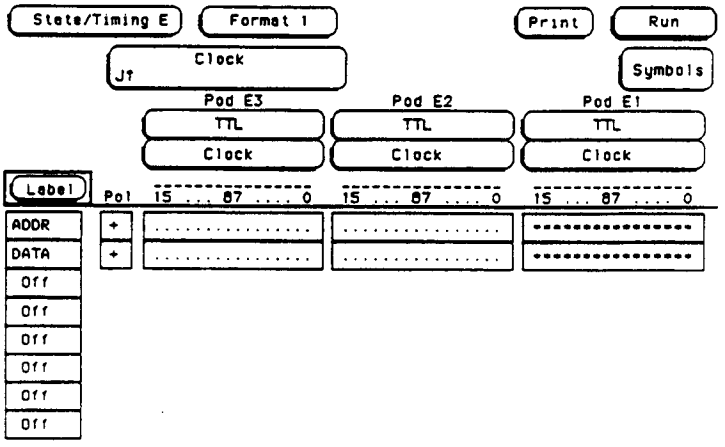


Figure 8-7. Pod E1 Bit Selection

4. Assign Pod E2 bits 0 through 15 to the label ADDR by repeating step 3.

5. Assign Pod E3 bits 0 through 7 to the label ADDR.

The State Format Specification menu should now look like that below.

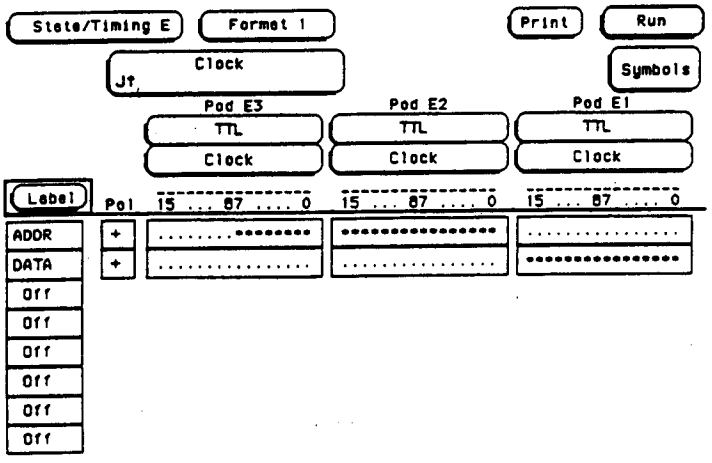


Figure 8-8. State Format Specification Menu with Bits Assigned

Specifying the J Clock

If you remember from "What's a State Analyzer" in *Feeling Comfortable With Logic Analyzers*, the state analyzer samples the data under the control of an external clock which is "synchronous" with your circuit under test. Therefore, you must specify which clock probe you will use for your measurement. In this exercise, you will use the J clock which is accessible through pod 1.

1. Display the State Format Specification menu.

2. Set the J Clock to sample on a negative-going edge.

   a. Touch the field labeled **Clock**.

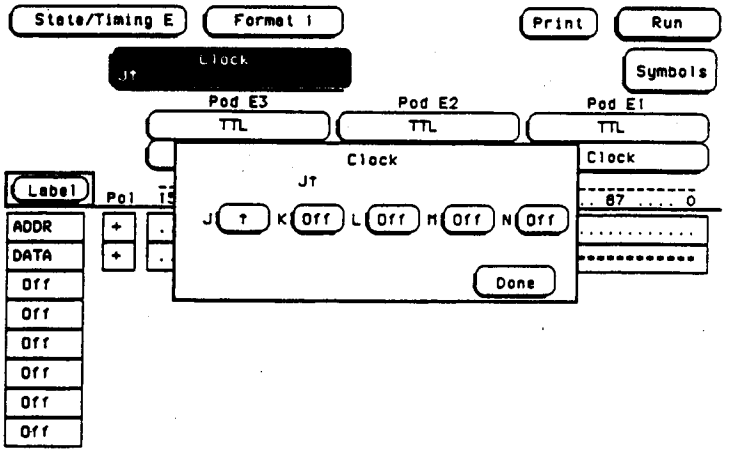


Figure 8-9. Clock Selection

b. In the pop-up, touch the field to the right of J.

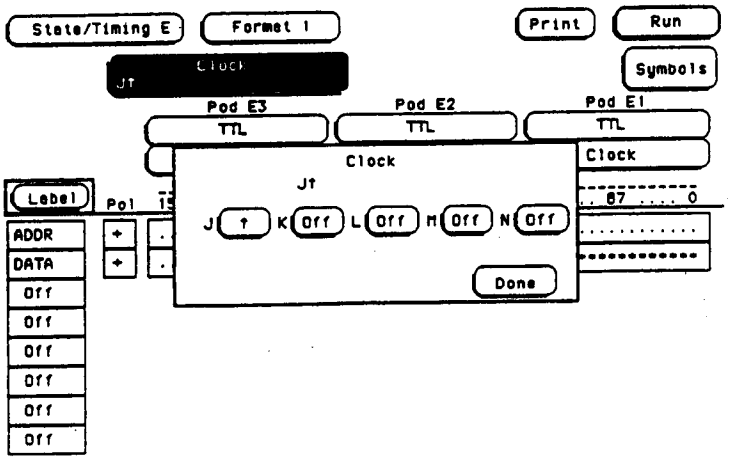


Figure 8-10. J Clock Selection

c. Touch the field with the arrow pointing down to select a negative going edge.

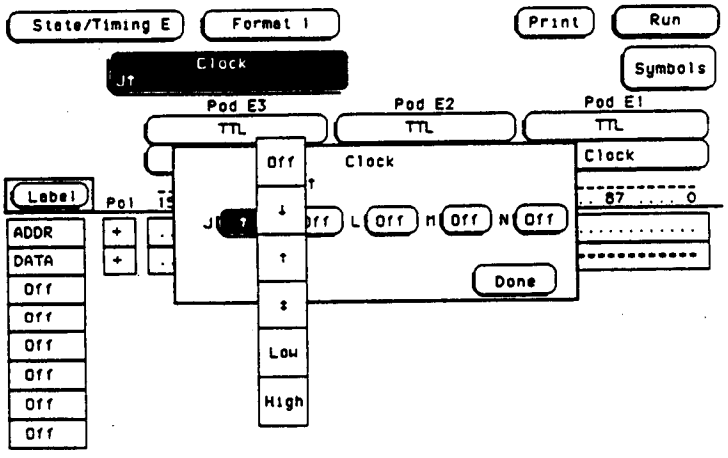


Figure 8-11. Negative-edge Selection

3. Turn off all other clocks (K-N) if any are on by repeating steps a through c using the **Off** option and then touch **Done** to close the pop-up.

The State Format Specification menu should look like that shown below.

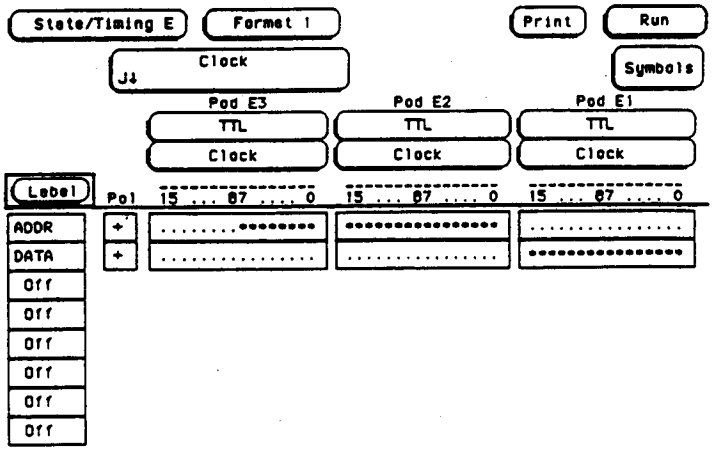


Figure 8-12. State Format Specification Menu

Specifying a Trigger Condition

To capture the data and place the data of interest in the center of the display of the state listing menu, you need to tell the state analyzer when to trigger. Since the first event of interest is address 0000, you need to tell the state analyzer to trigger when it detects address 0000 on the address bus.

1. Display the State Trace Specification menu.

   a. Touch the field second from the left at the top of the screen.

   b. Touch the field labeled **Trace 1**.

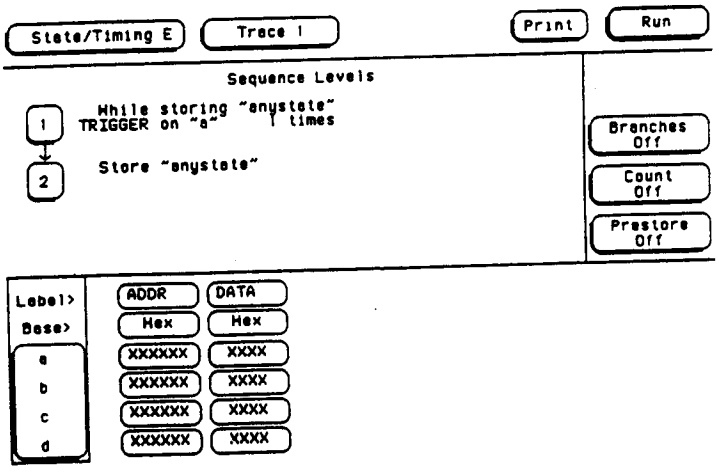


Figure 8-13. State Trace Specification Menu

2. Set the state analyzer so that it triggers on address 0000.

   a. Touch the **1** in the **Sequence Levels** field of the menu.

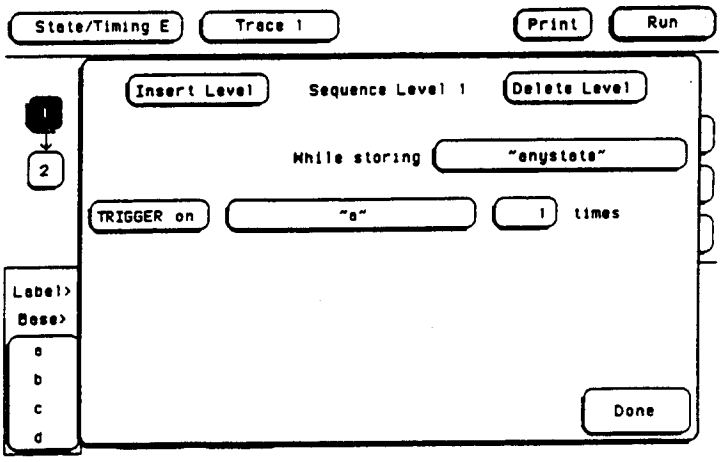


Figure 8-14. Sequence Levels

b. In the pop-up, touch the field to the right of the **TRIGGER on** field. This field may either contain **a** or **anystate**.

Another pop-up appears showing you a list of "TRIGGER on" options. Options **a** through **h** are qualifiers that allow you to assign a pattern for the trigger specification.

c. Touch the field with the "a" option.

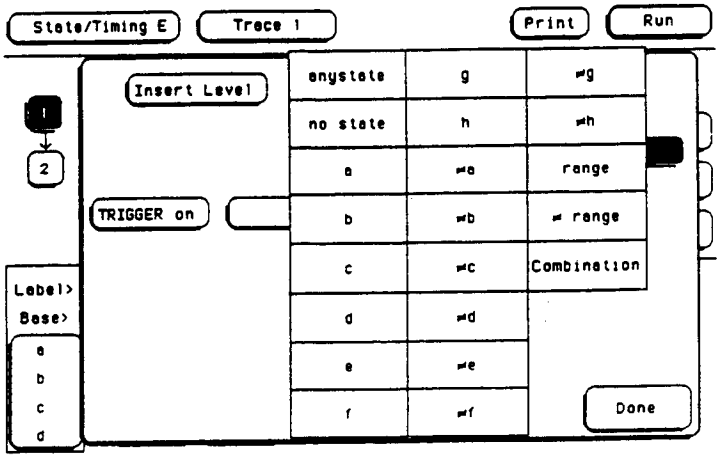


Figure 8-15. Sequence Level Option Selection

d. Touch the field labeled **Done** in the Sequence Levels pop-up.

e. Touch the field to the right of "a" under the label ADDR.

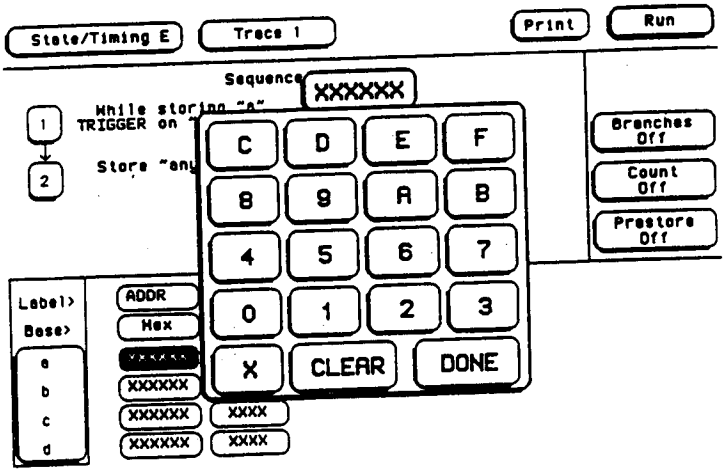


Figure 8-16. Address Pattern Selection Keypad

f. With the pop-up keypad, touch the 0 (zero) key until all zeroes appear in the display space above the keypad. Touch the **Done** field to close pop-up.

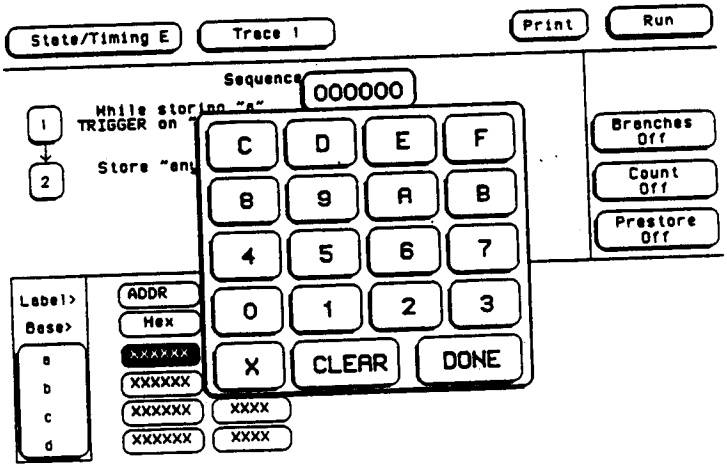


Figure 8-17. Setting the Pattern

Your trigger specification now states: "While storing anystate, trigger on "a" 1 times and then store anystate."

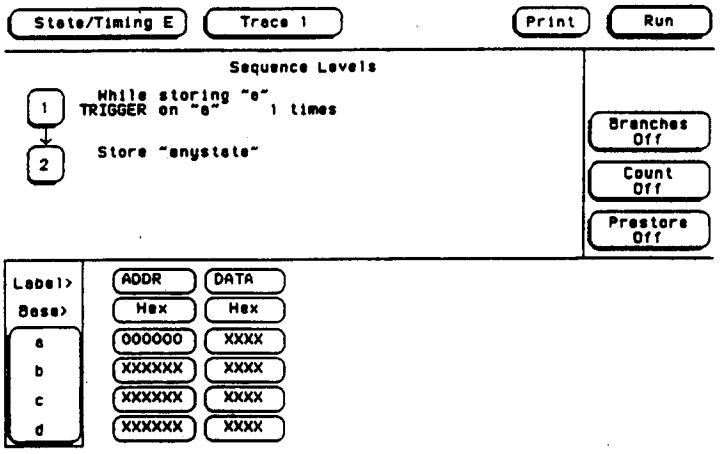


Figure 8-18. State Trace Specification

When the state analyzer is connected to your circuit and is acquiring data, it continuously stores until it sees 0000 on the address bus, at which time it begins to store anystate until the analyzer memory is filled.

Acquiring the Data

To acquire the data, you touch the green field in the upper right-hand corner of the screen labeled **Run**. After touching the **Run** field, don't lift you finger off the screen.

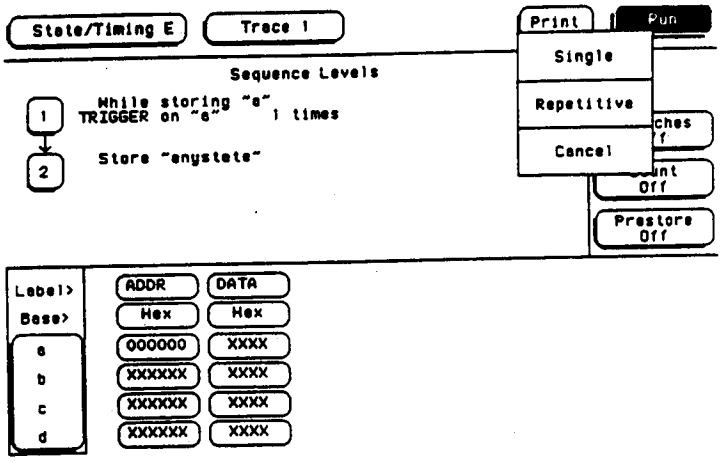


Figure 8-19. Acquiring Data

When you touch the **Run** field a pop-up appears next to it with the options **Single**, **Repetitive**, and **Cancel**. Without lifting your finger from the screen, move it to the field labeled **Single**. **Single** will turn white.

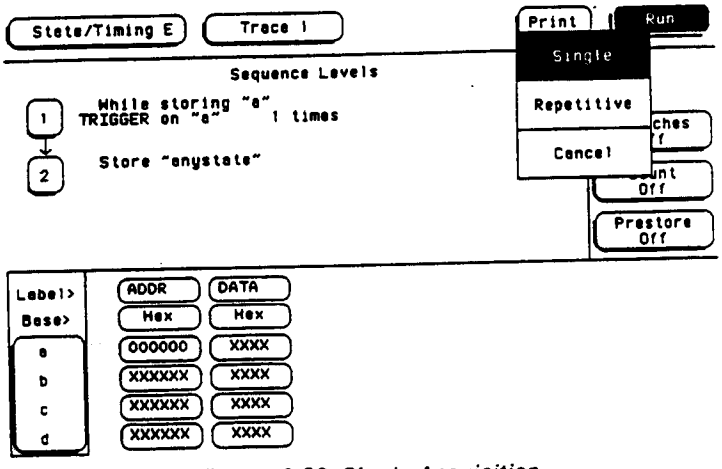


Figure 8-20. Single Acquisition

If you want to go to the state listing menu before taking a measurement, touch the field second from the left at the top of the screen. When the pop-up appears, touch the field labeled Listing 1.

Since you want to capture the data when the microprocessor sends address 0000 on the bus after power-up, you touch the **Run** field to arm the state analyzer and then force a reset of your circuit. When the reset cycle ends, the microprocessor should send address 0000, trigger the state analyzer and switch the display to the state Listing menu.

We'll assume this is what happens in this example, since the odds of the microprocessor not sending address 0000 are very low.

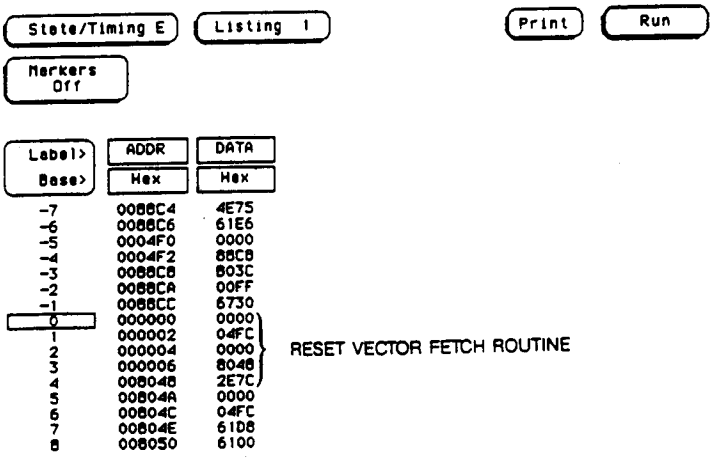


Figure 8-21. State Listing

The State Listing

The state listing displays three columns of numbers as shown:

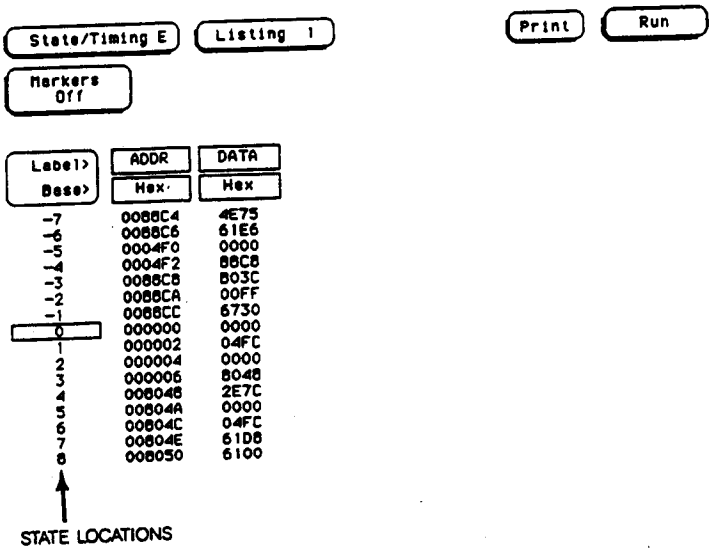


Figure 8-22. State Listing

The first column of numbers are the state line number locations as they relate to the trigger point. The trigger state is on the line 0 in the vertical center of the list area. The negative numbers indicate states occurring before the trigger and the positive numbers indicate the states occurring after the trigger.

The second column of numbers are the states (listed in HEX) the state analzyer sees on the address bus. This column is labeled ADDR.

The third column of numbers are the states (listed in HEX) the state analyzer sees on the data bus. This column is labeled DATA.

Finding the Answer

Your answer is now found in this listing of the states +0000 through +0004.

The 68000 always reads address locations 0, 2, 4, and 6 to find the stack pointer location and memory location for the instruction it fetches after power-up. The 68000 uses two words for each of the locations that it is looking for, a high word and a low word. When the software designer programs the ROM he must put the stack pointer location at address locations 0 and 2. 0 is the high word location and 2 is the low word location. Similarly, the high word of the instruction fetch location must be in address location 4 and the low word in location 6.

Since the software design calls for the reset vector to:

1. Set the stack pointer to be set to 04FC,
2. Read memory address location 8048 for its first instruction fetch,

you are interested in what is on both the address bus and the data bus in states 0 through 3.

You look at the following listing and see that states 0 and 1 do contain address locations 0 and 2 under the ADDR label, indicating the microprocessor did look to the correct locations for the stack pointer data. You also see that the data contained in these ROM locations are 0000 and 04FC, which are correct.

You then look at states 2 and 3. You see that the next two address locations are 4 and 6, which is correct, and the data found at these locations is 0000 and 8048, which is also correct.

So far you have verified that the microprocessor has performed the correct reset vector search. The next thing you must verify is whether the microprocessor addresses the correct location in ROM that it was instructed to address in state 4 and whether the data is correct in this ROM location. From the listing you see that the address in state 4 is 008048, which is correct, but the instruction found in this location is 2E7C, which is not correct. You have found your problem: incorrect data stored in ROM for the microprocessor's first instruction.

+0000 000000 0000 (high word of stack pointer location)
+0001 000002 04FC (low word of stack pointer location)
+0002 000004 0000 (high word of instruction fetch location)
+0003 000006 8048 (low word of instuction fetch location)
+0004 008048 2E7C (first microprocessor instruction)

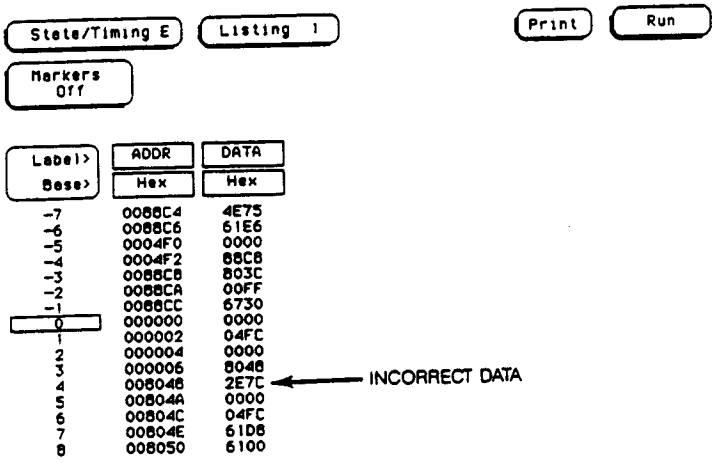


Figure 8-23. State Listing

Summary

You have just learned how to make a simple state measurement with the HP 16510A Logic Analyzer. You have:

- specified a state analyzer
- learned which probes to connect
- assigned pods 1, 2, and 3
- assigned labels
- assigned bits
- specified the J clock
- specified a trigger condition
- acquired the data
- interpreted the State Listing

You have seen how easy it is to use the state analyzer to capture the data on the address and data buses. You can use this same technique to capture and display related data on the microprocessor status, control, and various strobe lines. You are not limited to using this technique on microprocessors. You can use this technique anytime you need to capture data on multiple lines and need to sample the data relative to a system clock.

The next chapter teaches you how to use the logic analyzer as an interactive timing and state analyzer. You will see a simple measurement that shows you both timing waveforms and state listings and how they are correlated.

9 Using the Timing/State Analyzer

Introduction

In this chapter you will learn how to use the timing and state analyzers interactively by setting up the logic analyzer to make a simple measurement. We give you the measurement results as actually measured by the logic analyzer, since you may not have the same circuit available.

The exercise in this chapter is organized differently than the two previous chapters. Since you have already set up both the timing and state analyzers, you should be ready to set them up for this measurement by looking at the menu pictures.

Any new set-ups in this exercise will be explained in task format steps like the previous chapters.

How you use the steps depends on how much you remember from previous chapters. If you can set up each menu by just looking at the menu picture, go right ahead and do so. If you need a reminder of what steps to perform, follow the numbered steps. If you still need more information about "how," use the lettered steps.

Problem Solving with the Timing/ State Analyzer

In this example assume you have designed a microprocessor controlled circuit. You have completed the hardware, and the software designer has completed the software and programmed the ROM. When you turn your circuit on for the first time, your circuit doesn't work properly. You have checked the power supply voltages and the system clock and they are working properly.

Since the circuit has never worked before, you and the software engineer aren't sure if it is a hardware or software problem. The problem now requires some testing to find a solution.

You also notice the circuit fails intermittently. More specifically, it only fails when the microprocessor attempts to address a routine that starts at address 8930.

What Am I Going to Measure?

To see what might be causing the failure, you decide to start where the microprocessor goes to the routine that starts at address 8930.

The first thing you check is whether the microprocessor actually addresses address 8930. The next thing you check is whether the code is correct in all the steps in this routine.

Your measurement, then, requires verification of:

- whether the microprocessor addresses location 8930
- whether all the addresses within the routine are correct
- whether all the data at the addresses in the routine are correct

If the routine is correct, the state listing will display:

```
+0000   008930  B03C
+0001   008932  61FA
+0002   008934  67F8
+0003   008936  B03C
+0004   00892E  61FA
```

How Do I Configure the Logic Analyzer?

In order to make this measurement, you must configure the logic analyzer as a state analyzer because you want to trigger on a specific state (8930). You also want to verify that the addresses and data are correct in the states of this routine.

Configure the logic analyzer so that Analyzer 1 is a state analyzer as shown:

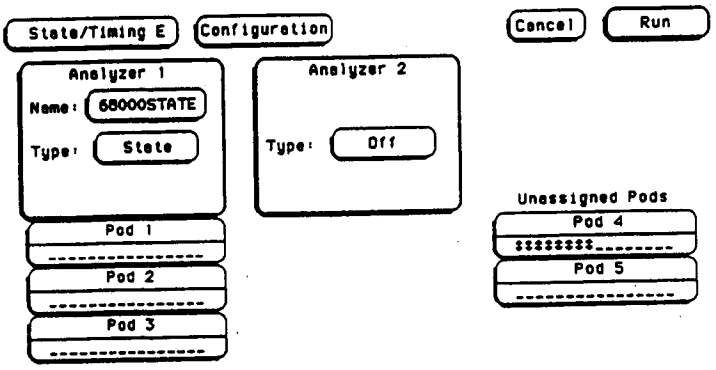


Figure 9-1. State/Timing E Configuration Menu

Configuring the State Analyzer

Now that you have configured the system, you are ready to configure the state analyzer.

Configure the State Format Specification (**Format 1**) as shown:

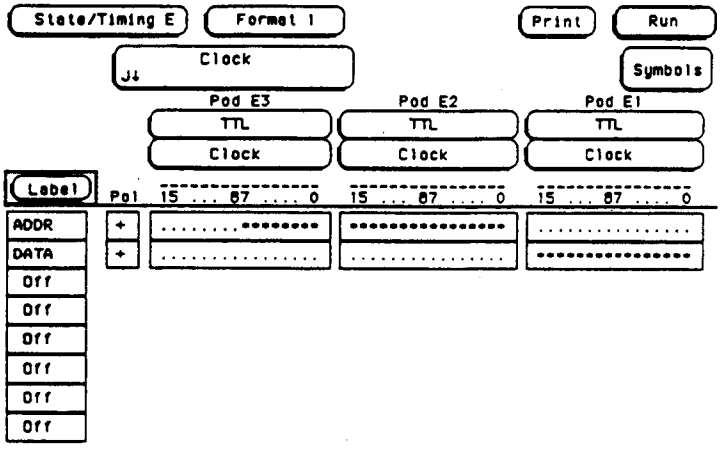


Figure 9-2. State Format Specification Menu

Configure the State Trace Specification (**Trace 1**) as shown:

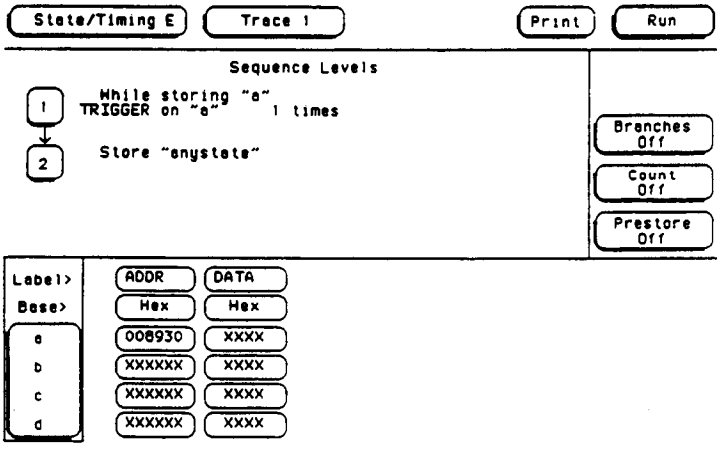


Figure 9-3. State Trace Specification Menu

Connecting the Probes

At this point, if you had a target system with a 68000 microprocessor, you would connect the logic analyzer to your system. Since you have assigned labels ADDR and DATA, you would hook the probes to your system accordingly.

- Pod 1 probes 0 through 15 to the data bus lines D0 through D15
- Pod 2 probes 0 through 15 to the address bus lines A0 through A15
- Pod 3 probes 0 through 7 to the address bus lines A16 through A23
- Pod 1, CLK (J clock) to the address strobe (LAS)

Acquiring the Data

Since you want to capture the data when the microprocessor sends address 8930 on the bus, you press the **Run** field to arm the state analyzer. If the microprocessor sends address 8930, it will trigger the state analyzer and switch the display to the State Listing.

We'll assume this is what happens in this example.

Finding the Problem

You look at this listing to see what the data is in states +0000 through +0004. You know your routine is five states long.

The 68000 does address location 8930 so you know that the routine is addressed. Now you need to compare the state listing with the following correct addresses and data:

```
+0000  008930  B03C
+0001  008932  61FA
+0002  008934  67F8
+0003  008936  B03C
+0004  00892E  61FA
```

As you compare the state listing (shown below), you notice the data at address 8932 is incorrect. Now you need to find out why.

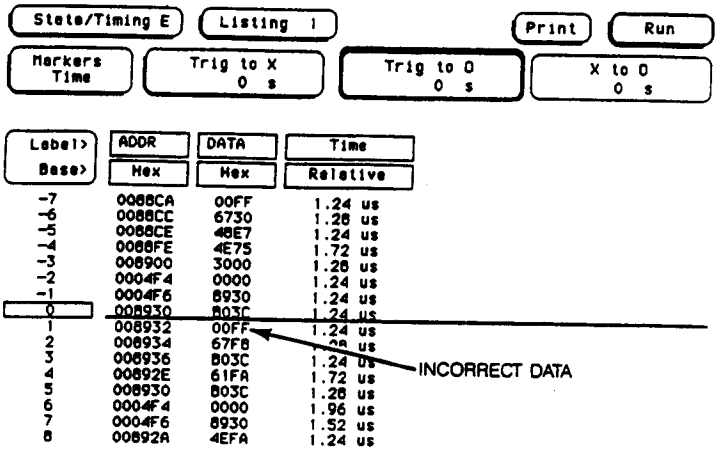


Figure 9-4. Incorrect Data

Your first assumption is that incorrect data is stored in this memory location. Assume this routine is in ROM since it is part of the operating system for your circuit. Since the ROM is programmed by the software designer, you have the software designer verify the data at address 8932 is correct. The software designer tells you that the data is correct. Now what do you do?

Now it's time to look at the hardware to see if it is causing incorrect data when the microprocessor reads this memory address. You decide you want to see what is happening on the address and data buses during this routine in the time domain.

In order to see the time domain, you need the timing analyzer.

What Additional Measurements Must I Make?

Since the problem exists during the routine that starts at address 8930, you decide you want to see the timing waveforms on the address and data bus when the routine is running. You also want to see the control signals that control the read cycle. You will then compare the waveforms with the timing diagrams in the 68000 data book.

Your measurement, then, requires verification of:

- correct timing of the control signals
- stable addresses and data during the memory read

The control signals you must check are:

- system clock
- address strobe (AS)
- lower and upper data strobes (LDS and UDS)
- data transfer acknowledge (DTACK)
- read/write (R/W)

How Do I Re-configure the Logic Analyzer?

In order to make this measurement, you must re-configure the logic analyzer so Analyzer 2 is a timing analyzer. You leave Analyzer 1 as a state analyzer since you will use the state analyzer to trigger on address 8930.

Configure the logic analyzer so Analyzer 2 is a timing analyzer as shown:

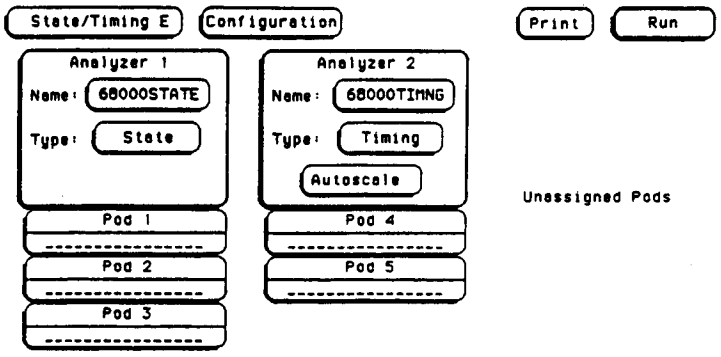


Figure 9-5. State/Timing E Configuration Menu

Connecting the Timing Analyzer Probes

At this point you would connect the probes of pods 4 and 5 as follows:

- Pod 4 bit 0 to address strobe (AS)
- Pod 4 bit 1 to the system clock
- Pod 4 bit 2 to low data strobe (LDS)
- Pod 4 bit 3 to upper data strobe (UDS)
- Pod 4 bit 4 to the read/write (R/W)
- Pod 4 bit 5 to data transfer acknowledge (DTACK)
- Pod 5 bits 0 through 7 to address lines A0 through A7
- Pod 5 bits 8 through 15 to data lines D0 through D7

Configuring the Timing Analyzer

Now that you have configured the system, you are ready to configure the timing analyzer.

Configure the Timing Format Specification (**Format 2**) as shown:

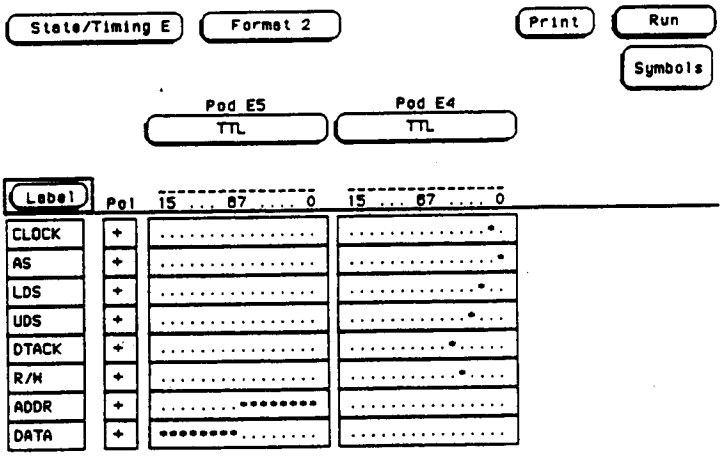


Figure 9-6. Timing Format Specification Menu

Configure the timing Trace specification (**Trace 2**) as shown:

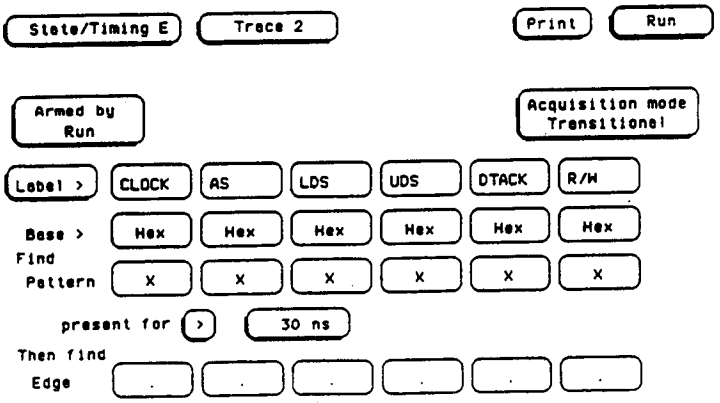


Figure 9-7. Timing Trace Specification Menu

Setting the Timing Analyzer Trigger

Your timing measurement requires the timing analyzer to display the timing waveforms present on the buses when the routine is running. Since you triggered the state analyzer on address 8930, you want to trigger the timing analyzer so the timing waveforms can be time correlated with the state listing.

To set up the logic analyzer so that the state analyzer triggers the timing analyzer, perform these steps:

1. Display the Timing Trace Specification menu (**Trace 2**).
2. Touch the field labeled **Armed by Run**.
3. In the pop-up, touch the field labeled **68000STATE**.

Your timing Trace specification should match the menu shown:

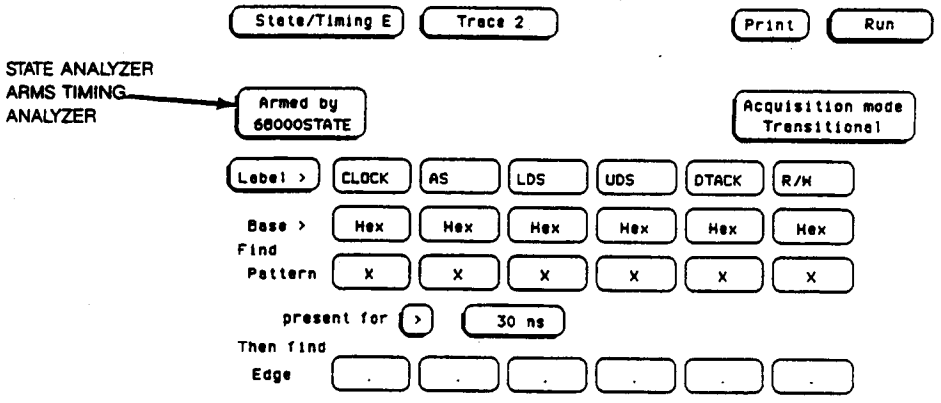


Figure 9-8. Armed by 68000STATE

Time Correlating the Data

In order to time correlate the data, the logic analyzer must store the timing relationships between states. Since the timing analyzer samples asynchronously and the state analyzer samples synchronously, the logic analyzer must use the stored timing relationship of the data to reconstruct a time correlated display.

To set up the logic analyzer to keep track of these timing relationships, turn on a counter in the State Trace Specification menu. The following steps show you how:

1. Display the State Trace Specification menu (**Trace 1**).

2. Touch the field labeled **Count Off**.

3. In the pop-up, touch the field labeled **Time**.

The counter will now be able to keep track of time for the time correlation.

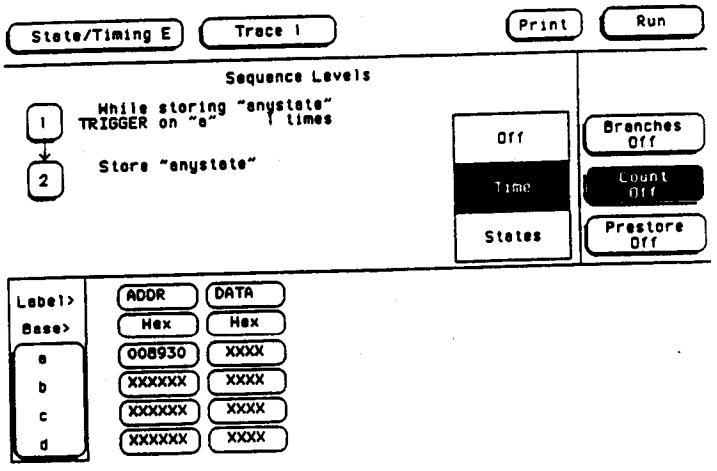


Figure 9-9. Count Time

The Timing Waveform Menu

After pods 4 and 5 are connected, you can re-acquire the data. However, first assign the labels in the Timing Waveform menu.

Displaying the Waveforms

Display the Timing Waveform menu. Touch the long blue field on the left side of the screen. The pop-up should look like that below:

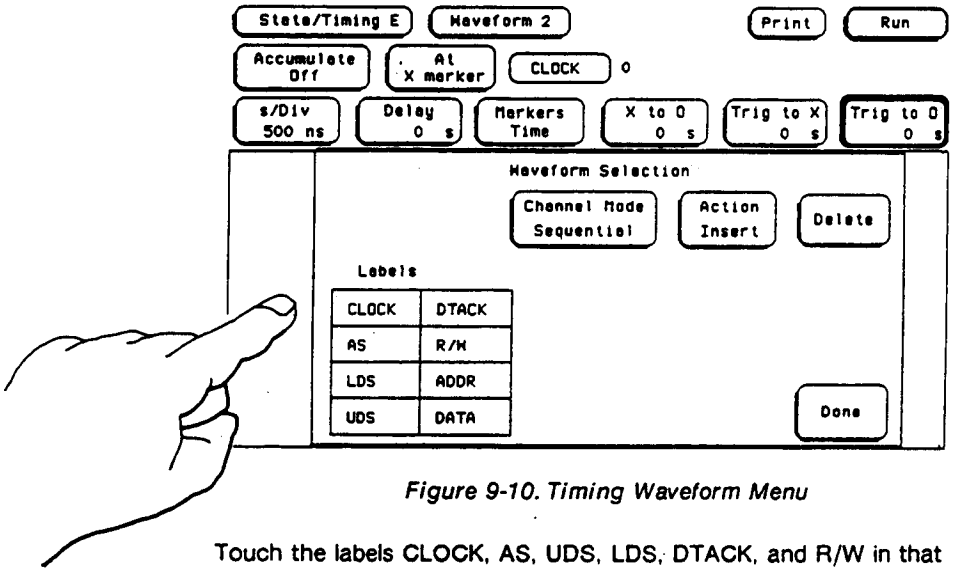


Figure 9-10. Timing Waveform Menu

Touch the labels CLOCK, AS, UDS, LDS, DTACK, and R/W in that order. They will appear in the blue label area.

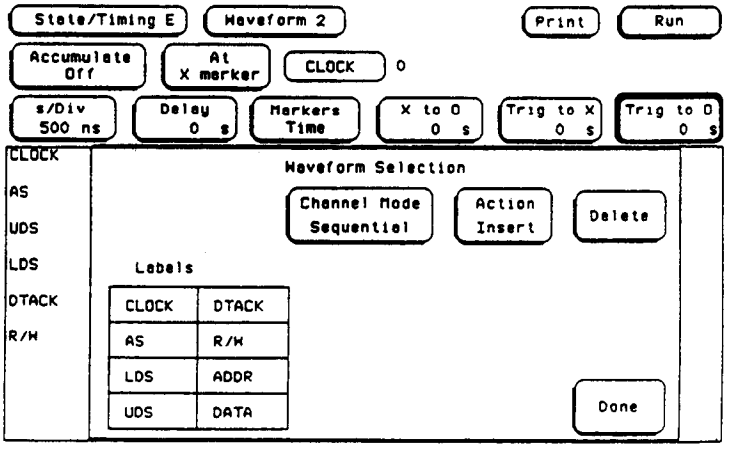


Figure 9-11. Waveform Selection Menu Labels

This is not the order we want them in. We want LDS before UDS. To correct this, follow these steps:

1. Use the knob to place the cursor on the label **LDS** in the long blue label field.

2. Touch the field labeled **Delete**. This erases LDS.

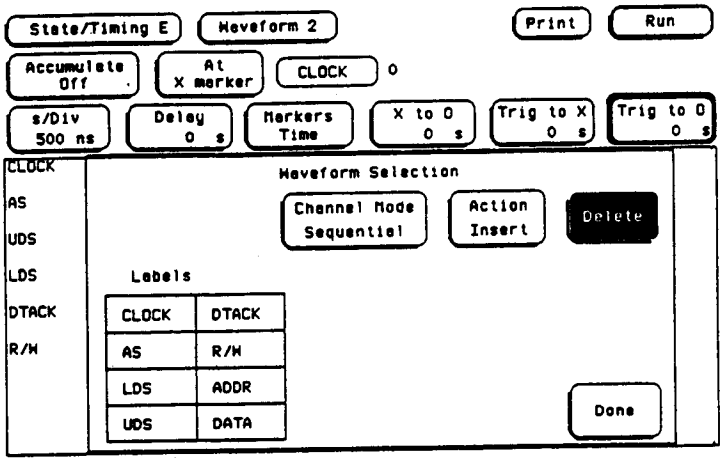


Figure 9-12. Delete Label

3. Use the knob to place the cursor over the label AS. Touch the **LDS** field under Labels in the pop-up.

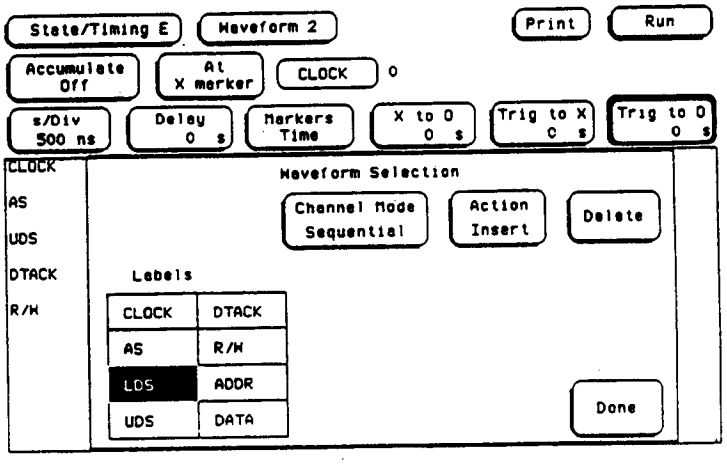


Figure 9-13. Replace Label

LDS appears in the blue label area in the correct position.

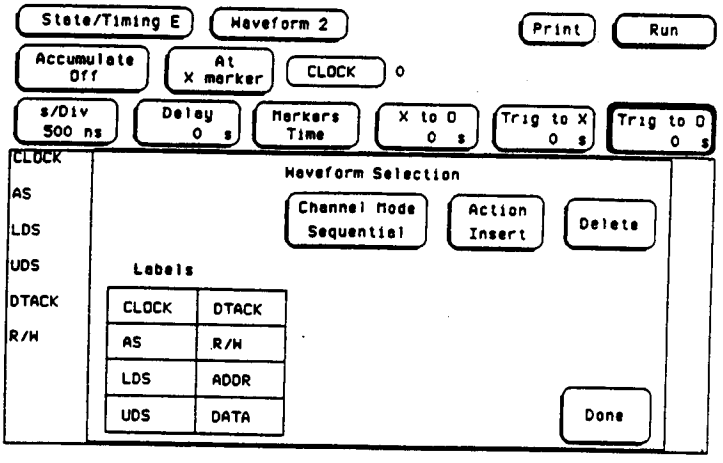


Figure 9-14. Labels in Correct Position

Now we want to put ADDR and DATA in the long blue label area.

Position the cursor on **R/W** in the long blue label field. Touch **ADDR** under Labels in the pop-up. Since ADDR has eight bits assigned to it, eight labels appear in the label field, one for each bit, as shown.

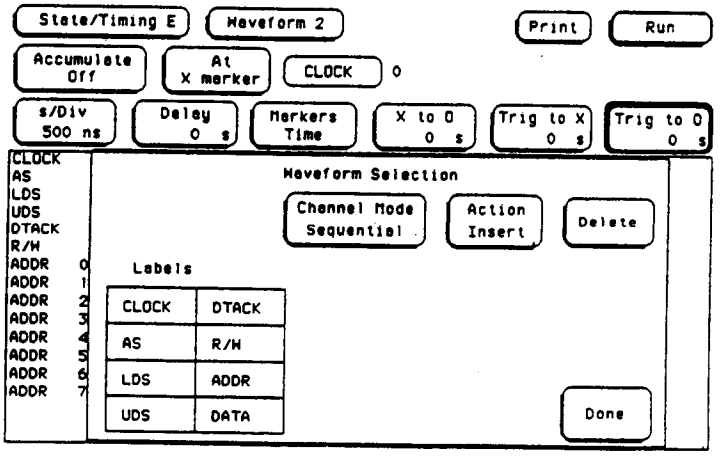


Figure 9-15. Timing Waveform Menu with Labels

This also occurs for DATA, as shown:

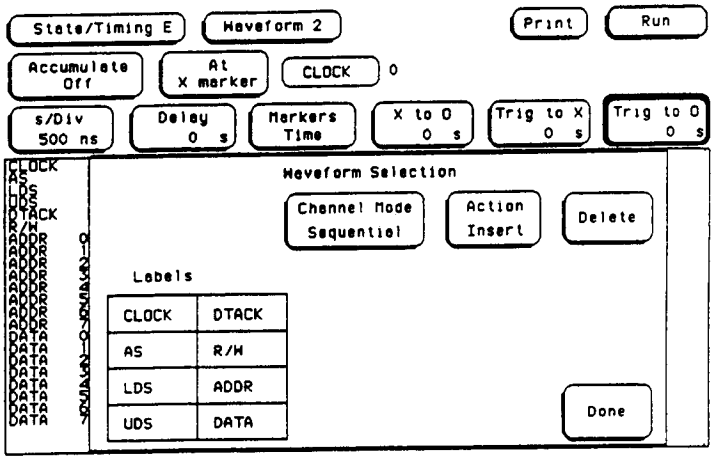


Figure 9-16. Individual Data Labels

If you want to see the waveforms of each bit, you would leave the display as it is. However, this makes the waveform display very crowded. An easy solution is overlapping the waveforms.

Overlapping Timing Waveforms

A convenient method of displaying the waveforms of all the bits in ADDR and DATA is to overlap them. To overlap the bits for ADDR and those for DATA, follow these steps.

1. Delete all the ADDR and DATA bit labels that were put in the label field in the last section.

2. Touch the filed labeled **Channel Mode Sequential.**

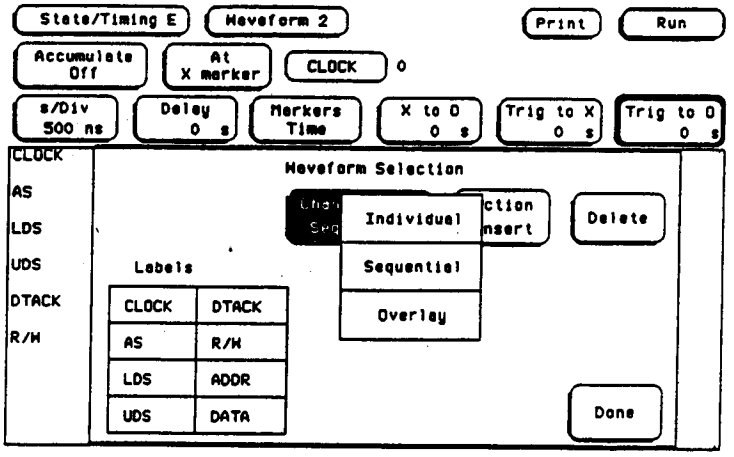


Figure 9-17. Channel Mode Sequential Menu

3. In the new pop-up, touch the field labeled **Overlay.**

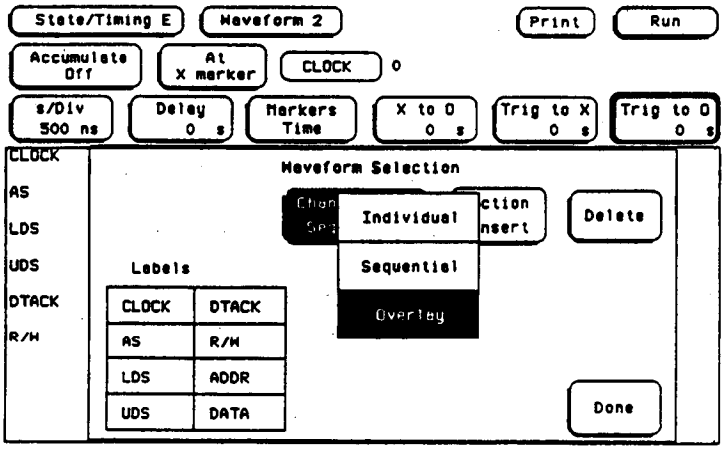


Figure 9-18. Overlay Selection

4. Touch the **ADDR** label field under Labels.

5. Touch the **DATA** label field under Labels. The screen should look like that shown below.

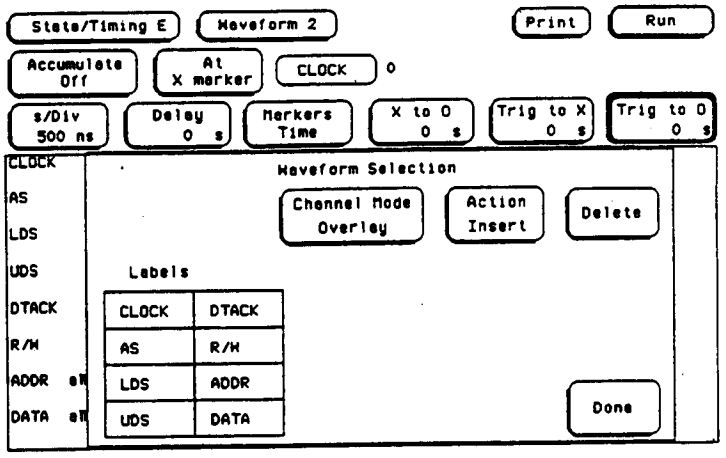


Figure 9-19. Overlapped Waveforms

In the long blue label field ADDR and DATA have "all" next to them to show that the bits are overlapped. Touch the **Done** field to close the pop-up.

Re-acquiring the Data

Now you are ready to acquire the data. Touch **Run**. The logic analyzer will display the timing waveforms, unless you switched to one of the state analyzer menus, in which case the state listing will be displayed. Regardless of which menu is displayed, change the display to the Mixed Mode Display.

Finding the Answer

As you look at the overlapping waveforms, you notice there are transitions on the data lines during the read, indicating the data is unstable, which is the probable cause of the problem you've been looking for.

You have found what is causing the problem in this routine. Additional troubleshooting of the hardware will lead you to the actual cause.

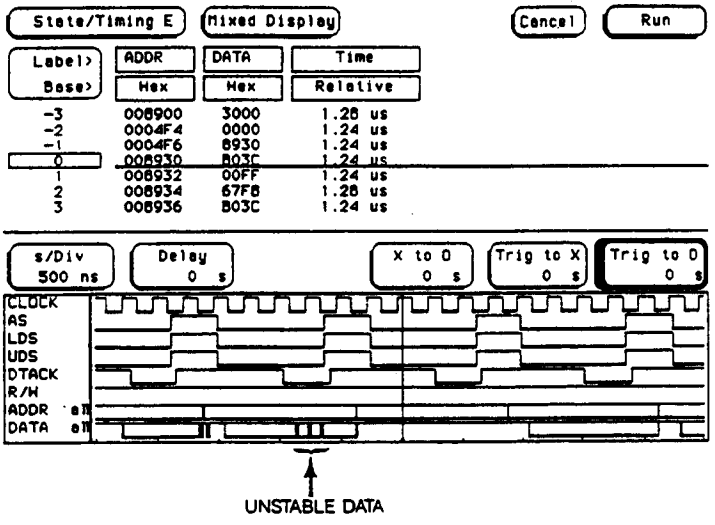


Figure 9-20. Mixed Mode Display with Unstable Data

Summary

You have just learned how to to use the timing and state analyzers interactively to find a problem that first appeared to be a software problem, but actually is a hardware problem.

You have learned to:

- trigger one analyzer with the other
- time correlate measurement data
- interpret the Mixed mode display
- overlap timing waveforms

10 Using a Printer

Setting Printer Configuration

All printer parameters are set in the **System Configuration** menu. If you have just connected your printer and are unsure of how to set the configuration, refer to the *HP 16500A Reference Manual* chapter entitled "Connecting a Printer."

The HP 16500A supports HP-IB and selected RS-232C printers.

All the pictures in this manual were taken from an HP 16500A with one HP 16510A logic analyzer card. If the screens on your instrument differ from the pictures in this manual, it simply means that you have a different card configuration. All other functions will work the same except where noted.

Printing Options

All logic analyzer menus include a **Print** field in the upper right of the screen. If you are in the **Format** menu and touch the **Print** field, a pop-up like the one shown below appears.

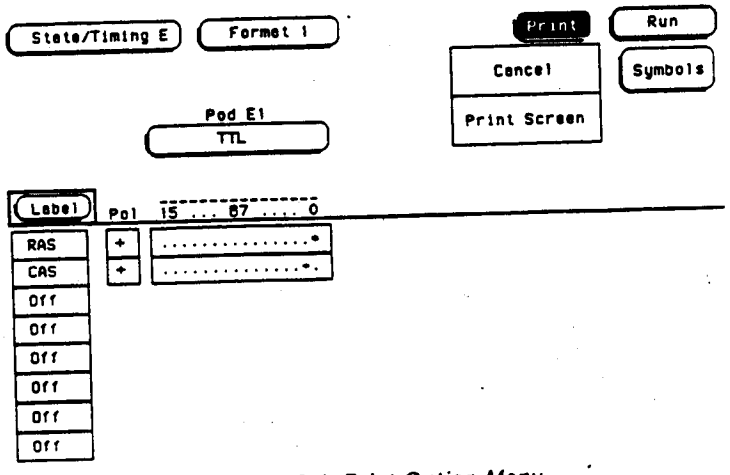


Figure 10-1. Print Option Menu

There are two fields in the pop-up, **Cancel** and **Print Screen**.

If you are in the **State Listing**, a slightly different pop-up will appear, like the one shown in figure 10-2.

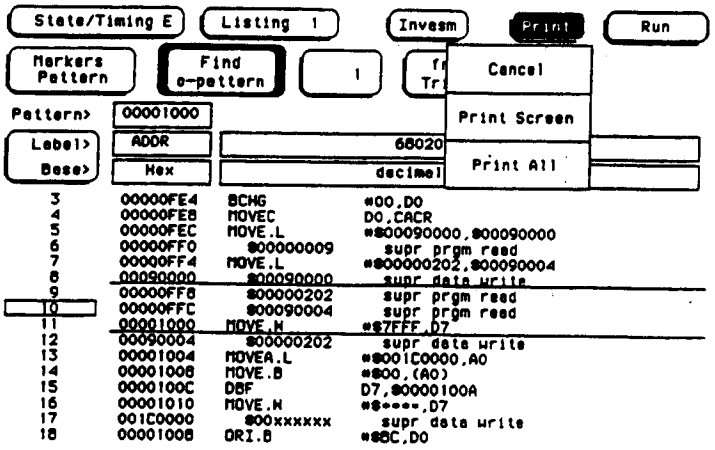


Figure 10-2. Print Option in Listing Menu

The pop-up contains three fields, **Cancel**, **Print Screen**, and **Print All**.

Printing On-Screen Data

If you want a hardcopy record of the screen, touch the **Print** field and then the **Print Screen** field from the pop-up. This will send a copy of the screen to the printer in graphics mode.

If you want to print part of a menu in graphics mode that is off screen, you must roll the screen vertically or horizontally to place the part on screen. When the desired part is on screen, touch the **Print Screen** field.

Printing Entire State Listing

If you need a hardcopy record of an entire state listing, touch the **Print** field and then the **Print All** field from the pop-up. The **Print All** field causes all the list and label data to be sent to the printer, but not in graphics mode like the **Print Screen** field. The data is sent in text mode to speed printing of long data lists.

11 Microprocessor Specific Measurements

Introduction

This chapter contains information about the optional accessories available for microprocessor specific measurements. In depth measurement descriptions are in the operating notes that come with each of these accessories. The accessories you will be introduced to in this chapter are the preprocessor modules and the HP 10269C General Purpose Probe Interface.

Microprocessor Measurements

A preprocessor module for your microprocessor enables you to quickly and easily connect the logic analyzer to your microprocessor under test. Most of the preprocessor modules require the HP 10269C General Purpose Probe Interface. The preprocessor descriptions in the following sections indicate which preprocessors require it.

Included with each preprocessor module is a 3.5-inch disc which contains a configuration file and an inverse assembler file. When you load the configuration file, it configures the logic analyzer for making state measurements on the microprocessor for which the preprocessor is designed. It also loads in the inverse assembler file.

The inverse assembler file is a software routine that will display captured information in a specific microprocessor's mnemonics. The DATA field in the state listing is replaced with an inverse assembly field (see Figure 11-1). The inverse assembler software is designed to provide a display that closely resembles the original assembly language listing of the microprocessor's software. It also identifies the microprocessor bus cycles captured, such as Memory Read, Interrupt Acknowledge, or I/O write.

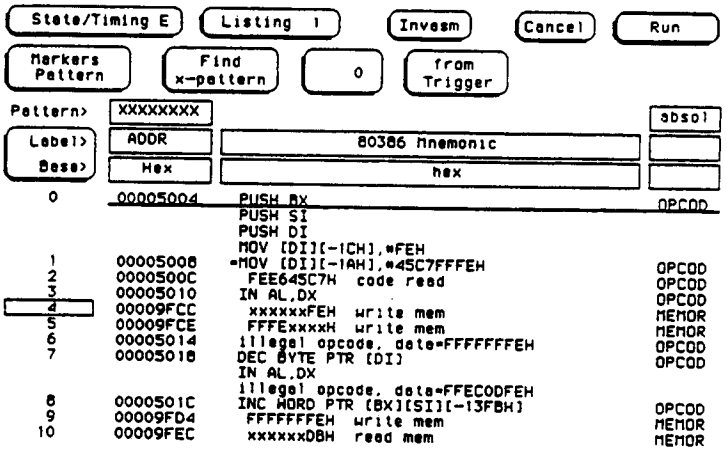


Figure 11-1. State Listing with Mnemonics

Microprocessors Supported by Preprocessors

This section lists the microprocessors that are supported by Hewlett-Packard preprocessors. Most of the preprocessors require the HP 10269C General Purpose Probe Interface. The HP 10269C accepts the specific preprocessor PC board and connects it to five connectors on the general purpose interface to which the logic analyzer probe cables connect.

Note

This chapter lists the preprocessors available at the time of printing. However, new preprocessors may become available as new microprocessors are introduced. Check with the nearest Hewlett-Packard office periodically for availability of new preprocessors.

Z80

CPU Package:	40-pin DIP
Accessories Required:	HP 10300B Preprocessor HP 10269C General Purpose Probe Interface
Maximum Clock Speed:	10 MHz clock input
Signal Line Loading:	Maximum of one 74LS TTL load + 35 pF on any line
Microprocessor Cycles Identified:	Memory read/write I/O read/write Opcode fetch Interrupt acknowledge RAM refresh cycles
Maximum Power Required:	0.3 A at + 5 Vdc, supplied by logic analyzer
Number of Probes Used:	Two 16-channel probes

NSC 800	CPU Package:	40-pin DIP
	Accessories Required:	HP 10304B Preprocessor HP 10269C General Purpose Probe Interface
	Maximum Clock Speed:	4 MHz clock input
	Signal Line Loading:	Maximum of one HCMOS load + 35 pF on any line
	Microprocessor Cycles Identified:	Memory read/write I/O read/write Opcode fetch Interrupt acknowledge RAM refresh cycles DMA cycles
	Maximum Power Required:	0.1A at + 5 Vdc, supplied by logic analyzer
	Number of Probes Used:	Two 16-channel probes

8085	CPU Package:	40-pin DIP
	Accessories Required:	HP 10304B Preprocessor HP 10269C General Purpose Probe Interface
	Maximum Clock Speed:	6 MHz clock output (12 MHz clock input)
	Signal Line Loading:	Maximum of one 74LS TTL load + 35 pF on any line
	Microprocessor Cycle Identified:	Memory read/write I/O read/write Opcode fetch Interrupt acknowledge
	Maximum Power Required:	0.8 A at + 5 Vdc, supplied by logic analyzer
	Number of Probes Used:	Two 16-channel probes

8086 or 8088	CPU Package:	40-pin DIP
	Accessories Required:	HP 10305B Preprocessor HP 10269C General Purpose Probe Interface
	Maximum Clock Speed:	10 MHz clock input (at CLK)
	Signal Line Loading:	Maximum of two 74ALS TTL loads + 40 pF on any line
	Microprocessor Cycles Identified:	Memory read/write I/O read/write Code fetch Interrupt acknowledge Halt acknowledge Transfer to 8087 or 8089 co-processors
	Additional Capabilities:	The 8086 or 8088 can be operating in Minimum or Maximum modes. The logic analyzer can capture all bus cycles (including prefetches) or can capture only executed instructions. To capture only executed instructions, the 8086 the 8086 or 8088 must be operating in the Maximum Mode.
	Maximum Power Required:	1.0 A at + 5 Vdc, supplied by the logic analyzer
	Number of Probes Used:	Three 16-channel probes

80186 or 80188	CPU Package:	68-contact LCC
	Accessories Required:	HP 10306B Preprocessor HP 10269C General Purpose Probe Interface
	Maximum Clock Speed:	8 MHz clock output (16 MHz clock input)
	Signal Line Loading:	Maximum of two 74ALS TTL loads + 40 pF on any line
	Microprocessor Cycles Identified:	Memory read/write (DMA and non-DMA) I/O read/write (DMA and non-DMA) Code fetch Interrupt acknowledge Halt acknowledge Transfer to 8087, 8089, or 82586 co-processors
	Additional Capabilities:	The 80186 or 80188 can be operating in Normal or Queue Status modes. The logic analyzer can capture all bus cycles (including prefetches) or can capture only executed instructions.
	Maximum Power Required:	0.66 A at + 5 Vdc, supplied by logic analyzer. 80186/188 operating current +0.15 A from system under test.
	Number of Probes Used:	Four 16-channel probes

80286	CPU Package:	68-contact LCC or 68-pin PGA
	Accessories Required:	HP 10312B Preprocessor HP 10269C General Purpose Probe Interface
	Maximum Clock Speed:	10 MHz clock output (20 MHz clock input)
	Signal Line Loading:	Maximum of two 74ALS TTL loads + 40 pF on any line
	Microprocessor Cycles Identified:	Memory read/write I/O read/write Code fetch Interrupt acknowledge Halt Hold acknowledge Lock Transfer to 80287 co-processor
	Additional Capabilities:	The logic analyzer captures all bus cycles, including prefetches
	Maximum Power Required:	0.66 A at +5 Vdc, supplied by logic analyzer. 80286 operating current from system under test.
	Number of Probes Used:	Three 16-channel probes

80386	CPU Package:	132-pin PGA
	Accessories Required:	HP 10314B Preprocessor HP 10269C General Purpose Probe Interface
	Maximum Clock Speed:	20 MHz clock output (40 MHz clock input)
	Signal Line Loading:	Maximum of two 74ALS TTL loads + 80 pF on any line
	Microprocessor Cycles Identified: Memory read/write	Memory read/write I/O read/write Code fetch Interrupt acknowledge, type 0-255 Halt Shutdown Transfer to 8087, 80287, or 80387 co-processors
	Additional Capabilities:	The logic analyzer captures all bus cycles, including prefetches
	Maximum Power Required:	1.0 A at +5 Vdc, supplied by logic analyzer
	Number of Probes Used:	Five 16-channel probes

6800 or 6802	CPU Package:	40-pin DIP
	Accessories Required:	HP 10307B Preprocessor HP 10269C General Purpose Probe Interface
	Maximum Clock Speed:	2 MHz clock input
	Signal Line Loading:	Maximum of 1 74LS TTL load + 35 pF on any line
	Microprocessor Cycle Identified:	Memory read/write DMA read/write Opcode fetch/operand Subroutine enter/exit System stack push/pull Halt Interrupt acknowledge Interrupt or reset vector
	Maximum Power Required:	0.8A at +5 Vdc, supplied by logic analyzer
	Number of Probes Used:	Two 16-channel probes

6809 or 6809E	CPU Package:	40-pin DIP
	Accessories Required:	HP 10308B Preprocessor HP 10269C General Purpose Probe Interface
	Maximum Clock Speed:	2 MHz clock input
	Signal Line Loading:	Maximum of one 74ALS TTL load + 35 pF on any line
	Microprocessor Cycles Identified:	Memory read/write DMA read/write Opcode fetch/operand Vector fetch Halt Interrupt
	Additional Capabilities:	The preprocessor can be adapted to 6809/09E systems that use a Memory Management Unit (MMU). This adaptation allows the capture of all address lines on a physical address bus up to 24 bits wide.
	Maximum Power Required:	1.0 A at +5 Vdc, supplied by logic analyzer
	Number of Probes Used:	Two 16-channel probes

68008	CPU Package:	40-pin DIP
	Accessories Required:	HP 10310B Preprocessor HP 10269C General Purpose Probe Interface
	Maximum Clock Speed:	10 MHz clock input
	Signal Line Loading:	Maximum of one 74S TTL load + one 74F TTL load + 35 pF on any line
	Microprocessor Cycles Identified:	User data read/write User program read Supervisor read/write Supervisor program read Interrupt acknowledge Bus grant 6800 cycle
	Additional Capabilities:	The logic analyzer captures all bus cycles, including prefetches
	Maximum Power Required:	0.4 A at +5 Vdc, supplied by logic analyzer
	Number of Probes Used:	Three 16-channel probes

68000 and 68010 (64-pin DIP)	CPU Package:	64-pin DIP
	Accessories Required:	HP 10311B Preprocessor HP 10269C General Purpose Probe Interface
	Maximum Clock Speed:	12.5 MHz clock input
	Signal Line Loading:	Maximum of one 74S TTL load + one 74F TTL load + 35 pF on any line
	Microprocessor Cycles Identified:	User data read/write User program read Supervisor read/write Supervisor program read Interrupt acknowledge Bus Grant 6800 cycle
	Additional Capabilities:	The logic analyzer captures all bus cycles, including prefetches
	Maximum Power Required:	0.4 A at + 5 Vdc, supplied by the logic analyzer
	Number of Probes Used:	Three 16-channel probes

68000 and 68010 (68-pin PGA)	CPU Package:	68-pin PGA
	Accessories Required:	HP 10311G Preprocessor
	Maximum Clock Speed:	12.5 MHz clock input
	Signal Line Loading:	100 KΩ + 10 pF on any line
	Microprocessor Cycles Identified:	User data read/write User program read Supervisor read/write Supervisor program read Interrput acknowledge Bus Grant 6800 cycle
	Additional Capabilities:	The logic analyzer captures all bus cycles, including prefetches.
	Maximum Power Required:	None
	Number of Probes Used:	Three 16-channel probes

68020	CPU Package:	114-pin PGA
	Accessories Required:	HP 10313G
	Maximum Clock Speed:	25 MHz clock input
	Signal Line Loading:	100 KΩ + 10 pF on any line
	Microprocessor Cycles Identified:	User data read/write User program read Supervisor read/write Supervisor program read Bus Grant CPU space accesses including: Breakpoint acknowledge Access level control Coprocessor commumication Interrupt acknowledge
	Additional Capabilities:	The logic analyzer captures all bus cycles, including prefetches. The 68020 microprocessor must be operating with the internal cache memory disabled for the logic analyzer to provide inverse assembly.
	Maximum Power Required:	None
	Number of Probes Used:	Five 16-channel probes

Loading Inverse Assembler Files

You load the inverse assembler file by loading the appropriate configuration file. Loading the configuration file automatically loads the inverse assembler file.

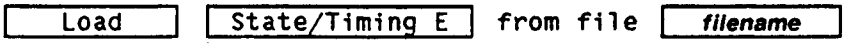
Selecting the Correct File

Most inverse assembler discs contain more than one file. Each disc usually contains an inverse assembler file for use with the HP 10269C and preprocessor as well as a file for general purpose probing. Each inverse assembler filename has a suffix which indicates whether it is for the HP 10269C and preprocessor or general purpose probing. For example, filename C68000_I indicates a 68000 inverse assembler file for use with the HP 10269C and the 68000 preprocessor. Filename C68000_P is for general purpose probing. Specific file descriptions and recommended usage is contained in each preprocessor operating note.

Loading the Desired File

To load the inverse assembler file you want, insert the 3.5-inch disc you received with your preprocessor in the disc drive. Select **System** in the upper left field. Touch **Front Disc** or **Rear Disc**, depending which drive the disc is in, in the field second from the left at the top of the display. The logic analyzer will read the disc and display the disc directory.

Configure the second row of fields as follows:



Touch **Execute** to load the selected file.

Connecting the Logic Analyzer Probes

The specific preprocessor and inverse assembler you are using determines how you connect the logic analyzer probes. Since the inverse assembler files configure the **State/Timing Configuration**, State **Format** Specification, and State **Trace** Specification menus, you must connect the logic analyzer probe cables accordingly so that the acquired data is properly grouped for inverse assembly. Refer to the specific inverse assembler operating note for the proper connections.

How to Display Inverse Assembled Data

The specific preprocessor and inverse assembler you are using determines how the inverse assembled data is displayed. When you touch RUN, the logic analyzer acquires data and displays the State **Listing** menu.

The State **Listing** menu will display as much information about the captured data as possible. For some microprocessors, the display will show a completely disassembled state listing.

Some of the preprocessors and/or the microprocessors under test do not provide enough status information to disassemble the data correctly. In this case, you will need to specify additional information (i.e. tell the logic analyzer what state contains the first word of an opcode fetch). When this is necessary an additional field (**Invasm**) will appear in the top center of the state listing menu (see figure 11-2). This field allows you to point to the first state of an Op Code fetch.

For complete details refer to the Operating Note for the specific preprocessor.

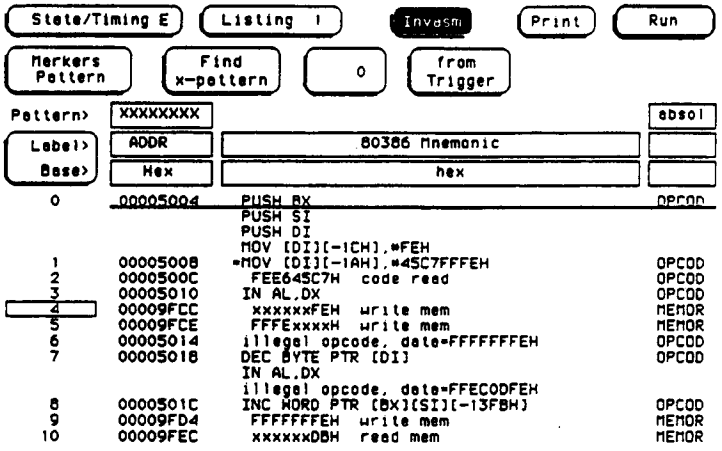


Figure 11-2. Inverse Assemble Field

A Installing New Logic Analyzer Boards into the Mainframe

Introduction

This appendix explains, how to initially inspect the HP 16510A State/Timing Module, how to prepare it for use, storage and shipment. Also included are procedures for module installation.

Initial Inspection

Inspect the shipping container for damage. If the shipping container or cushioning material is damaged, it should be kept until the contents of the shipment have been checked for completeness and the module has been checked mechanically and electrically. The contents of the shipment should be as listed in the "ACCESSORIES SUPPLIES" paragraph located in Chapter 1.

If the contents of the container are incomplete, there is mechanical damage or defect, or the instrument does not pass the performance tests, notify the nearest Hewlett-Packard office. Procedures for checking electrical performance are in Section III of the *HP 16510A Service Manual.*

If the shipping container is damaged, or the cushioning material shows signs of stress, notify the carrier as well as the Hewlett-Packard office. Keep the shipping material for the carrier's inspection. The Hewlett-Packard office will arrange for repair or replacement at Hewlett-Packard's option without waiting for claim settlement.

Power Requirements

All power supplies required for operating the HP 16510A State/Timing Module are supplied to the module through the backplane connector of the HP 16500A Logic Analysis System mainframe.

Probe Cable Installation

The HP 16510A State/Timing Module comes with probe cables installed by the factory. If a cable is to be switched or replaced, refer to "PROBE CABLE REPLACEMENT" in Section VI of the *HP 16510A Service Manual.*

Installation

CAUTION

Do not install, remove or replace the module in the instrument unless the instrument power is turned off.

The HP 16510A State/Timing Module will take up one slot in the card cage. For every additional HP 16510A State/Timing Module you install, you will need an additional slot. They may be installed in any slot and in any order. Procedures for installing the logic analyzer module cards are shown in the step-by-step procedure in the following paragraphs.

Module Installation

The following procedure is for the installation of the HP 16510A Logic Analyzer Module.

CAUTION

The effects of ELECTROSTATIC DISCHARGE can damage electronic components. Use grounded wriststraps and mats when you are performing any kind of service to this module.

Installation Considerations

- The HP 16510A State/Timing Module(s) can be installed in any available card slot and in any order.
- Cards or filler panels below the empty slots intended for module installation do not have to be removed.
- The probe cables do not have to be removed to install the module.

Procedure

a. Turn the front and rear panel power switchs off, unplug power cord and disconnect any input BNCs.

b. Starting **from the top**, loosen thumb screws on filler panel(s) and card(s).

c. Starting **from the top**, begin pulling card(s) and filler panel(s) out **half way**. See figure A-1.

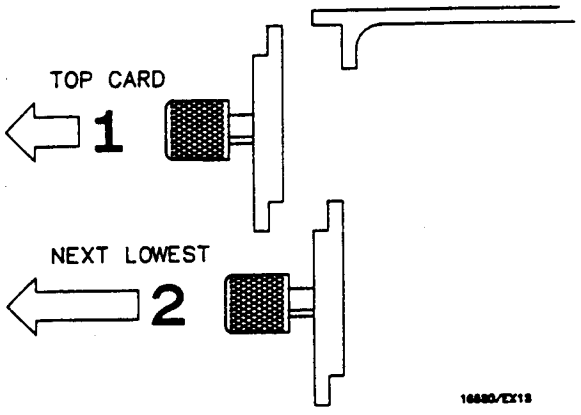


Figure A-1. Endplate Overlap

d. Lay the cable(s) flat and pointing out to the rear of the card. See figure A-2.

e. Slide the analyzer card approximately half way into the card cage.

f. If you have more analyzer cards to install repeat step d and e.

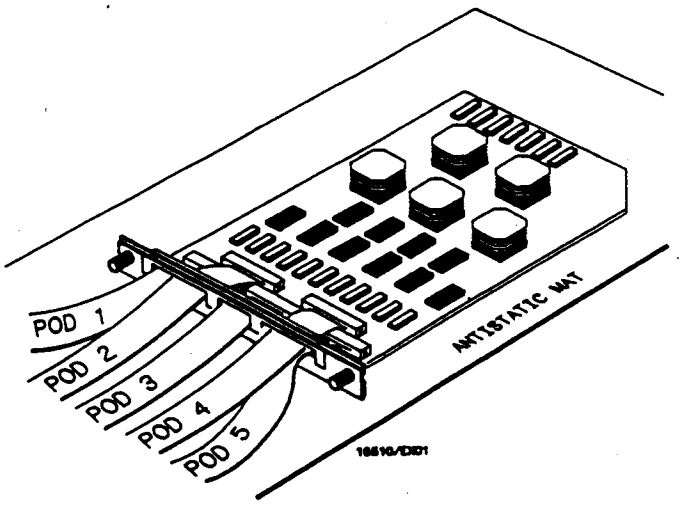


Figure A-2. Cable Position

g. Firmly seat bottom card into backplane connector. **Keep applying pressure to the center of card endplate while tightening thumb screws finger tight.**

h. Repeat for all cards and filler panels in a **bottom to top** order. See figure A-3.

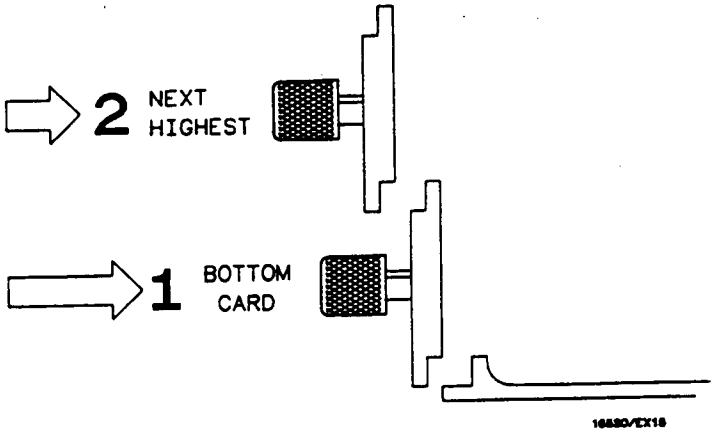


Figure 2-3. Endplate Overlap

i. Any filler panels that are not used should be kept for future use. Filler panels **must** be installed in all unused card slots for correct air circulation.

Operating Environment

The operating environment is listed in "General Characteristics" in Appendix C of this manual. Note should be made of the non-condensing humidity limitation. Condensation within the instrument can cause poor operation or malfunction. Protection should be provided against internal condensation.

The HP 16510A State/Timing Card will operate at all specifications within the temperature and humidity range given in Appendix C. However, reliability is enhanced when operating the module within the following ranges.

Temperature: +20 to +35° C (+68 to +95° F)
Humidity: 20% to 80% non-condensing

Storage

The module may be stored or shipped in environments within the following limits:

Temperature: -40° C to +75° C
Humidity: Up to 90% at 65° C
Altitude: Up to 15,300 meters (50,000 feet)

The module should also be protected from temperature extremes which cause condensation on the module.

Packaging

The following general instructions should be used for repacking the module with commercially available materials.

- Wrap module in anti-static plastic.
- Use a strong shipping container. A double-wall carton made of 350 lb. test material is adequate.
- Use a layer of shock-absorbing material 70 to 100 mm (3 to 4 inch) thick around all sides of the module to provide firm cushioning and prevent movement inside the container.
- Seal shipping container securely.
- Mark shipping container FRAGILE to ensure careful handling.
- In any correspondence, refer to module by model number and board number.

Tagging for Service

If the module is to be shipped to a Hewlett-Packard office for service or repair, attach a tag showing owner (with address), complete board number, and a description of the service required.

B Error Messages

This appendix lists the error messages that require corrective action to restore proper operation of the logic analyzer. There are several messages that you will see that are merely advisories and are not listed here. For example, "Load operation complete" is one of these advisories.

The messages are listed in alphabetical order and in bold type.

Autoscale aborted. This message is displayed when the STOP key is pressed or if a signal is not found 15 seconds after the initiation of autoscale.

Hardware ERROR: trace point in count block. Indicates the data from the last acquisition is not reliable and may have been caused by a hardware problem. Repeat the data acquisition to verify the condition. If this message re-appears, the logic analyzer requires the attention of service personnel.

Insufficient memory to load IAL - load aborted. This message indicates that there is not a block of free memory large enough for the inverse assembler you are attempting to load even though there may be enough memory in several smaller blocks. Try to load the inverse assembler again. If this load is unsuccessful, load the configuration and the corresponding inverse assembler separately.

Inverse assembler not loaded--bad object code. Indicates a bad inverse assembler file on the disc. A new disc or file is required.

Maximum number of symbols already allocated. Indicates an attempt to create more than 200 symbols.

Maximum of 32 channels per label. Indicates an attempt to assign more than 32 channels to a label. Reassign channels so that no more than 32 are assigned to a label.

Must have at least one edge specified. A state clock specification requires at least one clock edge. This message only occurs if you turn off all edges in the state clock specification.

No labels specified. Indicates there are no labels to which to assign symbols.

(x) Occurrences Remaining in Sequence (y). Indicates the logic analyzer is waiting for (x) number of occurrences in sequence level (y) of the state trace specification before it can go on to the next sequence level.

(x) Secs Remaining in Trace. Indicates the amount of time remaining until acquisition is complete in Glitch mode.

Search failed - O pattern not found. Indicates the O pattern does not exist in the acquired data. Check for a correct O marker pattern specification.

Search failed - X pattern not found. Indicates the X pattern does not exist in the acquired data. Check for a correct X marker pattern specification.

Slow Clock or Waiting for Arm. Indicates the state analyzer is waiting for a clock or arm signal. Re-check the state clock or arming specification.

Slow or missing Clock. Indicates the state analyzer has not recognized a clock for 100 ms. Check for a missing clock if the intended clock is faster than 100 ms. If clock is present but is slower than 100 ms, the data will still be acquired when a clock is recognized and should be valid.

Specified inverse assembler not found. Indicates the inverse assembler specified in the configuration file cannot be found on the disc.

State clock violates overdrive specification. Indicates the data from the last acquisition is not reliable due to the state clock signal not being reliable. Check the clock threshold for proper setting and the probes for proper grounding.

(x) States Remaining to Post Store. Indicates the number of states required until memory is filled and acquisition is complete.

Time correlation of data is not possible. "Count" must be set to "Time" in both machines to properly correlate the data. This message is also displayed when the data from this state/timing module cannot be time correlated in an intermodule "Group Run" configuration.

Time from arm to trace point > 41.943 ms. The correlation counter overflows when the time from a machine's arm to the machine's trigger exceeds 41.493 ms. It may be possible to add a "dummy" state to the machine's trigger specification that is closer in time to the arm signal.

(x) Transitions Remaining to Post Store. Indicates the number of transitions required until memory is filled and acquisition is complete.

Waiting for Arm. Indicates the arming condition has not occurred.

Waiting for Prestore. Indicates the prestore condition has not occurred (timing analyzer only).

Waiting for Trigger. Indicates the trigger condition has not occurred.

C Specifications and Characteristics

Specifications

Probes

Minimum Swing: 600 mV peak-to-peak.

Threshold Accuracy:

Voltage Range	Accuracy
-2.0V to +2.0V	±150 mV
-9.9V to -2.1V	±300 mV
+2.1V to +9.9V	±300 mV

Dynamic Range: ± 10 volts about the threshold.

State Mode

Clock Repetition Rate: Single phase is 25 MHz maximum. With time or state counting, minimum time between states is 60 ns. Both mixed and demultiplexed clocking use master-slave clock timing; master clock must follow slave clock by at least 10 ns and precede the next slave clock by >50 ns.

Clock Pulse Width: ≥10 ns at threshold.

Setup Time: Data must be present prior to clock transition, ≥ 10 ns.

Hold Time: Data must be present after rising clock transition on all pods; 0 ns.

Data must be present after falling clock transition on pods 1,3 and 5; 0 ns.

Data must be present after falling clock transition on pods 2 and 4; 1 ns.

Timing Mode

Minimum Detectable Glitch: 5 ns wide at the threshold.

Operating Characteristics

Probes

Input RC:	100 KΩ ±2% shunted by approximately 8 pF at the probe tip.
TTL Threshold Preset:	+1.6 volts.
ECL Threshold Preset:	-1.3 volts.
Threshold Range:	-9.9 to +9.9 volts in 0.1V increments.
Threshold Setting:	Threshold levels may be defined for pods 1, 2, and 3 on an individual basis and one threshold may be defined for pods 4 and 5.
Minimum Input Overdrive:	250 mV or 30% of the input amplitude, whichever is greater.
Maximum Voltage:	±40 volts peak.

Measurement Configurations

Analyzer Configurations:

Analyzer 1

Timing
Off

State
Off

Timing
State

State
Off

Analyzer 2

Off

Timing
Off

State
State

Timing
State

Off

Channel Assignment: Each group of 16 channels (a pod) can be assigned to Analyzer 1, Analyzer 2, or remain unassigned. The HP 16510A contains 5 pods.

State Analysis

Memory

Data Acquisition: 1024 samples/channel.

Trace Specification

Clocks: Five clocks are available and can be used by either one or two state analyzers at any time. Clock edges can be ORed together and operate in single phase, two phase demultiplexing, or two phase mixed mode. Clock edge is selectable as positive, negative, or both edges for each clock.

Clock Qualifier: The high or low level of up to four clocks can be ANDed with the clock specification. Setup time: 20 ns; hold time: 5 ns.

Pattern Recognizers: Each recognizer is the AND combination of bit (0, 1, or X) patterns in each label. Eight pattern recognizers are available when one state analyzer is on. Four are available to each analyzer when two state analyzers are on.

Range Recognizers: Recognizes data which is numerically between or on two specified patterns (ANDed combination of 0s and/or 1s). One range term is available and is assigned to the first state analyzer turned on. The maximum size is 32 bits.

Qualifier: A user-specified term that can be anystate, nostate, a single pattern recognizer, range recognizer, or logical combination of pattern and range recognizers.

Sequence Levels: There are eight levels available to determine the sequence of events required for trigger. The trigger term can occur anywhere in the first seven sequence levels.

Branching:	Each sequence level has a branching qualifier. When satisfied, the analyzer will restart the sequence or branch to another sequence level.
Occurrence Counter:	Sequence qualifier may be specified to occur up to 65535 times before advancing to the next level.
Storage Qualification:	Each sequence level has a storage qualifier that specifies the states that are to be stored.
Enable/Disable:	Defines a window of post-trigger storage. States stored in this window can be qualified.
Prestore:	Stores two qualified states that precede states that are stored.

Tagging

State Tagging:	Counts the number of qualified states between each stored state. Measurement can be shown relative to the previous state or relative to trigger. Maximum count is 4.4×10^{12}.
Time Tagging:	Measures the time between stored states, relative to either the previous state or the trigger. Maximum time between states is 48 hours. With tagging on, the acquisition memory is halved; minimum time between states is 60 ns.

Symbols

Pattern Symbols:	User can define a mnemonic for the specific bit pattern of a label. When data display is SYMBOL, mnemonic is displayed where the bit pattern occurs. Bit pattern can include 0s, 1s, and don't cares.
Range Symbols:	User can define a mnemonic covering a range of values. Bit pattern for lower and upper limits must be defined as a pattern of 0s and 1s. When data display is SYMBOL, values within the specified range are displayed as mnemonic + offset from base of range.

Number of Pattern and Range Symbols:	100 per analyzer. Symbols can be down-loaded over RS-232-C.

Timing Analysis

Transitional Timing Mode

Sample is stored in acquisition memory only when the data changes. A time tag stored with each sample allows reconstruction of waveform display. Time covered by a full memory acquisition varies with the number of pattern changes in the data.

Sample Period:	10 ns.
Maximum Time Covered By Data:	5000 seconds.
Minimum Time Covered By Data:	10.24 μs.

Glitch Capture Mode

Data sample and glitch information stored every sample period.

Sample Period:	20 ns to 50 ms in a 1-2-5 sequence dependent on s/div and delay settings.
Memory Depth:	512 samples/channel.
Time Covered by Data:	Sample period X 512.

Waveform Display

Sec/div:	10 ns to 100 s; 0.01% resolution.
Delay:	-2500 s to 2500 s; presence of data dependent on the number of transitions in data between trigger and trigger plus delay (transitional timing).
Accumulate:	Waveform display is not erased between successive acquisitions.
Overlay Mode:	Multiple channels can be displayed on one waveform display line. Primary use is to view summary of bus activity.

Maximum Number Of Displayed Waveforms:	24
Time Interval Accuracy	
Channel to Channel Skew:	4 ns typical.
Time Interval Accuracy:	± (sample period + channel-to-channel skew + 0.01% of time interval reading).
Trigger Specification	
Asynchronous Pattern:	Trigger on an asynchronous pattern less than or greater than specified duration. Pattern is the logical AND of specified low, high, or don't care for each assigned channel. If pattern is valid but duration is invalid, there is a 20 ns reset time before looking for patterns again.
Greater Than Duration:	Minimum duration is 30 ns to 10 ms with 10 ns or 0.01% resolution, whichever is greater. Accuracy is +0 ns to -20 ns. Trigger occurs at pattern + duration.
Less Than Duration:	Maximum duration is 40 ns to 10 ms with 10 ns or 0.01% resolution, whichever is greater. Pattern must be valid for at least 20 ns. Accuracy is +20 ns to -0 ns. Trigger occurs at the end of the pattern.
Glitch/Edge Triggering:	Trigger on glitch or edge following valid duration of asynchronous pattern while the pattern is still present. Edge can be specified as rising, falling or either. Less than duration forces glitch and edge triggering off.

Measurement and Display Functions

Autoscale (Timing Analyzer Only)

Autoscale searches for and displays channels with activity on the pods assigned to the timing analyzer.

Acquisition Specifications

Arming:	Each analyzer can be armed by the run key, the other analyzer, or the Intermodule Bus.
Trace Mode:	Single mode acquires data once per trace specification; repetitive mode repeats single mode acquisitions until stop is pressed or until time interval between two specified patterns is less than or greater than a specified value, or within or not within a specified range. There is only one trace mode when two analyzers are on.

Labels

Channels may be grouped together and given a six character name. Up to 20 labels in each analyzer may be assigned with up to 32 channels per label. Primary use is for naming groups of channels such as address, data, and control busses.

Indicators

Activity Indicators:	Provided in the Configuration, State Format, and Timing Format menus for identifying high, low, or changing states on the inputs.
Markers:	Two markers (X and O) are shown as dashed lines on the display.
Trigger:	Displayed as a vertical dashed line in the timing waveform display and as line 0 in the state listing display.

Marker Functions

Time Interval:	The X and 0 markers measure the time interval between one point on a timing waveform and trigger, two points on the same timing waveform, two points on different waveforms, or two states (time tagging on).
Delta States: **(State Analyzer Only)**	The X and 0 markers measure the number of tagged states between one state and trigger, or between two states.
Patterns:	The X and 0 markers can be used to locate the nth occurrence of a specified pattern before or after trigger, or after the beginning of data. The 0 marker can also find the nth occurrence of a pattern before or after the X marker.
Statistics:	X to 0 marker statistics are calculated for repetitive acquisitions. Patterns must be specified for both markers and statistics are kept only when both patterns can be found in an acquisition. Statistics are minimum X to 0 time, maximum X to 0 time, average X to 0 time, and ratio of valid runs to total runs.

Run/Stop Functions

Run:	Starts acquisition of data in specified trace mode.
Stop:	In single trace mode or the first run of a repetitive acquisition, STOP halts acquisition and displays the current acquisition data. For subsequent runs in repetitive mode, STOP halts acquisition of data and does not change current display.

Data Display/Entry

Display Modes: State listing; timing waveforms; interleaved, time-correlated listing of two state analyzers (time tagging on); time-correlated state listing and timing waveform display (state listing in upper half, timing waveform in lower half, and time tagging on).

Timing Waveform: Pattern readout of timing waveforms at X or O marker.

Bases: Binary, Octal, Decimal, Hexadecimal, ASCII (display only), and User-defined symbols.

Auxiliary Power

Power Through Cables: 2/3 amp @ 5V maximum per cable.

Current Draw Per Card: 2 amp @ 5V maximum per HP 16510A

Operating Environments

Temperature: Instrument, 0° to 55° C (+32° to 131° F). Probe lead sets and cables, 0° to 65° C (+32° to 149° F).

Humidity: Instrument, up to 95% relative humidity at +40° C (+122° F).

Altitude: To 4600 m (15,000 ft).

Vibration: **Operation:** Random vibration 5-500 Hz, 10 minutes per axis, ~0.3 g (rms).

Non-operating: Random vibration 5-500 Hz, 10 minutes per axis, ~ 2.41 g (rms); and swept sine resonant search, 5-500 Hz, 0.75 g (0-peak), 5 minute resonant dwell @ 4 resonances per axis.

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