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User's Reference

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For Safety information, Warranties, and Regulatory information, see the pages behind the Index.

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Agilent Technologies 16557D 135-MHz State/ 500-MHz Timing Logic Analyzer

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In This Book

The User's Reference manual contains field and feature definitions. Use this manual to learn what the menu fields do, what they are used for, and how the features work.

The manual is divided into chapters covering general product information, probing, and separately tabbed chapters for each analyzer menu. Chapters on error messages and instrument specifications are also provided.

In the Configuration menu, you have the choice of configuring an analyzer as either a State analyzer or a Timing analyzer. Some menus in the analyzer will change depending on the analyzer type you choose. For example, because a Timing analyzer does not use external clocks, the clock assignment fields in the Format menu will not be available.

If a menu field is only available to a particular analyzer type, the field is designated (Timing only) or (State only) after the field name. If no designation is shown, the field is available for both types.

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General Information

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Logic Analyzer Description

The Agilent Technologies 16557D State/Timing Analyzer module is part of a new generation of general-purpose logic analyzers. It is used with the Agilent Technologies 16500C Logic Analysis System mainframe, which is designed as a standalone instrument for use by digital and microprocessor hardware and software designers. The 16557D logic analyzer is not compatible with earlier models of the 16500 logic analysis system. The 16500C mainframe has GPIB and RS-232-C interfaces for hard copy printouts and control by a host computer.

The State/Timing Analyzer module has 64 data channels and four clock/data channels. Two additional 16557D cards can be added to expand the module to 200 data and 4 clock/data channels. Up to two more 16557D cards can be added to expand the module to 336 data and 4 clock/data channels, but the state speed decreases to 100 MHz.

Memory depth on the 16557D is 2M in all pod pair groupings, or 4M on just one pod (timing half-channel mode). All available resource terms can be assigned to either configured state or timing analyzer machine.

Measurement data is displayed as data listings or waveforms.

The 135-MHz state analyzer has master, slave, and demultiplexed clocking modes available. Measurement data can be stamped with either state or time tags. For triggering and data storage, the state analyzer uses 12 sequence levels with two-way branching, 10 pattern resource terms, 2 range terms, and 2 timers/counters.

The 500-MHz conventional timing analyzer has variable width, depth, and speed selections. Sequential triggering uses 10 sequence levels with two-way branching, 10 pattern resource terms, 2 range terms, 2 timers/counters and 2 edge/glitch terms.

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User Interface

The Agilent Technologies 16500C Logic Analysis System has four easy-to-use user interface devices: the knob, the touchscreen, the mouse, and the optional keyboard.

The knob on the front panel is used to move the cursor on certain menus, to increment or decrement numeric fields, and to roll the display.

The touchscreen fields can be selected by touch or with the mouse or keyboard. To activate a touchscreen field by touch, simply press the screen over any dark blue box on the display with your finger until the field changes color. Then remove your finger from the screen to activate your selection.

To activate a field with the mouse, position the cursor (+) of the mouse over the desired field and press the button on the upper-left corner of the mouse.

The optional keyboard can control all instrument functions by using special function keys, the arrow keys, and the ENTER key. Alphanumeric entry is simply typed in.

All user interface devices are discussed in more detail in the **Agilent Technologies 16500C User's Reference**.

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Configuration Capabilities

The 16557D can be configured as a single card, two-card, three-card, four-card, or five-card module. The number of data channels ranges from 68 channels using just one card, to 340 channels when five cards are installed. A half-channel acquisition mode is available for timing analyzers which reduces the channel width by half, but doubles memory depth from 2M-deep to 4M-deep per channel.

Modules are made of cards cabled together to form a single timebase. An 16557D module may use from one to five 16557D cards. Because the clock is common to all cards in a module, the data is always synchronized. For tightly coupled measurements involving multiple 16557D modules, your analyzer module provides an external reference clock. The reference clock prevents large data samples from becoming unsynchronized towards the end of a measurement. Because the internal clock on each logic analyzer card is accurate to 100 parts per million, in a 2M timing measurement using two modules, the last sample of each may be separated as much as 100 times the sample period. The external reference clock prevents this by having multiple modules share the same clock. There is no limit to how many modules may share the clock.

See Also

"Connecting the External Reference Clock" in chapter 2, Probing, for information on configuring the external reference clock.

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Key Features for the 16557D

- Lightweight passive probes for easy hookup and compatibility with previous Agilent logic analyzers and preprocessors.
- GPIB and RS-232-C interface for programming and hard copy printouts.
- Variable setup/hold time, 3.0-ns window.
- External arming to and from other modules through the intermodule bus.
- 2-M deep memory on all channels with 4 Mbytes in half-channel modes.
- Marker measurements.
- 12 levels of trigger sequencing for State and 10 levels of sequential triggering for Timing.
- Both state and timing analyzers can use 10 pattern resource terms, two range terms, and two timer/counters to qualify and trigger on data. The timing analyzer also has two edge terms available.
- Time (8-ns resolution) and number-of-qualified-states tagging.
- Full programmability.
- Mixed State/Timing and State/State (interleaved) display.
- Waveform display.

One, Two, or Three-Card 16557D

- 135-MHz state and 500-MHz timing acquisition speed.
- 64 data channels/4 clocks expandable to 200 data/4 clock channels.

Four or Five-Card 16557D

- 100-MHz state and 500-MHz timing acquisition speed.
- 268 data/4 clock channels or 336 data/4 clock channels.

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Accessories Supplied

The table below lists the accessories supplied with your logic analyzer. If any of these accessories are missing, contact your nearest Agilent Technologies Sales Office. If you need additional accessories, refer to the Accessories for Agilent Logic Analyzers brochure.

Table 1-1 **Accessories Supplied**

Accessory	Agilent Part No.	Quantity
Probe tip assemblies	01650-61608	4
Probe cables	16557-61601	2
Cable kit for multicard	16555-68705	1
Grabbers (20 per pack)	5090-4356	4 pkgs
Extra probe leads (5 per pack)	5959-9333	1 pkg
Probe cable and pod labels	01650-94312	1
Double probe adapter	16542-61607	1
External reference cable	16555-61608	1
Probe grounds (5 per pack)	5959-9334	4
Operating system disks	Call	1
User's Reference	Call	1

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Accessories Available

There are a number of accessories available that will make your measurement tasks easier and more accurate. You will find these listed in Accessories for Agilent Logic Analyzers, available from your Agilent Technologies Sales Office.

Preprocessor Modules

The preprocessor module accessories enable you to quickly and easily connect the logic analyzer to your microprocessor under test.

Included with each preprocessor module is a 3.5-inch disk which contains a configuration file and an inverse assembler file. When you load the configuration file, it configures the logic analyzer for making state measurements on the microprocessor for which the preprocessor is designed.

Configuration files from other analyzer modules can also be loaded. For information on translating other configuration files into the analyzer, refer to "Preprocessor File Configuration Translation and Pod Connections" in chapter 2, "Probing".

The inverse assembler file is a software routine that will display captured information in a specific microprocessor's mnemonics. The DATA field in the State Listing is replaced with an inverse assembly field. The inverse assembler software is designed to provide a display that closely resembles the original assembly language listing of the microprocessor's software. It also identifies the microprocessor bus cycles captured, such as Memory Read, Interrupt Acknowledge, or I/O write.

Many of the preprocessor modules require the Agilent Technologies 10269C General Purpose Probe Interface. The 10269C accepts the specific preprocessor PC board and connects it to five connectors on the general purpose interface to which the logic analyzer probe cables connect.

A list of preprocessor modules is found in the Accessories for Agilent Technologies Logic Analyzers brochure. Descriptions of the preprocessor modules are found with the preprocessor module accessories.

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2

Probing

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Probing

This chapter contains a description of the probing system for the logic analyzer. It also contains the information you need for connecting the probe system components to each other, to the logic analyzer, and to the system under test.

Probing Options

You can connect the logic analyzer to your system under test in one of the following ways:

- The standard general purpose probing (provided).
- Agilent Technologies E2445A User-Definable Interface (optional).
- Direct connection to a 20-pin, 3M-Series type header connector using the termination adapter (optional).
- Microprocessor and bus specific interfaces (optional).

General-Purpose Probing

General-purpose probing involves connecting the logic analyzer probes directly to your target system without using any interface. General purpose probing does not limit you to specific hook up schemes, as for example, the probe interface does. General-purpose probing uses grabbers that connect to both through hole and surface mount components.

General-purpose probing is the standard probing option provided with the logic analyzer. There is a full description of its components and use later in this chapter.

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The Agilent Technologies E2445A User-Definable Interface

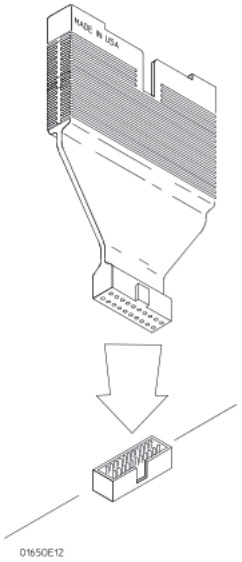
The optional Agilent Technologies E2445A User-Definable Interface allows you to connect the logic analyzer to the microprocessor in your target system. The E2445A includes a breadboard that you custom-wire for your system.

You will find additional information about the E2445A in the Accessories for Agilent Logic Analyzers brochure.

The Termination Adapter

The optional termination adapter allows you to connect the logic analyzer probe cables directly to test ports on your target system without the probes.

The termination adapter is designed to connect to a 20-pin (2x10), 4-wall, low-profile header connector, 3M-Series 3592 or equivalent.



Termination Adapter

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Microprocessor and Bus-Specific Interfaces

There are a number of microprocessor and bus-specific interfaces available as optional accessories which are listed in Microprocessor and Bus Interfaces and Software Accessories for Agilent Logic Analyzers. Microprocessors are supported by Universal Interfaces or Preprocessor Interfaces, or in some cases both.

Preprocessor interfaces are aimed at hardware turn-on and hardware/software integration, and will provide the following:

- All clocking and demultiplexing circuits needed to capture the system's operation.
- Additional status lines to further decode the operation of the CPU.
- Inverse assembly software to translate logic levels captured by the logic analyzer into microprocessor mnemonics.
- Bus interfaces to support bus analysis for GPIB, RS-232-C, RS-449, SCSI, VME, VXI, ISA, EISA, MCA, FDDI, Futurebus+, JTAG, SBus, PCI, and PCMCIA.

Universal Interfaces are aimed at initial hardware turn-on, and will provide fast, reliable, and convenient connections to the microprocessor system. Universal Interfaces do not provide inverse assembly of software instructions.

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Preprocessor File Configuration Translation and Pod Connections

Configuration files for the Agilent Technologies 16554, 16555A/D, and 16556A/D logic analyzers can be used by the 16557D. For the 16554-6 to the 16557D, no pod translation is necessary. Preprocessor configuration files from an Agilent Technologies 16550A can be used by the 16557D logic analyzer. However, some pods must be connected differently in order for the configuration files to work properly. The tables on the next several pages provide information on what configuration files to load and the required connections between the preprocessor interface and the 16557D pods.

In the tables, expansion and master card pods are referred to as either A or B pods. Those designations are done for convenience. The letter designation of pods in your module will depend on the slots in which your cards reside. They may use any letter from A through E for the 16500 Logic Analysis System mainframe, or F through J for the 16501A Expander Frame

In a five-card module, for example, the master card pods would be labeled C. The expansion card pods then would be labeled A, B, D, and E. Look at the Format menu for the slot designators for expansion cards in your system.

The following three tables provide configuration file names and pod connections for older microprocessors. Look in the microprocessor-specific preprocessor manual for configuration and connection information for newer microprocessors.

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Software and Hardware Translation Information

Table 2-1

Single-card 16550A configuration loaded into single-card 16557D

Agilent Model	Processor	16550A Config Filename	Master Card Pods B4 B3 B2 B1	Clocks	Drop Pods
10300B	Z80	FZ80	-- P2 -- P1	J+L	No
Inverse Assembler Labels: P1=DATA/STAT.clk P2=ADDR.clk					
10304B	8085	C8085_IF	-- P3 P2 P1	J, K mclk, sclk	No
Inverse Assembler Labels: P1=DATA/STAT.master_clk P2=ADDR.slave_clk					
10305B	8086	F8086_I	P3 P2 -- P1	J	No
Inverse Assembler Labels: P1=DATA.clk P2=ADDR P3=ADDR/STAT					
10305B	8088	F8088_I	P3 P2 -- P1	J	No
Inverse Assembler Labels: P1=DATA.clk P2=ADDR P3=ADDR/STAT					
10315G/H	68HC11	F68HC11	-- P2 -- P1	L, J mclk, sclk	Timing P3, P4
Inverse Assembler Labels: P1=ADDR/DATA.slave_clk P2=ADDR/STAT.master_clk					
10341B	1553	F1553	-- P2 -- P1	J	Timing
Inverse Assembler Labels: P1=DATA.clk (no Inverse Assembler capability)					P3
10342B	RS232	FRS232	-- P3 P4 P1	K	No
Inverse Assembler Labels: P1=DATA/STAT P4=.clk					
10342B	HPIB	FHPIB	. P3 P2	J	No
Inverse Assembler Labels: P2=DATA/STAT.clk P3=DATA					

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Table 2-1 (continued)

Single-card 16550A configuration loaded into single-card 16557D

Agilent Model	Processor	16550A Config Filename	Master Card Pods B4 B3 B2 B1	Clocks	Drop Pods
10342G	HPIB	FHPIB	-- J2 -- J2	J	No
Inverse Assembler Labels: J2=DATA/STAT.clk					
E2409B	80286	F80286S	P3 P2 -- P1	J	Timing
Inverse Assembler Labels: P1=Data.clk P2=ADDR P3=ADDR/STAT					P4, P5
E2409B	80286	F80286T	P3 P2 -- P4	Timing	Timing
Inverse Assembler Labels: n/a					P5
E2413B	68331/2	F68332	P4 P3 P5 P1	J	State
Inverse Assembler Labels: P1=DATA.clk P3=ADDR P4=ADDR P5=STAT					P2, P6
E2414B	68302	F68302	-- P4 P3 P1	J	No
Inverse Assembler Labels: P1=DATA.clk P3=ADDR P4=ADDR/STAT					
E2415A	MCS-51	FMCS51	-- P2 P3 P1	J	State
Inverse Assembler Labels: P1=DATA.clk P2=ADDR P3=STAT					P5
E2416A	MCS-96	FMCS96	-- P3 P2 P1	J	No
Inverse Assembler Labels: P1=DATA.clk P2=ADDR P3=STAT					
E2418A	320C20/25	F320C25	J3 J1 -- J2	J	No
Inverse Assembler Labels: J1=DATA J2=ADDR.clk J3=STAT					
E2419A	68HC16	FHC16	P4 P3 P5 P1	J	State
Inverse Assembler Labels: P1=DATA.clk P3=ADDR P5=STAT (P4=ADDR not required)					P2, P6

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Table 2-1 (continued)

Single-card 16550A configuration loaded into single-card 16557D

Agilent Model	Processor	16550A Config Filename	Master Card Pods B4 B3 B2 B1	Clocks	Drop Pods
E2423A	SCSI-2	FSCSI2	P4 P3 P2 P1	J	No
Inverse Assembler Labels: P1=STAT.clk P2=ADDR/DATA					
E2424B	68340	F68340	P4 P3 P5 P1	K	No
Inverse Assembler Labels: P1=DATA P3=ADDR P5=STAT.clk (P4=ADDR_B not required)					
E2424B	68340	FEV340	P4 P3 P5 P1	J	No
Inverse Assembler Labels: P1=DATA.clk P3=ADDR P5=STAT (P4=ADDR not required)					
E2431A	320C30/31	P_320C3X	P4 P3 P2 P1	J	No
Inverse Assembler Labels: P1=DATA.clk P2=DATA P3=ADDR P4=ADDR/STAT					
E2431A	320C30/31	Q_320C30	P6 P5 -- P7	J	No
Inverse Assembler Labels: P5=DATA P6=DATA P7=ADDR/STAT.clk					
Note: A single-card 16557D is not recommended for this preprocessor because it does not allow simultaneous viewing of both the primary and expansion microprocessor buses.					
E2434A	80186XL/88	C186EA09	P4 P3 -- P1	J	No
Inverse Assembler Labels: P1=DATA.clk P3=ADDR P4=ADDR/STAT					
E2434A	80186XL/88	C186EA10	P6 P5 P4 P2	Timing	No
Inverse Assembler Labels: n/a					
E2434B	80186/88EB	C186EB_7	P4 P3 -- P1	J	No
Inverse Assembler Labels: P1=DATA.clk P3=ADDR P4=ADDR/STAT					
E2434B	80186/88EB	C186EB_8	P6 P5 P4 P2	Timing	Timing
Inverse Assembler Labels: n/a					P7

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Table 2-1 (continued)

Single-card 16550A configuration loaded into single-card 16557D

Agilent Model	Processor	16550A Config Filename	Master Card Pods B4 B3 B2 B1	Clocks	Drop Pods
E2434C	80186/88EC	C186EC_7	P4 P3 P6 P1	J	No
Inverse Assembler Labels: P1=DATA.clk P3=ADDR P4=ADDR/STAT					
E2434C	80186/88EC	C186EC_8	P5 P6 P7 P2	Timing	Timing
Inverse Assembler Labels: n/a					P8
E2442A	TMS320C5X	D_320C5X	P5 P2 P3 P1	J+K+L	State
Inverse Assembler Labels: P1=DATA.clk P2=STAT.clk P3=ADDR.clk					P4, P6
E2447AA	68000	F68000	P6 P1 P4 P3	K	No
Inverse Assembler Labels: P1=DATA P3=ADDR P4=ADDR/STAT.clk					
E2447AA	68010	F68010	P6 P1 P4 P3	K	No
Inverse Assembler Labels: P1=DATA P3=ADDR P4=ADDR/STAT.clk					
E2447AB	68EC000	FEC000	P6 P1 P4 P3	K	No
Inverse Assembler Labels: P1=DATA P3=ADDR P4=ADDR/STAT.clk					
E2451A	Ethernet	CETH_4	P4 P3 P2 P1	J	No
Inverse Assembler Labels: P1=DATA.clk P2=ADDR/DATA_B P3=ADDR/DATA_B P4=STAT					
E2453A	DS1	C_DS1_6	. -- xx	J·	No
Inverse Assembler Labels: Carrier/Customer=ADDR/DATA/STAT.clk					
E2453A	DS1	C_DS1_7	-- Cu -- Ca mach2 mach1	J· L· mach1 mach2	No
Inverse Assembler Labels: Carrier=ADDR/DATA/STAT.clk Customer=ADDR/DATA/STAT.clk					

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Table 2-2

Single-card 16550A configuration loaded into multi-card 16557D

Agilent Model	Processor	16550A Config Filename	Expansion Card Pods A4 A3 A2 A1	Master Card Pods B4 B3 B2 B1	Clocks	Drop Pods
10300B	Z80	FZ80		-- P2 -- P1	J+L	No
Inverse Assembler Labels: P1=DATA/STAT.clk P2=ADDR.clk						
10304B	8085	C8085_IF	. -- P3	. P2 P1	J, K mclk, sclk	No
Inverse Assembler Labels: P1=DATA/STAT.master_clk P2=ADDR.slave_clk						
10305B	8086	F8086_I	. P3 P2	. -- P1	J	No
Inverse Assembler Labels: P1=DATA.clk P2=ADDR P3=ADDR/STAT						
10305B	8088	F8088_I	. P3 P2	. -- P1	J	No
Inverse Assembler Labels: P1=DATA.clk P2=ADDR P3=ADDR/STAT						
10315G/H	68HC11	F68HC11		-- P2 -- P1	L, J mclk, sclk	Timing P3, P4
Inverse Assembler Labels: P1=ADDR/DATA.slave_clk P2=ADDR/STAT.master_clk						
10341B	1553	F1553	. -- P2	-- P3 -- P1	J	No
Inverse Assembler Labels: P1=DATA.clk (no Inverse Assembler capability)						
10342B	RS232	FRS232		-- P3 P4 P1	K	No
Inverse Assembler Labels: P1=DATA/STAT P4=.clk						
10342B	HPIB	FHPIB		. P3 P2	J	No
Inverse Assembler Labels: P2=DATA/STAT.clk P3=DATA						
10342G	HPIB	FHPIB		-- J2 --- J2	J	No
Inverse Assembler Labels: J2=DATA/STAT.clk						

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Table 2-2 (continued)

Single-card 16550A configuration loaded into multi-card 16557D

Agilent Model	Processor	16550A Config Filename	Expansion Card Pods A4 A3 A2 A1	Master Card Pods B4 B3 B2 B1	Clocks	Drop Pods
E2409B	80286	F80286S	P5 P4 P3 P2	. -- P1	J	No
Inverse Assembler Labels: P1=DATA.clk P2=ADDR P3=ADDR/STAT						
E2409B	80286	F80286T	. P5 P4	P3 P2	Timing	No
Inverse Assembler Labels: n/a						
E2413B	68331/2	F68332	P6 P5 P4 P3	. P2 P1	J	No
Inverse Assembler Labels: P1=DATA.clk P3=ADDR P4=ADDR P5=STAT						
E2414B	68302	F68302	-- P4 -- P3	. -- P1	J	No
Inverse Assembler Labels: P1=DATA.clk P3=ADDR P4=ADDR/STAT						
E2415A	MCS-51	FMCS51	P5 P3 -- P2	. -- P1	J	No
Inverse Assembler Labels: P1=DATA.clk P2=ADDR P3=STAT						
E2416A	MCS-96	FMCS96	. -- P3	. P2 P1	J	No
Inverse Assembler Labels: P1=DATA.clk P2=ADDR P3=STAT						
E2418A	320C20/25	F320C25	-- J3 -- J1	. -- J2	J	No
Inverse Assembler Labels: J1=DATA J2=ADDR.clk J3=STAT						
E2419A	68HC16	FHC16	P6 P5 P4 P3	. P2 P1	J	No
Inverse Assembler Labels: P1=DATA.clk P3=ADDR P5=STAT (P4=ADDR not required)						
E2419A	68HC16EVB	FHC16	P6 P5 P3 P1	. P4 P2	J	No
Inverse Assembler Labels: P2=DATA.clk P1=ADDR P5=STAT (P3=ADDR not required)						

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Table 2-2 (continued)

Single-card 16550A configuration loaded into multi-card 16557D

Agilent Model	Processor	16550A Config Filename	Expansion Card Pods A4 A3 A2 A1	Master Card Pods B4 B3 B2 B1	Clocks	Drop Pods
E2423A	SCSI-2	FSCSI2		P4 P3 P2 P1	J	No
Inverse Assembler Labels: P1=STAT.clk P2=ADDR/DATA						
E2424B	68340	F68340	P4 P3 -- P1	. -- P5	J	No
Inverse Assembler Labels: P1=DATA P3=ADDR P5=STAT.clk (P4=ADDR_B not required)						
E2424B	68340	FEV340	-- P5 P4 P3	. -- P1	J	No
Inverse Assembler Labels P1=DATA.clk P3=ADDR P5=STAT (P4=ADDR not required)						
E2431A	320C30/31	O_320C30	-- P7	P2 P1 P4 P3	J+L	No
Inverse Assembler Labels: P1=DATA.clk P2=DATA P3=ADDR.clk P4=ADDR/STAT P7=STAT						
Note: This is actually a 16510 configuration file.						
E2434A	80186XL/88	C186EA09	. P4 P3	. -- P1	J	No
Inverse Assembler Labels: P1=DATA.clk P3=ADDR P4=ADDR/STAT						
E2434A	80186XL/88	C186EA10	. P6 P5	P4 P2	Timing	No
Cable Mapping: 1-B3 2-B4 3-A1 4-A2 5-B1 6-B2						
Inverse Assembler Labels: n/a						
E2434B	80186/88EB	C186EB_7	. P4 P3	. -- P1	J	No
Inverse Assembler Labels: P1=DATA.clk P3=ADDR P4=ADDR/STAT						
E2434B	80186/88EB	C186EB_8	-- P7 P6 P5	P4 P2	Timing	No
Inverse Assembler Labels: n/a						
E2434C	80186/88EC	C186EC_7	. P4 P3	. P6 P1	J	No
Inverse Assembler Labels: P1=DATA.clk P3=ADDR P4=ADDR/STAT						
E2434C	80186/88EC	C186EC_8	-- P8 P5 P6	P7 P2	Timing	No
Inverse Assembler Labels: n/a						

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Table 2-2 (continued)

Single-card 16550A configuration loaded into multi-card 16557D

Agilent Model	Processor	16550A Config Filename	Expansion Card Pods A4 A3 A2 A1	Master Card Pods B4 B3 B2 B1	Clocks	Drop Pods
E2442A	TMS320C5X	D_320C5X	. -- P4	P5 P2 P3 P1	J+K+L	No
Inverse Assembler Labels: P1=DATA.clk P2=STAT.clk P3=ADDR.clk						
E2447AA	68000	F68000	. P6 P1	. P4 P3	K	No
Inverse Assembler Labels: P1=DATA P3=ADDR P4=ADDR/STAT.clk						
E2447AA	68010	F68010	. P6 P1	. P4 P3	K	No
Inverse Assembler Labels: P1=DATA P3=ADDR P4=ADDR/STAT.clk						
E2447AB	68EC000	FEC000	. P6 P1	. P4 P3	K	No
Inverse Assembler Labels: P1=DATA P3=ADDR P4=ADDR/STAT.clk						
E2451A	Ethernet	CETH_4	. P4 P3	. P2 P1	J	No
Inverse Assembler Labels: P1=DATA.clk P2=ADDR/DATA_B P3=ADDR/DATA_B P4=STAT						
E2453A	DS1	C_DS1_6		. -- xx	J·	No
Inverse Assembler Labels: Carrier/Customer=ADDR/DATA/STAT.clk						
E2453A	DS1	C_DS1_7		-- Cu -- Ca mach2 mach1	J· L· mach1 mach2	No
Inverse Assembler Labels: Carrier=ADDR/DATA/STAT.clk Customer=ADDR/DATA/STAT.clk						

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Table 2-3

Two-card 16550A configuration loaded into multi-card 16557D (or single-card 16550 which requires more than four pods for inverse assembly)

Agilent Model	Processor	16550A Config Filename	Expansion Card Pods A4 A3 A2 A1	Master Card Pods B4 B3 B2 B1	Clocks	Drop Pods
E2401A	R3000	FR3KA	-- P7 P6 P5	P4 P3 P2 P1	J·	No
Inverse Assembler Labels: P1=STAT.clk P2=DATA P3=DATA P4=ADDR/STAT P5=ADDR P6=ADDR P7=STAT						
	FR3KB	Same as FR3KA				
	FR3KC	Same as FR3KA				
E2403A	80486	UI_486_21	-- J4 J6 J7	J3 J5 J1 J2	J	No
E2406A	68030	C68030_4	. P5 P4	-- P3 P2 P1	K+L	No
Inverse Assembler Labels: P1=DATA P2=DATA.clk P3=STAT.clk P4=ADDR P5=ADDR						
E2411C	80486	F486S2	-- P7 P6 P5	P4 P3 P2 P1	(J)*(K=1)	No
Inverse Assembler Labels: P1=STAT.clk P2=STAT.clk P3=DATA P4=DATA P5=ADDR P6=ADDR						
E2412A	I860XP	F_I860XP	P6 P5 P9 P8	P3 P2 P7 P1	J	No
Inverse Assembler Labels: P1=STAT.clk P2=DATA P3=DATA P5=DATA_B P6=DATA_B P7=STAT P8=ADDR P9=ADDR						
E2420A	68040	F68040	P4 P3 P2 P1	. -- P5	J	No
Inverse Assembler Labels: P1=ADDR P2=ADDR P3=DATA P4=DATA P5=STAT.clk						
E2426A/B	68020	F68020E	P6 P5 P2 P1	. P4 P3	J	No
Inverse Assembler Labels:						
P1=DATA P2=DATA P3=ADDR.clk P4=ADDR P5=STAT (P6=STAT_B not accessed by inverse assembler)						
E2426A/B	68EC020	FEC020E	P6 P5 P2 P1	. P4 P3	J	No
Inverse Assembler Labels:						
P1=DATA P2=DATA P3=ADDR.clk P4=ADDR P5=STAT (P6=STAT_B not accessed by inverse assembler)						

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Table 2-3 (continued)

Two-card 16550A configuration loaded into multi-card 16557D (or single-card 16550 which requires more than four pods for inverse assembly)

Agilent Model	Processor	16550A Config Filename	Expansion Card Pods A4 A3 A2 A1	Master Card Pods B4 B3 B2 B1	Clocks	Drop Pods
E2432A	80960CA	PI960CA_06	-- P7 P5 P4	P3 P2 P6 P1	J·	No
Inverse Assembler Labels: P1=STAT.clk P2=DATA P3=DATA P4=ADDR P5=ADDR						
E2435A	I860XR	I860XR3	-- P7 P6 P5	P3 P2 P4 P1	J	No
Inverse Assembler Labels: P1=STAT.clk P2=ADDR P3=ADDR P4=DATA_B P5=DATA P6=DATA P7=DATA_B						
E2438A	R4000	F_R4K	P6 P5 P4 P3	P8 P7 P2 P1	J·+K	State
P9						
Inverse Assembler Labels: P1=STAT.clk P2=STAT.clk P3=DATA P4=DATA P5=ADDR P6=ADDR P7=DATA_B P8=DATA_B						
E2441B	VME/VXI	FE2441	P6 P5 P4 P3	. P2 P1	J	No
Inverse Assembler Labels: P1=DATA.clk P2=DATA P3=ADDR P4=ADDR P5=STAT						
E2443B	Pentium	CPENT_2	P6 P5 P4 P3	P8 P7 P2 P1	(J)*(K=0)	State
P9, P10						
Inverse Assembler Labels: P1=STAT.clk P2=STAT.clk P3=ADDR P4=ADDR P5=DATA P6=DATA P7=DATA_B P8=DATA_B						
E2444A	80386DX	PI386_04	-- P5 P4 P3	. P2 P1	J	No
Inverse Assembler Labels: P1=DATA.clk P2=DATA P3=ADDR P4=ADDR P5=STAT						

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Table 2-3 (continued)

Two-card 16550A configuration loaded into multi-card 16557D (or single-card 16550 which requires more than four pods for inverse assembly)

Agilent Model	Processor	16550A Config Filename	Expansion Card Pods A4 A3 A2 A1	Master Card Pods B4 B3 B2 B1	Clocks	Drop Pods
E2448A	68360	C68360_0	P6 P5 P4 P3	. P2 P1	J	No
		^ Asynchronous Operation				
Inverse Assembler Labels: P1=STAT.clk P2=STAT P3=DATA P4=DATA P5=ADDR P6=ADDR						
E2448A	68360	C68360_4	. P4 P3	P6 P5 P2 P1	J+L,K	No
		^Synchronous Operation				
Inverse Assembler Labels:						
P1=STAT.master_clk P2=STAT.slave_clk P3=DATA P4=DATA P5=ADDR.master_clk P6=ADDR						
E2457A	P54C	CP54C_2	P6 P5 P4 P3	P8 P7 P2 P1	(J)*(K=0)	State
P9, P10						
Inverse Assembler Labels:						
P1=STAT.clk P2=STAT.clk P3=ADDR P4=ADDR P5=DATA P6=DATA P7=DATA_B P8=DATA_B						

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General-Purpose Probing System Description

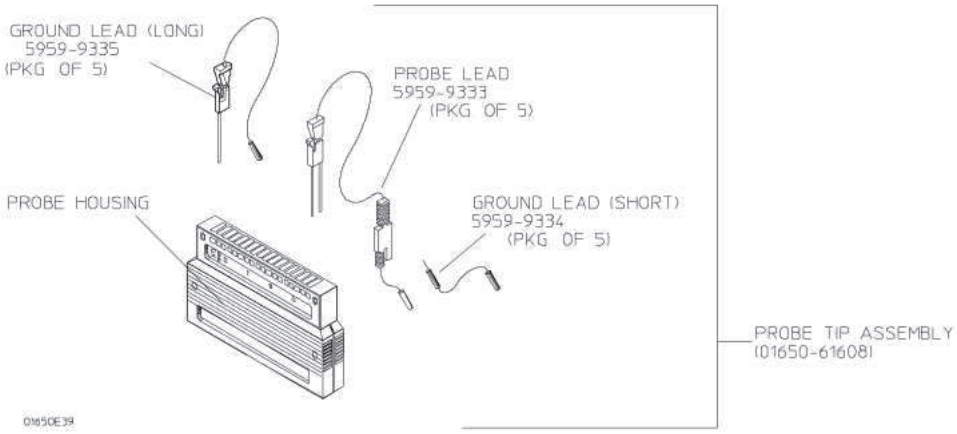
The standard probing system provided with the logic analyzer consists of a probe tip assembly, probe cable, and grabbers. Because of the passive design of the probes, there are no active circuits at the outer end of the cable.

The passive probing system is similar to the probing system used with high-frequency oscilloscopes. It consists of a series RC network (90 kΩ in parallel with 8 pF) at the probe tip, and a shielded resistive transmission line. The advantages of this system include the following:

- 250 Ω in series with 8-pF input capacitance at the probe tip for minimal loading.
- Signal ground at the probe tip for higher speed timing signals.
- Inexpensive removable probe tip assemblies.

Probe Tip Assemblies

Probe tip assemblies allow you to connect the logic analyzer directly to the target system. This general-purpose probing is useful for discrete digital circuits. Each probe tip assembly, or pod, contains 16 probe leads (data channels), one clock lead, a pod ground lead, and a ground tap for each of the 16 probe leads.



Probe Tip Assembly

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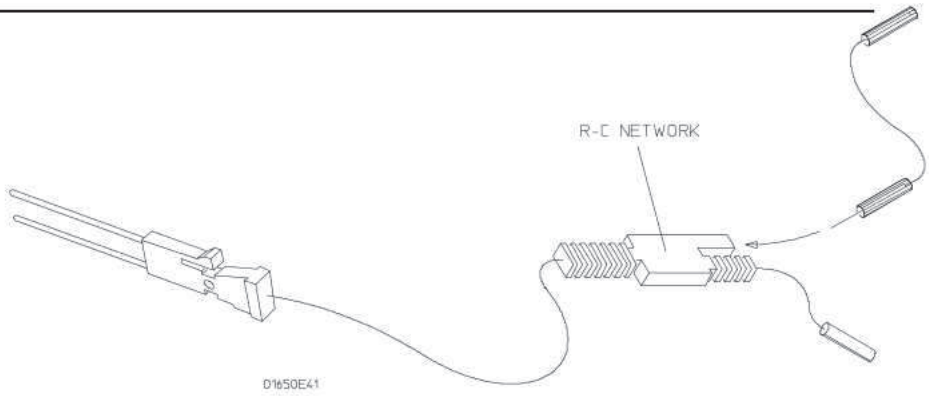
Probe and Pod Grounding

Each pod is grounded by a long black pod ground lead. You can connect the ground lead directly to a ground pin on your target system or use a grabber. To connect the ground lead directly to grounded pins on your target system, you must use 0.63 mm (0.025 in) square pins, or use round pins with a diameter of 0.66 mm (0.026 in) to 0.84 mm (0.033 in). The pod ground lead should always be used.

Each probe can be individually grounded with a short black extension lead that connects to the probe tip socket. You can then use a grabber or the grounded pins on your target system in the same way you connect the data lines.

When probing signals with rise and fall times of 1 ns, grounding each probe lead with the 2-inch ground lead is recommended. In addition, always use the probe ground on a clock probe.

Probe ground lead



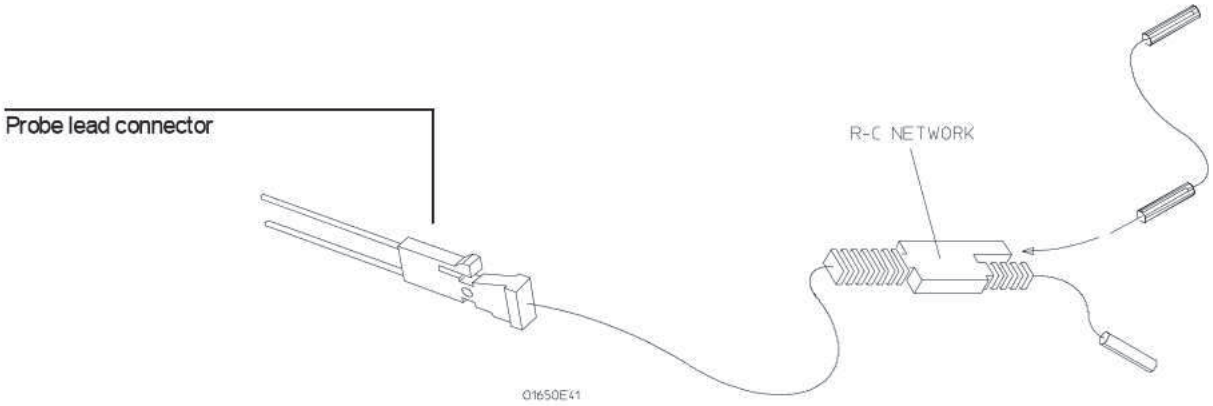
Probe Grounds

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Probe Leads

The probe leads consists of a 12-inch twisted pair cable, a ground tap, and one grabber. The probe lead, which connects to the target system, has an integrated RC network with an input impedance of 100 kΩ in parallel with approximately 8 pF, and all in series with 250 Ω.

The probe lead has a two-pin connector on one end that snaps into the probe housing.



Probe Lead

Grabbers

The grabbers have a small hook that fits around the IC pins and component leads. The grabbers have been designed to fit on adjacent IC pins on either through-hole or surface-mount components with lead spacing greater than or equal to 0.050 in.

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Probe Cable

The probe cable contains 18 signal lines, 17 chassis ground lines, and two power lines for preprocessor use. The cables are woven together into a flat ribbon that is 4.5 feet long. The probe cable connects the logic analyzer to the pods, termination adapter, Agilent Technologies 10269C General-Purpose Probe Interface, or preprocessor. Each cable is capable of carrying 0.33 amps for preprocessor power.

CAUTION

DO NOT exceed this 0.33 amps per cable or the cable will be damaged.

WARNING

Preprocessor power is protected by a current limiting circuit. If the current limiting circuit is activated, the fault condition must be removed. After the fault condition is removed, the circuit will reset in one minute.

Minimum Signal Amplitude

Any signal line you intend to probe with the logic analyzer probes must supply a minimum voltage swing of 500 mV to the probe tip. If you measure signal lines with a voltage swing of less than 500 mV, you may not obtain a reliable measurement.

Maximum Probe Input Voltage

The maximum input voltage of each logic analyzer probe is 40 volts peak.

Pod Thresholds

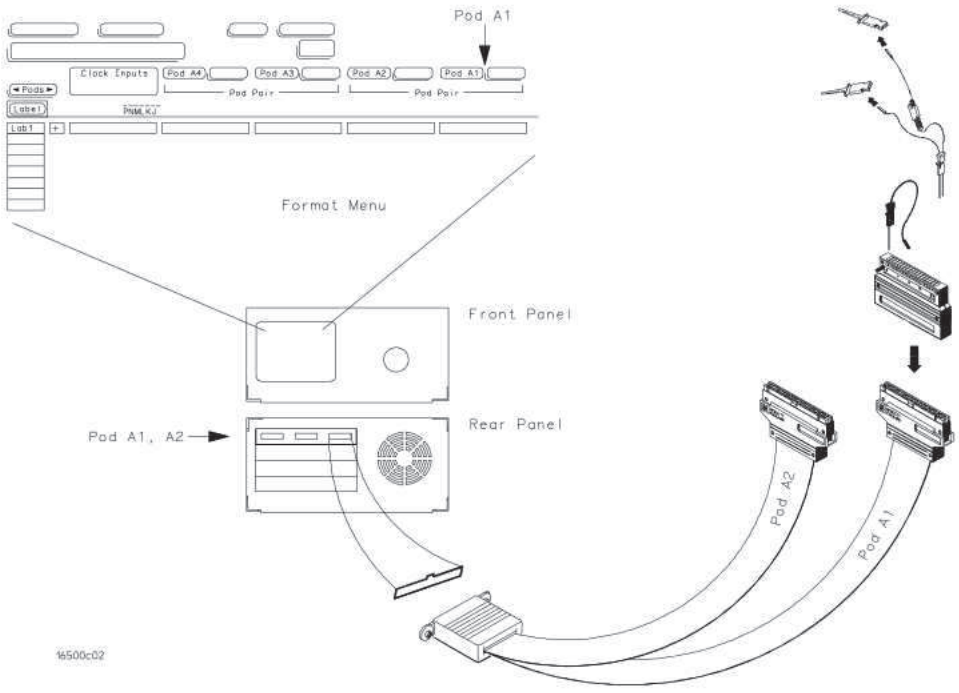
Logic analyzer pods have two preset thresholds and a user-definable threshold. The two preset thresholds are ECL (– 1.3 V) and TTL (+1.5 V). The user-definable threshold can be set anywhere between – 6.0 volts and +6.0 volts in 0.05-volt increments.

All pod thresholds are set independently.

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Assembling the Probing System

The general-purpose probing system components are assembled as shown below to make a connection between the measured signal line and the pods displayed in the Format menu.



Connecting Probe Cables to the Logic Analyzer

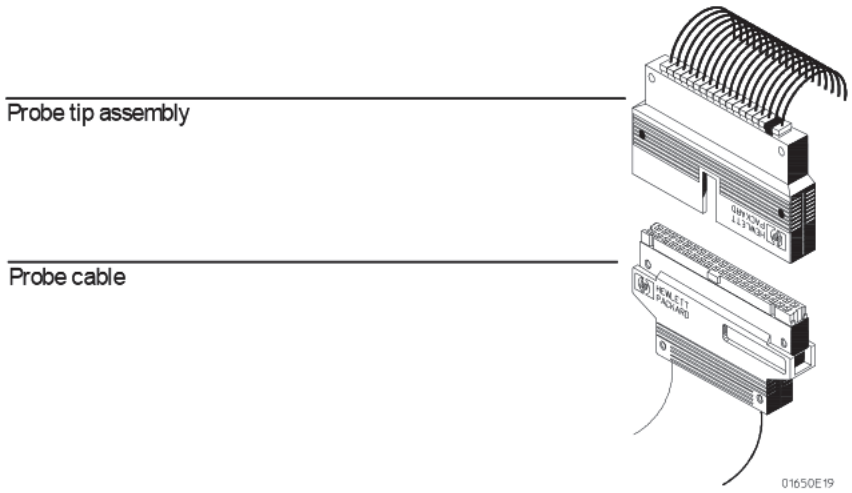
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Connecting Probe Cables to the Logic Analyzer

All probe cables are installed at Agilent Technologies. If you need to replace a probe cable, refer to the Agilent Technologies 16557D Logic Analyzer Service Guide, available from your Agilent Technologies Sales Office.

Connecting the Probe Tip Assembly to the Probe Cable

To connect a probe tip assembly to a cable, align the key on the cable connector with the slot on the probe housing and press them together.



Connecting Probe Tip Assembly

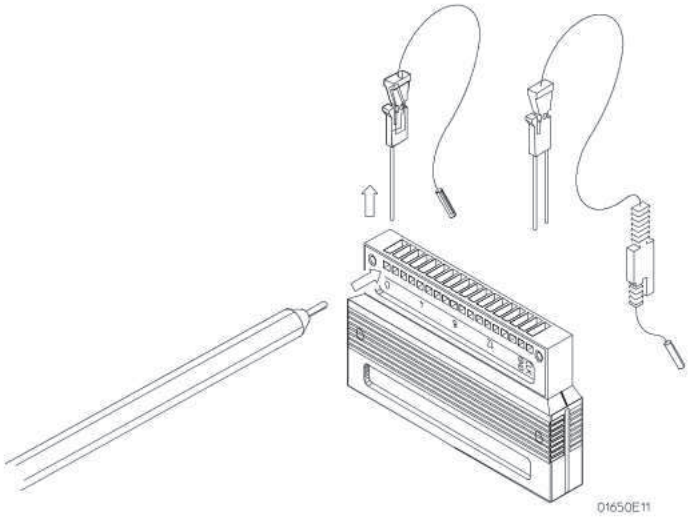
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Disconnecting Probe Leads from Probe Tip Assemblies

When you receive the logic analyzer, the probe leads are already installed in the probe tip assemblies. To keep unused probe leads out of your way during a measurement, you can disconnect them from the pod.

To disconnect a probe, insert the tip of a ball-point pen into the latch opening. Push on the latch while gently pulling the probe out of the pod connector as shown in the figure below.

To connect the probes to the pods, insert the double pin end of the probe into the probe housing. Both the double pin end of the probe and the probe housing are keyed so they will fit together only one way.

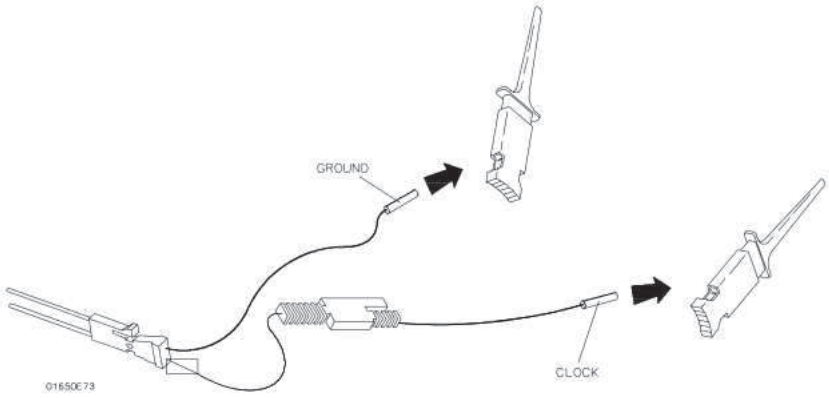


Installing Probe Leads

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Connecting the Grabbers to the Probes

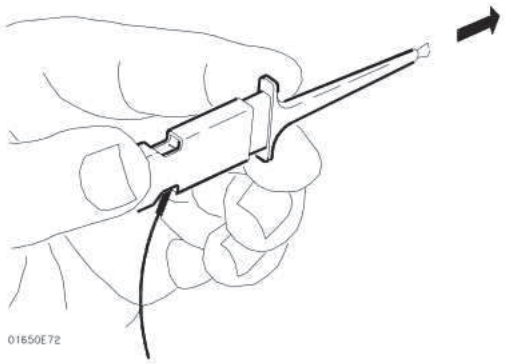
Connect the grabbers to the probe leads by slipping the connector at the end of the probe onto the recessed pin located in the side of the grabber. If you need to use grabbers for either the pod or the probe grounds, connect the grabbers to the ground leads in the same manner.



Connecting Grabbers to Probes

Connecting the Grabbers to the Test Points

The grabbers have a hook that fits around the IC pins and component leads. Connect the grabber to the test point by pushing the rear of the grabber to expose the hook. Hook the lead and release your thumb as shown.



Connecting Grabbers to Test Points

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Connecting the External Reference Clock

The external reference clock synchronizes deep-memory logic analyzer modules. Within a module, the individual cards all share a common clock and are thus automatically synchronized. However, each module clock is accurate only to 100 parts per million. So, two deep-memory logic analyzers with identical settings may capture their trigger at the same time but show discrepancies in the final sample. Sharing an external reference clock prevents this.

To Connect the External Reference Clock

You can either supply your own external reference clock, or choose one of the logic analyzer modules to supply the clock signal. Either method keeps all connected modules synchronized.

1 If you are supplying the clock signal, connect it to the "reference clock in" of the master card of the top module.



The Reference Clock field lets you specify whether to use the internal clock provided on the card, or an external clock. If you select the external clock, you must connect a clock signal to the card using the Reference Clock In/Out ports on the back of the analyzer.

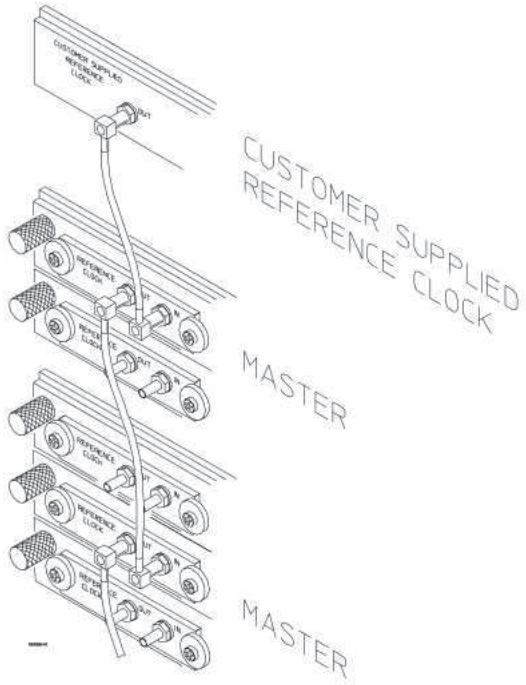
CAUTION

Do not exceed 1 V, peak-to-peak, at a maximum voltage offset of 20 V on the Reference Clock In/Out ports.

2 Cable the top module's "reference clock out" to the "reference clock in" of the master card of the next module.

3 Continue connecting the modules in this manner.

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Connecting the External Reference Clock

Note that only the master card of a module should be connected. Connecting the clocks of the expander cards will not synchronize the module. Any number of modules may be synchronized together. Any modules that have external reference clock ports may be connected together.

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3

The Configuration Menu

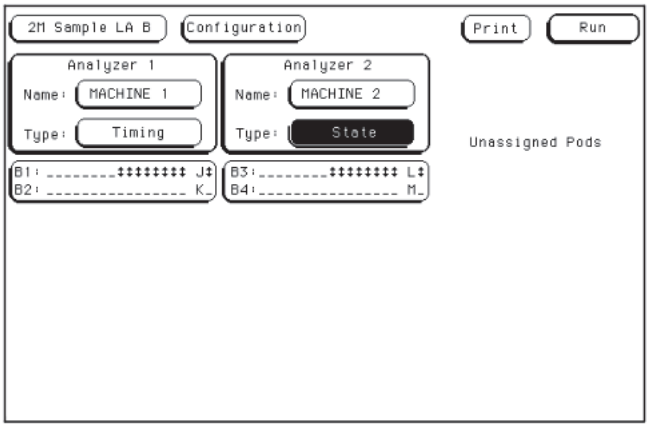
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The Configuration Menu

The Configuration menu allows you to set module level parameters. You can partition the module into one or two independent analyzers. You can also assign pods to either analyzer, select the type of clocking needed (state or timing), and provide names for each analyzer.

The fields on this menu are:

- Analyzer Name Field
- Analyzer Type Field
- Pod Fields
- Activity Indicators

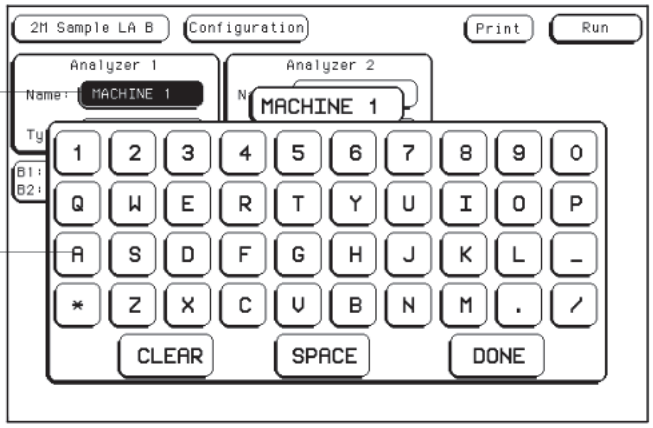


Configuration Menu

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Analyzer Name Field

The Name field lets you assign a specific name to the analyzer machine. Use the pop-up alphanumeric keypad to enter the name. When you have stored several configurations to disk and later reload them, having assigned a specific name to an analyzer can help identify the measurement setup.



Name Field

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Analyzer Type Field

The Type field allows you to configure each analyzer as either a state or timing analyzer. When the Type field is selected, the following choices are available.

- Off
- Timing
- State
- State Compare
- SPA

Timing

When you select Timing, the analyzer uses its own internal clock to clock measurement data into the acquisition memory. This clock is asynchronous to the signals in the target system. When this option is selected, some fields specific to external clocks will not appear in the analyzer menus.

You can configure the machine with only one timing analyzer. If you select both analyzers as timing analyzers, the first will be turned off.

State

When you select State, the analyzer uses a clock from the system under test to clock measurement data into acquisition memory. This clock is synchronous with the signals in the target system. You can configure both analyzers as state analyzers. State mode does not allow you to access the Compare menu.

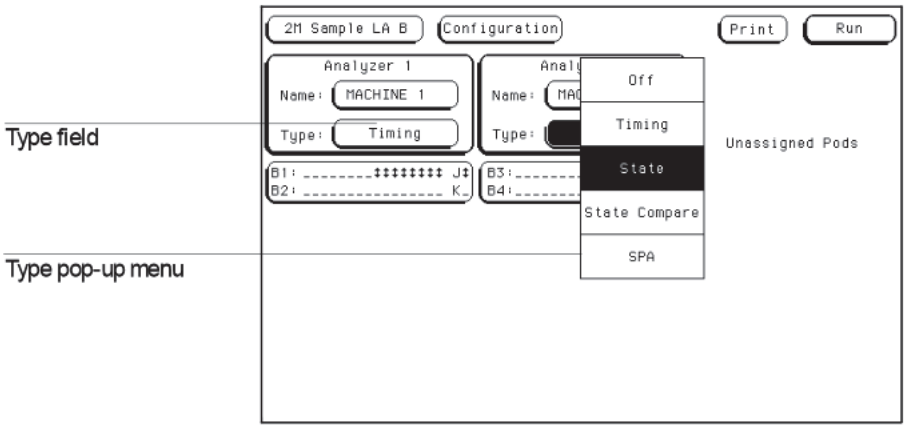
State Compare

When State Compare is selected, the Compare menu is available in the main menu selection. For more details on Compare, see chapter 9, "The Compare Menu." State Compare mode functions much like State mode, except that total memory is reduced by one-fourth.

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SPA

SPA stands for System Performance Analysis. It uses an external clock like a state analyzer but measures overall system performance rather than recording discrete activity. For more details, see Chapter 11.

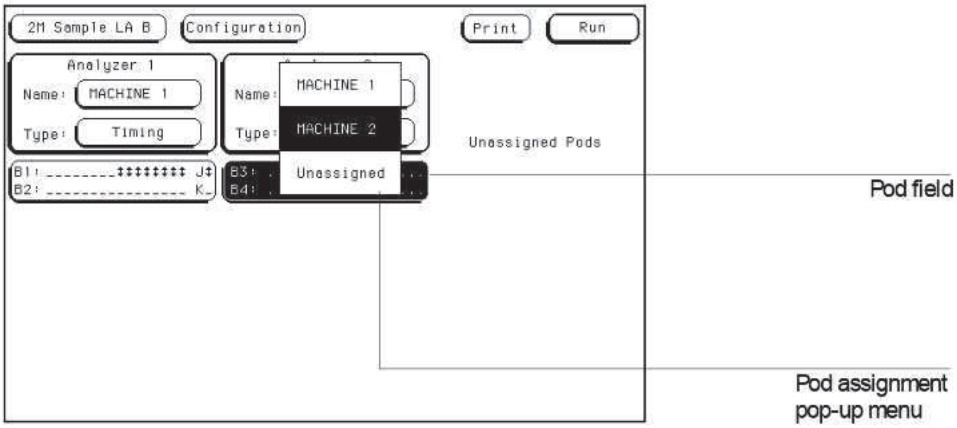


Type Field

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Pod Fields

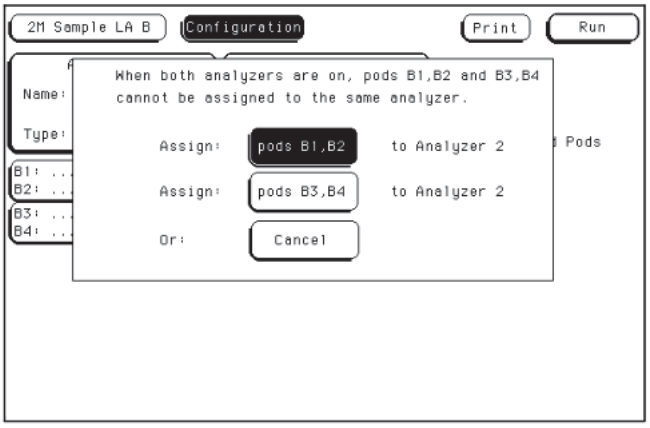
The list of unassigned pods in the Configuration menu shows the available pods for the module configuration. Pod grouping and assignment is by pod pairs. When you want to assign a pod pair to an analyzer, touch the pod field. From the assignment menu, select a destination for the pod pair. Use the same procedure to reassign pod pairs that have previously been assigned to an analyzer.



Unassigned Pods Display

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When both analyzers are turned on, the pods of the master card cannot be assigned to the same analyzer. If you attempt to assign them to the same analyzer, you'll get an error message when you try to exit the configuration menu. The error message gives an explanation of the problem and provides selection fields with options for reassigning one of the pod pairs.



Pod Reassignment Menu

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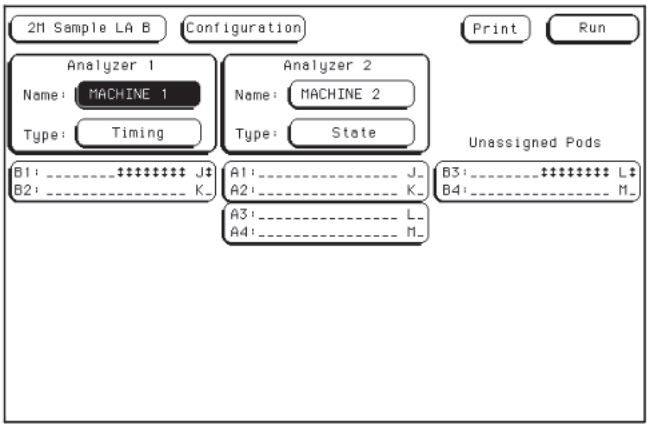
Activity Indicators

Within each pod pair you'll notice activity indicators for each bit of each pod. These indicators appear in two places. One is in the pod pair displays of this Configuration menu. The other place is in the bit reference line in the Format menu just above the pod bit numbers.

When the logic analyzer is properly connected to an active target system, you'll see either a high-level dash, a low-level dash, or a transitional arrow in the Activity Indicator displays for each pod pair. These indicators are very useful in showing proper probe connections and that the logic levels are as expected.

See Also

The "Bit Assignment Fields" in chapter 4, "The Format Menu," for more information on the activity indicators.



Activity Indicators

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4

The Format Menu

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The Format Menu

Use the Format menu to select which data channels are measured and to set up the clocking arrangement to capture valid data. It allows you to group and label the data channels from the system under test to fit your particular measurement. In addition, for your convenience in recognizing bit groupings, you can specify symbols to represent them. If the analyzer is configured as a state analyzer, there are master and slave clocks, clock qualifiers, and a variable clock setup and hold to further qualify what data is captured. In addition, you can set individual pod clock threshold levels. The Format menu contains the following fields:

- State Acquisition Mode Field (State, State Compare, and SPA only)
- Timing Acquisition Mode Field (Timing only)
- Data on Clocks Display
- Pod Field
- Pod Clock Field (State only)
- Master and Slave Clock Field (State only)
- Setup/Hold Field (State only)
- Symbols Field
- Label Assignment Field
- Rolling Labels and Pods Field
- Label Polarity Fields
- Bit Assignment Fields
- Pod Threshold Field

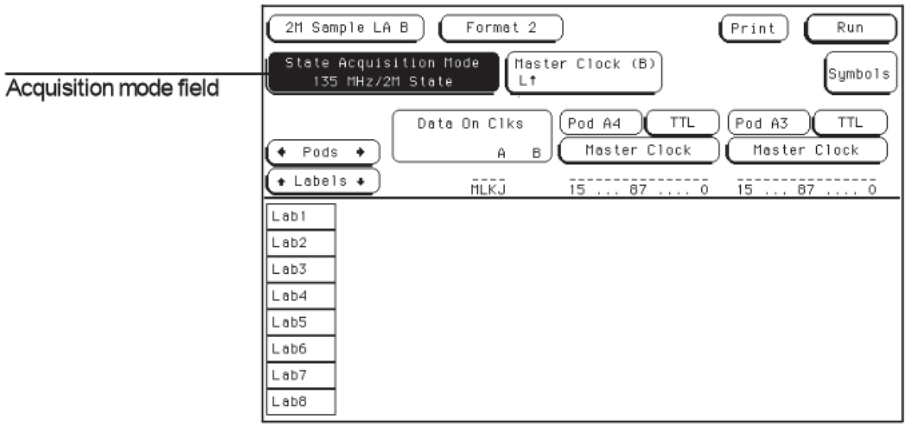
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State Acquisition Mode Field (State, State Compare, and SPA only)

The State Acquisition Mode field identifies the speed and memory depth of the acquisition mode. In four or five-card systems, speed is reduced to 100 MHz. In State Compare mode, some memory depth is used for information needed to perform a comparison.

135 MHz [100 MHz]/2M State

The State Acquisition Mode uses both pods in a pod pair. If time or state tags are turned on, the total memory is split between data acquisition storage and time or state tag storage. To maintain the full 2M per channel depth, leave one pod pair unassigned. State clock speed is 135 MHz [100 MHz for four or five-card configurations].



Acquisition Mode Field

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Timing Acquisition Mode Field (Timing only)

The Timing Acquisition Mode field displays the acquisition type, the channel width, and sampling speed of the present acquisition mode. In timing acquisition mode, the analyzer stores measurement data at each sampling interval. Use the Timing Acquisition Mode field to access an acquisition mode selection menu.

2M Sample Full Channel 250MHz

The total memory depth is 2M, with data being sampled and stored at most every 4 ns.

4M Sample Half Channel 500MHz

The total memory depth is 4M, with data being sampled and stored at most every 2 ns.

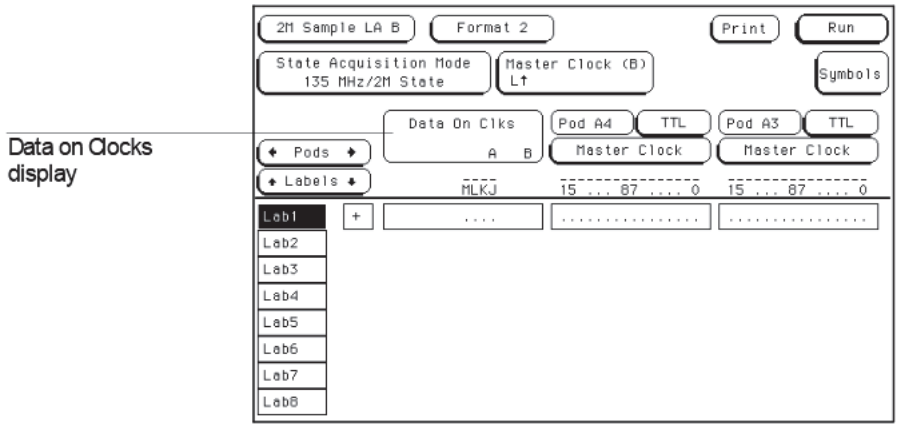
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Data on Clocks Display

This display shows the clock input channels available for the present configuration. There are four clock input channels (J, K, L, and M) for each card of a module, one for each pod. This display shows only the clock input channels for those pods that are assigned in the present configuration.

A single-card module has four clock input channels, each of which may be used as a state clock (when the machine is configured for state mode) or as a data channel (in either state or timing modes). In a multi-card module, only the four clock input channels connected to the Clock Master card of the module are available for use as state clocks, but all of the clock input channels of the module (there are four for each card in the module) may be used as data channels. A clock input channel, when used as a data channel, is treated as an ordinary data channel, except it cannot be included in a Range resource.

In the display panel, the clock input channels of the Clock Master card are grouped on the right, underneath the slot letter of the Clock Master card, with the clock input channels of the other cards displayed to the left of those of the Clock master card. If any clock input channel is used as a data channel, that bit must be assigned. Activity indicators above the clock identifier show signal activity on that clock input channel.

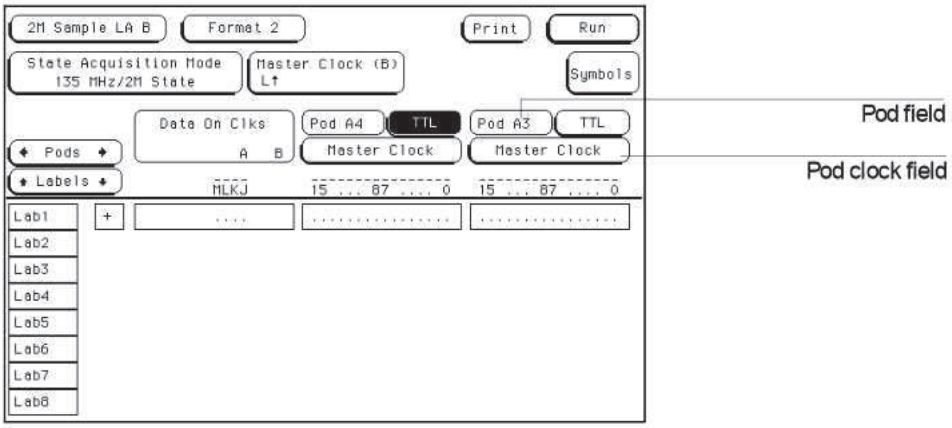


Data on Clocks Display

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Pod Field

The Pod field identifies which pod of a pod pair is affected by the settings of the bit assignment field, pod threshold field, and pod clock fields. In the full-channel modes, this field is simply an identifier and is not selectable. However, in the half-channel mode, the Pod field turns dark, which means it is selectable. In the half-channel mode, one pod of a pod pair is selectable and all pod settings affect the selected pod.



Pod Field

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Pod Clock Field (State only)

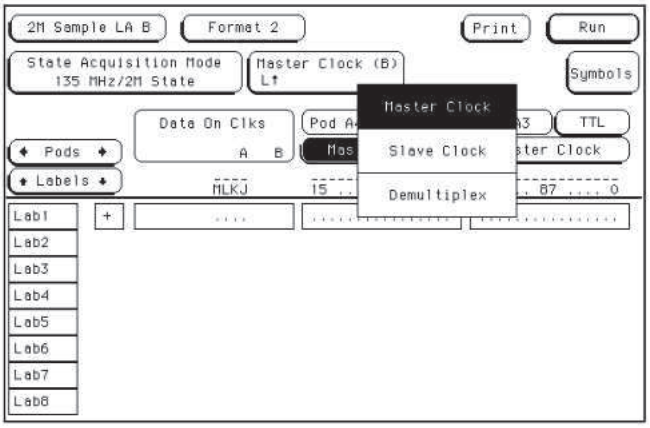
There is one Pod Clock field for each pod in the machine, and it is used to indicate whether that pod's data lines are to be strobed into memory by the Master clock, Slave clock, or both, in the Demultiplex mode of operation. When the Pod Clock field is selected, a clock menu appears with the following choices:

- Master
- Slave
- Demultiplex

The Master and Slave clock events are specified in the Master and Slave clock fields. These clock functions are available only in a state analyzer.

See Also

The "Master and Slave Clock Field" later in this chapter for information about configuring a clocking arrangement.



Pod Clock Field

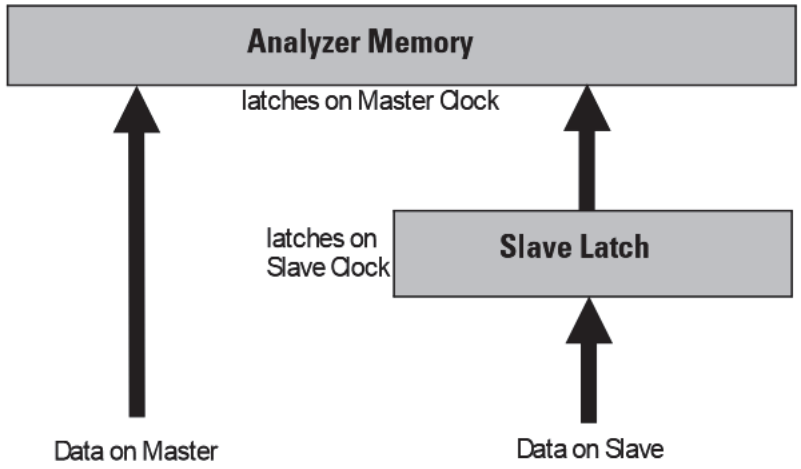
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Master

This option specifies that data on all pods designated "Master Clock," in a single analyzer, are strobed into memory when the status of the clock lines matches the clocking arrangement specified under the Master Clock.

Slave

This option specifies that data on a pod designated "Slave Clock" is latched when the status of the state clock inputs meets the requirements of the slave clocking arrangement. Then, followed by a match of the master clock and the master clock arrangement, the slave data is strobed into analyzer memory along with the master data. If multiple slave clocks occur between master clocks, only the data latched by the last slave clock prior to the master clock is strobed into analyzer memory.

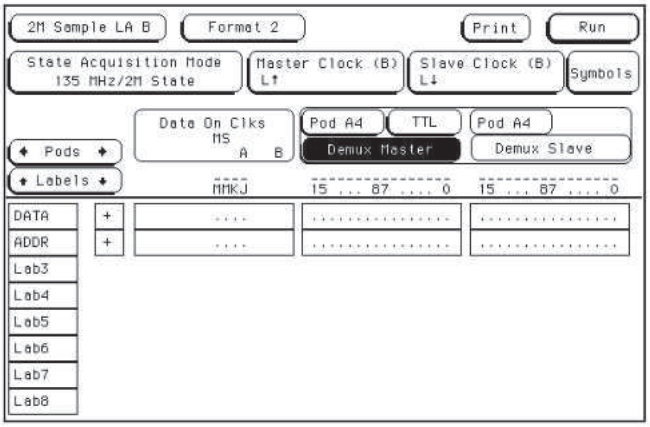


Latching Slave Data

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Demultiplex

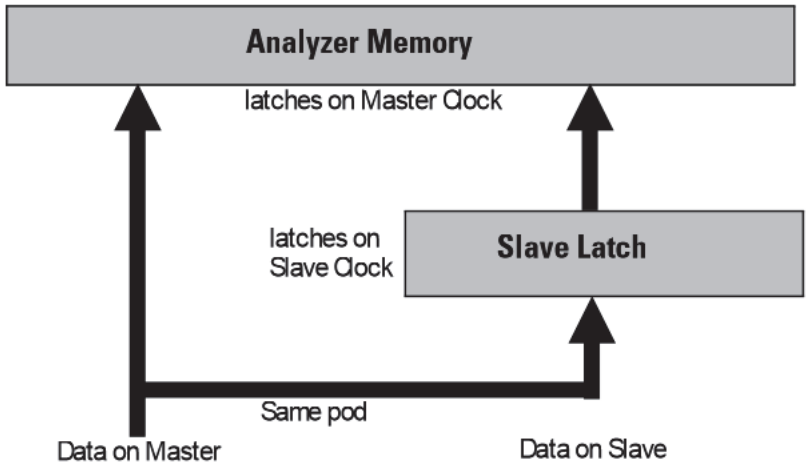
The Demultiplex mode is used to store two different sets of data that occur at different times on the same channels. In Demultiplex mode, only one pod of the pod pair is used, and that pod is selectable. Both the master and slave clocks are used in the Demultiplex mode. Channel assignments are displayed as Demux Master and Demux Slave. For easy recognition of the two sets of data, assign slave and master data to separate labels.



Demultiplex Clocking Mode

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When the analyzer sees a match between the state clock inputs and the slave clock specification, Demux Slave data is latched. Then, followed by a match of the state clocks and the master clock specification, the slave data is strobed into analyzer memory along with the master data. If multiple slave clocks occur between master clocks, only the data latched by the last slave clock prior to the master clock is strobed into analyzer memory.



Latching Slave Data in Demultiplex Mode

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Pod Threshold Field

Use the Pod Threshold field to set a voltage level the data must reach before the analyzer recognizes and displays it as a change in logic levels. You specify a threshold level for each pod. The level specified for each pod is also assigned to the pod's clock threshold. When the Pod Threshold field is touched, a threshold selection pop-up menu appears with the following choices:

TTL

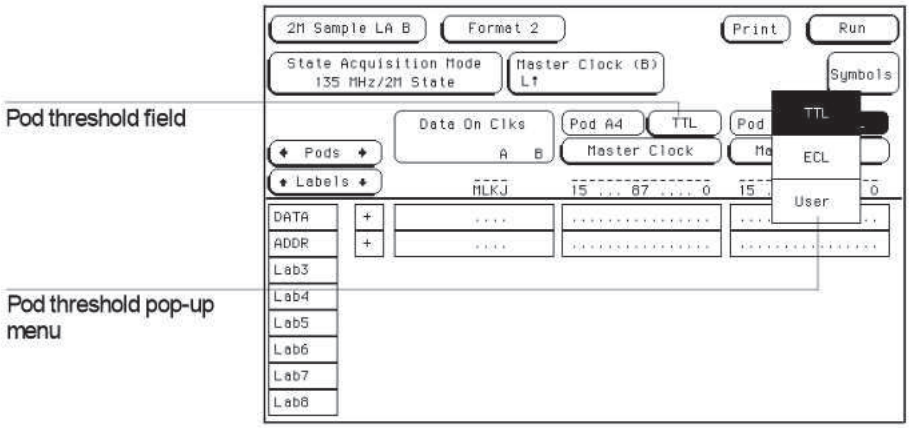
When TTL is selected as the threshold level, the data signals must reach +1.5 volts.

ECL

When ECL is selected as the threshold level, the data signals must reach –1.3 volts.

USER

When USER is selected as the threshold level, the data signals must reach a user selectable value between –6.0 volts to +6.0 volts.



Pod Threshold Field

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Master and Slave Clock Fields (State only)

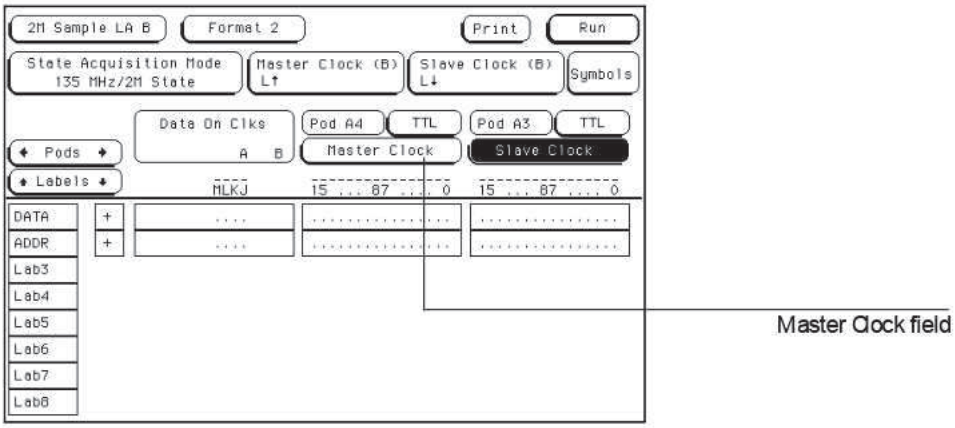
The Master and Slave Clock fields are used to construct a clocking arrangement. A clocking arrangement is the assignment of appropriate clocks, clock edges, and clock qualifier levels which allow the analyzer to synchronize itself on valid data.

When the Master or Slave Clock field is selected, a clock/qualifier selection menu appears showing the available clocks and qualifiers for a clocking arrangement. There are four clocks available (J, K, L, M), and four clock qualifiers available (Q1 through Q4).

A single-card module can use any of its four clocks as a state clock for specifying Master and Slave clocking arrangements. For a multi-card module, only the four clocks of the Clock Master board are available for use as state clocks. Any unassigned clocks may be used as data channels.

See Also

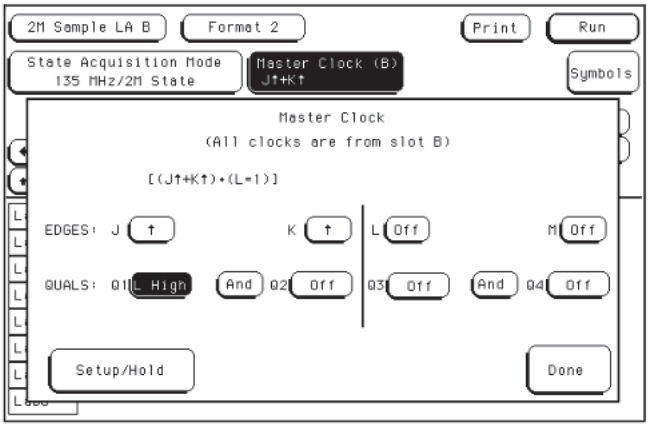
The "Pod Clock Field" earlier in this chapter for information on selecting clocking arrangement types such as Master, Slave, or Demultiplex.



Master Clock Field

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All combinations of the J and K clock and Q1 and Q2 qualifiers are ORed to the clock combinations of the L and M clocks and Q3 and Q4 qualifiers. Clock edges are ORed to clock edges, clock qualifiers are ANDed to clock edges, and clock qualifiers can be either ANDed or ORed together. The clock threshold level is the same as the level assigned in the Pod Threshold field.



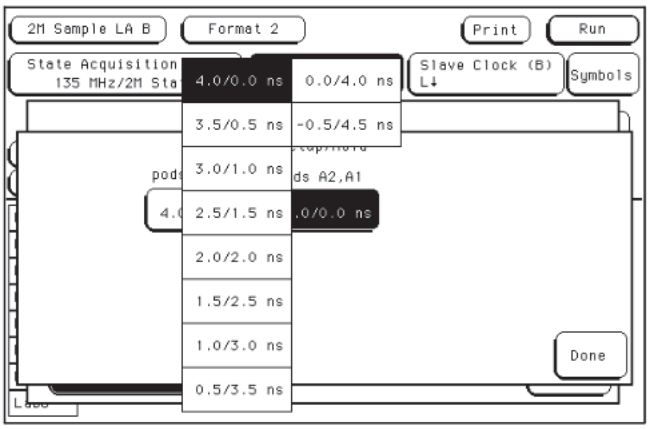
Clock Edges and Levels

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Setup/Hold Field (State only)

Setup/Hold adjusts the relative position (in time) of the clock edge with respect to the time period that data is valid. When the Setup/Hold field is selected, a configuration menu appears. Use this Setup/Hold configuration menu to select each pod in the analyzer and assign a Setup/Hold selection from the selection list.

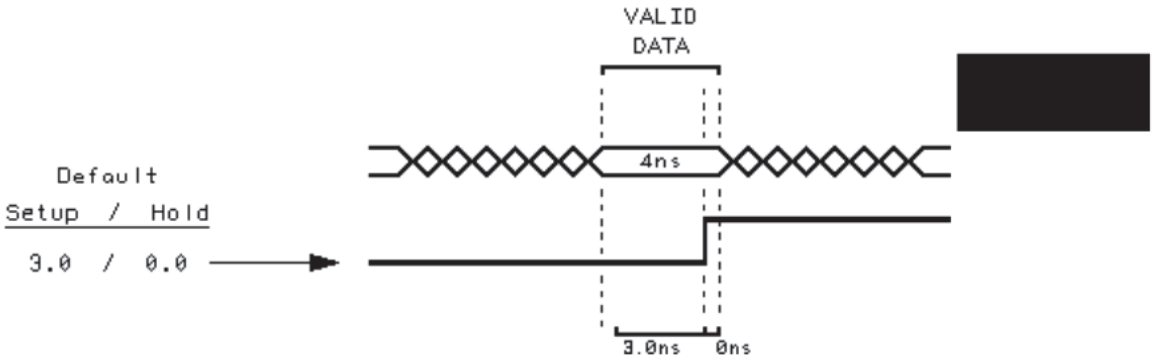
With a single clock edge assigned, the choices range from 3.0 ns Setup/0.0 ns Hold to -0.5 ns Setup/3.5 ns Hold. With both edges of a single clock assigned, the choices are from 3.5 ns Setup/0.0 ns Hold to -0.5 ns Setup/4.0 ns Hold. If the analyzer has multiple clock edges assigned, the choices range from 4.0 ns Setup/0.0 ns Hold to -0.5 ns Setup/4.5 ns Hold.



Setup and Hold Menu

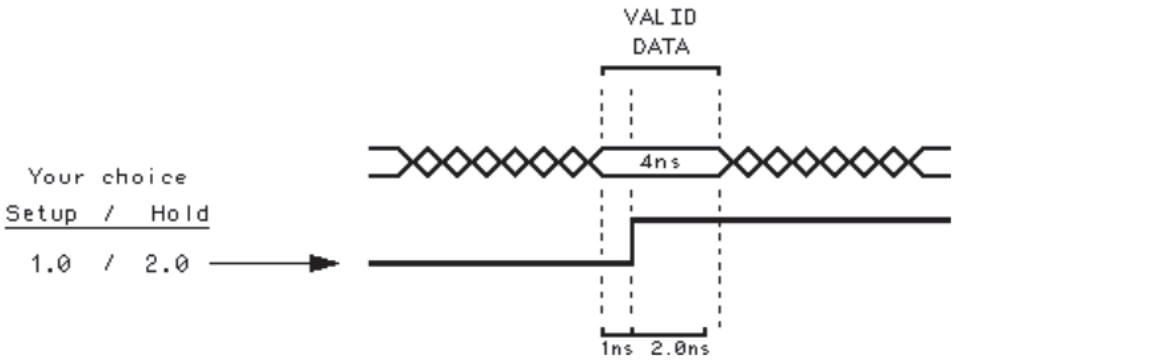
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The relationship of the clock signal and valid data under the default setup and hold is shown below.



Default Setup and Hold

If the relationship of the clock signal and valid data is such that the data is valid for 1 ns before the clock occurs and 3 ns after the clock occurs, you could use 1.0/2.0 or 0.5/2.5 or 0.0/3.0, but 0.5/2.5 would be the best choice.



Clock Position in Valid Data

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Symbols Field

See Also

Symbols Assignment in "Common Module Operations" in the Agilent Technologies 16500C User's Reference for complete information on using symbols.

Label Assignment Fields

See Also

Labels Assignment in "Common Module Operations" in the Agilent Technologies 16500C User's Reference for complete information on using labels.

Rolling Labels and Pods

The rolling function is the same for all items that are stored offscreen.

See Also

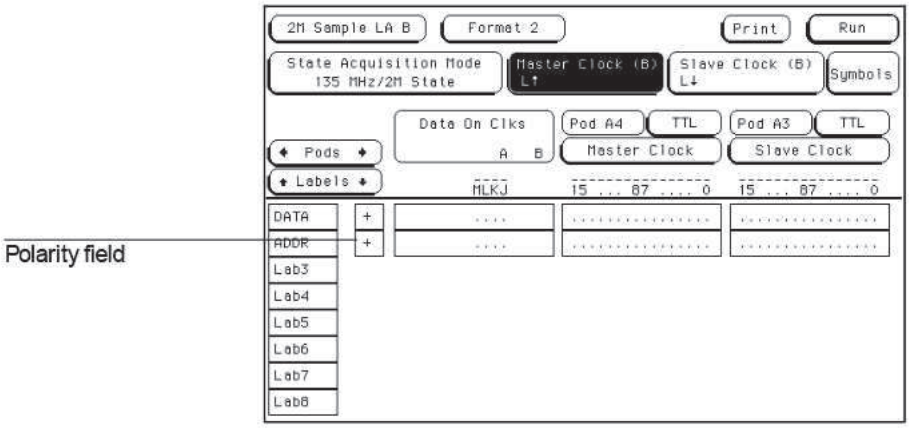
Labels Assignment in "Common Module Operations" in the Agilent Technologies 16500C User's Reference for complete information about rolling labels and pods.

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Label Polarity Fields

Use the Label Polarity fields to assign a polarity to each label. The default polarity for all labels is positive (+). Change the label polarity by touching the polarity field. This toggles between positive (+) and negative (–) polarity.

When the polarity is inverted, all data, as well as bit pattern specific configurations used for identifying, triggering, or storing data, reflect the change of polarity. In a timing analyzer with the data inverted, the waveform display does not change.



Polarity Field

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Bit Assignment Fields

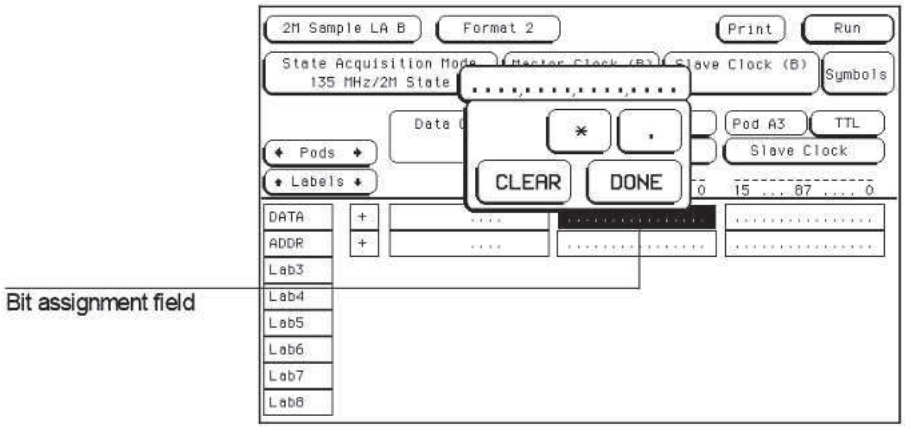
The bit assignment fields are used to assign bits (channels) to labels. The convention for bit assignment is as follows:

- * (asterisk) indicates an assigned bit.
- . (period) indicates an unassigned bit.

To change a bit assignment, select the bit assignment field and, using the knob, move the cursor to the bit you want to change, then select an asterisk or a period. When the bits are assigned as desired and you close the pop-up menu, the screen displays the new bit assignment.

See Also

"Activity Indicators" in chapter 3, "The Configuration Menu," for more information on the bit reference line and the activity indicators on the bit reference line.

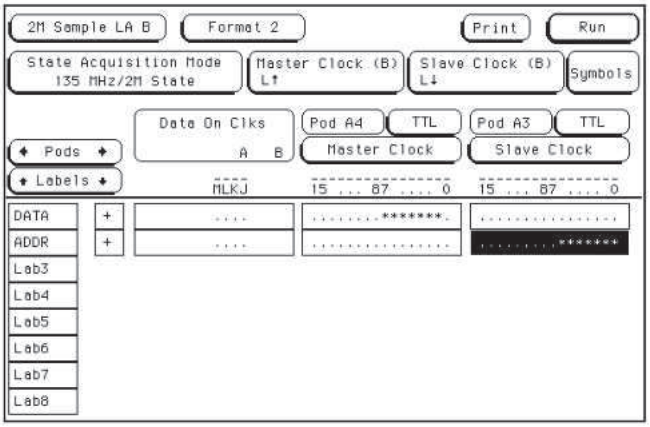


Bit Assignment Field

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Labels may have from 1 to 32 channels assigned to them. If you try to assign more than 32 channels to a label, the logic analyzer will beep and a message will appear at the top of the screen telling you that 32 channels per label is the maximum. Channels assigned to a label are numbered from right to left, with the least significant bit on the far right, numbered 0.

Although labels can contain split fields, assigned channels are always numbered consecutively within a label.



Bit Assignment Example

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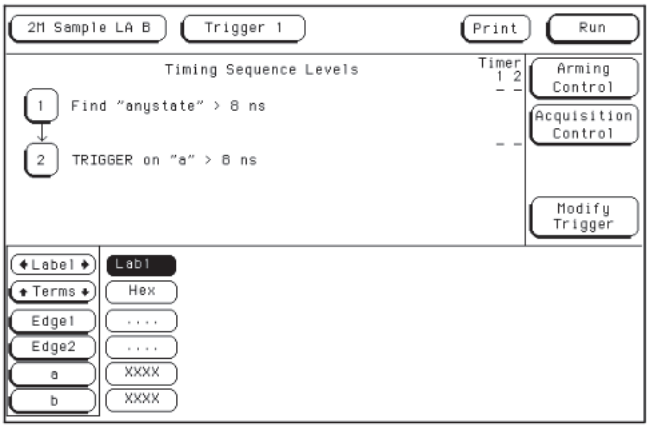
The Trigger Menu

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The Trigger Menu

The Trigger menu is used to specify when the analyzer triggers and what the analyzer stores in acquisition memory. The Trigger menu can be viewed as having four functionally different sections:

- Automatic Sequence Levels, located in the large light blue center box
- Manual Sequence Levels, also located in the large light blue center box
- Resource Terms, located at the bottom of the menu
- Control Fields, located at the right side of the display



The Trigger Menu

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Predefined Trigger Macros

The state and timing acquisition modes each have a macro library containing predefined trigger macros. Each macro will require at least one sequence level, and in some cases, several levels. Macros can be branched to by combining a user-defined level with a macro level. To use these predefined trigger macros, see "Using Macros to Create a Trigger Specification" on the next page. The macro libraries are as follows:

Timing Trigger Macro Library:

- User Mode (user-defined macro)
- Basic Macros
- Pattern/Edge Combination Macros
- Time Violation Macros
- Delay Macros

State Trigger Macro Library:

- User Mode (user-defined macro)
- Basic Macros
- Sequence Dependent Macros
- Time Violation Macros
- Delay Macros

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Using Macros to Create a Trigger Specification

1. From the Trigger menu, enter the desired sequence level by selecting the Modify Trigger field or by selecting a sequence level number.

See Also "Modify Trigger Field" for information on accessing levels.

2. From within the sequence level, select the Select New Macro field

3. Scroll to highlight the macro you want, then select the Done field.

4. Select the appropriate assignment fields and insert the desired predefined resource terms, numeric values, and other parameter fields required by the macro. Select the Done field.

See Also "Resource Terms" for information on using predefined resource terms.

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Timing Trigger Macro Library

The following list contains the macros in the Timing Trigger Macro Library. They are listed in the order in which they appear on the screen.

User Mode

User level - custom combinations, branching

The User level lets you manually design a sequence level. It uses one internal sequence level.

Basic Macros

1. Find anystate n times

This macro becomes true with the nth state it sees. It uses one internal sequence level.

2. Find pattern present/absent for > duration

This macro becomes true when it finds a pattern you have designated that has been present or absent for greater than or equal to the set duration. It uses one internal sequence level.

3. Find pattern present/absent for < duration

This macro becomes true when it finds a pattern you have designated that has been present or absent for less than the set duration. It uses four or five internal sequence levels.

4. Find edge

This macro becomes true when the edge you have designated is seen. It uses one internal sequence level.

5. Find Nth occurrence of an edge

This macro becomes true when it finds the occurrence of an edge you have designated. It uses one internal sequence level. The 500-MHz trigger sequencer may not count edges captured closer than 2 ns apart.

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Pattern/Edge Combinations

1. Find edge within a valid pattern

This macro becomes true when a selected edge type is seen within the time window defined by a pattern you have designated. It uses one internal sequence level.

2. Find pattern occurring too soon after edge

This macro becomes true when a pattern you have designated is seen occurring within a set duration after a selected edge type is seen. It uses three or four internal sequence levels.

3. Find pattern occurring too late after edge

This macro becomes true when one edge type you have selected occurs and, for a designated period after that first edge is seen, a pattern is not seen. It uses two internal sequence levels.

Time Violations

1. Find 2 edges too close together

This macro becomes true when a second selected edge is seen occurring within a period you have designated after the occurrence of a first selected edge. It uses three or four internal sequence levels.

2. Find 2 edges too far apart

This macro becomes true when a second selected edge occurs beyond a period you have designated after the first selected edge. It uses two internal sequence levels.

3. Find width violations on a pattern/pulse

This macro becomes true when the width of a pattern violates minimum and maximum width settings you have designated. It uses four or five internal sequence levels.

Delay

1. Wait t sec

This macro becomes true after a period you have designated has expired. It uses one internal sequence level.

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State Trigger Macro Library

The following list contains the macros in the State Trigger Macro Library. They are listed in the order in which they appear on the screen.

User Mode

User Level - custom combinations, loops

The User level lets you manually design a sequence level. It uses one internal sequence level.

Basic Macros

1. Find anystate n times

This macro becomes true with the nth state it sees. It uses one internal sequence level.

2. Find event n times

This macro becomes true when it sees an event you have specified occurring a designated number of times. The events may occur consecutively, but does not have to. It uses one internal sequence level.

3. Find event n consecutive times

This macro becomes true when it sees an event you have specified occurring a designated number of consecutive times. It uses one internal sequence level.

4. Find event2 immediately following event1

This macro becomes true when the first event you have specified is seen immediately followed by a second designated event. It uses two internal sequence levels.

Sequence Dependent Macros

1. Find event2 n times after event1, before event3 occurs

This macro becomes true when it first finds a designated event1, followed by a selected number of occurrences of a designated event2. In addition, if a designated event3 is seen anytime while the sequence is not yet true, the sequence starts over. If event2's nth occurrence is coincident with event3, the sequence starts over. It uses two internal sequence levels.

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2. Find too few states between event1 and event2

This macro becomes true when a designated event1 is seen, followed by a designated event2, and with less than a selected number of states occurring between the two events. It uses three or four internal sequence levels.

3. Find too many states between event1 and event2

This macro becomes true when a designated event1 is seen, followed by more than a selected number of states, before a designated event2. It uses two internal sequence levels.

4. Find n-bit serial pattern

This macro becomes true when a specified serial pattern of n bits is found.

Time Violations

1. Find event2 occurring too soon after event1

This macro becomes true when a designated event1 is seen, followed by a designated event2, and with less than a selected period occurring between the two events. It uses two internal sequence levels.

2. Find event2 occurring too late after event1

This macro becomes true when a designated event1 is seen, followed by at least a selected period, before a designated event2 occurs. It uses two internal sequence levels.

Delay

1. Wait n external clock states

This macro becomes true after a number of user clock states you have designated has occurred. It uses one internal sequence level.

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Sequence Levels

The Sequence Levels section controls when the analyzer triggers, what the analyzer triggers on, and what data is stored in memory before and after triggering occurs. By using sequence levels, you create a sequence of instructions for the analyzer to follow. The instructions contain user-defined resource terms representing such things as timers, ranges, edges, and bit patterns.

As the resource terms are evaluated and acted upon by the analyzer, all subsequent branching and storing within the sequence flow is directed by your instructions. The path taken resembles a flow chart, and the end result is the storage of only the data you need.

The state analyzer has 12 sequence levels available. The timing analyzer has 10 sequence levels available.

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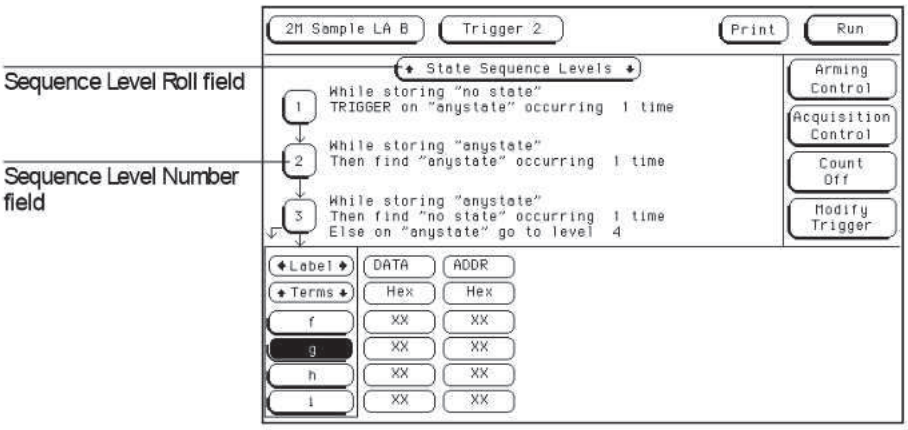
Sequence Level Number Field

The Sequence Level Number field identifies an instruction to be evaluated by the analyzer. In addition, use the number field to access the Sequence Instruction menu, which allows you to define the automated trigger macros and to manually construct sequence instructions.

The sequence instruction for each level is displayed in text and located just to the right of the level number. The timer status in each level is also displayed to the right of the instruction text.

Sequence Level Roll Field

The field rolls offscreen sequence levels back on screen by using the knob when the Sequence Levels field is light blue. If the field is dark blue, select it, turning it light blue.



Sequence Level Number

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Sequence Instruction Menu

When a Sequence Level Number field is selected, a Sequence Instruction menu appears. Use this menu to create instructions for the Sequence Level Number, to insert adjacent sequence levels, select a new macro, or to delete the current level. The instruction you create will read like a sentence, with the assigned resource terms directing how the analyzer qualifies and stores the desired data. This Sequence Instruction Menu contains the following fields to help you set up trigger conditions:

- Insert Level and Delete Level Fields
- Select New Macro field
- Term assignment fields
- Occurrence counter fields
- Branching fields
- Duration counter field (Timing only)
- Timer Control field

Insert Level and Delete Level Fields

The Insert Level field is used to add another sequence level. When this field is selected, depending on the analyzer configuration, you are given choices to add a field before or after the current sequence level. A message appears letting you know when all available sequence levels are inserted. The Delete Level field is used to delete a selected sequence level.

See Also "Resource Term Fields" later in this chapter for information on assigning a value to the Resource Terms.

Select New Macro Field

The Select New Macro field brings up a list of triggers that have been built with predefined macros. There are separate libraries of predefined triggers for State and Timing acquisition.

See Also "Predefined Trigger Macros" in this chapter for more information on predefined trigger macros.

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Term Assignment Fields

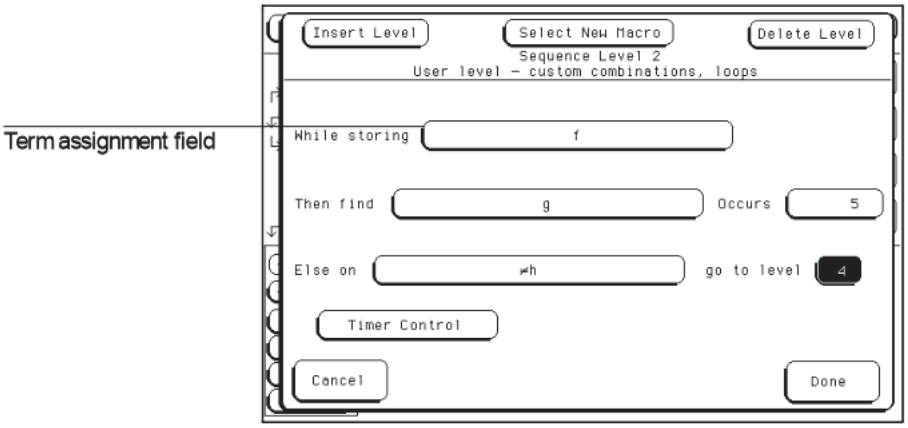
The Term Assignment fields hold user-defined bit patterns, ranges, timers, and logical combination resource terms. You can logically combine different resource terms to form the kind of instruction needed to qualify the trigger and store operations.

Occurrence Counter Field

The Occurrence Counter field indicates the number of times the analyzer must see the resource term before it is allowed to advance to the next sequence level. To assign an occurrence number, simply turn the knob, or select the Occurrence Counter field and use the keypad that appears. The maximum number of occurrences is 1048575. If the "Else on" term is seen before all specified occurrences have taken place, the flow of the sequence instruction goes to the sequence level designated in the Branching field.

See Also

For information on selecting resource term choices and how to assign a value to a resource term, refer to the term types, such as bit pattern, range, or timers in this chapter.



Occurrence Counter Field

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Branching Field

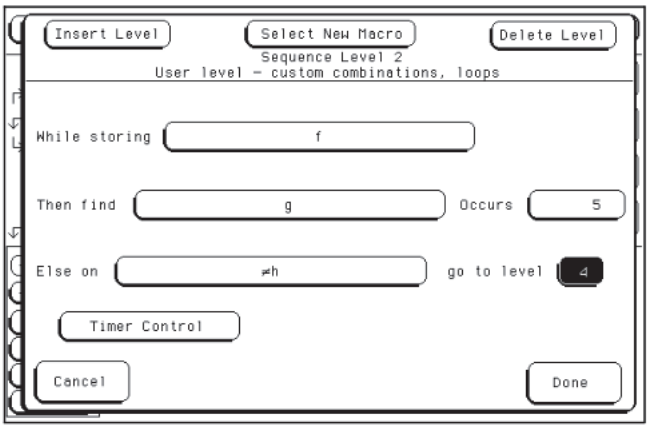
Each sequence level has two-way branching. If the first resource term is found, the branch is to the next sequence level. If the first resource term is not found, the analyzer evaluates the "Else on" secondary branching term.

If the "Else on" term is found, the secondary branch taken is to the designated sequence level in the Branching field. If the "Else on" term is not found, the analyzer continues to loop within the sequence level until one of the two branches is found. If the "Else on" branch is taken, the occurrence counter is reset even if the "go to level" branch is to the same level.

If both terms are found at the same time, the branch is to the next sequence level after the required number of first term occurrences.

Branching across trigger levels is possible. If this occurs, the sequence level evaluation could loop without ever seeing a trigger term. Take care in designing your flowchart and constructing the sequence instructions to avoid this possibility.

To set a sequence level branch, select the Branching field, then select a destination sequence level number.



Branching in a Sequence Instruction

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Duration Counter Field (Timing only)

The Duration Counter field displays a user-definable period for which the resource term must be valid before the analyzer continues with the sequence evaluation.

> Field When the greater-than sign(>) precedes the Duration Counter field, the analyzer continues sequence level evaluation only after the resource term has been true for a period greater than or equal to the duration specified.

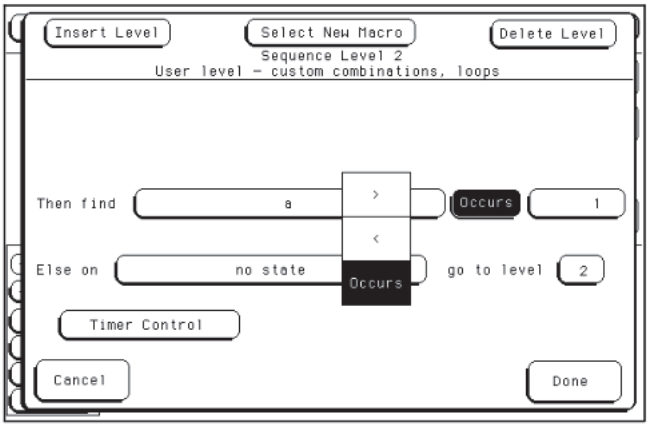
< Field When the less-than sign (<) precedes the Duration Counter field, the analyzer continues sequence level evaluation only after the resource term has been true for a period less than or equal to the duration specified. Each less-than assignment (<) uses three sequence levels.

When < or > duration is assigned, the secondary branching (Else on) is not available. To assign a duration, simply turn the knob, or select the Duration Counter field and use the keypad that appears.

Occurs Field When "Occurs" is selected, the Duration Counter field changes to an occurrence counter, and the sequence evaluation is delayed until the resource term has occurred for the number of occurrences selected. To assign an occurrence number, simply turn the knob, or select the occurrence field and use the keypad that appears. The maximum number of occurrences is 1048575.

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When the "Occurs" selection is made, the "Else on" resource term (secondary branch) becomes available for a second branching option. If the first resource term (primary branch) is not found, and the second resource term is found, the analyzer branches to the sequence level designated in the Branching field.

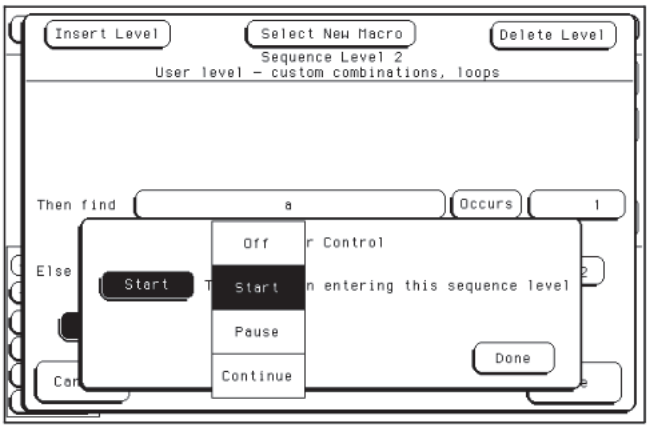


Sequence Level Instruction

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Timer Control Field

The Timer Control field is used to access the Timer Control menu. Use the Timer Control menu to Start, Stop, Pause, or Continue timer operation as the analyzer enters a sequence level. You can control the same timer from each sequence level. The default timer condition in all sequence levels is Off.



Timer Control Menu

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Resource Terms

Resource terms are the user-defined variables that you can place in the Term Assignment fields of the sequence instructions. Resource terms can take the form of bit patterns, ranges, timers, or edge terms. They are used separately or in logical combinations with other terms. The analyzer evaluates the sequence instruction and resource terms and determines if the instruction is true or false. Depending on a true or false evaluation, the appropriate branching direction occurs. The terms and fields are:

- Resource Term Fields
- Bit Pattern Terms
- Range Terms
- Timer Terms
- Edge Terms (Timing only)
- Combination of Terms

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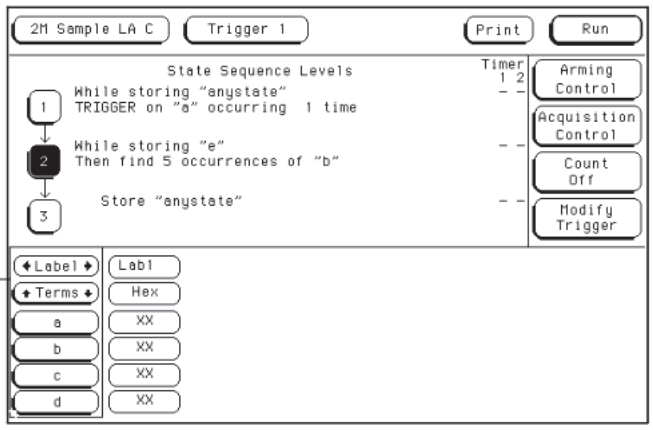
Resource Term Fields

The Resource Term fields identify the terms available for use within the analyzer. The Resource Term fields are also used to access the Resource Term Configuration menu.

Just to the right of the Resource Term fields are the corresponding assignment fields which display the assigned values and are also used to access an assignment keypad.

Resource Terms Roll Field

Offscreen resource terms are rolled back onscreen by using the knob when the Terms field is light blue. If the Terms field is dark blue, it must be selected, which then turns it light blue.



Resource Term Fields

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Resource Term Configuration Menu

When any of the Resource Term fields are selected, a Resource Terms Configuration menu appears. Use this configuration menu to assign a resource term to an analyzer, set the resource term to a value, or customize the name of a resource term. The following functions can also be accomplished by selecting the assignment field and using the pop-up keypad.

Clear (=X) Sets the Term Assignment fields as follows:

In Terms a – j, the assignment field is set to all Xs (don't cares).

In Range 1 and 2 terms, the two assignment fields are set to maximum (Fs) and minimum (0s) settings.

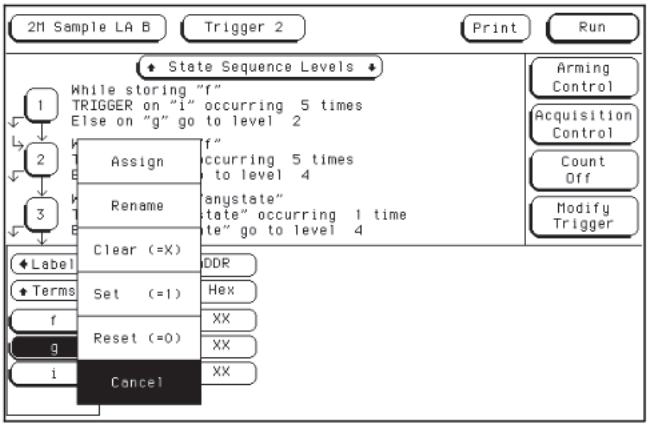
In Timer 1 and 2 terms, the assignment field is reset to a minimum time of 400 ns.

In Edge 1 and 2 terms, the assignment field is reset to a period (.).

Set (=1) Sets the Term Assignment fields as follows:

In Terms a – j, the assignment field is set to all 1s (highs).

This option is not available for the two Range, Timer, and Edge terms.



Resource Terms Configuration Menu

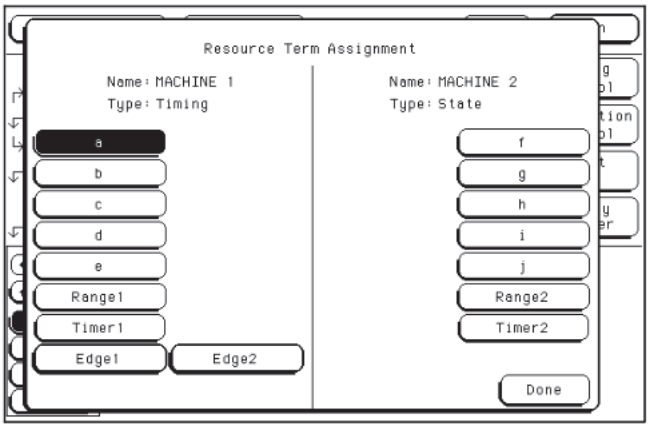
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Reset (=0) Sets the assignment fields as follows:

In Terms a – j, the assignment field is set to all 0s (lows). This option is not available for the two Range, Timer, and Edge terms.

Rename This function accesses a keypad that you use to create a custom name for the resource term. This function works for all resource terms.

Assign All of the available resource terms except Edge terms can be assigned to any analyzer. The Edge terms are only used in a timing analyzer. A term, however, can be assigned to only one analyzer at a time. When a resource term is selected, it toggles between analyzers.



Resource Term Assignment Menu

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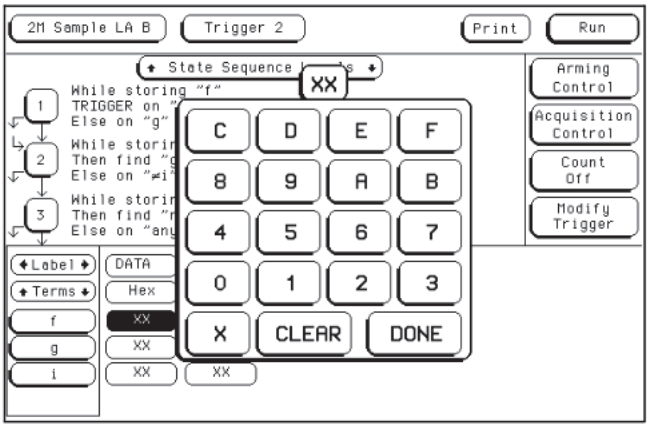
Bit Pattern Terms

Bit Pattern terms are set to match the numeric value or bit pattern of a group of data channels. The ten available Bit Pattern terms are "a" through " j." Each term can be assigned to either of the two analyzers, but not both. The complement of the bit patterns you specify for "a" through "j" are available by selecting "≠a" through "≠j."

Bit Pattern Assignment

The assignment of a bit pattern to the resource terms "a" through "j" can be done in two ways. If you want a pattern of all 1s, all 0s, or all Xs (don't cares), you can insert these values by selecting the resource term field itself, then select your choice from the Resource Term Configuration menu.

If you want some other pattern, use the pop-up keypad to assign the bit pattern. The keypad becomes available when you select the assignment field for each term.

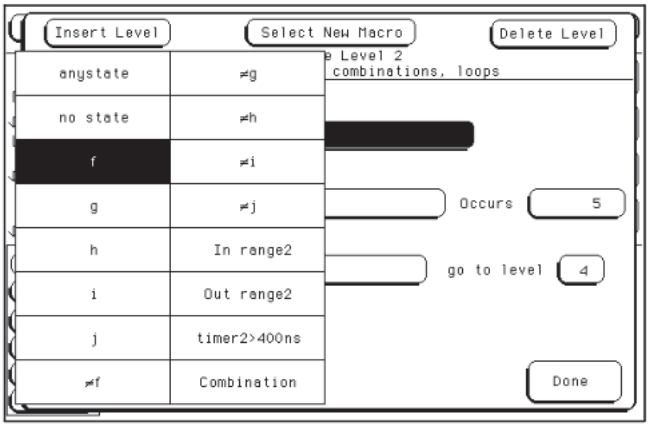


Bit Pattern Resource Term

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Bit Pattern Selection

After the resource terms have values assigned, they are inserted into the sequence instruction where they direct the flow of that sequence instruction. Insert Bit Pattern terms into a sequence instruction by selecting the Term Assignment field, then selecting a term "a" through "j" from the pop-up selection list.



Bit Pattern Term Selection

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Range Terms

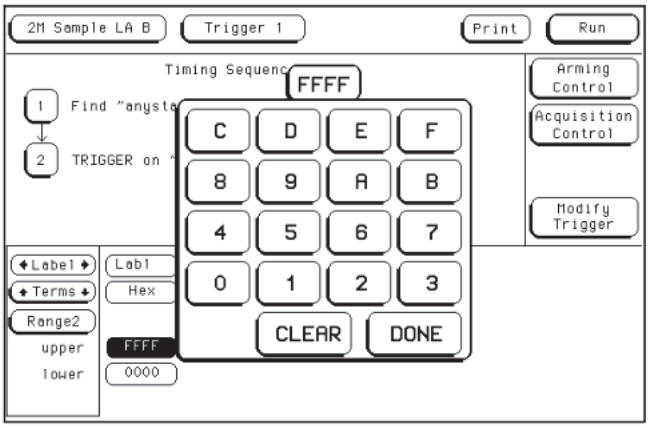
Range terms bracket groups of bit patterns. There are two available Range terms. Each Range term is assigned to either of the two analyzers, but not both.

When you assign an upper and lower bit pattern boundary, the range is recognized when the data is numerically between or on the two specified boundaries. In addition, the range must be contained in a single pod pair, with no clock bits allowed.

Range Assignment

To assign bit patterns to the upper and lower boundaries of a Range term, you use a pop-up keypad. The keypad appears when you select the upper or lower Range term assignment fields.

You can clear the range boundaries by setting them to all Xs (don't cares) by selecting the Range term field and selecting the Clear (=X) field from the Resource Term Configuration menu. The Clear (=X) option places zeros and Fs in the upper and lower boundaries respectively.



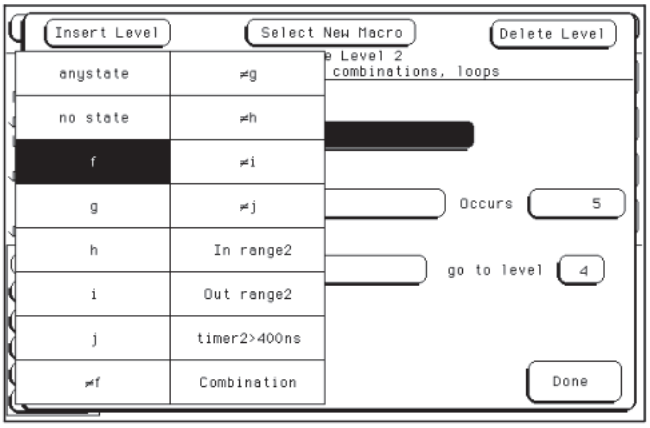
Range Term

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Range Term Selection

With upper and lower range boundaries assigned, insert the appropriate In range or Out range terms into the sequence instruction. The In range term is true when the analyzer recognizes a bit pattern on or between the assigned range boundaries. The Out range term is true when the In range term is false.

In and Out range terms are inserted into a sequence instruction by selecting the Term Assignment field, then selecting an "In range 1, 2" or "Out range 1, 2" term from the pop-up selection list.



Range Term Selection

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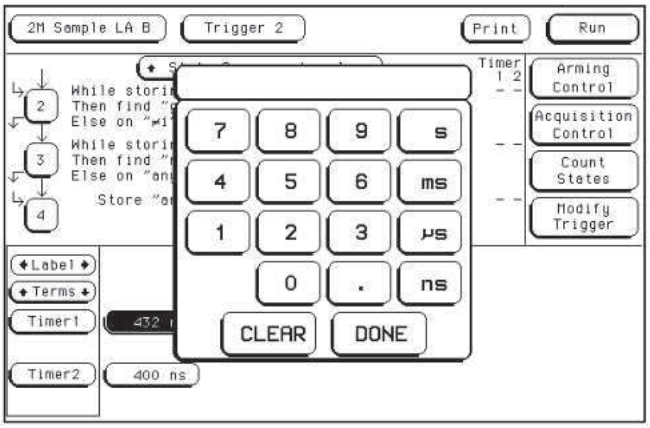
Timer Terms

There are two available Timer terms, each of which may be assigned to either of the two analyzers, but not both. Timers can be used as either the trigger term, the store term, or a branching term, within a sequence level. With timers inserted into sequence levels, you can start a timer in one level, pause it, or stop it in another sequence level.

As with other resource terms, timers are either true or false. Timers start as you enter the sequence level, and when its count expires, it becomes true. If a timer is paused in one level, it must be continued in another level before it can count through and become true. Timers can also be inverted, so a timer can start as true and become false when its count expires.

Timer Assignment

To assign a time value to the Timer 1, 2 terms, you use a pop-up keypad which appears when you select the assignment field.



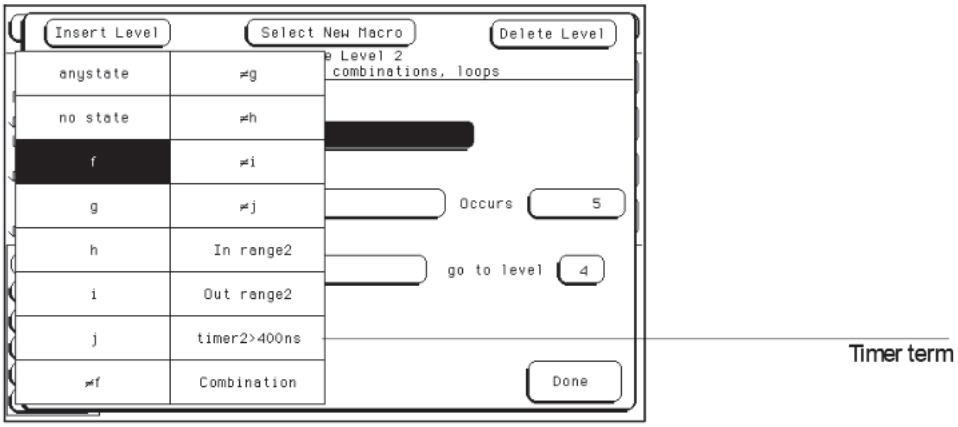
Timer Term Assignment

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The minimum value a timer can have is 400 ns, and that is the default value. As more sequence levels are added, the timer status in the new levels defaults to Off. Timers must be continued or started in each new level as is appropriate. When a timer expires or stops, its count resets to zero.

Timer Term Selection

Timer terms are inserted into a sequence instruction by selecting the Term Assignment field, then selecting a "Timer 1, 2" term from the pop-up selection list.



Timer Term Selection

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Edge Terms (Timing only)

Edges and glitches can be used to qualify a trigger, store, or branch operation within a sequence instruction. They can be used singularly or in combination with each other across all assigned channels. When you specify an edge or glitch on more than one channel, the analyzer ORs the edges and glitches. If you want to qualify a glitch, place an asterisk (*) on the data channel you are watching. If you want to qualify an edge, place the appropriate edge on the data channel you are watching. The following edge choices are available:

Positive edge (↑)

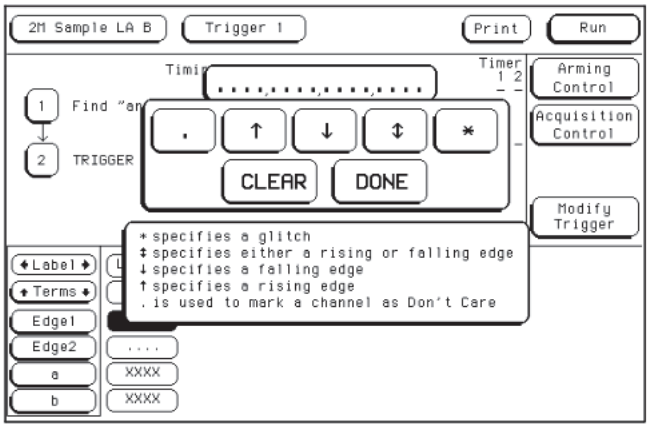
Negative edge (↓)

Either positive or negative (·)

No edge (.)

Edge Assignment

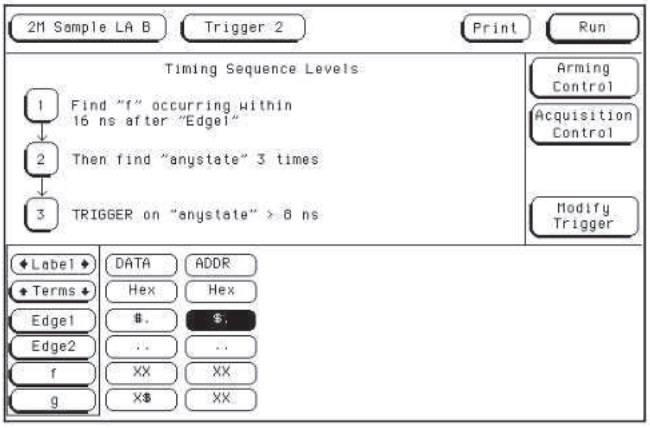
After you select the edge assignment field, an assignment menu appears. Use the knob to position the cursor over the bit you want to qualify, then select the glitch or edge choice.



Edge Term

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When you finish assigning edges and glitches, select Done. After the assignment menu closes, you will see "$" or "*" or both indicators in the assignment field display. These symbols signify an assigned edge ($) or glitch (*) qualifier. When Binary is selected for the numeric base, you see the actual edge and glitch assignments.



Edge and Glitch Identifiers

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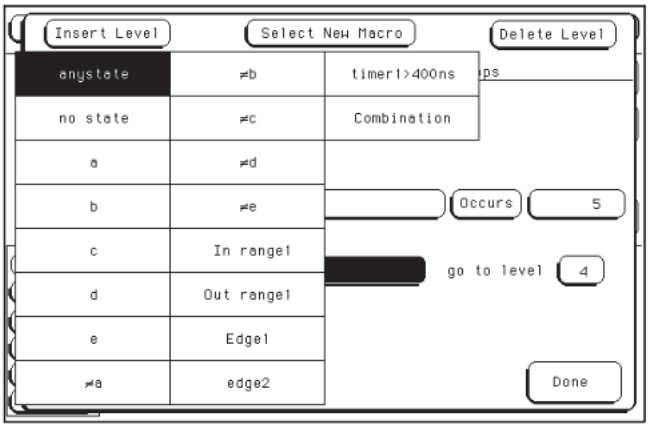
Combination of Terms

The Combination selection in the pop-up selection list allows you to create a resource term with a value that is the result of a combination process. The combination process uses the logical AND, NAND, OR, NOR, and XOR functions to combine predefined resource terms. All resource terms that have been assigned to the analyzer are available to influence the value of the combination resource term.

A combination of terms is used as either a trigger term, a store term, or a branching term within a sequence instruction.

Combination Assignment

To assign a combination of terms, first select "Combination" from the pop-up selection list, and then configure the process that creates the value for the combination.



Combination of Terms

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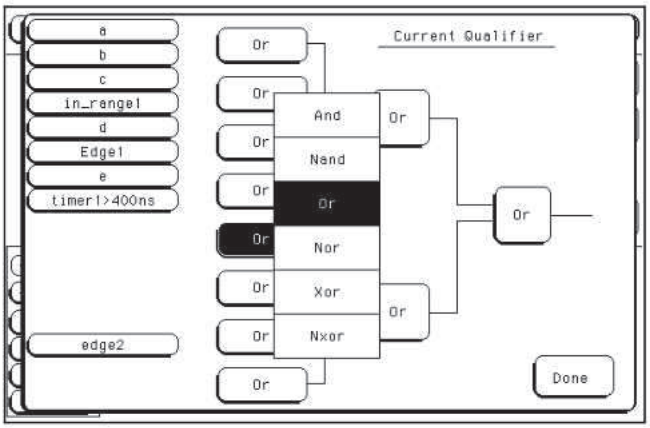
Combination Creation

Before a combination of terms is created and inserted into a sequence instruction, the combination process must be configured. When the Term Assignment field is selected, and "Combination" is selected from the pop-up selection list, a Logical Assignment menu appears. Use this menu to select predefined resource terms as inputs to a chain of logical operators.

Configure resource terms into the chain by selecting the desired term, then selecting to either include it (ON), turn it off, or include it in a complemented form (NEGATE).

Configure logical operators into the chain by selecting the Logical Operation field, and then selecting the desired operation from a selection list.

When the configuration process is complete, and the "Done" field is selected, the created Combination of terms is inserted into the Term Assignment field in the sequence instruction.



Logical Assignment Menu

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The Control fields are located to the right of the large light blue Sequence Levels box. The four control fields are:

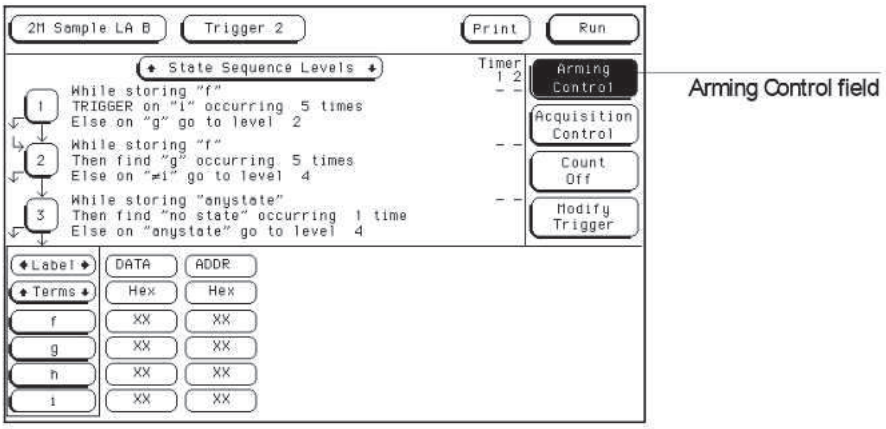
- Arming Control Field
- Count Field (State and State Compare only)
- Acquisition Control Field
- Modify Trigger Field

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Arming Control Field

The Arming Control field accesses an Arming Control menu which is used to configure the arm signals between analyzers and the Arm In/Out signals between other measurement modules in the mainframe. The arming signals influence the order in which the analyzers and other measurement modules trigger in cross-domain measurements. The three types of arming control are:

- Arming Control Between Analyzers
- Arming Control Between Modules
- OR'd Trigger



Arming Control Field

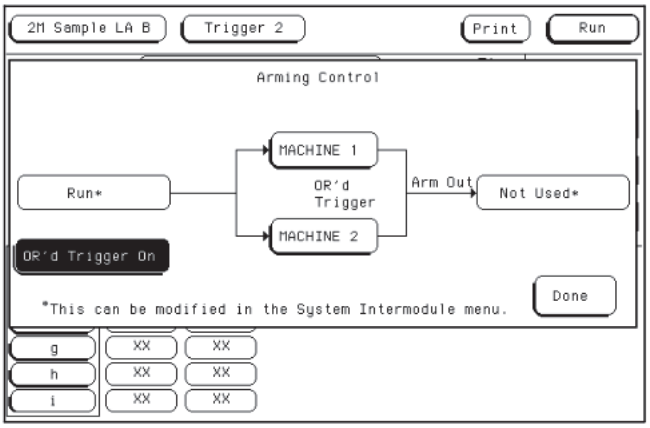
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Arming Control Between Analyzers

If both analyzers in a module are turned on, you can configure one analyzer to arm the other. For example, when a state analyzer triggers on a bit pattern, it could arm a timing analyzer which then captures and displays the waveform after it triggers. As you configure the Arming Control menu, a graphical representation of the analyzer arming configuration is displayed.

When you select the analyzer name field in the Arming Control menu, a pop-up menu appears that you use to select where the Arm In signal comes from. In addition, a sequence level number field appears which you use to select the sequence level in which an "arm" flag is placed.

When an analyzer receives an Arm-In signal, an "arm" term is placed in a user-selected sequence level and the analyzer automatically begins evaluating its trigger sequence instruction. If in the sequence evaluation, the "arm" term is seen first, the analyzer will trigger. However, if the "arm" term is placed down in the sequence level order, the preceding sequencing could trigger the analyzer before the "arm" term is seen. Generally, the "arm" term is evaluated and used in the same way as the other resource terms within the sequence instruction.



Two Analyzer Arming

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Arming Control Between Modules

A more complex arming example involves arming between modules in the mainframe. Intermodule arming requires using the Intermodule menu to configure all the modules involved. As you configure the Arming Control menu, a graphical representation of the analyzer arming configuration is displayed.

The first analyzer is armed by an Arm-In signal from another module in the mainframe. After the first analyzer triggers, it arms the second analyzer. After the second analyzer triggers, it can send a Port-Out signal to the Port-Out BNC on the back panel of the mainframe. This signal can be used to arm an external measurement module, such as an oscilloscope.

ORed Trigger

The ORed trigger allows you to configure two machines to trigger on completely different sets of data and allow either to trigger the other machine to capture data. Let's assume, for example, you have a system with two microprocessors. The system is having problems, and you aren't sure which microprocessor is causing the problem. You can connect one machine to microprocessor 1 and the other machine to microprocessor 2. When one of the microprocessors sees the problem, it will trigger the other, so you have captured parallel data for both machines. This data is time correlated to help you determine the cause of the problem.

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Count Field (State and State Compare only)

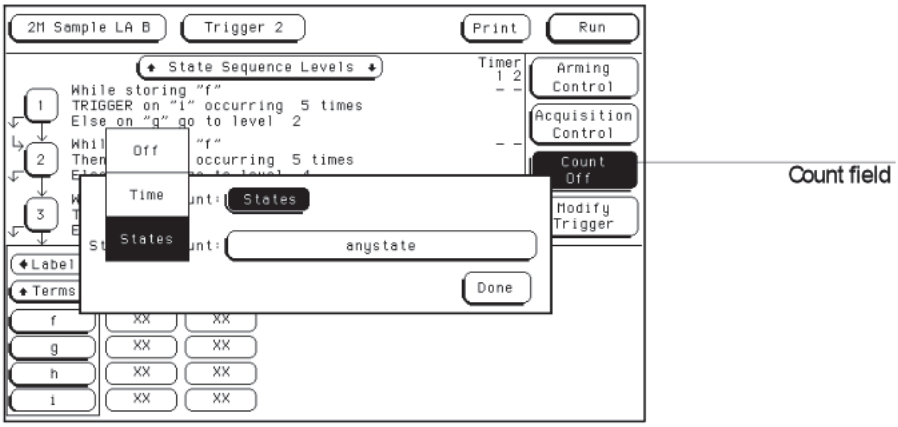
The Count field accesses a selection menu which stamps the acquisition data at each memory location with either a Time tag or a State tag. If you have all pod pairs assigned, the state acquisition memory is reduced by half when time or state tags are turned on. You can maintain full memory depth if you leave a pod pair unassigned. This section discusses:

- State Tags
- Time Tags
- Memory Depth Considerations

State Tags

If you select Count States, each time the system stores a data record it counts the number of occurrences of a particular combination of states that you specify, until a new data record is stored. The system then stores the count, or "state tag," along with the new data record, and the process repeats. When the measurement is completed, each piece of stored data is displayed with its associated "state tag" count.

State tags displayed this way are RELATIVE to the previous count, or they can be displayed as ABSOLUTE, indicating cumulative counts relative to the trigger point.



Count Field

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Time Tags

If you select Count Time, the system places a time stamp on all displayed data. Time tag values can be displayed as either relative to the previous memory location or absolute from the trigger point. When viewing absolute time tags, data stored before the trigger has negative values and data stored after the trigger has positive values. Select Absolute or Relative by toggling the Absolute/Relative field.

Time tag resolution is 8 ns. If the target system's state clock rate is less than 8 ns (that is, greater than 125 MHz), the time-tagger hardware will occasionally assign two adjacent states with the same absolute time tag value. When two states with the same absolute time-tag value are detected, the second state's time-tag value will be adjusted by 4 ns so that absolute time tags are not displayed as identical. Relative time tags will show a 4 ns offset relative to the previous state.

Memory Depth Considerations

If you have all pod pairs assigned, the state acquisition memory is reduced by half when time or state tags are turned on. To retain the full memory depth when using time or state tags, you must have at least one unassigned pod pair.

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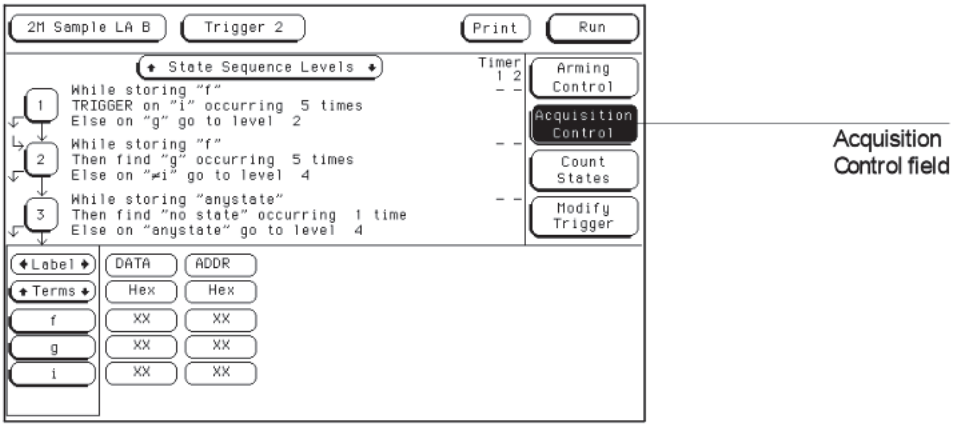
Acquisition Control Field

The Acquisition Control field accesses an Acquisition Control menu from which you can set the acquisition mode and trigger position within available memory. In a state analyzer you can set whether or not the data that causes a branch to be taken is stored into memory. In a timing analyzer, you can set the sample period.

In a state analyzer, the acquisition control settings are imposed on the qualified data after the trigger has occurred. Depending on what data is qualified in the sequence levels and when the trigger occurred, the additional data qualifying by the acquisition control will result in more efficient use of available memory.

Five control fields accessed are from the acquisition control menu:

- Acquisition Mode Field
- Trigger Position Field
- Memory Length Field
- Reference Clock Field
- Sample Period (Timing only) or Branches Taken (State and State Compare)



Acquisition Control field

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Acquisition Mode Field

The Acquisition Mode field toggles between Automatic and Manual. When set to Automatic in a state analyzer, the trigger position is computed based on the sequence specification. In a timing analyzer, the trigger position and sample period are computed based on the sec/Div and delay settings in the Waveform menu.

When the Acquisition Mode field is set to Manual, additional configuration fields become available. Use these fields to further qualify what data is stored. The additional configuration fields work together with the sequence instructions, in a prioritized manner, to position the trigger point relative to the beginning and end of stored data.

Trigger Position Field

In a state analyzer, the trigger point position is determined after the sequence instructions are evaluated. This process could result in a varying portion of available memory being filled with post-trigger data. The remainder of memory is considered free and is filled with less significant data.

In a timing analyzer, after the specified trigger term is found, memory is filled with post-trigger data starting at the trigger position represented by a blue graphic bar with the "Trig" indicator line. If the trigger position is set to store pre-trigger data, any true sequence instruction or trigger seen is ignored until the proper amount of pre-trigger data has been stored.

The Trigger Position field accesses a selection of options:

- Start
- Center
- End
- User Defined
- Delay

Start When the trigger position is set to Start, it places the trigger near the beginning of memory and most of the data in memory is post-trigger data.

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Center When the trigger position is set to Center, the trigger is placed at the middle of memory and half of the data is pre-trigger data and half is post-trigger data.

End When the trigger position is set to End, the trigger is placed near the end of memory and most of the data in memory is pre-trigger data.

User Defined When the trigger position is set to User Defined, a Post Store field appears which shows what the percentage of the data captured will be post-trigger data. Use this field to set the trigger position between 0% and 100%.

Delay In a timing analyzer, a Delay option is available. Use the Delay field to delay the start of acquisition storage after the trigger. The range of the delay is affected by the sample period but can range between 16 ns to 8 ks. There may be a variable number of stored samples displayed prior to the user-defined delayed start point for acquisition storage.

Memory Length Field

The memory length field lets you specify how much data you want to acquire. Large traces are useful for hunting for trends, but take longer to analyze. Short, focused traces are easier to search through. The exact values available in the Memory Length field depend upon the analyzer configuration. You can change the value using the knob on the Agilent Technologies 16500C, or by selecting the field and entering a value. If the entry is not a currently available option, the nearest valid size will be used.

Reference Clock Field



The Reference Clock field lets you specify whether you want to use the internal clock provided on the module, or an external clock. If you select the external clock, you must connect a clock signal to the module via the Reference Clock In/Out ports on the back of the analyzer.

Caution

Do not exceed 1 V, peak-to-peak, at a maximum voltage offset of 20 V on the Reference Clock In/Out ports.

The Reference Clock is provided so that you can have several modules running off the same clock. Running individual modules off the same Reference Clock prevents data skew, which could cause slight discrepancies between large data sets. The default clock is internal.

See Also

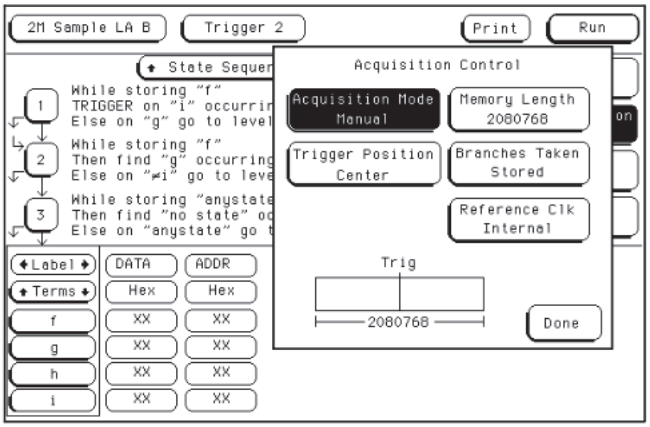
"Connecting the External Reference Clock" in Chapter 2, "Probing."

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Branches Taken Stored / Not Stored

The Branches Taken field is a toggle field which tells the analyzer to store or not to store the resource term that caused the analyzer to branch.

As the analyzer steps through the sequence instructions, it may repeatedly branch to secondary branches because the first resource term was bypassed (false) and the second "Else" resource term is qualified (true). With Branches Taken set to Stored, the state data values that caused the secondary branches are stored in memory.

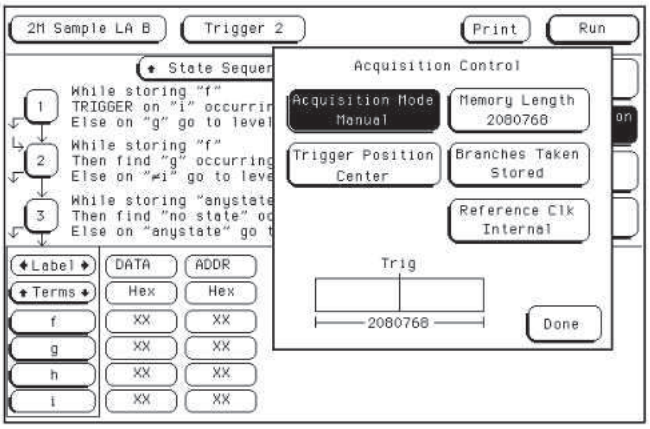


Acquisition Control Selection Menu (State Analyzer)

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Sample Period Field

The Sample Period field is used to set the time period between data samples. Every time a new sample is taken, the analyzer will see updated measurement data.

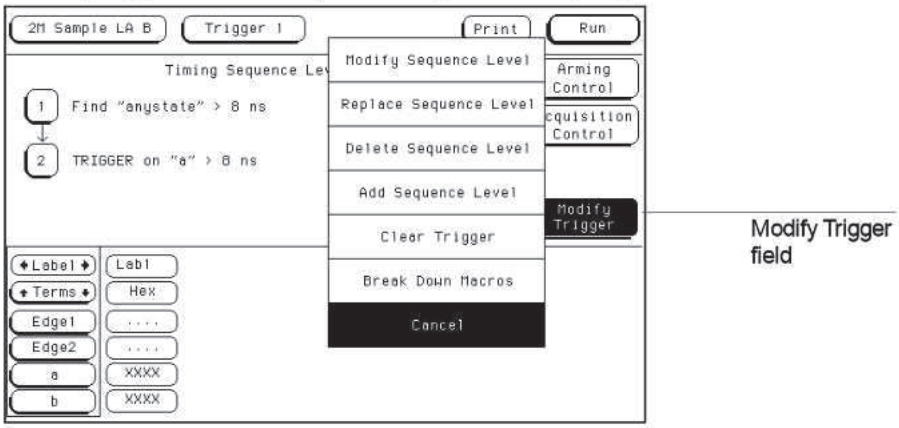


Acquisition Control Menu (Timing Analyzer)

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Modify Trigger Field

The Modify Trigger field allows you to modify the statements of any single sequence level as well as other high level actions like global clearing of existing trigger statements, and adding or deleting sequence levels.



Modify Trigger

Modify Sequence Level

If there is more than one sequence level assigned, you are asked which level to modify. Once in the desired sequence level, make all appropriate resource changes, then select Done.

Replace Sequence Level

If there is more than one sequence level assigned, you are asked which level to replace. When you replace a level, you pick a new macro to replace the old one. You then assign the appropriate resource in the new level.

Break Down Macros / Restore Macros

When a pre-defined macro is broken down, the contents of that macro are displayed in the same long form used in the User-level macro. If the macro uses multiple internal levels, all levels are separated out and displayed in the sequence level area of the Trigger menu. Once the macros in your trigger specification are broken down, the Break Down Macros field changes to Restore Macros. Use the Restore Macros field to restore all macros to their original structure.

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While in a broken down form, you can change the structure. However, when the macros are restored, all changes are lost and any branching that is part of the original structure is restored.

Use the Break Down Macros if you want to view a particular macro part in its long form to see exactly what flow the sequencer is following. It can also be used as an aid in creating a custom trigger specification. In this application, you would start with a pre-defined macro, break it down, then customize the long form to meet your needs.

When a macro is broken down, you have all the assignment fields and branching options available as if you have configured a User-level macro.

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The Listing Menu

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The Listing Menu

The Listing menu allows you to display data stored to memory during state or timing analyzer measurements. The acquired data is displayed in the order the analyzer placed the data into analyzer memory and is grouped by label and in a selectable numeric base. Labeled data from other analyzer machines can be interleaved into the same display. You can access three kinds of markers:

- Pattern Markers
- Time Markers
- Statistics Markers

See Also

"Interleaving State Listings" in chapter 10, The Mixed Display Menu, for more information on interleaving state data.

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Markers Field

The Markers field is used to access the markers selection menu. When this field is selected, a marker selection menu appears with the choices available for the present analyzer configuration.

State Analyzer Types

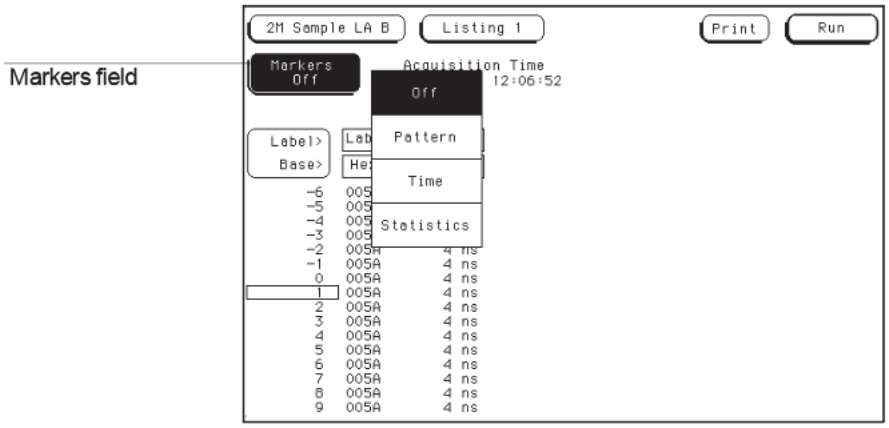
In a state analyzer with time and state count turned off in the Trigger menu, only Pattern markers are available. With time count turned on, choices of Pattern, Time, and Statistics markers become available. With States count turned on, Pattern and States markers are available.

Timing Analyzer Types

In a timing analyzer you have marker choices of Pattern, Time, and Statistics.

Off

The Off selection turns marker operations off. If a Stop measurement was previously specified, and the Stop measurement criteria are met, the measurement will stop even though the markers are off.



Markers Field

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When Pattern markers are selected, two markers labeled X and O become available. These markers are used to identify and mark unique bit patterns in the data listing. Once the unique bit patterns are marked, they can be used as reference points or as criteria for a stop measurement.

The markers are color coded for easy recognition in the data listing. The X marker is represented by a horizontal green line and the O marker is represented by a horizontal yellow line.

When a marker is positioned in the Listing menu, it is also positioned in the Waveform menu.

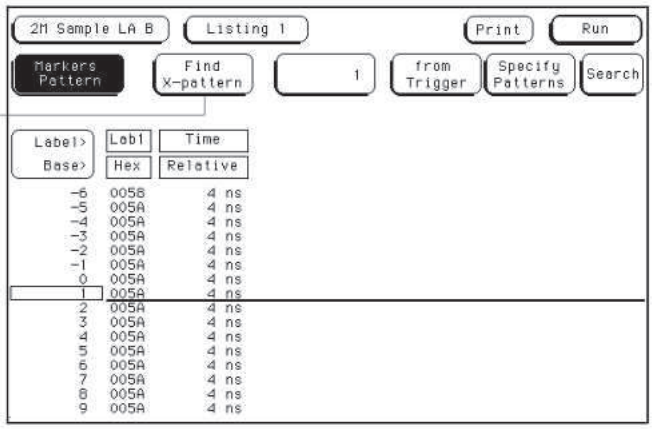
The fields associated with Pattern Markers are:

- Find X-pattern / O-pattern Field
- Pattern Occurrence Fields
- From Trigger / Start / X Marker Field
- Specify Patterns Field
- Label / Base Roll Field
- Stop Measurement Field
- Clear Pattern Field

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Find X-pattern / O-pattern Field

The Find X-pattern / O-pattern field is a toggle field. When selected, the target of occurrence and trace start field assignments switches to the other marker. In addition, when this field is selected, the data listing will shift so the data marker will appear at center screen.



Find X-pattern / O-pattern Field

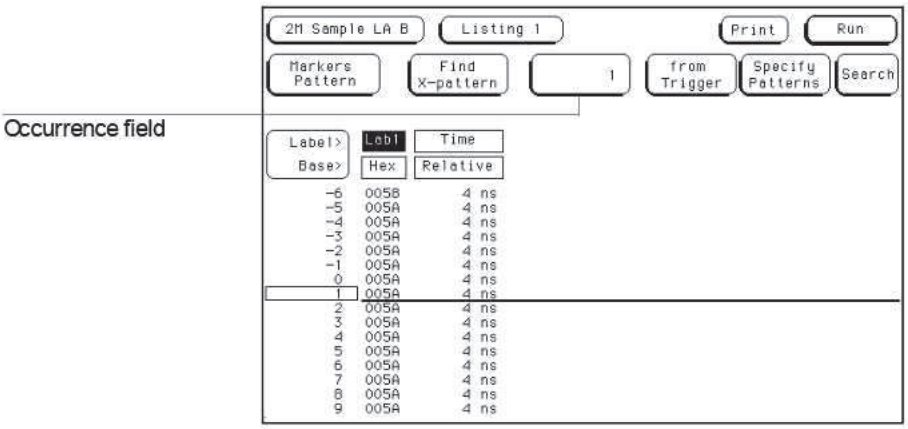
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Pattern Occurrence Fields

The X-pattern and O-pattern occurrence fields designate which pattern occurrence the marker is placed on. The range for the occurrence counter is set by the number of samples acquired.

The occurrence field can be set in two ways. When the field is selected one time, it turns light blue and knob operation becomes the entry method. If the field is selected a second time, a pop-up keypad appears and becomes the entry method.

The reference point from which the occurrence counter starts is either the trigger point, the start of the trace, or in the case of the O marker, the X marker. This is set in the From Trigger/Start/Marker field (see next page). If a negative occurrence number is set, the analyzer will search for pre-trigger occurrences.



X-pattern and O-pattern Occurrence Fields

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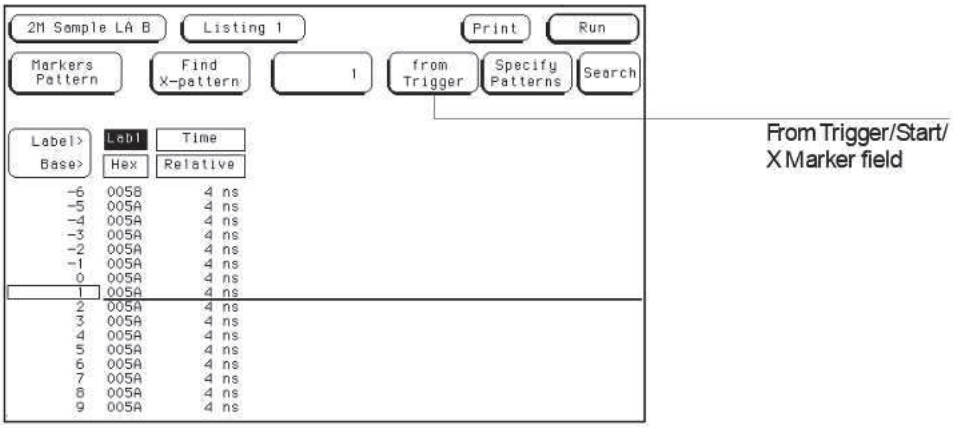
From Trigger / Start / X Marker Field

The From Trigger/Start/X Marker field is used to access the selection pop-up for the start point of the X and O marker occurrence counters.

The start points available for the green X marker are either the trace start point or the trigger point.

The start points available for the yellow O marker are either the trace start point, trigger point, or the X marker.

If the marker pattern can not be found, a message appears at the top of the display indicating the search failed. If the O marker is referenced from the X marker, and the X marker is not found, the search for both markers will fail.

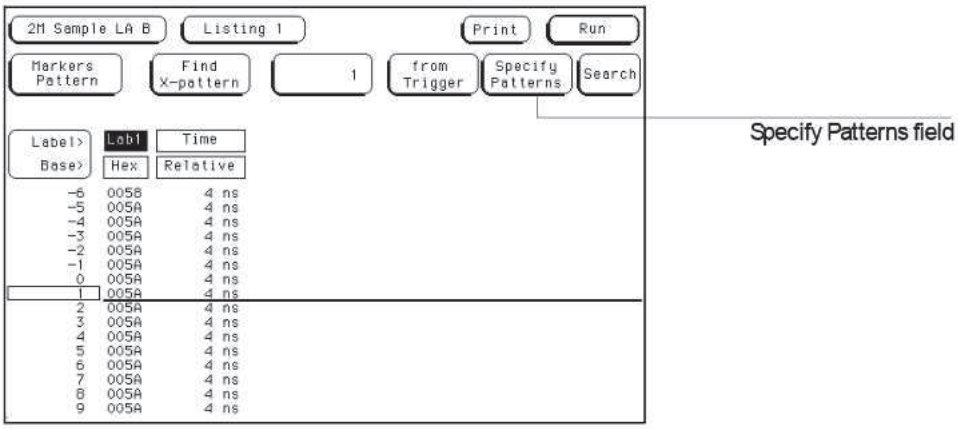


Trigger/Start/X Marker Field

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Specify Patterns Field

The Specify Patterns field appears only when the markers are set to Pattern. When the Specify Patterns field is selected, a pop-up menu appears in which you can assign the bit patterns for the X and O markers, the X and O entering/leaving, and the Stop measurement criteria.



Specify Patterns Field

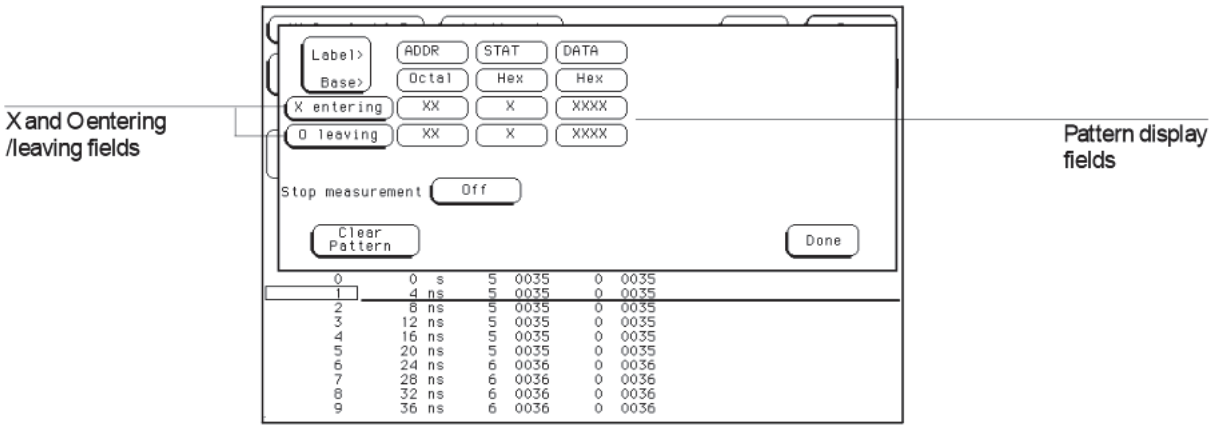
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X and O entering / leaving Fields (Timing only)

If the analyzer is configured as Timing, the X and O pattern markers are placed at either the beginning of the pattern occurrence (entering) or at the end of the pattern occurrence (leaving). When the entering/leaving field of either X or O markers is selected, it toggles between the two choices. Whichever choice you toggle the field to, the pattern you place in the pattern display field will apply to that choice.

X marker and O marker (State only)

If the analyzer is configured as State, X marker and O marker replace the X and O entering/leaving fields. The pattern you place in the pattern display field will apply to the marker labeled at the left.



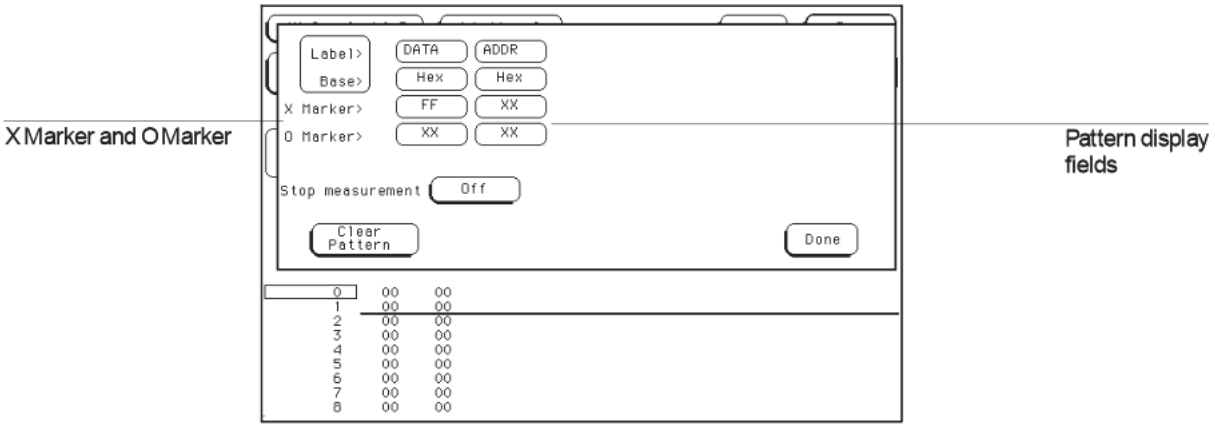
X and O entering / leaving Fields

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Pattern Display Fields

The pattern display fields display the alphanumeric bit pattern specified for each X and O marker in all designated labels. The bit pattern is displayed in the same numeric base and same order as the data listing. When the pattern display field is selected, a pop-up keypad appears which is used to set the bit pattern.

When there are more labels assigned than can be displayed in a single screen, the pattern display fields are rolled back onscreen by selecting the Label/Base roll field and scrolling with the knob.



Pattern Display Field

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Label and Base Fields

The Label and Base fields show up together in all menus except the Format and Configuration menus. When a new label is assigned, a base field is automatically assigned to that label.

Label Field Labels in the Specify Patterns menu will be displayed throughout the analyzer as they were assigned in the Format menu.

To reorder currently displayed labels, select the label you want to move, then from the selection menu that appears, choose the label you want to switch positions with.

Base Field The function of the Base field is the same in all menus. To change the numeric base, select the base field, then choose the desired base from the selection menus.

Label / Base Roll Field

The rolling function is the same for all items that are stored offscreen. For more information on rolling labels, base, and pods, refer to "Label Assignment" chapter in the "Common Module Operations" section of the Agilent Technologies 16500C User's Reference for complete information.

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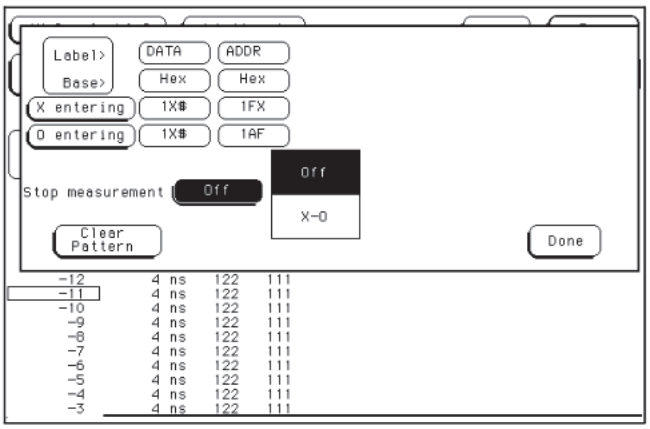
Stop Measurement Field

The Stop measurement function allows you to specify a condition which stops the analyzer measurement during a repetitive run. If two analyzers are configured, both analyzers will stop when either specified stop condition is satisfied.

When the Stop measurement field is selected, a Stop measurement type menu appears. Depending on the analyzer configuration, you have the choices of Off, X-O, and Compare.

Off

The Off selection turns all Stop measurement operations off. If the Stop measurement operation is not turned off and the stop criteria are met, the measurement will stop even though the markers are set to other types or turned off.



Stop Measurement Field

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X-O

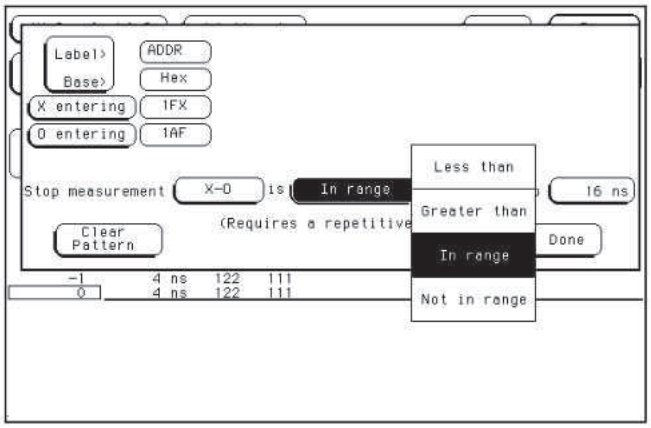
The X-O option is available in the timing analyzer, and in the state analyzer with its count set to Time. When X-O is selected, a repetitive run is stopped when a comparison of the time period between the X and O markers and one of the following time period options is true:

Less Than X-O time must be less than the time value that you specify in the Time field.

Greater Than X-O time must be greater than the time value that you specify in the Time field.

In Range X-O pattern must be within the time range value that you specify in the two Time fields.

Not in Range X-O pattern must not be within the time range value that you specify in the two Time fields.

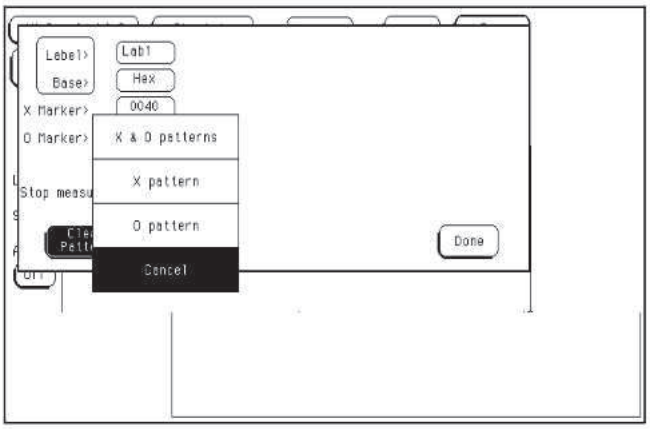


X-O Field

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Clear Pattern Field

The Clear Pattern field is used to reset the X and O Marker pattern display fields to default (don't care = X). The Clear Pattern field accesses a selection menu with the choices of X and O patterns, X pattern, or O pattern.



Clear Pattern

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Time Markers

Time markers are indicators in the data listing that are used as reference marks to obtain time values between markers or between each marker and the trigger point.

In a state analyzer, time markers become available only when the Count field is set to Time in the Trigger menu.

The markers are color-coded for easy recognition. The X marker is represented by a horizontal green line and the O marker is represented by a horizontal yellow line.

If pattern markers have been assigned, the time markers will be placed initially at the same locations in the data listing. You can set values for time markers using the following fields:

- Trig to X / Trig to O Fields

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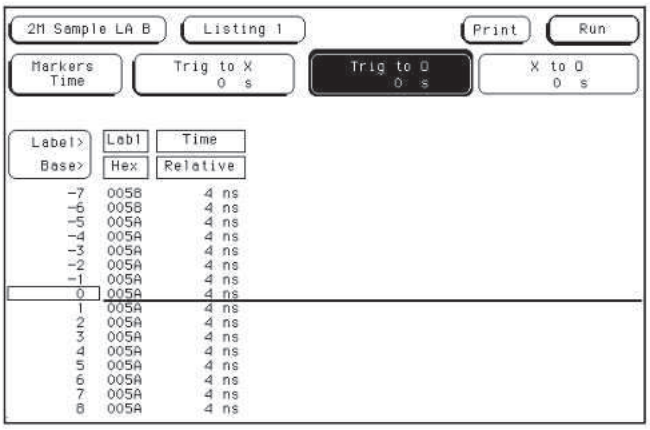
Trig to X / Trig to O Fields

The Trig to X and Trig to O fields are both display and configuration fields. Set the marker position by selecting the fields, then, after the fields turn light blue, rotate the knob. You can also set the marker position by selecting the light blue field a second time and entering a value using the pop-up keypad.

The Trig to X and Trig to O fields display the time between the trigger point and the marker.

X to O Display Field

The X to O display field is a "read only" field that displays the time between the X and O markers. As the X and O markers are changed, the display changes accordingly.



Trig to X / Trig to O Fields

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After you have assigned patterns to the X and O markers, statistical information is available when you set markers to Statistics. The logic analyzer displays the following information:

- Number of valid runs (runs where Pattern markers were able to be placed on specified patterns).
- Minimum time between the X and O Pattern markers.
- Maximum time between the X and O Pattern markers.
- Average time between the X and O Pattern markers.

In a state analyzer, Statistics markers become available only when the Count field in the Trigger menu is set to Time.

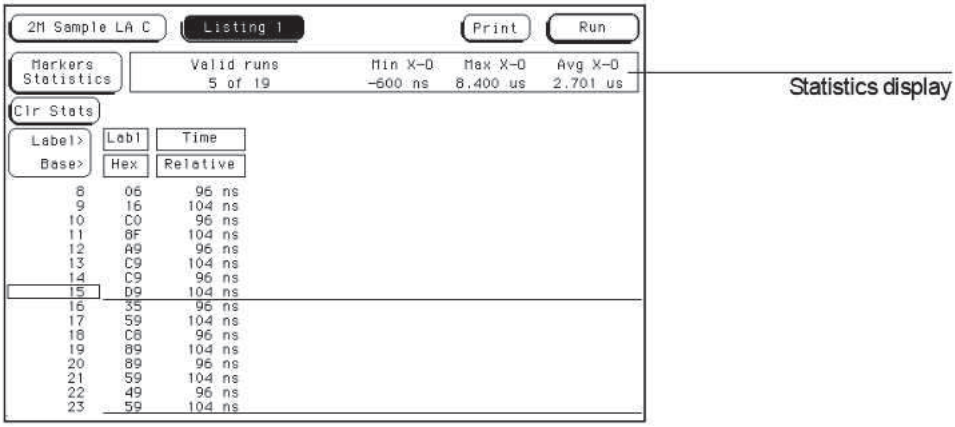
The markers are color-coded for easy recognition in the data listing. The X marker is represented by a horizontal green line and the O marker is represented by a horizontal yellow line.

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Statistics are based on the time between the X and O markers, therefore both markers must be found before valid statistical information is displayed.

In repetitive run mode, the display is updated each time a valid run occurs until you select Stop. If you select Run after selecting Stop, the statistics continue to update without loss of information.

In single run mode, each time you select Run an additional valid run will be added to the data and the statistics will be updated. This process continues unless you change the placement of the X and O Pattern markers between runs.



Statistics Display

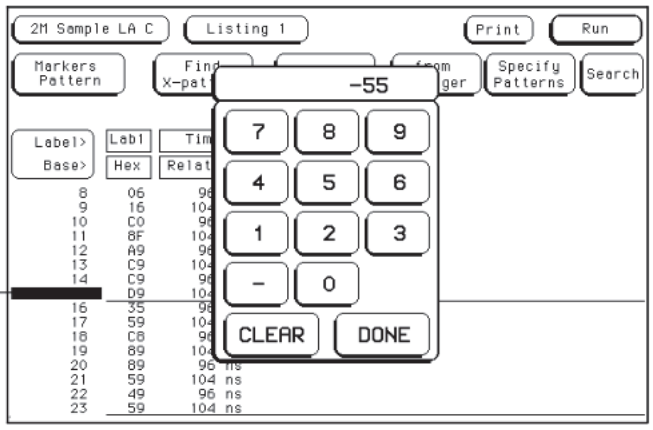
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Data Roll Field

The column of numbers at the far left represents the location of the acquired data in the state analyzer's memory. The numbered positions are also known as the state locations and are relative to the trigger state location. The column of state location along with its data can be rolled to display other data by using the data roll field.

The data roll field is the small rectangular box located in the middle of the state location column. The data roll field is used to either roll the data listing or to select an exact state for display. When the data roll field is light blue, the knob is active and can roll data in either direction.

If you touch the data roll field when it is light blue, a pop-up keypad appears for the number of an exact state. When the pop-up keypad is used, the data listing shifts, leaving the selected state in the light blue data roll box.



Data Roll Field

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