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About this Manual

We've added this manual to the Agilent website in an effort to help you support your product. This manual is the best copy we could find; it may be incomplete or contain dated information. If we find a more recent copy in the future, we will add it to the Agilent website.

Support for Your Product

Agilent no longer sells or supports this product. Our service centers may be able to perform calibration if no repair parts are needed, but no other support from Agilent is available. You will find any other available product information on the Agilent Test & Measurement website, www.tm.agilent.com.

HP References in this Manual

This manual may contain references to HP or Hewlett-Packard. Please note that Hewlett-Packard's former test and measurement, semiconductor products and chemical analysis businesses are now part of Agilent Technologies. We have made no changes to this manual copy. In other documentation, to reduce potential confusion, the only change to product numbers and names has been in the company name prefix: where a product number/name was HP XXXX the current name/number is now Agilent XXXX. For example, model number HP8648A is now model number Agilent 8648A.

Installation and Service Guide

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For Safety information, Warranties, and Regulatory information, see the pages behind the index.

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HP Processor Probe for PowerPC 603/603e

HP processor probe—At a Glance

The HP processor probe provides a low-cost way to debug embedded software for IBM/Motorola PowerPC™ microprocessors.

Supported processors

Your HP processor probe is pre-programmed for either the PowerPC 603 or PowerPC 603e processor.

The floppy disk contains firmware to program your HP processor probe for additional PowerPC processors.

The target connection

The HP processor probe connects to your target microprocessor via a special connector on the target system.

The configuration switches

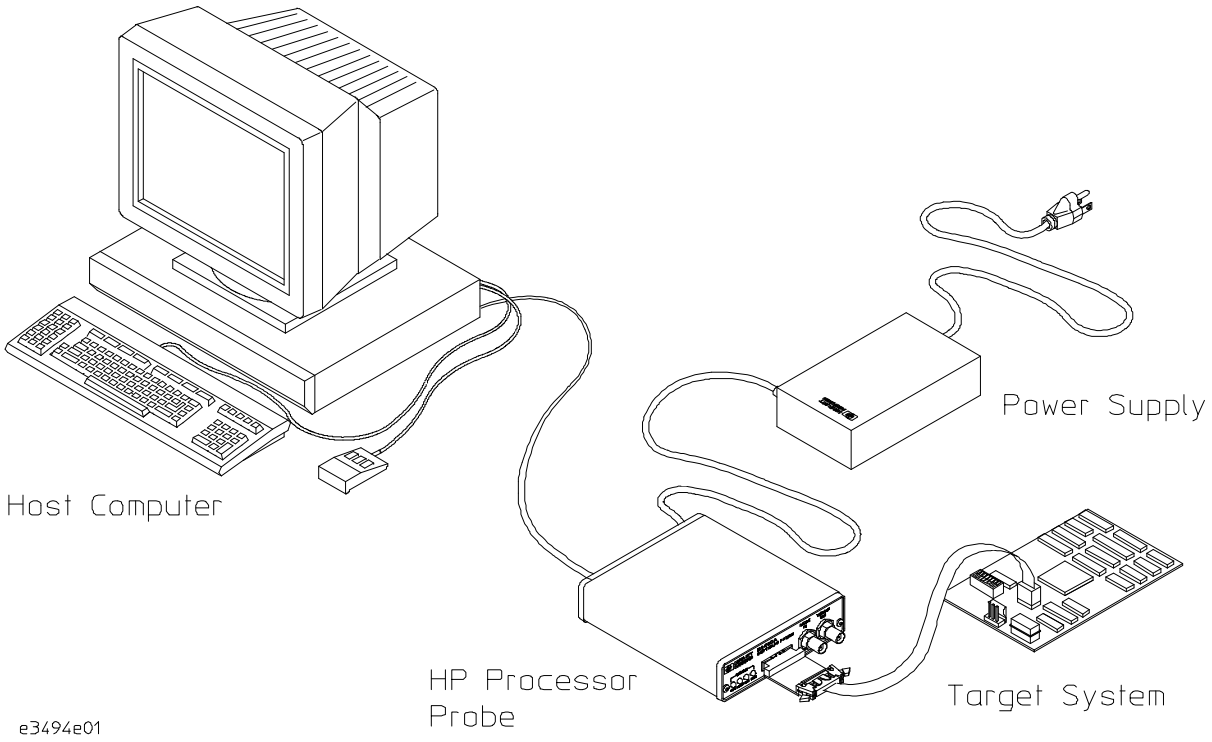
Use the switches to configure communication to the HP 16505A. There is a guide to these switches on the bottom of the HP processor probe.

The status LEDs

LEDs show the status of the power supply, the target system, and the connection to the LAN.

Compatibility with other products

The HP processor probe requires the use of a host based software debugger. No debuggers for the HP processor probe are sold by Hewlett-Packard so you must purchase a software debugger from a third party.


Host Computer
Power Supply
HP Processor
Probe
Target System
e3494e01

Contents

Part 1 Installation

1 Connecting to the Host Computer

Connecting the HP processor probe to a Power Source 5

To choose a power cord 5
To connect the power cord and turn on the HP processor probe 8

Setting Up a LAN Connection 9

To obtain an IP address 10
To configure LAN parameters using the built-in terminal interface 11
To configure LAN parameters using "ipconfig700" 14
To configure LAN parameters using BOOTP 17
To set the 10BASE-T configuration switches 19
To verify LAN communications 20

Setting Up a Serial Connection 21

To set the serial configuration switches 22
To connect a serial cable 22
To verify serial communications 24

Setting up the Host Software 25

2 Connecting to the Target System

Connector provided 28
To test the HP processor probe 29
To connect to a target system via the IEEE 1149.1 (JTAG) Port 29

Part 2 Using the HP processor probe

3 Configuring the HP Processor Probe for PowerPC 603/603e

To configure the HP processor probe 38

General Configuration Items 39

To set restrict to real-time runs 39
Setting the JTAG Clock Speed (communications speed) 40
Configuring reset operation 41
Setting memory read delays 42
Setting memory write delays 43
Setting BNC Break In operation 44
Setting BNC trigger out operation 45
Generating parity bits on memory operations 46
Setting databus size 47

Processor Memory Cache Configuration Items 48

Enabling data retry mode 49
Configuring the memory read operation 50
Configuring data memory write operations 51
Configuring instruction memory write operations 52

Part 3 Reference

4 Designing a Target System

Target System Requirements for PowerPC 603 58
Target System Requirements for PowerPC 603e 59
Target System Requirements for other PowerPC Processors 60
Motorola MVME 160X, Ultra, Atlas and Series E Target Boards 61
PowerPC 603 JTAG Interface Connections and Resistors 62

5 Specifications and Characteristics

Processor Compatibility 66
Electrical Specifications 66
Environmental Specifications 68
Product Regulations 68

6 Updating Firmware

To update firmware using prgflash.xxx 71
To run prgflash.xxx on Unix workstations 72
To run prgflash.exe on MS-DOS 72

To display current firmware version information 73
If the firmware doesn't appear to be updated 74
If there is a power failure during a firmware update 74

7 Solving Problems

Status Lights 78

Problems with the LAN Interface 79

If you cannot verify LAN communication 79
If you have LAN connection problems 80
If the "POL" LED is lit 81
If it takes a long time to connect to the network 81

Problems with the Serial Interface 82

If you cannot verify RS-232 communication 82
If you have RS-232 connection problems with the MS Windows Terminal program 82

Problems with the HP Processor Probe Itself 84

To run the power up self test 84
To execute the built-in performance verification test 86

Returning the HP processor probe to Hewlett-Packard for Service 92

To return the HP processor probe to Hewlett-Packard 92
To obtain replacement cables 93

Part 1

Installation

1

Connecting to the Host Computer

Connecting to the Host Computer

To use the HP processor probe you need to:

- Connect the HP processor probe to a power source
- Connect the HP processor probe to the host computer via a LAN or serial connection
- Set up the host software
- Connect the HP processor probe to the target system (described in the next chapter)

HP does not provide a debugger interface to the PowerPC processor. You must purchase a debugger interface from a third party. Setting up the host software is not covered in this manual, please refer to the manuals provided by the debugger vendor.

If you plan to use a version of the PowerPC other than the one for which your HP processor probe is programmed, you must reprogram your HP processor probe with the appropriate firmware. See the "Updating Firmware" chapter (page 69) for instructions on reprogramming the HP processor probe; see the "readme" file on the floppy disk for a list of supported processors.

Connecting the HP processor probe to a Power Source

The HP processor probe does not have an On/Off switch. To turn the HP processor probe on or off, plug or unplug it from the power supply.

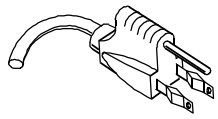
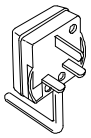
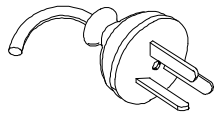
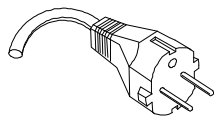
To choose a power cord

The HP processor probe is shipped from the factory with a power supply and cord appropriate for your country. You should verify that you have the correct power cable for installation by comparing the power cord you received with the HP processor probe with the drawings under the "Plug Type" column of the following table.

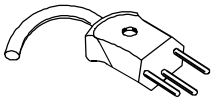
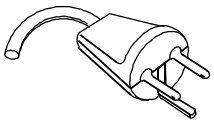
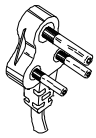
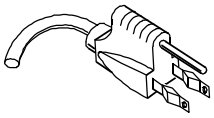
If the cord you received is not appropriate for your electrical power outlet type, contact your Hewlett-Packard sales and service office.

Warning Use only the supplied HP power supply and cord.
Failure to use the proper power supply could result in electric shock.

Caution Use only the supplied HP power supply and cord.
Failure to use the proper power supply could result in equipment damage.

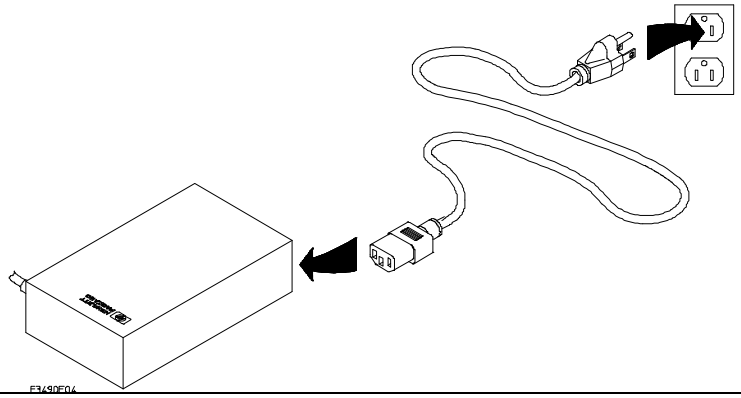
Plug Type	Cable Part No.	Plug Description	Length in/cm	Color
Opt 903 125V ** 	8120-1378 8120-1521	Straight * NEMA5-15P 90°	90/228 90/228	Jade Gray Jade Gray
Opt 900 250V 	8120-1351 8120-1703	Straight * BS136A 90°	90/228 90/228	Gray Mint Gray
Opt 901 250V 	8120-1369 8120-0696	Straight * NZSS198/ASC 90°	79/200 87/221	Gray Mint Gray
Opt 902 250V 	812001689 8120-1692 8120-2857	Straight * CEE7-Y11 90° Straight (Shielded)	79/200 79/200 79/200	Mint Gray Mint Gray Coco Brown

* Part number shown for plug is industry identifier for plug only.
Number shown for cable is HP part number for complete cable including plug.
** These cords are included in the CSA certification approval for the equipment.

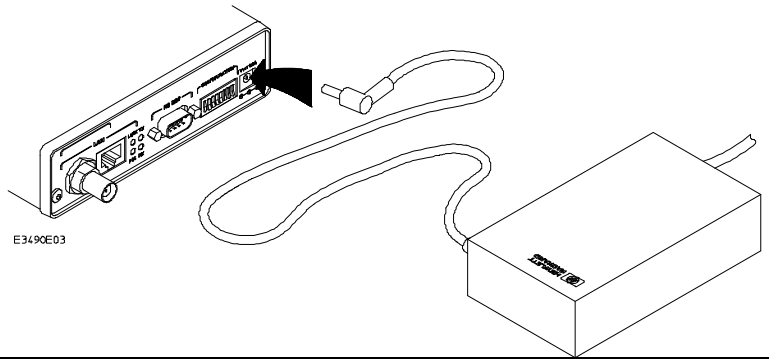
Plug Type	Cable Part No.	Plug Description	Length in/cm	Color
Opt 906 250V 	8120-2104 8120-2296	Straight * SEV1011 1959-24507 Type 12 90°	79/20 79/200	Mint Gray Mint Gray
Opt 912 220V 	8120-2957	Straight *DHCK107 90°	79/200 79/200	Mint Gray Mint Gray
Opt 917 250V 	8120-4600 8120-4211	Straight SABS164 90°	79/200 79/200	Jade Gray
Opt 918 100V 	8120-4753 8120-4754	Straight Miti 90°	90/230 90/230	Dark Gray
* Part number shown for plug is industry identifier for plug only. Number shown for cable is HP part number for complete cable including plug. ** These cords are included in the CSA certification approval for the equipment.				

To connect the power cord and turn on the HP processor probe

1 Connect the power cord to the power supply and to a socket outlet.



2 Connect the 5V power cord to the back of the HP Software Probe.



The power light on the target side of the HP Software Probe will be illuminated. The HP Software Probe does not have an On/Off switch.

Setting Up a LAN Connection

The HP processor probe has two LAN connectors:

- A BNC connector that can be directly connected to a IEEE 802.3 Type 10BASE2 cable (ThinLAN). When using this connector, the HP processor probe provides the functional equivalent of a Medium Attachment Unit (MAU) for ThinLAN.
- An IEEE 802.3 Type 10BASE-T (StarLAN) connector.

Use either the 10BASE2 or the 10BASE-T connector. Do *not* use both. The HP processor probe will not work with both connected at the same time.

You must assign an IP address (Internet address) to the HP processor probe before it can operate on the LAN. You can also set other network parameters such as a gateway address. The IP address and other network parameters are stored in nonvolatile memory within the HP processor probe.

The HP processor probe automatically sets a subnet mask based on the subnet mask used by other devices on the network.

You can configure LAN parameters in any of the following ways:

- Using the built-in terminal interface. This is the easiest method.
- Using ipconfig700. The ipconfig700 program is supplied with HP emulator user interfaces which run on HP and Sun workstations.
- Using BOOTP. BOOTP is part of the HP-UX, SunOS, and Solaris operating systems.

To obtain an IP address

1 Obtain the following information from your local network administrator or system administrator:

- An IP address for the HP processor probe.
- The gateway address.

The gateway address is an IP address and is entered in integer dot notation. The default gateway address is 0.0.0.0, which only allows connections on the local network or subnet. If connections are to be made to workstations on other networks or subnets, this address must be set to the address of the gateway machine.

2 Find out whether port numbers 6470 and 6471 are already in use on your network.

The host computer interfaces communicate with the HP processor probe through two TCP service ports. The default base port number is 6470. The second port has the next higher number (default 6471).

The default numbers (6470, 6471) can be changed if they conflict with some other product on your network. TCP service port numbers must be greater than 1024. If you change the base port, the new value must also be entered in the /etc/services file on the host computer. For example, you could add or modify the line:

hp64700 6470/tcp

To change the port numbers, see page 11. If you have already set the IP address, you can use a telnet connection instead of a serial connection to connect to the HP processor probe.

3 Write down the link-level address of the HP processor probe.

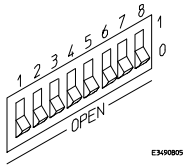
You will need this address if you use BOOTP or ipconfig700 to set the IP address.

The link-level address (LLA) is printed on a label above the LAN connectors on the HP processor probe. This address is configured in each HP processor probe shipped from the factory and cannot be changed.

To configure LAN parameters using the built-in terminal interface

1. **Set configuration switches S1 through S4 to CLOSED, and set the other switches as appropriate for your serial interface.**

   Switch settings are printed on the bottom of the HP processor probe. If you will use a baud rate of 9600 baud, set the switches like this:



2. **Connect an ASCII terminal (or terminal emulator) to the HP processor probe's RS-232 port with a 9-pin RS-232 cable.**

   Complete instructions for setting up a serial connection begin on page 21.

3. **Plug in the HP processor probe's power cord. Press the terminal's <RETURN> key a couple times. You should see a "p>" or "U>" prompt.**

   At this point, you are communicating with the HP processor probe's built-in terminal interface.

4. **Display the current LAN configuration values by entering the lan command:**

```
R>lan
lan is disabled
lan -i 0.0.0.0
lan -g 0.0.0.0
lan -p 6470
Ethernet Address: 08000903212f
```

   The "lan -i" line shows the current IP address (IP address) of the HP processor probe.

   The Ethernet address, also known as the link level address, is preassigned at the factory, and is printed on a label above the LAN connectors.

5. **Enter the following command:**

```
lan -i <internet> [-g <gateway>] [-p <port>]
```

   The lan command parameters are:

`-i <internet>` The IP address which you obtained from your network administrator.

`-g <gateway>` The gateway address. Setting the gateway address allows access outside your local network or subnet.

`-p <port>` This changes the base TCP service port number.

The default numbers (6470, 6471) can be changed if they conflict with some other product on your network. TCP service port numbers must be greater than 1024. If you change the base port, the new value must also be entered in the /etc/services file on the host computer. For example, you could add or modify the line:

hp64700 6470/tcp

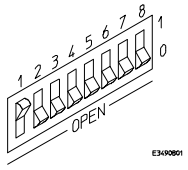
6 Disconnect the power cord from the HP processor probe, and connect the the HP processor probe to your network.

This connection can be made by using either the 10BASE-T connector or the 10BASE2 (BNC) connector on the HP processor probe. Do not use both connectors at the same time.

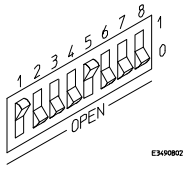
7 Set the configuration switches to indicate the type of connection that is to be made.

Switch S1 must be set to OPEN, indicating that a LAN connection is being made.

Switch S5 should be 1 if you are connecting to the BNC connector:



Switch S5 should be 0 if you are connecting to the 10BASE-T connector:



Set all other switches to CLOSED.

8 Connect the power cord to the HP processor probe.

9 Verify your HP processor probe is now active and on the network. See "To verify LAN communications" on page 20.

Once you have set a valid IP address, you can use the telnet utility to connect to the HP processor probe, and use the lan command to change LAN parameters.

Example

For example, to assign an IP address of 192.6.94.2 to the HP processor probe, enter the following command:

```
R>lan -i 192.6.94.2
```

The IP address and any other LAN parameters you change are stored in nonvolatile memory and will take effect the next time the HP processor probe is powered off and back on again.

See Also

"Solving Problems," page 75, if you have problems verifying LAN communication.

To configure LAN parameters using "ipconfig700"

If you are using an HP 9000 Series 300/400/700 computer or Sun SPARCsystem computer and you have installed the HP B1471 64700 Operating Environment software, you can configure the HP processor probe's LAN parameters with the ipconfig700 command.

The ipconfig700 command sets the IP address and gateway address for the HP processor probe. An IP address must be configured before a network interface connection can be made.

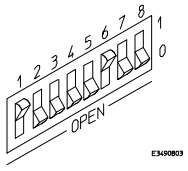
The ipconfig700 command cannot be used if your workstation is running a bootp daemon. If this is the case, use BOOTP to configure LAN parameters. To determine if BOOTP is enabled on your computer, see "To configure LAN parameters using BOOTP" in this chapter.

The following steps need to be taken when configuring the network parameters with ipconfig700.

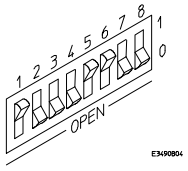
1. **Connect the the HP processor probe to your network. This connection can be made by using either the 10BASE-T connector or the 10BASE2 BNC connector on the HP processor probe.**
2. **Set the configuration switches to indicate the type of connection that is to be made.**

   Switch S1 must be set to OPEN, indicating that a LAN connection is being made. Switch S6 must bet set to OPEN, to allow programming of the LAN parameters.

   Switch S5 should be 1 if you are connecting to the BNC connector:



   Switch S5 should be 0 if you are connecting to the 10BASE-T connector:



   Set all other switches to CLOSED.
3. **Turn ON power to the HP processor probe.**

4. Wait at least 20 seconds for the HP processor probe to connect to the LAN.
5. Become the root user on the system from which you wish to configure the HP processor probe.
6. Enter the following command:

   ```
   ipconfig700 -l <link> -i <internet> [-g <gateway>]
   ```

   The ipconfig700 parameters are:

   `-l <link>` The link-level address. Enter any letters in the address in upper case.

   `-i <internet>` The IP address.

   `-g <gateway>` The gateway address.

   If the ipconfig700 command is entered without any options, the program interactively prompts for the necessary information.
7. Set switch S6 back to CLOSED.
8. Verify your HP processor probe is now active and on the network. See "To verify LAN communications" on page 20.

Example

If the link-level address on your HP processor probe read 08000F090F30, and your system administrator gave you the IP address 192.35.12.6, you could enter the following command:

```
$ ipconfig700 -l 08000F090B30 -i 192.35.12.6 <RETURN>
```

Because no gateway address was entered, this value would default to 0.0.0.0. When the IP address is successfully programmed, ipconfig700 will display the HP processor probe version information.

Limitations of ipconfig700

The ipconfig700 command generally will not work if:

- the workstation and the HP processor probe are on different subnets, or
- a BOOTP daemon running elsewhere on your network is configured to respond to the link-level address of the HP processor probe, or
- a BOOTP daemon is already running on your workstation.

To configure LAN parameters using BOOTP

Use this method only if your HP-UX or SUN workstation is already running bootpd, the BOOTP daemon. The ipconfig700 command does the same thing as BOOTP and is easier to use.

1 Make sure that your host computer supports BOOTP.

If the following commands yield the results shown below, your machine supports the BOOTP protocol.

```
$ grep bootp /etc/services
bootps      67/udp
bootpc      68/udp
$ grep bootp /etc/inetd.conf
bootps  dgram  udp  wait    root  /etc/bootpd   bootpd
```

If the commands did not yield the results shown, you must either add BOOTP support to your workstation or use a different method to configure the HP processor probe LAN parameters.

2 Add an entry to the host BOOTP database file, /etc/bootptab. For example:

```
# Global template for options common to all HP 64700
emulators and processor probes.
# Gateway addresses can be specified differently if
# necessary.

hp64700.global:\
        :gw=0.0.0.0:\
        :vm=auto:\
        :hn:\
        :bs=auto:\
        :ht=ether

# Specific emulator entry specifying hardware address
# (link-level address) and ip address.

hpprobe.div.hp.com:\
        :tc=hp64700.global:\
        :ha=080009090B0E:\
        :ip=192.6.29.31
```

In the example above, the "ha=080009090B0E" identifies the link-level address of the HP processor probe.

The "ip=192.6.29.31" specifies the IP address that is assigned to the HP processor probe.

The node name is "hpprobe.div.hp.com".

For additional information about using bootpd, refer to the HP-UX man pages.

3 Connect the the HP processor probe to your network.

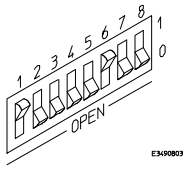
This connection can be made by using either LAN connector on the HP processor probe.

4 Set the configuration switches to indicate the type of connection that is to be made.

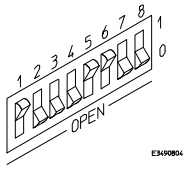
Switch S1 must be set to OPEN, indicating that a LAN connection is being made.

Switch S6 must be set to OPEN to enable BOOTP mode.

Switch S5 should be set to CLOSED if you are connecting to the BNC connector



Switch S5 should be set to OPEN if you are connecting to the 10BASE-T connector.



Set all other switches to CLOSED.

5 Connect the power cord to the HP processor probe.

Verify that the power light stays on after 10 seconds.

The IP address will be stored in EEPROM.

6 Set switch S6 back to CLOSED.

Do this so that the HP processor probe does not request its IP address each time power is cycled. The IP address is stored in EEPROM, so BOOTP does not need to be run again. Leaving this switch on will result in slower

performance, increased LAN traffic, and even failure to power up (if the BOOTP server becomes inactive).

7 Verify your HP processor probe is now active and on the network. See "To verify LAN communications" on page 20.

To set the 10BASE-T configuration switches

Set switches S7 and S8 to CLOSED unless one of the following conditions is true:

- **If the LAN cable exceeds the standard length, set switch S7 to OPEN.**

  The HP processor probe has a switch-selectable, twisted-pair receiver threshold. With switch S7 set to OPEN, the twisted-pair receiver threshold is lowered by 4.5 dB. This should allow you to use cable lengths of up to about 200 meters. If you use a long cable, you should consult with your LAN cabling installer to ensure that:

  - The device at the other end of the cable has long cable capability, and
  - The cable is high-grade, low-crosstalk cable with crosstalk attenuation of greater than 27.5 dB.

  When switch S7 is set to CLOSED, the LAN port operates at standard 10BASE-T levels. A maximum of 100 meters of UTP cable can be used.

- **If your network doesn't support Link Beat integrity checking or if the HP processor probe is connected to a non 10BASE-T network (such as StarLAN) set this switch to LINK BEAT OFF (0 or OPEN).**

  In normal mode (switch S8 set to CLOSED), a link integrity pulse is transmitted every 15 milliseconds in the absence of transmitted data. It expects to receive a similar pulse from the remote MAU. This is the standard link integrity test for 10BASE-T networks. If your network doesn't support the Link Beat integrity checking or if the processor probe is used on a non 10BASE-T network (such as StarLAN) set this switch to LINK BEAT OFF (OPEN).

Note **Setting switch S8 to OPEN when Link Beat integrity checking is required by your network will cause the remote MAU to disable communications.**

To verify LAN communications

1. Verify your HP processor probe is now active and on the network by issuing a **telnet** to the IP address.

   This connection will give you access to the HP processor probe's built-in terminal interface.
2. To view the LAN parameters, enter the **lan** command at the terminal interface prompt.
3. To exit from this telnet session, type <CTRL>D at the prompt.

   The best way to change the HP processor probe's IP address, once it has already been set, is to telnet to the HP processor probe and use the terminal interface lan command to make the change. Remember, after making your changes, you must cycle power or enter a terminal interface init -p command before the changes take effect. Doing this will break the connection and end the telnet session.

If You Have Problems

If you encounter problems, refer to the "Problems" chapter (page 75).

Example

$ telnet 192.35.12.6

```
R>lan
lan is enabled
lan -i 192.35.12.6
lan -g 192.34.12.1
lan -p 6470
Subnet Mask: 255.255.255.0
Ethernet Address: 08000F090B30
```

Setting Up a Serial Connection

To set up a serial connection, you will need to:

- Set the serial configuration switches
- Connect the HP processor probe to the RS-232 interface
- Connect a serial cable between the host computer and the HP processor probe
- Verify communications

Serial connections

You should not use a serial connection, except to set LAN parameters. If you must use the serial connection for anything other than setting LAN parameters, hardware handshaking is required.

If you are using a UNIX workstation as the host computer, you need to use a serial device file. If a serial device file does not already exist on your host, you need to create one. Once it exists, you need to ensure that it has the appropriate permissions so that you can access it. See the system documentation for your workstation for help with setting up a serial device.

If you are using a PC as the host computer, you do not need to set up any special files.

To set the serial configuration switches

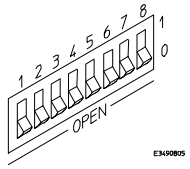
1. Set switch S1 to CLOSED (RS-232).
2. Set switches S2-S4 to CLOSED.
3. Set switch S5 to CLOSED (HW HANDSHAKE ON) if your serial interface uses the DSR:CTS/RTS lines for flow control. Set S5 to OPEN (HW HANDSHAKE OFF) if your serial interface uses software flow control (XON/XOFF).

   If your serial interface supports hardware handshaking, you should use it (set switch S5 to CLOSED). Hardware handshaking will make the serial connection much more reliable.
4. Set switches S6-S8 for the baud rate you will use. These switch settings are listed on the bottom of the HP processor probe.

   The higher baud rates may not work reliably with all hosts and user interfaces. Make sure the baud rate you choose is supported by your host and user interface.

Example

To use a baud rate of 9600 baud, set the switches as follows:



To connect a serial cable

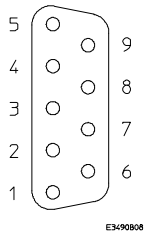
CAUTION

Use a grounded, shielded cable. If the cable is not shielded, or if the cable is not grounded at the serial controller, the HP processor probe may be damaged by electrostatic discharge.

1. Connect an RS-232C modem cable from the host computer to the HP processor probe.

   The recommended cable is HP part number C2932A. This is a 9-pin cable with one-to-one pin connections.

If you want to build your own RS-232 cable, follow the pinout shown in the following figure:



Serial Cable Pinout

Pin Number	Signal	Signal Description
1	DCD	Data Carrier Detect (not used)
2	TD	Transmit Data (data coming from HP processor probe)
3	RD	Receive Data (data going to HP processor probe)
4	DTR	Data Terminal Ready (not used)
5	GND	Signal Ground
6	DSR	Data Set Ready (Output from HP processor probe)
7	RTS	Request to Send (Input to HP processor probe)
8	CTS	Clear to Send (connected to pin 6)
9	RING	Ring Indicator (not used)

To verify serial communications

1. **Start a terminal emulator program on the host computer.**

   If you are using a PC, the Terminal application in Microsoft Windows will work fine.

   If you are using a UNIX workstation, you can use a terminal emulator such as cu or kermit.

2. **Plug the power cord into the HP processor probe.**

   When the HP processor probe powers up, it sends a message (similar to the one that follows) to the serial port and then displays a prompt:

```
                Copyright (c) Hewlett-Packard Co. 1987
All Rights Reserved.  Reproduction, adaptation, or translation without prior
written permission is prohibited, except as allowed under copyright laws.

  HPE3499A Series Emulation System
    Version:   A.06.00 14Feb96
    Location:  Generics

 HPE3494A PowerPC 603 (Rev3) JTAG Emulator
    Version:   A.01.04 28Feb96

U>
```

   The version numbers may be different for your HP processor probe.

3. **Press the Return or Enter key a few times.**

   You should see a prompt such as "M>", "U>" or "p>".

See Also "Problems with the Serial Interface," page 82.

Setting up the Host Software

The HP processor probe requires the use of user interface software on your host computer. HP does not supply a debugger interface for the HP processor probe. You must purchase a debugger interface from a third party. Please refer to the debugger manuals for information about setting up your host software.

2

Connecting to the Target System

Connecting to a Target System

The HP processor probe can be connected to a target system through the IEEE 1149.1 (JTAG) Port 16 pin connector.

Connector provided

The following components are provided with the HP processor probe for the purpose of testing the probe and connecting to a target system.

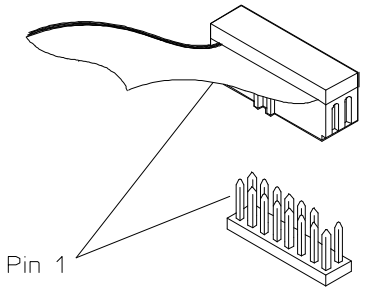
- A 16-conductor cable assembly (HP part number E3494-61601)
- A transition board (HP part number E3494-61602)
- A self-test connector (HP part number E3490-61604)

To test the HP processor probe

If this is the first time that you have used the HP processor probe, you should run the built-in performance verification test before you connect to a target system. Refer to chapter 6 for information on performance verification.

To connect to a target system via the IEEE 1149.1 (JTAG) Port

In order to connect the HP processor probe to the microprocessor, a 16-pin male 2x8 header connector must be available on the target system (see chapter 5 for information on designing a target system for use with the HP processor probe).



Note that pin 14 of the header should not contain a pin. The cable provided will not plug into the header if pin 14 has not been removed from the header.

1. Remove power from the target system and the probe.
2. Plug the transition board in the HP processor probe.
3. Plug the end of the 16-pin cable with all 16 pin sockets available into the transition board.
4. Plug the other end of the 16-pin cable with pin-14 filled in into the connector on the target system.
6. Turn on the power to the probe, then turn on the power to the target system.

Part 2

Using the HP processor probe

3

Configuring the HP Processor Probe for PowerPC 603/603e

Configuring the HP Processor Probe

This chapter tells you how to configure the HP processor probe for PowerPC 603/603e

The HP processor probe has a number of user configurable parameters. These parameters may be customized for specific target systems and saved in configuration files for future use. Since the HP processor probe can be used with a number of third party debuggers, specific details for sending the configuration commands to the probe cannot be given here. However, all debuggers should provide a way of directly entering terminal mode commands to the probe. Ideally, you would create a file that contains the configuration entries you need modified that can be sent to the probe at the beginning of each debugger session. See your debugger manual for more details.

What can be configured

There are two categories of configuration items: general configuration and cache configuration. The default powerup configuration will generally work with many target systems if the cache is turned off, but there are a few configuration items that must be set for correct target operation.

The general configuration items must all be set correctly. If the instruction and data caches are both turned off, the cache configuration items are meaningless and can be ignored. If either instruction or data cache is enabled on the 603, the "cf drtry" setting must be set correctly based on your target system (the debug port for the 603e does not require any differences based on DRTRY mode so this configuration entry does not exist for the 603e).

The current mask rev dd1 of the 603e silicon does not work in debug mode with either cache enabled. The cache configuration items have no effect with the current 603e silicon.

The general configuration commands and their default values are:

- cf rrt - restrict to real-time runs
  Default: yes
- cf reset - selects the action desired for the reset command
  Default: runrom
- cf speed - set the speed of the JTAG clock
  Default: 1 (fastest speed)
- cf parity - generate parity bits on memory operations
  Default: off (no parity bits generated)
- cf mrddel - set memory read delays
  Default: 0 (no delay)
- cf mwrdel - set memory write delays
  Default: 0 (no delay)
- cf 32bitmode - set 32-bit data bus size
  Default: off (64-bit data bus)
- cf breakin - set BNC break in operation
  Default: off (BNC input ignored)
- cf trigout - set BNC trigger out operation
  Default: fixhigh (BNC trigger out always high)

The cache configuration commands and their default values are:

- cf drtry - enable data retry mode of processor (603 only)
  Default: off (do not use data retry mode)
- cf mrdop - configure the memory read operation
  Default: mm (memory model, reads from cache if valid)
- cf dmwrop - configure the data memory write operation
  Default: mm (memory model, writes to cache if valid)
- cf imwrop - configure the instruction memory write operation
  Default: upd_dcu (instruction cache update, data cache update)

For versions of the PowerPC other than the 603 and 603e, and in future firmware versions, configuration items may be different. To see a complete list of configuration items, use the command "help cf". For example:

```
M>help cf

  cf - display or set emulation configuration

    cf                - display current settings for all config items
    cf <item>         - display current setting for specified <item>
    cf <item>=<value> - set new <value> for specified <item>
    cf <item> <item>=<value> <item> - set and display can be combined

  help cf <item>    - display long help for specified <item>

  --- VALID CONFIGURATION <item> NAMES ---
    rrt       - Restrict to real-time runs
    reset     - Configure reset actions
    speed     - Set JTAG clock
    mrdop     - Configure mem read operation
    dmwrop    - Configure D mem write operation
    imwrop    - Configure I mem write operation
    mrddel    - Set memory read delay
    mwrdel    - Set memory write delay
    breakin   - Select BNC break input option
    trigout   - Select BNC trigger output option
    parity    - Enable/disable data parity
    drtry     - Select DRTRY mode
    32bitmode - Enable/disable 32 bit mode
M>
```

To see a more detailed description of any configuration item, use the command "help cf <item>". For example:

```
M>help cf rrt

  Restrict to real-time runs

    cf rrt=yes
    cf rrt=no

  If yes (and while the processor is running the user program), any
  command that requires the processor to be stopped will be rejected.
  For example 'reg' and 'm'.

  If no, commands that require the processor to be stopped will
```

```
  actually stop the processor, execute then resume running the
  processor.

M>
```

To see a list of the current configuration settings, use "cf":

```
M>cf
  cf rrt=yes
  cf reset=runrom
  cf speed=1
  cf mrdop=mm
  cf dmwrop=mm
  cf imwrop=upd_dcu
  cf mrddel=0
  cf mwrdel=0
  cf breakin=off
  cf trigout=fixhigh
  cf parity=off
  cf drtry=off
  cf 32bitmode=off
M>
```

To configure the HP processor probe

Use one of the following ways to configure the HP processor probe:

- **Start a user interface without specifying a configuration file.**
  In this case the configuration of HP processor probe is not changed from the last configuration settings. If the user interface does not provide a way to issue terminal mode commands directly to the probe, you can telnet to the probe and set the configuration manually before starting the user interface. When power is cycled on the HP processor probe, the configuration is restored to the default values listed above.
- **Start a user interface, loading a configuration file (for interfaces that allow loading a configuration file).**
  In this case, the HP processor probe is initialized with the values in the configuration file. The configuration file should be a list of "cf" commands to be sent to the probe.
- **Modify the configuration from within the user interface.**
  When a user interface is started, individual "cf" commands can be sent to the probe either through the user interface or by using telnet to connect to the probe. A telnet session and user interface can be connected to the probe at the same time.

General Configuration Items

The general configuration items must be set correctly for each target system.

To set restrict to real-time runs

`cf rrt=yes`

When the processor is running user code, no operations that require stopping the processor like reading memory or modifying registers will be performed, an error will be issued instead. The processor must be explicitly stopped before these commands can be performed.

`cf rrt=no`

When running user code, the probe will automatically stop the processor, perform a command and restore the processor to running when commands that need the processor stopped are requested.

For most debuggers, changing this setting has no effect since most debuggers require you to stop the processor to perform any action like reading memory or changing registers. If your debugger allows displaying or modifying memory or registers while the processor is running, you must set rrt=off in order to use this feature.

Default: cf rrt=yes

Setting the JTAG Clock Speed (communications speed)

The HP processor probe needs to be configured to communicate at a rate which is compatible with your target processor. The JTAG Clock speed is independent of processor clock speed. In general, speed=1 can always be used and provides the best performance. With some target systems that have additional loads on the JTAG lines or with target systems that do not quite meet the requirements described in chapter 4, setting speed to a slower setting may enable the probe to work.

Allowed speed settings

cf speed =	TCK =
1	10 MHz
2	5 MHz
3	2.5 MHz
4	1.25 MHz
5	625 kHz
6	312 kHz
7	156 kHz

Default: cf speed=1

Configuring reset operation

The reset configuration item controls what kind of reset is performed and what state the processor will be in after the reset.

`cf reset=runrom`

Issuing a reset from the HP processor probe will reset the processor and cause it to start running user code at address FFF00100H.

`cf reset=rom`

Issuing a reset from the HP processor probe will reset the processor and cause it to stop at address 0FFF00100H.

`cf reset=runram`

Issuing a reset from the HP processor probe will reset the processor and cause it to start running user code at address 00000100H.

`cf reset=ram`

Issuing a reset from the HP processor probe will reset the processor and cause it to stop at address 00000100H.

`cf reset=jtag`

Issuing a reset from the HP processor probe will just reset the JTAG interface on the processor, the processor itself will not be reset. This may help in some cases where communications are lost, however all the other reset settings reset the JTAG interface as part of the reset sequence so this setting will only rarely be useful.

Default: cf reset=runrom

Setting memory read delays

The memory read delay setting delays the number of microseconds specified during memory reads. It is provided for accessing slow devices like memory mapped IO.

`cf mrddel=<delay in usec>`

The <delay in usec> must be in the range 0-10000000. This should be set to the smallest number possible for best performance since it delays all reads by the number of microseconds specified.

Default: cf mrddel=0

Setting memory write delays

The memory write delay setting delays memory writes by the number of microseconds specified. It is provided for accessing slow devices like memory mapped IO.

`cf mwrdel=<delay in usec>`

The <delay in usec> must be in the range 0-10000000. This should be set to the smallest number possible for best performance.

Default: cf mwrdel=0

Setting BNC Break In operation

The cf breakin command selects the operation of the Break In BNC on the front of the HP processor probe for connection to a logic analyzer.

```
cf breakin=off
```

This causes any Break In signals to be ignored

```
cf breakin=on
```

A rising edge on the Break In BNC will cause the probe to stop the processor if it is running user code. There is a delay about 400 µsec of between receiving the edge and stopping the processor.

Default: cf breakin=off

Setting BNC trigger out operation

The cf trigout command selects the operation of the Trigger Out BNC on the front of the HP processor probe for connection to a logic analyzer.

`cf trigout=fixhigh`

The BNC output is always high.

`cf trigout=fixlow`

The BNC output is always low.

`cf trigout=monlow`

The BNC output will be low when the processor is stopped and high when running user code.

`cf trigout=monhigh`

The BNC output will be high when the processor is stopped and low when running user code.

Default: cf trigout=fixhigh

Generating parity bits on memory operations

The PowerPC processor generates parity bits on both address and data lines when running user code. When used in debug mode these bits must be generated separately slowing down memory operations. Since memory operations on the PowerPC are slow as it is and many target systems do not check parity, parity is only generated if requested.

`cf parity=off`

Do not generate the parity bits for memory operations from the processor probe. This provides better performance, but will not work correctly when accessing devices that check the parity bits.

`cf parity=on`

Generate the parity bits for memory operations. Currently, only parity bits for the memory data lines are generated. Parity bits on the address lines are not. This may change in future firmware versions.

Default: cf parity=off

Setting databus size

The PowerPC 603 and 603E processors supports both 32 bit and 64 bit data buses. The processor determines bus size based on the value of the TLBISYNC pin during a reset. The 32bitmode cf option must match the data bus size of the target system for proper memory reads and writes from the processor probe.

`cf 32bitmode=off`

Processor is in 64 bit mode.

`cf 32bitmode=on`

Processor is in 32 bit mode. Maximum access size used will be 32 bits. (Access size can still be set to 8, but the processor probe will only do 4 byte memory accesses.)

Default: cf 32bitmode=off

Processor Memory Cache Configuration Items

The memory cache configuration items only have meaning if the instruction or data caches are enabled. The HP processor probe will not work with the current (mask rev dd1) PowerPC 603e processor with either cache turned on, so this configuration section currently only applies to the PowerPC 603 processor. The data retry mode is the only configuration item that must be set for correct operation. The default settings for the other cache configuration items will work correctly for all target systems. These other configuration items are provided for debugging target system cache coherency problems.

Enabling data retry mode

The PowerPC 603 processor can be powered on with data retry mode enabled or not depending on the state of the $\overline{\text{DRTRY}}$ processor pin. This cannot be detected by the HP processor probe. This mode is only used when the cache is enabled. If either the instruction and/or data cache is enabled, this configuration item must match the state of the processor as determined by the $\overline{\text{DRTRY}}$ pin on powerup. If the cache is disabled, this setting has no effect. The debug mode of the PowerPC 603e does not require different actions based on the $\overline{\text{DRTRY}}$ mode, so this configuration item does not exist for the 603e.

`cf drtry=off`

Disable the data retry mode of the PowerPC 603

`cf drtry=on`

Enable the data retry mode of the PowerPC 603

Note

The drtry setting must be set correctly if either cache is used. Failure to do so will cause incorrect data to be displayed or written and possibly communication problems between the processor probe and the target system.

Default: drtry=off

Configuring the memory read operation

The memory read operation configuration entry defines how the memory and cache interact during a memory read operation. If both instruction and data caches are turned off (bits ICE and DCE in the register HID0 are zero), this configuration setting has no effect and a memory read will always return the contents of physical memory.

```
cf mrdop=mm
```

A memory read from an address that is valid in either the data or instruction cache will return the contents of the cache. Memory reads from addresses not valid in either cache will return the contents of the physical memory.

```
cf mrdop=phys
```

A memory read will always return the contents of physical memory.

Note Using the mrdop=phys setting with the cache enabled may show data that is no longer valid. Use this setting only for solving cache problems where you really need to see the contents of physical memory. For general operation, the "mm" setting should always be used.

Default: cf mrdop=mm

Configuring data memory write operations

Although the PowerPC processor has one contiguous physical memory address space that can hold both data and instructions, it has separate caches for instructions and data. These separate caches must be considered in order to keep the caches and memory coherent during memory write operations. These settings are only used for memory write operations. Code download always writes to physical memory and disables any cache entries containing addresses written for improved performance. Some host interfaces use the code download mode for all memory write operations so this setting may or may not have any effect on your debugger.

Only the memory write command allows specifying instruction or data memory operations. This may not be provided by your debugger interface. If not specified, memory write operations are always instruction memory.

If the data cache is disabled, a data memory write will always write to physical memory and this configuration setting is ignored.

`cf dmwrop=mm`

A data writes to addresses that are valid in the data cache will write the value only to the cache and mark the cache line modified as "dirty" which will indicate to the cpu that the cache line must be written to memory. A data write that is not valid in the data cache will only be written to physical memory.

`cf dmwrop=thru`

A data memory write to an address that is valid in the data cache will write to both cache and physical memory. If the address is not valid in the cache, only physical memory will be modified.

`cf dmwrop=bypass`

A data memory write will only be written to physical memory ignoring the cache.

Note

The cf dmwrop=bypass setting should be used with extreme caution because dirty cache entries may be written by the processor over the new data value written to memory by the HP processor probe.

Default: cf dmwrop=mm

Configuring instruction memory write operations

Although the PowerPC processor have one contiguous physical memory address space that can hold both data and instructions, it has separate caches for instructions and data. These separate caches must be considered in order to keep the caches and memory coherent during memory write operations. Code download always writes to physical memory and disables any cache entries containing addresses written for improved performance. Some host interfaces use the code download mode for all memory write operations so this setting may or may not have any effect on your debugger.

Only the memory write command allows specifying instruction or data memory operations. Access to this may not be provided by your debugger interface. If not specified, memory write operations are always instruction memory.

If the instruction and data caches are both disabled, an instruction memory write will always write to physical memory and this configuration setting is ignored. If the instruction cache is disabled, instruction memory writes will always write to physical memory and the data cache will be either updated or bypassed depending on this configuration setting.

This configuration setting controls the behavior of both caches when doing instruction memory writes so that instruction memory writes can be used for all memory operations if desired.

`cf imwrop=upd_dcb`

This stands for instruction cache update, data cache bypass. An instruction memory write to an address that is valid in the instruction cache will write the value to both the instruction cache and memory. The data cache will be bypassed even if the address is valid in the data cache.

`cf imwrop=upd_dcu`

This stands for update instruction cache and update data cache. An instruction memory write to an address that is valid in both caches will write the value to both caches and physical memory.

`cf imwrop=inv_dcb`

This stands for instruction cache invalidate and data cache bypass. An instruction memory write will invalidate the instruction cache if valid and write only to physical memory. The data cache is not modified even if valid.

`cf imwrop=inv_dcu`

This stands for instruction cache invalidate and data cache update. An instruction memory write will invalidate the instruction cache if valid and write to physical memory. The data cache will also be updated if the address is valid in the data cache.

Note

Setting imwrop to upd_dcb or inv_dcb should be used with caution since dirty cache entrys in the data cache may overwrite the memory just modified by the HP processor probe.

Default: cf imwrop=upd_dcu

Part 3

Reference

4

Designing a Target System

Designing a Target System

This chapter will help you design a target system that will work with the HP processor probe.

Target System Requirements for PowerPC 603

Only the mask revision dd3 of the PowerPC 603 chip can be used with the HP processor probe.

Target systems which use any of the following modes of operation are not currently supported:

- MMU when it is used for address translation. Only physical memory addresses are accessible.
- Little-endian byte ordering; memory display/modify is always in big-endian mode. Byte swapping may be handled by the host software.
- Address parity is not generated on external address bus operations. Accesses to devices that check parity will fail.

If the target development board does not use the $\overline{\text{QACK}}$ signal (PowerPC 603 pin #235), the board must have a pull down resistor to drive this signal low. This allows the PowerPC to enter the debug state. Recommended value: 1KΩ or less.

If the target system uses reduced pinout mode, $\overline{\text{QACK}}$ must be high during $\overline{\text{HRESET}}$, but must be low to enter debug mode. If neither $\overline{\text{QACK}}$ nor $\overline{\text{QREQ}}$ are being used, these two pins can be tied together and pulled high with a 1 KΩ pullup. If $\overline{\text{QACK}}$ or $\overline{\text{QREQ}}$ is used by the target, logic must be supplied to make $\overline{\text{QACK}}$ low after $\overline{\text{QREQ}}$ is asserted so that the PowerPC can go into debug mode.

TDO, TDI, TCK, TMS and $\overline{\text{TRST}}$ signal traces between the JTAG connector and the PPC603 must be less than 3 inches long. If these signals are connected to other nodes, the other nodes must be daisy chained between

the JTAG connector at one end and the PowerPC microprocessor at the other end. These signals are sensitive to crosstalk and must not be routed along active signals such as clock lines on the target board.

The TDI, TCK, TMS and $\overline{\text{TRST}}$ signals must not be actively driven by the target system when the debug port is being used.

The $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$ and $\overline{\text{TRST}}$ signals from the JTAG connector must be logically ORed with the $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$ and $\overline{\text{TRST}}$ signals that connect to the processor on the target system. They cannot be "dotted" or "wire-ORed" on the board. The ORed signals should only reset the processor and no other devices on the target system.

The HP processor probe adds about 40 pF to all target system signals routed to the JTAG connector. This added capacitance may reduce the rise time of the $\overline{\text{SRESET}}$ or the $\overline{\text{HRESET}}$ signal beyond the processor specifications. If so, the target may need to increase the pull-up current on these signal lines.

Additional target requirements may be specified in the release notes in the "readme" file on the provided floppy disk.

Target System Requirements for PowerPC 603e

Target systems which use any of the following modes of operation are not currently supported:

- Caches cannot be enabled for debug. A problem with the current CPU chip corrupts the cache valid and LRU bits when debugging through the JTAG port. The caches must be disabled for correct operation with the HP E3494 PowerPC processor probe.
- MMU when it is used for address translation. Only physical memory addresses are accessible.
- Little-endian byte ordering; memory display/modify is always in big-endian mode. Byte swapping may be handled by the host software.
- Address parity is not generated on external address bus operations. Accesses to devices that check parity will fail.
- The TLB entries cannot be accessed from the HP E3477 PowerPC probe.
- If the processor runs to a branch to self instruction (op code 48000000H) and the instruction is at an address ending with 04H or 0CH, the Probe will not be able to soft stop the processor. If the processor doesn't soft stop, it will be "hard stopped" and an error message will be generated. Once the

processor is hard stopped, memory and register contents can be read, but the processor cannot be stepped or run at this point. A reset is required to restore operation.

If the target development board does not use the $\overline{\text{QACK}}$ signal (PowerPC 603e pin #235), the board must have a pull down resistor to drive this signal low. This allows the PowerPC to enter the state required for reading and writing processor scan string data. Recommended value: 1KΩ or less.

If the target system uses reduced pinout mode, $\overline{\text{QACK}}$ must be high during $\overline{\text{HRESET}}$, but must be low to enter debug mode. If neither $\overline{\text{QACK}}$ nor $\overline{\text{QREQ}}$ are being used, these two pins can be tied together and pulled high with a 1 KΩ pullup. If $\overline{\text{QACK}}$ or $\overline{\text{QREQ}}$ is used by the target, logic must be supplied to make $\overline{\text{QACK}}$ low after $\overline{\text{QREQ}}$ is asserted so that the PowerPC can go into debug mode.

TDO, TDI, TCK, TMS and $\overline{\text{TRST}}$ signal traces between the JTAG connector and the PPC603e must be less than 3 inches long. If these signals are connected to other nodes, the other nodes must be daisy chained between the JTAG connector at one end and the PowerPC microprocessor at the other end. These signals are sensitive to crosstalk and must not be routed along active signals such as clock lines on the target board.

The TDI, TCK, TMS and $\overline{\text{TRST}}$ signals must not be actively driven by the target system when the debug port is being used.

The $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$ and $\overline{\text{TRST}}$ signals from the JTAG connector must be logically ORed with the $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$ and $\overline{\text{TRST}}$ signals that connect to the processor on the target system. They cannot be "dotted" or "wire-ORed" on the board. The ORed signals should only reset the processor and no other devices on the target system.

The HP Processor Probe adds about 40 pF to all target system signals routed to the JTAG connector. This added capacitance may reduce the rise time of the $\overline{\text{SRESET}}$ or the $\overline{\text{HRESET}}$ signal beyond the processor specifications. If so, the target may need to increase the pull-up current on these signal lines.

Additional target requirements may be specified in the release notes in the "readme" file on the provided floppy disk.

Target System Requirements for other PowerPC Processors

For PowerPC processors other than the 603 and 603e, all target requirements are described in the "readme" file on the provided floppy disk.

Motorola MVME 160X, Ultra, Atlas and Series E Target Boards

These boards have an unpopulated header location for installing the 16-pin connector.

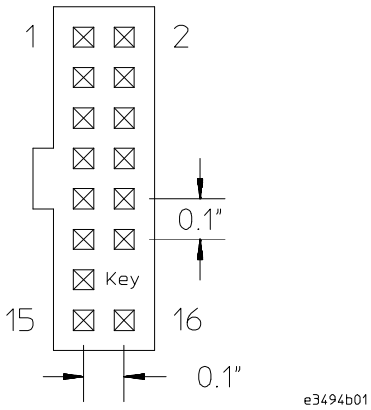
A resistor change is required to pull $\overline{QACK}$ low. The 1KΩ resistor on the $\overline{QACK}$ signal which goes between the MPC603 and the MPC105 must be changed to 10Ω. This is recommended as a short term modification for use with the HP processor probe. The 1KΩ resistor should be replaced for normal operations when the HP processor probe is no longer needed. For the MVME1603 series PM603 module this resistor is R27 on the 8018F, 8019F, 8100F and 8101F artwork. For the Atlas it is R42 on the Rev B 8115F artwork. For the Ultra, it is R10 on the 8107D and later artwork.

These boards use $\overline{DRTRY}$ mode, so the configuration entry cf drtry=on must be used if either cache is enabled. The standard boot roms that come with these boards enable the instruction cache (register HID0=00008000) so right out of the box, memory reads and writes will not work correctly and may corrupt the communications between the target board and the HP processor probe unless cf drtry is set to on or the cache is disabled.

The reset lines connected to the JTAG connector drive reset to other devices besides the CPU. This is in violation of the HP processor probe target system requirements. The consequence of this is the boot code that initializes the DRAM controller must be run from physical ROMS on the board before memory reads and writes will work. The cf reset=runrom setting must be used for correct operation of this board with the HP processor probe and valid boot ROMS that initialize the DRAM controller must be installed.

PowerPC 603 JTAG Interface Connections and Resistors

The target system should have a JTAG connector with the following dimensions:



Header Pin Number	Signal Name	I/O	PowerPC 603, 603e Pin No.[1]	Board Resistor
1	TDO	Out	198	
2	Not connected			
3	TDI	In	199	1KΩ pulldown[2]
4	$\overline{\text{TRST}}$[3]	In	202	10KΩ pullup
5	Not connected			
6	+3.3V[4]			1KΩ series[5]
7	TCK	In	201	10KΩ pullup
8	Not connected			
9	TMS	In	200	10KΩ pullup
10	Not connected			
11	$\overline{\text{SRESET}}$[3]	In	189	10KΩ pullup
12	Not connected			
13	$\overline{\text{HRESET}}$[3]	In	214	10KΩ pullup
14	KEY			
15	$\overline{\text{CHECKSTOP}}$[6]	Out	216	10KΩ pullup
16	GND			
	$\overline{\text{QACK}}$[7]	In	235	1KΩ pulldown
	L2_TEST_CLK	In	203	10KΩ pullup
	L1_TEST_CLK	In	204	10KΩ pullup
	$\overline{\text{LSSD_MODE}}$	In	205	10KΩ pullup

[1] Pin numbers are for PQFP packages.

[2] For the PowerPC 403 and 604, the TDI pullup should be 10KΩ.

[3] For the PowerPC 403, $\overline{\text{TRST}}$ and $\overline{\text{HRESET}}$ are Noconnects and the $\overline{\text{HALT}}$ line is connected to header pin 11 instead of $\overline{\text{SRESET}}$.

[4] The +3.3V signal is source from the target development board and is used as a reference signal. It should be the power signal being supplied to the processor. It does not supply power to the HP processor probe.

[5] This 1KΩ series resistor provides short circuit current limiting protection only. If the resistor is present, it should be 1KΩ or less.

[6] For the PowerPC 602 and 604 processors, this line is called $\overline{\text{CKSTP_OUT}}$.

[7] If the target development board does not use this signal, the board must have a 1KΩ pulldown resistor connected to this pin. This signal allows the HP processor probe to force the processor into soft stop mode.

5

Specifications and Characteristics

Processor Compatibility

The HP processor probe supports the Motorola/IBM PowerPC 603 (mask rev. dd3) with the E3494 firmware and 603e (mask rev dd1) with the E3477 firmware. Other mask revs of the PowerPC 603 and 603e processor are incompatible with the HP processor probe but may be available in the future. At this time, the HP processor probe can only be ordered for the PowerPC 603 or 603e. For other supported PowerPC processors, firmware is provided on the floppy disk shipped with the HP Processor Probe. See the "readme" file on the disk for details about the PowerPC processors available.

Electrical Specifications

BNC, labeled TRIGGER OUT

Output Drive Logic high level with 50-ohm load >= 2.0 V. Logic low level with 50-ohm load <= 0.4 V. Output function is selectable, see chapter 3, Configuring the HP processor probe.

BNC, labeled BREAK IN

Input Edge-triggered TTL level input (active high), 20 pf, with 2K ohms to ground in parallel. Maximum input: 5 V above $V_{CC;}$ 5 V below ground. Input function is selectable, see chapter 3, Configuring the HP processor probe.

Communications

Serial Port 9-pin female type “D” subminiature connector. RS-232 DCE to 115.2 kbaud.

10BASE-T LAN Port RJ-45 connector. IEEE 802.3 10BASE-T (StarLAN).

10BASE 2 LAN Port 50-ohm BNC connector. IEEE 802.3 10BASE2 (ThinLAN). When using this connector, the HP processor probe provides the functional equivalent of a Medium Attachment Unit (MAU) for ThinLAN.

Power Supply

Input 100-240 V, 9.75 A, 50/60 Hz, IEC 320 connector.

Output 5 V, 1.0 A

Accessory Output 100-240 V, 9.50 A, 50/60 Hz

Maximum Ratings

Characteristics for HP processor probe	Symbol	Min	Max
TDO, $\overline{\text{CHECKSTOP}}$	V_{ih}	2.0 V	5.5 V
	V_{il}	-0.5 V	0.8 V
	I_{ih}		20 µA
	I_{il}		-10 µA
	C_{in}		40 pF
TDI, TCK, TMS, $\overline{\text{TRST}}$ [1]	V_{oh} @ I_{oh} = -32 ma	2.0 V	3.3 V
	V_{ol} @ I_{ol} = 16 ma		0.4 V
	V_{ol} @ I_{ol} = 32 ma		0.5 V
	C_o		190 pF
+3.3V Power Sense [2]	V_{ih}	2.0 V	5.5 V
	V_{il}	-0.5 V	0.8 V
	I_{ih}		350 µA
	I_{il}		-10 µA
	C_{in}		40 pF
$\overline{\text{SRESET}}$, $\overline{\text{HRESET}}$	V_{oh} @ I_{oh} = -4 ma	3.0 V	3.3 V
	V_{ol} @ I_{ol} = 12 ma		0.4 V
	V_{ol} @ I_{ol} = 24 ma		0.5 V
	C_o		40 pF

[1] These signals must not be actively driven by the target system when the debug port is being used.

[2] Power Sense is used only to determine target powered status. The processor probe does not draw power from this source.

Environmental Specifications

Temperature Operating, +5 °C to +40 °C (+41 to +104 °F); nonoperating, -40 to +70 °C (-40 to +158 °F).

Altitude Operating/nonoperating 4600 m (15 000 ft).

Relative Humidity 15% to 95%.

Product Regulations

Safety

IEC 1010-1:1990+A1/EN 61010-1:1993
UL 3111
CSA-C22.2 No. 1010.1:1993

EMC

This product meets the requirements of the European communities (EC) EMC Directive 89/336/EEC.

Emissions: EN55011/CISPR 11 (ISM, Group1, Class A equipment)

Immunity: EN 50082-1	Code[1]	Notes[2]
IEC 801-2 (ESD) 4kV CD, 8kV AD	1	1
IEC 801-3 (Rad.) 3 V/m	1	
IEC 801-4 (EFT) 0.5kV Signal Lines, 1kV power	1	1

[1]Performance Codes:

1 PASS - Normal operation, no effect.
2 PASS - Temporary degradation, self recoverable.
3 PASS - Temporary degradation, operator intervention required.
4 FAIL - Not recoverable, component damage

[2]Notes:

1. The target cable with its adapter board was not attached during the ESD test. This assemmbly is ESD sensitive. Standard ESD preventative practices should be adhered to while handling the target cable assembly.

Sound Pressure Leve Not applicable

6

Updating Firmware

Updating Firmware

Hewlett-Packard formally supports only configurations that include the latest revisions of all software and firmware. Software updates can be ordered to get the latest firmware revisions.

You can update the firmware in the HP processor probe by running the prgflash.xxx utility program which downloads code from files on the host computer into Flash EPROM memory which is built-in to the HP processor probe.

If you plan to use a version of the PowerPC other than the one for which your HP processor probe is programmed, you must reprogram your HP processor probe with the appropriate firmware. See the "readme" file on the floppy disk for a list of supported processors.

Four different versions of this program are on the floppy provided with your HP Processor Probe. The program prgflash.hp7 runs on HP-UX Series 700 machines, prgflash.sun runs on Sun SPARC machines running SunOS 4.1, prgflash.sol runs on Sun SPARC machines running Solaris and prgflash.exe runs on MSDOS machines. The prgflash.xxx utility running on UNIX machines will only update the firmware over lan. On MS-DOS machines, prgflash.exe can only update the firmware over serial.

The floppy provided is in MS-DOS format and can be read directly on MS-DOS machines, HP-UX Series 700 and Solaris machines equipped with a 3.5 inch floppy drive.

To update firmware using prgflash.xxx

1. **Make a directory on your computer, change to that directory and copy the files from the floppy to that directory.**

   On HP-UX Series 700 machines, if your machine is equipped with a floppy drive, copy the file install.hp7 to this directory with the doscp command and execute it as follows:

```
mkdir ppcprobe
cd ppcprobe
doscp <floppy device>:install.hp7 .
./install.hp7 <floppy device>
```

   Where <floppy device> is the name of the floppy raw device file, typically "/dev/rdsk/0s1".

   On SUN Solaris machines, insert the floppy in the drive, run volcheck to "mount" the volume and copy the files to the current directory.

```
volcheck
mkdir ppcprobe
cd ppcprobe
cp /floppy/floppy0/* .
eject
```

   On SUN SunOS 4.1 machines, there are no standard utilities for reading MS-DOS format floppies. To find out if there are any non-standard means of reading PC format floppies on your machine, check with your system administrator.

   For MS-DOS machines, you can run prgflash.exe copy the files from the floppy drive to a directory on your hard drive.

```
md c:\hpprobe
a:
copy *.* c:\hpprobe
```

   For all UNIX machines that do not have floppy drives, you can copy the files from a LAN based PC using a LAN based file transfer utility like ftp or rcp, see your network administrator or LAN software documentation. Use binary mode when transferring the files from MS-DOS machines.

2. Run the **prgflash.xxx** command.

To run prgflash.xxx on Unix workstations

Use the command:

`prgflash.xxx [-v] [probe IP addr] [product to update]`

where xxx is hp7, sun or sol as described above.

The -v option means "verbose". It causes progress status messages to be displayed during operation.

The probe IP addr option is the ip address of the HP processor probe in either dotted decimal form or alias form (from /etc/hosts).

The product to update option names the products whose firmware is to be updated. For the PowerPC 603, the product name is "e3494" and for the PowerPC 603e, the product name is "e3477". Firmware for other members of the PowerPC family may also be provided on the floppy, check the "readme" file on the disk for more details.

If you enter the prgflash.xxx command without all options, it becomes interactive. You must always supply the "probe IP addr" option. If you don't include the "product to update" option, it displays the products which have firmware update files on the system and asks you to choose one. It will first look in the current directory for product files, if it does not find any there, it will check the directory $HP64000/inst/update if the $HP64000 environment variable is set or /usr/hp64000/inst/update if $HP64000 is not set. You can abort the interactive prgflash.xxx command by pressing <CTRL>c.

Example

To use update the firmware for the PowerPC 603 in "myprobe" from a series 700 HP-UX machine, you could enter the following command:

```
prgflash.hp7 -v myprobe E3494
```

To run prgflash.exe on MS-DOS

Use the command:

`prgflash [-v] [emul_com] [product to update]`

The -v and [product to update] options are the same as described above.

The [emul_com] option should be emul_com1, emul_com2, emul_com3, or emul_com4 which correspond to the com1, com2, com3 and com4 ports. The serial parameters for these ports is configured in the file 64700tab. The only configuration option that should be changed is the baud rate which should

match the baud rate specified by the configuration switches on the processor probe. These rate settings are described on the label on the bottom of the processor probe.

On MS-DOS, you can enter prgflash without any options and you will be prompted for the serial port and "product to update" option. It will first look in the current directory for product files, if it does not find any there, it will check the directory $HP64700\update if the $HP64700 environment variable is set or \hp64700\update if $HP64700 is not set. You can abort the interactive prgflash.exe command by pressing <CTRL>c.

Example

To use update the firmware for a PowerPC 603e over com1, you could enter the following command:

```
prgflash -v emul_com1 E3477
```

Prgflash.xxx will print "Flash programming SUCCEEDED" and return 0 if it is successful; otherwise, it will print "Flash programming FAILED" and return a nonzero (error).

You can verify the update by displaying the firmware version information.

To display current firmware version information

- Use **telnet** or a terminal emulator to access the built-in "terminal interface" and use the **ver** command to view the version information for firmware currently in the HP processor probe.

If the firmware doesn't appear to be updated

Though Flash EPROM is very reliable, it can fail. If the HP processor probe determines the Flash EPROM is not working, it will try to use the boot code in its Flash EPROMs. The only useful operation the boot code allows is running prgflash.

- ☐ Make sure the current version information is correct by comparing it with the version numbers of the update software.
- ☐ Try updating the firmware again.

  If none of these steps solves the problem, contact your local HP Representative.

If there is a power failure during a firmware update

If there is a power glitch during a firmware update, some bits may be lost during the download process, possibly resulting in an HP processor probe that will not boot up.

- ☐ Set switch S4 to OPEN, then cycle power. This tells the HP processor probe to ignore everything in the Flash EPROM except the boot code.
- ☐ Repeat the firmware update process.
- ☐ Set switch S4 to CLOSED, then cycle power. This restores the HP processor probe to its normal mode.

7

Solving Problems

Solving Problems

If you have problems with the HP processor probe, your first task is to determine the source of the problem. Problems may originate in any of the following places:

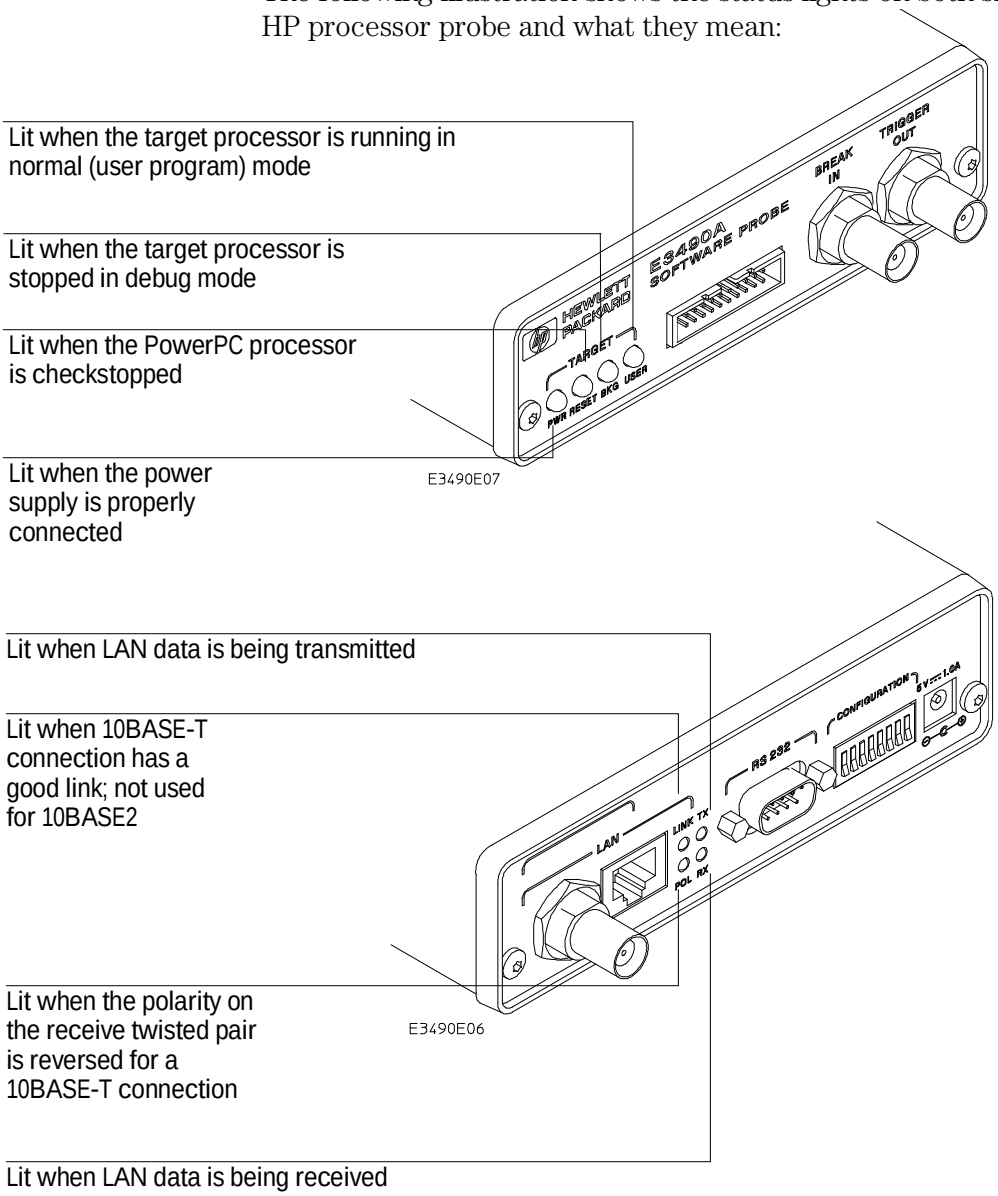
- The HP processor probe itself
- The connection between the HP processor probe and the target system
- The target system
- The connection between the third party debugger and the HP processor probe

You can use two means to determine the source of the problem:

- The status lights on the HP processor probe
- The HP processor probe "performance verification" tests

Status lights

The following illustration shows the status lights on both sides of the HP processor probe and what they mean:



Status Lights

The HP processor probe communicates various modes and error conditions via the status lights. The meanings of the status lights are shown on the previous page.

The following table gives more information about the meaning of the power and target status lights.

❍ = LED is off
● = LED is on
✳ = Not applicable (LED is off or on)

Power/Target Status Lights

Pwr/Target LEDs	Meaning
❍❍❍❍	HP processor probe is not connected to power supply
●❍❍❍	No target system power, or HP processor probe is not connected to the target system
●❍●●	Only boot firmware is good (other firmware has been corrupted)
●●❍❍	PowerPC CPU is in a checkstopped state. The CPU must be reset before it can be run or stepped from this state but register and memory access is available.
●❍●❍	PowerPC CPU is stopped in the debug mode
●❍❍●	PowerPC CPU is executing user code.
●●●●	PowerPC CPU is in an unknown state. A reset from the HP processor probe is required to clear this state.

Problems with the LAN Interface

If you cannot verify LAN communication

If you cannot verify connection using the procedure in "To verify LAN communication", or if the commands are not accepted by the processor probe:

- ☐ Make sure that you have connected the HP processor probe to the proper power source and that the power light is lit.
- ☐ Make sure that the LAN cable is connected. Refer to your LAN documentation for testing connectivity.
- ☐ Make sure that only one of the LAN ports is connected.
- ☐ Make sure the HP processor probe communication configuration switches are set correctly. Unplug the HP processor probe power cord, then plug it in again to make sure the switch settings are read correctly by the HP processor probe.
- ☐ Make sure that the HP processor probe's IP address is set up correctly. Use the RS-232 port to verify this that the IP address is set up correctly. When you are connected to the RS-232 port, run performance verification on the HP processor probe's LAN interface with the "pv" command.
- ☐ It's also possible for there to be a problem with the HP processor probe firmware while the LAN interface is still up and running. In this case, you must reboot the HP processor probe by disconnecting power to the HP processor probe and reconnecting it again.

- Make sure that the lan cable is a good cable, try replacing it with a different cable.

If you have LAN connection problems

- If the HP processor probe does not accept commands from the host computer:

  1. Check that switch S1 is "0" (attached to LAN, not RS-232).

  2. Check that switch S5 is in the correct position for your LAN interface (either 10BASE2 or 10BASE-T).

  (Remember: if you change any switch settings, the changes do not take effect until you cycle power.)

- If the HP processor probe still does not respond, you need to verify the IP address, gateway address and subnet mask of the HP processor probe. To do this, connect the HP processor probe to a terminal or terminal emulator (see page 21), change the switch settings so it is connected to RS-232, and enter the "lan" command. The output looks something like this:

```
lan is enabled using BNC
  lan -i 192.5.24.116
  lan -g 192.5.24.1
  lan -p 6470
  Subnet Mask: 255.0.0.0
  Ethernet Address: 08000909BAC1
```

  "lan -i" shows the internet address is 192.5.24.116 in this case. If the Internet address (IP) is not what you expect, you can change it with the "lan -i <new_IP>" command.

  "lan -g" shows the gateway address. Make sure it is the address of your gateway if you are connecting from another subnet. A gateway address of 0.0.0.0 is acceptable if all connections will be on the same subnet as the processor probe.

  "lan -p" shows the port is 6470. If the port is not 6470, you must change it with the "lan -p 6470" command (unless you have deliberately set the port number to a different value because of a conflict).

  The subnet mask determined from the network is displayed but cannot be changed. If the subnet mask is incorrect, then one or more devices on your network have incorrect subnet masks that should be corrected. Connecting a

terminal to the serial port during powerup of the probe will display the IP addresses of all devices with subnet masks differing from the first subnet mask received. The subnet mask displayed is only valid if the probe is connected to the LAN and the LAN is enabled for the correct connector.

If the "POL" LED is lit

The "POL" LED indicates that the polarity is reversed on the receive pair if you are using a 10BASE-T connection. The HP processor probe should still work properly in this situation, but other LAN devices may not work.

If it takes a long time to connect to the network

- **Check the subnet masks on the other LAN devices connected to your network. All of the devices must be configured to use the same subnet mask. Different subnet masks on the same subnet is not a supported configuration.**

  You may be able to continue using the HP processor probe if you get subnet mask error messages (seen over the serial port at powerup) if the PowerPC generally gets the correct subnet mask.

  The HP processor probe automatically sets its subnet mask based on the first subnet mask it detects on the network. If it then detects other subnet masks, it will generate error messages.

  If there are many subnet masks in use on the local subnet, the HP processor probe may take a very long time to connect to the network after it is turned on.

  To "clean up" the network, connect a terminal to the HP processor probe. You can then see error messages which will help you identify which devices on the network are using the wrong subnet masks.

Problems with the Serial Interface

If you cannot verify RS-232 communication

If the HP processor probe prompt does not appear in the terminal emulator window:

- Make sure that you have connected the HP processor probe to the proper power source and that the power light is lit.
- Make sure that you have properly configured the data communications switches on the HP processor probe and the data communications parameters on the host computer. You should also verify that you are using the correct cable.

  The most common type of data communications configuration problem involves the configuration of the HP processor probe as a DTE device instead of as a DCE device. If you are using the wrong type of cable, no prompt will be displayed.

  A cable with one-to-one connections will work with a PC or an HP Series 700 workstation.

  If serial communications are working to some extent but you are getting serial port overrun error messages from the probe, make sure you have enabled Hardware Handshaking on both the probe and the host computer. Also, make sure lan is disabled with the switch on the probe. If you still receive these errors, you should try using a slower baud rate.

If you have RS-232 connection problems with the MS Windows Terminal program

- Remember that Windows 3.1 only allows two active RS-232 connections at a time. To be warned when you violate this restriction, choose

Always Warn in the Device Contention group box under 386 Enhanced in the Control Panel.

- Use the "Terminal" program (usually found in the Accessories windows program group) and set up the "Communications..." settings as follows:

  ```
  Baud Rate: 9600 (or whatever you have chosen for the
  processor probe)
  Data Bits: 8
  Parity: None
  Flow Control: hardware
  Stop Bits: 1
  ```

  When you are connected, hit the Enter key. You should get a prompt back. If nothing echos back, check the switch settings on the HP processor probe.

- If the switches are in the correct position and you still do not get a prompt when you hit return, try turning OFF the power to the HP processor probe and turning it ON again.

- If you still don't get a prompt, make sure the RS-232 cable is connected to the correct port on your PC, and that the cable is appropriate for connecting the PC to a DCE device.

  With certain RS-232 cards, connecting to an RS-232 port where the HP processor probe is turned OFF (or is not connected) will hang the PC. The only way to get control back is to reboot the PC. Therefore, we recommend that you always turn ON the HP processor probe before attempting to connect via RS-232.

Problems with the HP Processor Probe Itself

To run the power up self test

1 Unplug the HP processor probe, then plug it in.

2 Watch the status lights. They should show the following pattern:

❍ = LED is off
● = LED is on
✳ = Not applicable (LED is off or on)

Normal sequence during power up self test

	Pwr/Target LEDs	Meaning
1	●●●●	Initial power up, system reset
2	●❍❍❍	XILINX array initialized successfully
3	●❍❍●	XILINX array tested successfully
4	●❍●❍	BOOT ROM space tested successfully
5	●❍❍●	GENERIC ROM space tested successfully
6	●❍●❍	DRIVER ROM space tested successfully
7	●❍❍●	RESERVED ROM space tested successfully
8	●❍●❍	RAM tested successfully
9	●❍●●	LAN internal feedback tested successfully
10	●❍●●	Start system, load drivers, initialize LAN

If the power up self test fails, the RESET LED will flash the number of the test, then stay lit.

If any of the LEDs fail to change, there is a system failure.

Following power up, the LEDs will enter one of the following states:

●❍❍❍	No target system power, or HP processor probe is not connected to the target system, or
●❍❍●	PowerPC is running user code

●●○○	PowerPC is checkstopped
●●●●	PowerPC is in an unknown state
●○●●	Only the boot ROM was used; other firmware in the Flash EPROM has been corrupted

Starting a user interface will change the pattern to the one requested by the interface.

If the power up self tests fail, try the following:

- ☐ Check and reset the LAN address as shown in the "Connecting to the Host Computer chapter. LAN powerup failures will occur if the HP processor probe does not have a valid Link Level Address and IP Address.
- ☐ Disconnect all external connections, including the LAN, serial (RS-232), and BNC Break and Trigger cables, then cycle power.
- ☐ To ensure that the firmware is working as it should, reprogram the firmware, then cycle power.

To execute the built-in performance verification test

Besides the powerup tests, there are additional performance verification tests available. A list of these tests is available with the command "pv -l".

Most of these tests can be invoked from a terminal mode window in a debugger interface or by telnetting to the probe. The LAN tests can only be executed through the RS-232 port.

To perform the PV tests from a lan connection:

1. Disconnect the target cable from the target system, and attach the terminator to the end of the target system cable.
2. To execute the all the tests one time type:

   ```
   pv 1
   ```

   (the lan tests will not be executed from a lan connection). The results will appear on screen.

LAN Tests

The LAN tests can only be executed through the RS-232 port. The remainder of this section assumes that the tests are being run from a terminal emulator connected to the RS-232 port.

For the BREAK IN, TRIGGER OUT BNC FEEDBACK TEST, connect a coaxial cable between BREAK IN and TRIGGER OUT
For the TARGET PROBE FEEDBACK TEST, replace target cable with feedback connector E3490-61604

1. Set all of the switches to OPEN.

   This is standard RS-232 at 9600 baud which can be connected directly to a 9 pin RS-232 interface that conforms to the IBM PC-AT 9 pin standard.
2. Use a terminal emulator to connect to the HP processor probe.
3. Enter the **pv** command.

   Options available for the "pv" are explained in the help screen displayed by typing "help pv" or "? pv" at the prompt. The help screen output will appear similar to the screen shown on the following page:

```
M>? pv

  pv <options> <count> - Execute the performance verification diagnostics.

    pv              - display pv warning message
    pv -l           - list available pv tests only (do not execute)
    pv -d           - execute emulator subsystem tests only
    pv -t <[-y]>    - select system test number <x> or range <x-y> only
    pv -t *         - select all system tests
    pv -d -t        - select emulation subsystem test  only
    pv -v <verbose> - set verbose level;  valid levels: 0-9
    pv -f           - force tests to execute (HP internal use only)
    pv -n           - do not initialize system (HP internal use only)
    pv <count>      - execute diagnostics <count> number of times,
                      <count> of 0 repeats until keyboard break
  --- SYSTEM SETUP ---
    o Connect a coaxial cable between the BREAK IN and TRIGGER OUT BNCs.
    o Replace the target cable with the SELFTEST LOOPBACK connector.
    o To execute the LAN Feedback tests, disconnect the LAN BNC connector
      from the network and terminate with two 50 ohm terminators on a tee.
      (Run pv from the RS232 Port with LAN disabled)

  *** WARNING *** This command performs a system initialization after
                  all pv execution is completed.
M>
```

Examples: To execute both tests one time:

```
pv 1
```

To execute test 2 with maximum debug output repeatedly until a ^C is entered:

```
pv -t2 -v9 0
```

To execute tests 3, 4, and 5 only for 2 cycles:

```
pv -t3-5 2
```

The tests available through this command can be displayed as follows:

```
c>pv -l
  Tests Available in Performance Verification;
    Test # 1: Powerup PV Results
    Test # 2: LAN 10Base2 Feedback Test
    Test # 3: LAN 10BaseT Feedback Test
    Test # 4: Break In and Trigger Out BNC Feedback Test
    Test # 5: Target Probe Feedback Test
    Test # 6: Boundary Scan Master Test
c>
```

The results on a good system are as follows:

```
c>pv 1

  Testing: HPE3499A Series Emulation System
    Test # 1: Powerup PV Results                          passed!
    Test # 2: LAN 10Base2 Feedback Test                   passed!
    Test # 3: LAN 10BaseT Feedback Test                   passed!
    Test # 4: Break In and Trigger Out BNC Feedback Test  passed!
    Test # 5: Target Probe Feedback Test                  passed!
    Test # 6: Boundary Scan Master Test                  passed!
  PASSED  Number of tests: 1          Number of failures: 0

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  HPE3499A Series Emulation System
    Version:   A.06.00 14Feb96
    Location:  Generics

  HPE3494A PowerPC 603 (rev3) JTAG Emulator
    Version:   A.01.04 28Feb96

?>
```

You may get an error like "!ERROR 172! Bad status code (0xff) from the hard reset sequence" just before the prompt. This is because the selftest loopback connector is installed instead of being connected to a real PowerPC target system. You will also get either a "c>" or "?>" prompt for the same reason, this is normal and expected. Any errors after the "PASSED Number of tests: 1 Number of failures: 0" line can be ignored.

There are some things you can do if a failure is found on one of these tests. Details of Failure can be obtained through using a verbose level of 2 or more.

TEST 2: LAN 10BASE2 Feedback Test

For LAN 10BASE2 test, the following is an example of a failure which is *not* caused by a broken HP processor probe.

```
c>pv -t2 -v2 1

  Testing: HPE3499A Series Emulation System
    Test # 2: LAN 10Base2 Feedback Test                    failed!
      FAILED - no lan connection (LAN probably not terminated)
  FAILED  Number of tests: 1           Number of failures: 1
```

Check to see that the port under test has a good cable connected to it and that the cable is properly terminated with a 50 ohm terminator on each end of the overall cable.

```
c>pv -t2 -v2 1

  Testing: HPE3499A Series Emulation System
    Test # 2: LAN 10Base2 Feedback Test                    failed!
      FAILED due to excessive collisions
  FAILED  Number of tests: 1           Number of failures: 1
```

The most common cause of this problem is poor termination of the cable or failure to remove the port under test from the LAN before performing the test. Check to see that the terminators are good (50 Ohms) and that you are isolated from any traffic on a system LAN.

```
c>pv -t2 -v2 1

  Testing: HPE3499A Series Emulation System
    Test # 2: LAN 10Base2 Feedback Test                    failed!
      FAILED - invalid Ethernet address in EEPROM
  FAILED  Number of tests: 1           Number of failures: 1
```

First check to see that a correct LLA and IP address have been set in the virtual EEPROM through the "lan" command. If the "lan" command shows bad information for the LLA and IP, then try to set them to correct values. If you are unable to set them to correct values, their is a failure in the FLASH ROM which requires service from HP.

Test 3: 10BaseT Feedback Test

```
c>pv -t3 -v2 1

  Testing: HPE3499A Series Emulation System
    Test # 3: LAN 10BaseT Feedback Test                    passed!
  PASSED  Number of tests: 1          Number of failures: 0
```

In addition to the internal checks performed in Test 2, this test also checks for shorts on the cable connected to the network. If this test fails, disconnect the cable and run the test again. If it then passes, the cable is faulty. If it still fails, it requires service from HP.

If the HP processor probe passes this "pv" test, additional testing can be performed through exercising the connection to the network. To run this test, set configuration switch 1 and switch 5 to OPEN, all other configuration switches CLOSED (this enables LAN using 10BaseT). Cycle power and wait for 15 to 30 seconds. Then "ping" the HP processor probe from your host computer or PC. See the LAN documentation for your host computer for the location and action of the "ping" utility. If the HP processor probe fails to respond to the "ping" request, verify that the lan parameters (IP address and gateway address) are set correctly and that your host computer recognizes the IP address of the HP processor probe. If all else is good, then failure to respond to ping indicates a faulty HP processor probe.

TEST 4: Break In and Trigger Out BNC Feedback Test

```
c>pv -t4 -v2 1

  Testing: HPE3499A Series Emulation System
    Test # 4: Break In and Trigger Out BNC Feedback Test    failed!
      Break In not receiving Break Out HIGH
  FAILED  Number of tests: 1          Number of failures: 1
```

Before returning to HP, check to ensure that you have connected a good Coaxial cable between the two BNCs. If the cable is good, the probe bad.

TEST 5: Target Probe Feedback Test

A verbose output on this test can be extensive. For example, the following is the output of this test if you forget to plug in the E3490-61604 connector.

```
p>pv -t5 -v2 1

  Testing: HPE3499A Series Emulation System
    Test # 5: Target Probe Feedback Test                    failed!
      Bad 20 Pin Status Read when unconnected = 0x7fb7
                               Expected Value = 0xffb7
      Bad 20 Pin Status Read when connected= 7fb7
                              Expected Value = 0x7fb7
      Output 19 Low not received on Input 11
      Output 11 Low not received on Input 19
      Output 13 Low not received on Input 1
      Output 12 High not received on Input 6
      Output 12 and Input 6 not pulled high on release
      Output 8 Low not received on Input 10
      Output 7 Low not received on Input 20
      Output 4 Low not received on Input 14
      Output 2 Low not received on Input 18
  FAILED  Number of tests: 1           Number of failures: 1
```

If the you get a verbose output like this, check to make sure that the self test loopback connector was connected properly.

Returning the HP processor probe to Hewlett-Packard for Service

To return the HP processor probe to Hewlett-Packard

1. **Follow the procedures in this chapter to make sure that the problem is caused by a failure in the HP processor probe or power supply, not by configuration or communication problems.**
2. **Call your nearest HP sales office. Ask them for the address of the nearest HP service center.**

   A list of HP sales offices is included at the back of this binder.
3. **Package the HP processor probe or the power supply and send it to the HP service center.**

   If only the HP processor probe is broken, keep the power supply and cables . If only the power supply is broken, keep the HP processor probe and cables.
4. **When the HP processor probe or the power supply has been replaced, it will be sent back to you.**

   The unit returned to you will have the same serial number as the unit you sent to HP.

To obtain replacement cables

- Order one of the following parts from your HP sales office:

Cable part numbers

Exchange Assemblies

Part Number	Description
E3494-69401	Program Assembly

Replacement Assemblies

Part number	Description
0950-2372	Power Supply
E3494-61601	16-conductor cable assembly
E3490-61604	self-test connector
E3494-66502	transition board
5061-7342	7 ft. 10Base-T point-to-point network cable assembly

To obtain replacement cables

Index

A
address, IP
  See IP address
altitude specifications, 68
Atlas target board, 61
AUI connector on LAN interface, 9

B
BKG light, 77
BNC, LAN, 9, 66
BOOTP, 17–18

C
cable
  LAN, 19
  power, 8–9
  replacing, 93–94
  serial, 22–23
cables, 28
clocks
  specifications, 66–67
connecting to the host workstation, 3–26
connecting to the target system, 27–30
connection problems, LAN, 80
connection problems, RS-232, 82–83
connector, 28
  10BASE-T, 66
  10BASE2, 66
  serial, 66

D
data communications
  specifications, 66
DCE or DTE selection and RS-232 cable, 82

E
ethernet address, 11

F
files
  workstation setup, 25
firmware version, 73
firmware, updating, 70
Flash EPROM, 70

G
gateway, 80
gateway address, 12, 14–15

H
HP 64700 LAN port number, 80
HP 64700 switch settings, LAN, 80
HP 64700 switch settings, RS-232, 82–83

I
IEEE 802.3, 9
internet address
  See IP address
IP address, 9–11, 14–15, 79–80
ipconfig700, 14–16

J
JTAG connections, 62–64

L
LAN connection problems, 80, 89–90
LAN interface, 9
LAN parameters, configuring, 9
  BOOTP, 17–18
  ipconfig700, 14–16
  terminal interface, 11–13
lights
  See status lights
link beat, 19
link level address, 11, 15, 18
LINK light, 77

M
mask, subnet, 81
MAU, 9, 66

P
performance verification test, 86–91
ping command, 80
POL light, 77, 81
port number, 12
power cord, 5, 8–9
power failure during firmware update, 74
power up self test, 84–85
prgflash, 70
probe, testing, 91

R
RESET light, 77
resistors for JTAG connection, 62–64
restriction on number of RS-232 connections, 82–83
RS-232
  See serial connection

S
self test, 84–85
self-test connector, 28
serial connection
  DCE or DTE selection, 82
  number of connections, 82–83
  problems, 82–83
  setting up, 21
  verifying, 24–26
service ports, TCP, 12
service, how to obtain, 92
specifications
  altitude, 68
  clock, 66–67
  data communications, 66
  temperature, 68
  trigger in/out, 66
StarLAN, 9, 19
status lights, 78, 84–85
subnet mask, 9, 80–81
switches
  bootp, 18
  serial configuration, 22

T
target system
  connecting to, 28
telnet, 20, 79
temperature specifications, 68
terminal (MS Windows program), 82–83
terminal interface, 20
  LAN parameters, setting, 11–13
ThickLAN, 9
ThinLAN, 9, 66
transition board, 28
trigger
  in/out specifications, 66
turning on power, 8–9
TX light, 77

U
Ultra target board, 61
update, firmware, 70
USER light, 77

V
version, firmware, 73

W
workstation files, 25

DECLARATION OF CONFORMITY

according to ISO/IEC Guide 22 and EN 45014

Manufacturer's Name: Hewlett-Packard Company

Manufacturer's Address: Colorado Springs Division
1900 Garden of the Gods Road
Colorado Springs, CO 80907 U.S.A.

declares, that the product

Product Name: Processor Probe

Model Number(s): E3494A

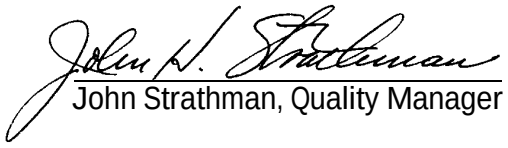
Product Option(s): All

conforms to the following Product Specifications:

Safety:	IEC 1010-1:1990+A1/EN61010-1:1993	
	UL 3111	
	CSA-C22.2 No. 1010.1:1993	
EMC:	CISPR 11:1990 / EN 55011:1991	Group 1, Class A
	IEC 555-2:1982 + A1:1985 / EN 60555-2:1987	
	IEC 555-3:1982 + A1:1990 / EN 60555-3:1987 + A1:1991	
	IEC 801-2:1991 / EN 50082-1:1992	4 kV CD, 8 kV AD
	IEC 801-3:1984 / EN 50082-1:1992	3 V/m, {1kHz 80% AM, 27-1000 MHz}
	IEC 801-4:1988 / EN 50082-1:1992	0.5 kV Sig. Lines, 1 kV Power Lines

Supplementary Information:
The product herewith complies with the requirements of the Low Voltage Directive 73/23/EEC and the EMC Directive 89/336/EEC.
This product was tested in a typical configuration with Hewlett-Packard test systems.

Colorado Springs, 6/15/94



John Strathman, Quality Manager

European Contact: Your local Hewlett-Packard Sales and Service Office or Hewlett-Packard GmbH, Department ZQ / Standards Europe, Herrenberger Strasse 130, D-71034 Böblingen Germany (FAX: +49-7031-14-3143)

Product Regulations

Safety IEC 1010-1:1990+AMD 1:1992
UL 3111

EMC This product meets the requirement of the European Communities (EC) EMC Directive 89/336/EEC.

Emissions EN55011/CISPR 11 (ISM, Group 1, Class A equipment)
SABS RAA Act No. 24 (1990)

Immunity EN50082-1	Code[1]	Notes[2]
IEC 801-2 (ESD) 4kV CD, 8kV AD	3	
IEC 801-3 (Rad.) 3 V/m	1	
IEC 801-4 (EFT) 1kV	1	

[1] Performance Codes:
1 PASS - Normal operation, no effect.
2 PASS - Temporary degradation, self recoverable.
3 PASS - Temporary degradation, operator intervention required.
4 FAIL - Not recoverable, component damage.

[2] Notes:
(none)

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Safety Symbols



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Hazardous voltage symbol.



Earth terminal symbol: Used to indicate a circuit common connected to grounded chassis.

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The Warning sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in personal injury. Do not proceed beyond a Warning sign until the indicated conditions are fully understood and met.

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