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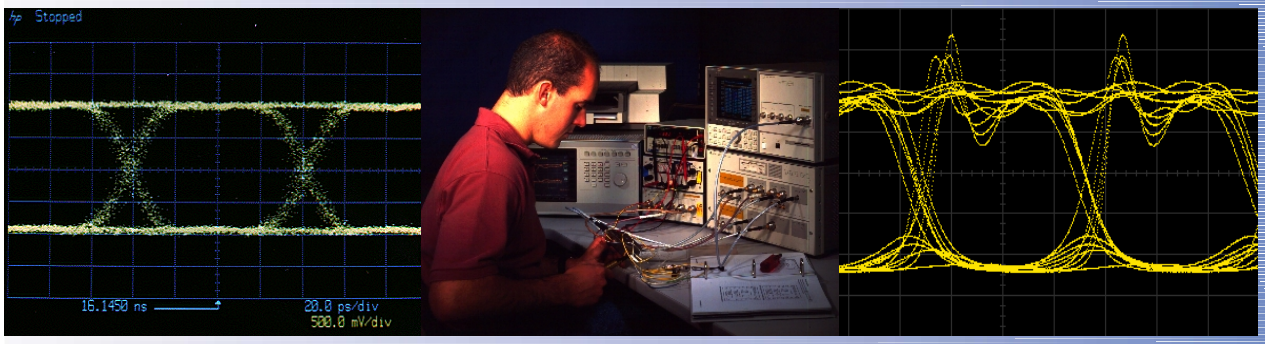
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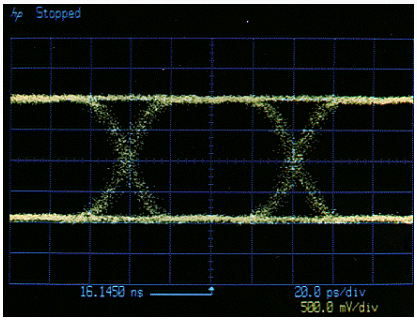


Accurately characterize your Gbit systems and devices

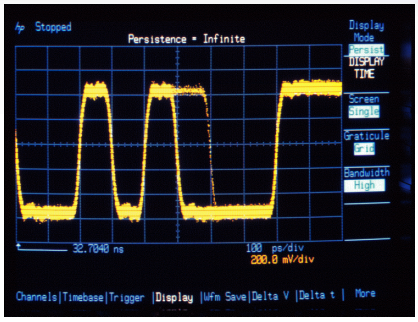
HP 71612B 12 Gb/s error performance analyzer

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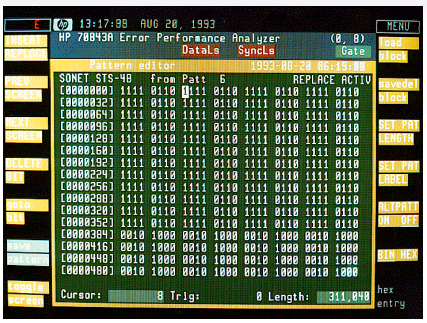
Design and manufacture reliable Gbit transmission modules and system hardware



Fast transition time and low jitter of the data output eye diagram at 12 Gb/s.



See captured errored bit on an oscilloscope.



8 Mbit programmable memory allows creation of complete, structured SONET and SDH frames on the HP 71612B analyzer's display.

Use the HP 71600 Series of Gbit testers to measure bit error ratio (BER) and to verify the performance and quality of your components and system hardware.

- Lightwave submarine cable systems
- SONET/SDH synchronous network transmitters and receivers
- Gbit datacom serial links
- Lasers and photodetectors
- High-speed logic devices
- Optical amplifiers and modulators
- Decision circuits
- Multiplexers and output drivers.

For high-performance pattern generation and error analysis across the entire 100 Mb/s to 12 Gb/s range, use an HP 71612B error performance analyzer with optional low-rate clock.

Thoroughly test and verify device performance

When looking at pulse shapes, eye diagrams and waveform distortions, use the pattern generator with a high-speed oscilloscope from the HP 83480 Series for characterizing components up to 12 Gb/s.

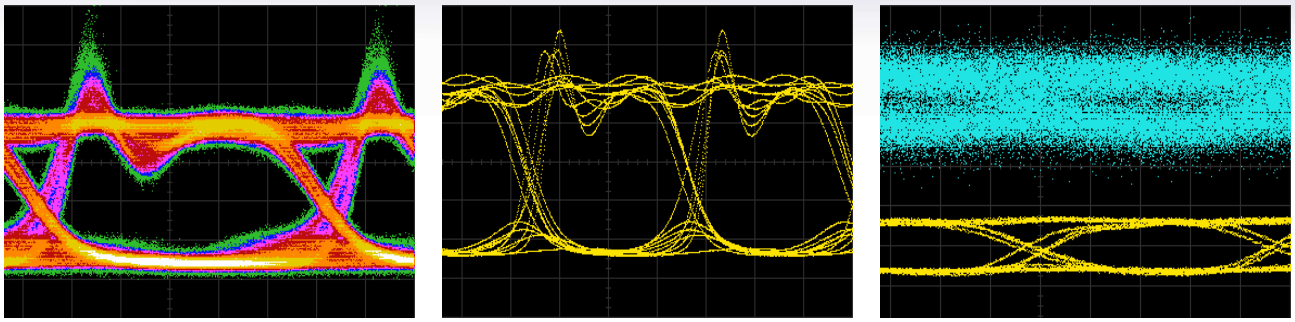
Both pattern generator and error analyzer provide a wide range of PRBS and user-defined patterns, with versatile triggering facilities. And to help you identify the address of the errored bits use optional error location analysis. Once the position of an errored bit is identified, the flexible triggering features can be used to view the errored pattern on an oscilloscope for further diagnosis.

The HP 71600 Series of Gbit testers help you be more competitive in today's rapidly developing global communications marketplace

- Exceptional waveform performance (even with reflective or poor terminations)
- Display maybe totally dedicated to pattern editing
- Error location analysis identifies individual errored bits in custom patterns; measure bit, block or total pattern BER
- Flexible pattern trigger allows oscilloscope to be triggered on any bit in custom pattern, allowing errored bits to be displayed on oscilloscope
- Cost effective addition of 12 Gb/s jitter analysis with the HP 71501C jitter analyzer
- Eye line display with HP 83480A communications analyzer
- Q measurement and eye-contour analysis with HP E4543A application software.

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Design better lightwave and Gbit devices



Optional, powerful eye analysis features are enabled when the HP 83480A is used with an HP 71600 Series pattern generator. HP Eye line mode allows recovery of low level eye diagrams from the noise, and display of the eye diagram as continous traces instead of dots. (Above example shows unfiltered laser output.)

Create powerful, practical test patterns

Perform real-time editing of your longest test patterns, too. Use the efficient, on-screen pattern editor to copy, cut, and paste at the touch of a key, then save patterns to the non-volatile memory or to the integral flexible disk. The large CRT displays in binary or hex, as you wish.

Thoroughly stress test components and sub-systems

Use your own patterns that accurately represent the type of signal carried by a transmission system.

Simulate multiple SONET/SDH frames, and check out alarms and frame alignment circuits. The error performance analyzer has over 8 Mbit of user-programmable memory. This is large enough for your most complex, structured test patterns and ideal for up to six OC-192/ STM-64 frames.

Efficiently edit and transfer patterns off-line

To help you start testing, we've included a disk with sample SONET/SDH frames and with clock-recovery stress patterns. In addition, use HP E4544A STM-64/OC-192 functional test application software with a personal computer off-line to create, edit, and store your own SONET/SDH test patterns. This way, it's also easy to exchange test patterns among your other test stations.

Easily investigate pattern-dependent errors

It's often important to know how devices and systems such as line terminals and multiplexers respond to sudden changes of pattern. So, use the "hitless" pattern switch to change error-free between two patterns. Each may be up to 4 Mbit long.

Improve productivity – set up and measure fast

The auto-decision error detector threshold setting, and auto-phase alignment simplify measurements for you.

They quickly and automatically locate the optimum decision point in the eye, clearly displaying eye width and height for user-defined error ratio thresholds.

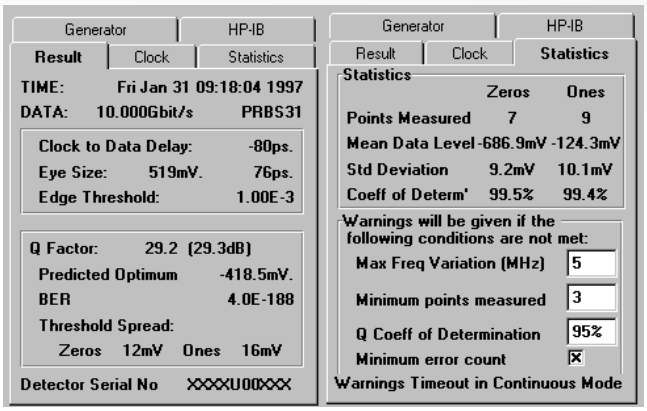
View only the measurements of interest to you by building a display from any of the set of standard measurements.

Improve device performance specifications

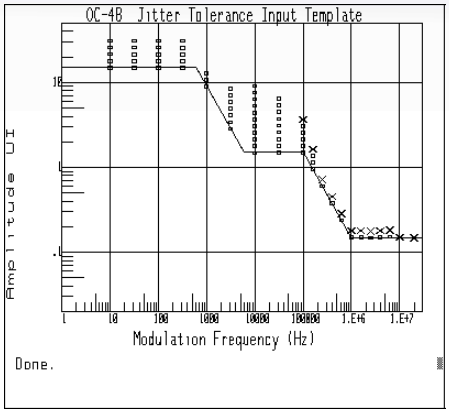
When making accurate measurements on critical devices you need the very fast transition times and low jitter capability typical of an HP 71612B error performance analyzer.

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A host of powerful additonal capabilities



Perform Q measurements using HP E4543A application software.



Create a frequency agile jitter analysis system that can work at any rate up to 12 Gb/s.

Simulate long-distance testing

Make reliable fiber cable tests by simulating long runs using a short fiber loop on the bench. The fast PRBS synchronization algorithm allows you to make reliable BER tests using burst gating. Now there's no need for you to make up bulky and expensive cable drums for your fiber testing.

Fully evaluate system performance

You'll find there is comprehensive bit error analysis to characterize performance fully. The simultaneous analysis of both errored ones and errored zeros is especially useful for locating sources of errors.

Quickly find out what effect those small circuit adjustments have on error ratio. The error-bar display with audio output provides an easy way for you to adjust devices for minimum errors without the need to interpret figures. And, continuously updated delta error count and delta error ratio measurements conveniently track each minor adjustment you make.

Find out how to improve your products and reach tomorrow's marketplace today

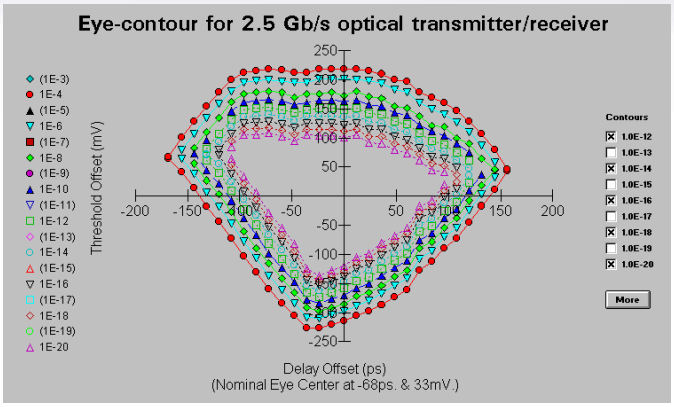
Flexible gating

Increase the value of long-term, unattended trials on prototype systems by defining total measurement period by time, number of bits received or number of errors measured. Print your choice of informative results summaries at regular intervals on an external printer.

Application software

Enhance the flexible gating capability with the HP E4543A application software to perform Q-factor measurements, or generate eye-contour diagrams to 10^{-20} to reveal even the smallest degradations in the signal, quickly and efficiently.

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Use HP E4543A application software to derive eye contours to 10^{-20} BER from Q measurement.



Error location anlaysis has identified bit 57 of a long, repetitive pattern to be in error. The preceding 28 bits and three following bits are also displayed. The separate analysis of 1→0 and 0→1 errors helps you locate sources of errors. If you need to view more of the pattern that may have caused the error, the pattern editor is on hand to let you view all of the pattern.

Go even further

Finally, extend your ability to evaluate system performance by adding the HP 71501C jitter analyzer to create a frequency agile jitter analysis system that can work at any rate up to 12 Gb/s.

For more information refer to related products section on rear cover.

Make Gbit test interfacing easy

When measuring device distortion, or testing differentially driven components, you will value the independent control you have of the pattern generator's dc-coupled complementary clock and data outputs – indispensable for accurate characterization of optical devices.

To avoid damage when changing sensitive devices in test fixtures, use the data output on/off control to remove the data signal.

If you're responsible for the research, development or manufacturing test of Gbit lightwave and digital semiconductor components, devices and sub-systems, give HP a call – today.

Error location analysis

Makes it easier for you to find the source of systematic errors — Vital when you're under continuous pressure to develop more reliable high-speed components and subsystems.

- **Bit BER**
  Locate the cause of systematic errors causing a specific bit to change value. Just specify any bit in a user-defined pattern and perform bit error measurements upon it.
- **Block BER**
  Essential when trying to locate the cause of systematic errors which affect longer runs of bits, for example a corrupt header in a SONET or SDH frame. Perform bit error rate measurements on a range of bits within a user-defined pattern.
- **Error-location capture**
  Helps you discriminate between random and systematic errors. In a user-defined pattern, automatically highlight the position of each errored bit in turn – displaying the address of the errored bit – and show the surrounding bit pattern. Then automatically measure BER of each errored bit. If the error rate of a captured bit remains significant over a period, there is probably a pattern-dependent, systematic error.

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HP 71612B error performance analyzer specifications

Items marked "typical" or "nominal" are supplemental characteristics intended to provide information useful in applying the instrument by giving typical but non-warranted, performance parameters.

Test patterns

- **PRBS:** $2^{31} - 1$, $2^{23} - 1$, $2^{15} - 1$, $2^{10} - 1$, $2^{7} - 1$.
- **User-defined pattern:** Up to 8 Mbit.
- **Zero substitution:** Extends the longest run of zeros up to pattern length less one bit on patterns 2^{13}, 2^{11}, 2^{10}, 2^{7}.
- **Variable mark density ratio:** 1/8 to 7/8 in 1/8 steps on patterns 2^{13}, 2^{11}, 2^{10}, 2^{7}.
- **STM-64 and OC-192 patterns :** Samples supplied on disk along with other stress patterns.

In the pattern generator, any pattern may be split into two equal-length patterns, with hitless switching between them. The user-defined patterns may be loaded from, or saved to, a 3-½ inch, MS-DOS® format floppy disk.

Pattern generator

There are inputs for an external clock, external error inject, alternate-pattern switch and data output on/off switch. There are outputs for clock and inverted clock, data and inverted data and pattern trigger, sub-rate (quarter-rate) clock; also four outputs for quarter-rate data.

Clock input
Frequency range: 100 MHz to 12 GHz.
Interface: 0.45 to 0.90 V p-p, dc coupled, 50 ohms. (≤ 10 GHz), 0.65 to 0.9 V p-p (> 10 GHz).

Clock outputs – main
Frequency range: 100 MHz to 12 GHz.
Interface: Complementary, dc coupled, 50 ohms, reverse terminated. (Independent control of outputs available).
Amplitude: 0.5 to 2 V p-p in 10 mV steps.
Range: +1.5 to –3.0 V in 10 mV steps.

Data outputs – main
Interface: Complementary, dc coupled, 50 ohms, reverse terminated NRZ, normal or inverted. (Independent control of outputs available).
Amplitude: 0.5 to 2 V p-p in 10 mV steps.
Transition times (10% to 90%): < 30 ps (typical at 2 V p-p).
Jitter: < 20 ps p-p; < 15 ps p-p at 10 Gb/s.
Range: +1.5 to –3.0 V in 10 mV steps.
Clock/data delay: ±1 ns (100 MHz to 500 MHz), one clock period (500 MHz to 12 GHz).
Resolution: 1 ps.

Clock and data outputs – subrate
Frequency range: ¼ of main clock rate.
Interface: dc coupled, 50 ohms, reverse terminated.
Amplitude: 0.5 to 1 V p-p in 10 mV steps.
Range: 0 to –2.0 V in 10 mV steps.

Trigger output: Pattern; clock/32; clock/8.

Error add
Internal: Single on command, or fixed ratio 1 in 10^{n} bits, where n = 3 to 9.
External: TTL levels (active low).

Error detector

The error detector has clock and data inputs and an input which inhibits error counting. There are outputs for errors and pattern trigger. The error detector has both manual and automatic setting of decision threshold and clock/data phase alignment.

Clock input
Frequency range: 100 MHz to 12 GHz.
Interface: 0.45 to 0.90 V p-p dc coupled, 50 ohms to 0 V or –2 V.
Sensitivity: < 200 mV p-p (typical at 10 Gb/s).

Data input
Sensitivity: < 50 mV p-p (typical for $2^{23} - 1$ PRBS input at 10 Gb/s. 0 V high level).
Impedance: 50 ohms to 0 V or –2 V, dc coupled.
Decision threshold range: +1 to –3 V in 1 mV steps.
Clock/data phase alignment: ±1 ns (100 MHz to 500 MHz); 1 clock period (500 MHz to 12 GHz).
Resolution: 1 ps.

Trigger output: Pattern or clock/8.
Error output: 0 to –0.4 V nominal.

Measurement modes: Manual, single period, repetitive period.
Measurement period: 1 s to 100 days; 10, 100, 1000 errors; 10^{7} to 10^{15} bits.

Pattern synchronization: Automatic or manual.
Selectable threshold: 10^{-1} to 10^{-8}.

Audible output: Proportional to error ratio.

Result logging: Time-stamped results to an external printer.

Clock source

The standard integral clock source has a clock output and an external reference input. It provides a variable-frequency, synthesized clock signal to the pattern generator.
See HP 70340A signal generator data sheet for full specifications

Frequency range: 1 to 20 GHz.
Resolution: 1 kHz.

Measurements

- Error count and ratio for:
  - errored ones
  - errored zeros
  - all logic errors
- Errored and error-free intervals of:
  - seconds
  - deciseconds
  - centiseconds
  - milliseconds
- Clock frequency
- Error location analysis (optional)
  Specific bit BER
  - Bit BER
  - Bit error count
  - Delta bit BER
  - Delta bit error count

  Block BER
  Error location capture

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HP 71612B error performance analyzer available with pattern generator, error detector and integral 12 GHz clock source.

Ordering information

12 Gb/s BER measurement and analysis systems

All provide mainframe, color display with integral keypad, base unit, set of operating and installation manuals.

HP 71612B option UHF: 1 to 12 Gb/s error performance analyzer system with pattern generator, error detector and clock source.

HP 71612B option UHG: 1 to 12 Gb/s system with pattern generator and clock source (no error detector provided).

HP 71612B option UHH: 0.1 to 12 Gb/s error detector (no pattern generator or clock source).

Error location analysis
HP 71612B option UHJ: Adds enhanced error detection to help identify sources of systematic errors.
Do not order with option UHG.

No clock source
HP 71612B option UKC: Deletes clock source.
Do not order with option UHH.

HP 71612B option 806:
Replaces HP 70340A standard clock source (1 to 12 Gb/s) with HP 83752A clock source (0.1 to 12 Gb/s), extending the operation of the system down to 100 Mb/s.

12 Gb/s BER measurement and analysis system – without display and clock source

All provide base unit, set of operating and installation manuals.

If you have your own MMS display and clock source, or you wish to build your own test bays, order only the parts you need for your 12 GHz applications.

HP 70843B option UHF: 0.1 to 12 Gb/s error performance analyzer with pattern generator and error detector (no clock source provided).

HP 70843B option UHG: 0.1 to 12 Gb/s system with pattern generator only (no error detector or clock source provided).

HP 70843B option UHH: 0.1 to 12 Gb/s system with error detector only (no pattern generator or clock source provided).

Error location analysis.
HP 70843B option UHJ: Adds enhanced error location analysis to help identify sources of systematic errors.
Do not order with option UHG.

Accessories

Available for both HP 71612B and 70843B analyzers.

Option 0B1: Extra set of manuals.
Option 1CM: Rack mount kit without front handles fitted.
Option 1CP: Rack mount kit with front handles fitted.
Option +W30: Two years additional hardware support beyond the standard one-year warranty.

Note: If you have already purchased pattern generator-only or error detector-only units (options UHG or UHH) and wish to upgrade these to full analysis systems (option UHF), factory retrofits are available. Please contact your HP representative for further details.

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Related literature

HP E4544A STM-64/OC-192 functional test application software	Profile	5965-6411E
HP E4543A Q-factor and eye-contour application software	Profile	5965-6412E
Locating errors in Gigabit transmission systems and components	Technique	5968-2811E
Testing 10 Gb/s SONET/SDH equipment and components	Technique	5968-2812E
Methods for faster high-speed digital communications design	Brochure	5966-4258E
Frequency agile jitter measurement system	Application Note 1267	5963-5353E
HP 71501C jitter analysis system	Product Overview	5965-0801E
HP 83480A Series digital communications analyzer	Product Overview	5964-2238E

Hewlett-Packard manufactures the HP 71612B/70843B analyzers under a quality system approved to the international standard ISO 9002 plus TickIT (BSI Registration Certificate No FM 10987).

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