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Agilent ParBERT 81250

Agilent E4809A 13.5 GHz Central Clock Module
Agilent E4808A High Performance Central Clock Module
Agilent E4805B 675 MHz Central Clock Module

Technical Specifications

Each ParBERT 81250 system consists of at least one clock module, which generates the system clock for at least one generator or analyzer or any mix.
Please see the table to the right for a complete compatibility overview!

Sequencing
The sequencing can be used to specify the data flow:
- single
- looped
- infinitely
- event handling (branch)
- synchronization.

Event Handling
With the event handling the flow of data generation and Analysis can be influenced with external signals at run time.
Usage of Events:
- stop and go of data
- match loop
- intergration with other equipment (ATE)
- trigger on error

For event trigger resources and reaction

Modules/Central Clock	E4805B	E4808A	E4809A
E4832A - ParBERT 675 Mb/s	•	•	•
E4861A - ParBERT 2.7/1.6 Gb/s	•	•	
E4861B - ParBERT 3.35 Gb/s		•	•
E4810A/11A - ParBERT 3.3.5 Gb/s optical		•	•
E4866A/67A - ParBERT 10.8 Gb/s		•	
N4872A/73A - ParBERT 13.5 Gb/s			•
E4868B/69B - ParBERT 45 Gb/s		•	

E4809A, E4808A and E4805B Sequencing Features

Number of Segments	1 to 30 (every segment looped once) 1 to 60 (no segment looped)
Looping levels	Up to 4 nested loops plus one optional infinite loop Loops can be set independently from 1 to 2 repetitions
Start/stop	External input, manual, programmed (stop with E4832A only)
Event handling	React on internal and external events.

E4809A, E4808A and E4805B Event Handling

Event trigger sources
Events can be defined as any combination of the following sources.
A maximum of 10 events can be defined.
- 8-line trigger input pod for TTL signals
- VXI trigger lines TO and T1
- Any capture error/or no error detected by one of the analyzer channels
- Software command control: an event trigger command issued locally or remotely

Reactions to an event can be set per data segment immediately or deferred and can be any combination of:
- Data segment jump
- Launch trigger pulse to the trigger output of the Clock Module
- VXI trigger lines TO and T1 can be set to 01, 10 or 11

Technical Specifications
All specifications describe the instrument's warranted performance. Non-warranted values are described as typical. All specifications are valid from 10° to 40° ambient temperature after a 30 minute warm-up phase, with outputs and inputs terminate with 50 Ohms to ground at ECL levels if not specified otherwise.

Agilent Technologies

Master slave, multi-mainframe, different clock groups.
Up to 3 clock modules can be combined to run in one clock grouping by connecting the master slave cable. This is used to combine channels which do not fit into one frame into one clock group. Omitting the master-slave connection will run the channels within separated clock groups. A system can be operated using different clock groups. So a bunch of channels are combined with a clock module. The frequencies used can be totally asynchronous or m/n ratio (see clock input multiplier/divider). For separated clock groups the master slave must not be connected. Within one system the modules must always be of the same type.

E4809A, E4808A and E4805B Trigger Pod characteristics		
Input Lines	8, single-ended	
Input levels	TTL compatible	
Input threshold	1.5 V	
Input termination	5 k Ohm pullup to +5 V	
Absolute max ratings for input voltages	-1.2 V to + 7.0 V	
Cable delay	11 ns typical	
sampling clock frequency	system frequency/segment length resolution	
	TRIGGER OUTPUT	CLOCK/REF INPUT
Setup time*	2.5ns	-12.5ns
Hold time*	5 ns	20 ns

***includes the cable delay**

E4809A 13.5 GHz Central Clock Module

General:
E4809A is a 2-slot central clock module enhancing the capabilities of the E4808A by a 13GHz clock distribution. ParBERT 81250 13.5 Gb/s modules are designed to run with the E4809A 13.5 GHz Central Clock module.

E4809A Clock Module specifications		
Frequency range	20.834MHz...13,5GHz	
Resolution	1Hz	
SSB Phase Noise (at 10kHz offset)	<-75dBc at 10GHz	
Latency (typical)	to trigger output	to channel output
External Start	16ns ±1clock	tbd ns ±1clock
	Add 3ns if an expander frame is used	

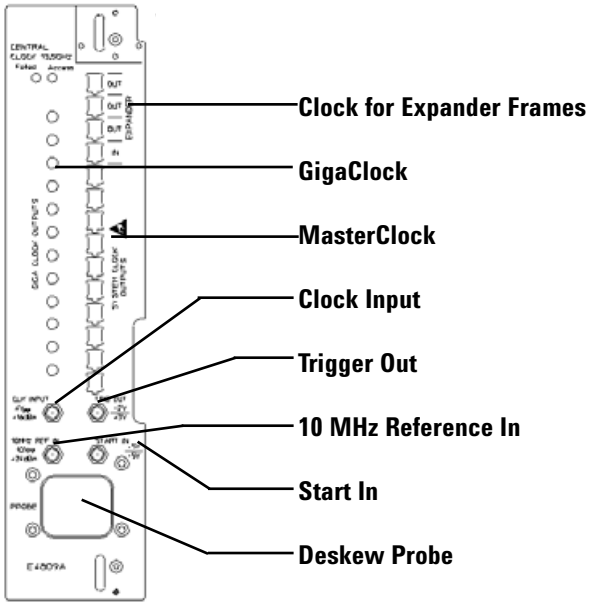


Figure 1: E4809A

Timing Capabilities

The E4809A supports three different operation modes.

- **E4809A as system clock**

The E4809A distributes clock signals to connected modules in the range from 20.834 MHz up to 13.5 GHz. The E4809A provides GigaClock signals in a range from 500 MHz up to 13.5 GHz to the ParBERT 81250 13.5 Gb/s modules (N4872A, N4873A). All other supported modules are working with the E4809A MasterClock.

- **External Clock mode**

The system will run synchronously to an external clock, which is connected to the clock module's clock input. There are two different sub-modes available.
In the **direct** clock mode, the PLL (Phase Locked Loop) is bypassed and an external clock signal can be distributed to all GigaClock connected modules. This direct external clock mode is operating in a range from 500 MHz to 13.5 GHz. In this mode the external clock may be FM or PM modulated.
In the **indirect** external clock mode, the clock modules internal PLL is used to generate flexible MasterClock and GigaClock signals.

- **Clock Data Recovery (CDR) mode**

If the CDR is used, the CDR Out of the Analyzer must be connected to the Clock Input of the Clock module.

Start Input

A data sequence generation can be started by an external signal.

Start Input	
Start Input	DC coupled; 3.5mm(f)
Threshold range	-1.40V to +3,70V
Zin/Termination voltage	50 Ohm typ. / -2V to +3V
Sensitivity/max. levels	200mVpp / -3V...+6V

Reference Input

The Reference Input allows ParBERT to run synchronously with an external 10MHz clock. Usage of a continuous clock is necessary. Burst clock can not be used as an external clock.

Reference Input	
Reference Input	AC coupled; 3.5mm(f)
Frequency	10MHz
Input transition/slope	<20ns
Required Duty cycle	50 ±10%
Zin	50 Ohm
Sensitivity	200mVpp

Clock Input

This input runs ParBERT synchronously with an external clock. Usage of a continuous clock is necessary. Burst clock can not be used as an external clock. Two modes are selectable: Indirect external clock mode (clock module PLL is used) and Direct external clock mode (clock module is bypassed).

Clock Input	
Clock Input	AC coupled; 3.5mm(f)
Frequency range	
Indirect mode	20.834MHz...13.5GHz
Direct mode	500MHz...13.5GHz
Clock Input (Indirect mode only)	m=1...256; n=1...256
Multiplier(m)/divider(n)	m*n<=1024; m/n*input frequency must fit data range input frequency/n>=1,3MHz
Input transition/slope	30 ps typ.
Zin	50 Ohm
Sensitivity	<150mV

Trigger Output

This output will be used to deliver a trigger signal to a DUT, a Digital Communication Analyzer (Agilent 86100B Series) or as a stimulus for the Analyzer deskew.

Trigger Output	
Trigger Output	DC coupled, SMP (f)
Frequency	Tbd
Output transition/slope	70 ps typ. 10/90
Zout/Termination voltage	50 Ohm / -2 to +3V
Output voltage window	-2V to +3V
Output level	0.1 to 1.8 Vpp

E4805B and E4808A Central Clock Modules

The central clock module includes a PLL (Phase-Locked Loop) frequency generator to provide a system clock. Depending on the frequency chosen, the data modules can be clocked at a ratio of 1, 2, 4, 8, 16, 32, 64 or 256 times higher or lower than the system clock.

External start/stop: The data running can be started by an external signal applied to the external input. With module E4832A there is also Stop and Gate mode.

Ext. Clock/Ext. Reference: This input runs ParBERT 81250 synchronously with an ext. clock, or when a more accurate reference is needed than the internal oscillator. Usage of a continuous clock is necessary. Burst clock cannot be used as an external clock. Maximum external clock is 2.7 GHz for the E4805B and 10.8Gbit/s for the E4808A. (Note: no improvement of jitter specifications will be achieved).

Guided deskew: Individual semi-automatic deskew per channel. The deskew probe 15447A allows deskew on the DUT's (Device Under Test) fixture.

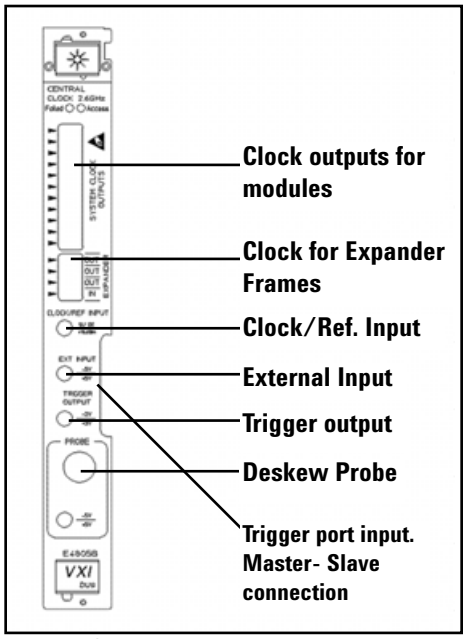


Figure1: Clock Module

E4805B and E4808A Clock Module specifications

	E4805B	E4808A
Frequency range*	1kHZ to 675 MHZ	170 kHz to 675 MHz
(can be entered as	E4805B will run with:	E4808A will run with:
period or frequency)		- E4866A/E4867A in range of 9.5GHz to 10.8GHz
E4808A Clock	- E4861A in range of 334 MHz to 2.7GHz	- E4861B in range of 20.834 MHz to
Module specifications	- E4832A in range of 334KHZ to 675 MHz	3.35GHz- E4861A in range of 334 MHz to 2.7GHz
		- E4832A in range of 334KHZ to 675 MHz
Resolution	1 Hz	1 Hz
Accuracy	±50 ppm with internal PLL reference	±50 ppm with internal PLL reference

May be limited or enhanced by modules or frontends

External input and ext. clock/ext. ref. input

	E4805B		E4808A	
Zin/Termination voltage	50 Ohm/-2.10 V to 3.30 V		50 Ohm/-2.10 V to 3.30 V	
Sensitivity/max levels	400 mVpp/-3 V to + 6 V		200 mVpp/-3 V to + 6V for < 9.5Gbit/s 300mVpp/-3V to+ 6V for > 9.5 Gbit/s	
Coupling	dc,		dc,	
Ext. Input:	Threshold Range: -1.40 V to +3.70 V		-1.40 V to +3.70 V	
Ext. Clock/Ext. Ref:	ac		ac	
Input transitions/slope	< 20ns. Ext. input active edge is selectable		< 20 ns. Ext. Input active edge is selectable	
Clock input multiplier(m)/ divider (n)	m=1...256; n=1...256 m*n<=1024 m/n * input frequency must fit data range input frequency/n>=1.3 MHZ			
PLL lock time	100ms		100 ms	
Input frequency/period				
Ext. Clock	170 kHz - 2.7 GHz		170 kHz - 10.8 GHz	
Ext. Ref	1*, 2*, 5, or 10 MHz		1*, 2*, 5, or 10 MHz	
Required duty cycle	50 ±10 %		50 ±10 %	
Latency (typical):	to trigger Output	to channel output	to trigger Output	to channel Output
Ext. input	16ns ±1 clock	46ns ±1 clock	16ns ±1 clock	46ns ±1 clock**
Ext. clock	15ns	45ns	15ns	45ns
	Add 3ns if an expander frame is used		Add 3ns if an expander frame is used	

*** Jitter performance may be degraded**

**** If frequency=667MHz**

Trigger Ouput
Can be used in:
- clock mode
- sequence mode

In sequence mode a pulse will be set to mark the start of any segment.

The trigger output runs to a maximum of 675MHZ. If a higher speed performance clock is needed;
- A 2.7GHZ Clock can be obtained from a 2.7 Gb/s channel operated as a pulse port.
- A 10.8GHZ clock is available from the 10.8 Gb/s generated module as clock output.

Trigger output characteristics E4805B and E4808A	
Trigger output signals	- Clock mode (up to 675 MHz). - Sequence Mode
Output impedance	50 Ohm typ.
Output level	TTL (frequency < 180 MHz), 50 Ohm to GND ECL 50 Ohm to GND/-2 V, PECL 50 Ohm +3V
Trigger advance	30 ns typ. between trigger output and data output/sampling point (delay set to zero in both cases)
Maximum ext voltage	-2 V to +3.3 V
Jitter (int. reference/int. clock)	< 10 ps rms (5ps typ.)

Related Literature	Publication Number
• *Agilent ParBERT 81250 Parallel Bit Error Ratio Tester, Product Overview*	*5968-9188E*
• *Agilent ParBERT 81250 13.5 Gb/s Parallel Bit Error Ratio Test Platform, Photocard*	*5988-9201EN*

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(fax) (31 20) 547 2390

Japan:
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(fax) (81) 426 56 7840

Korea:
(tel) (82 2) 2004 5004
(fax) (82 2) 2004 5115

Latin America:
(tel) (305) 269 7500
(fax) (305) 269 7599

Taiwan:
(tel) 0800 047 866
(fax) 0800 286 331

Other Asia Pacific Countries:
(tel) (65) 6375 8100
(fax) (65) 6836 0252
Email: tm_asia@agilent.com

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Printed in Germany, July 31st, 2003
5988-9203EN



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