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Service Sheet 1

ASSEMBLY

- **A53 RF Power (Sensor Input Circuits)**

PRINCIPLES OF OPERATION

General

The load impedance of the power-sensing element dissipates the RF input power applied to the external power sensor (in the Sensor Module). A sampling gate (chopper) in the power sensor converts the dc output of the power-sensing element to a 220 Hz ac signal. The RF Power circuits amplify the ac signal and convert the signal back to dc for measurement by the Voltmeter.

Amplifier 1

The ac signal, which is proportional to the RF input power, is amplified by tuned ac amplifier stages in the external power sensor and the RF Power circuits. Amplifier 1 and the output amplifier of the external power sensor form a low-noise, high-gain operational amplifier. See Figure 8F-1. The ac gain of the amplifier is approximately 700. DC bias is set by R2, R3, R4, R5, and R6. Diodes CR1, CR2, VR1, and VR2 and associated components are part of a shaping network which compensates for the non-linear output of the power sensor's power sensing element. (The efficiency of the power-sensing element is slightly impaired when the RF input to the power sensor is near maximum power.) The shaping network reduces the gain of Amplifier 1 to give a linear overall response. R13 (RNG 4) and R16 (RNG 5) permit fine adjustment of the gain of the shaping circuit for high levels.

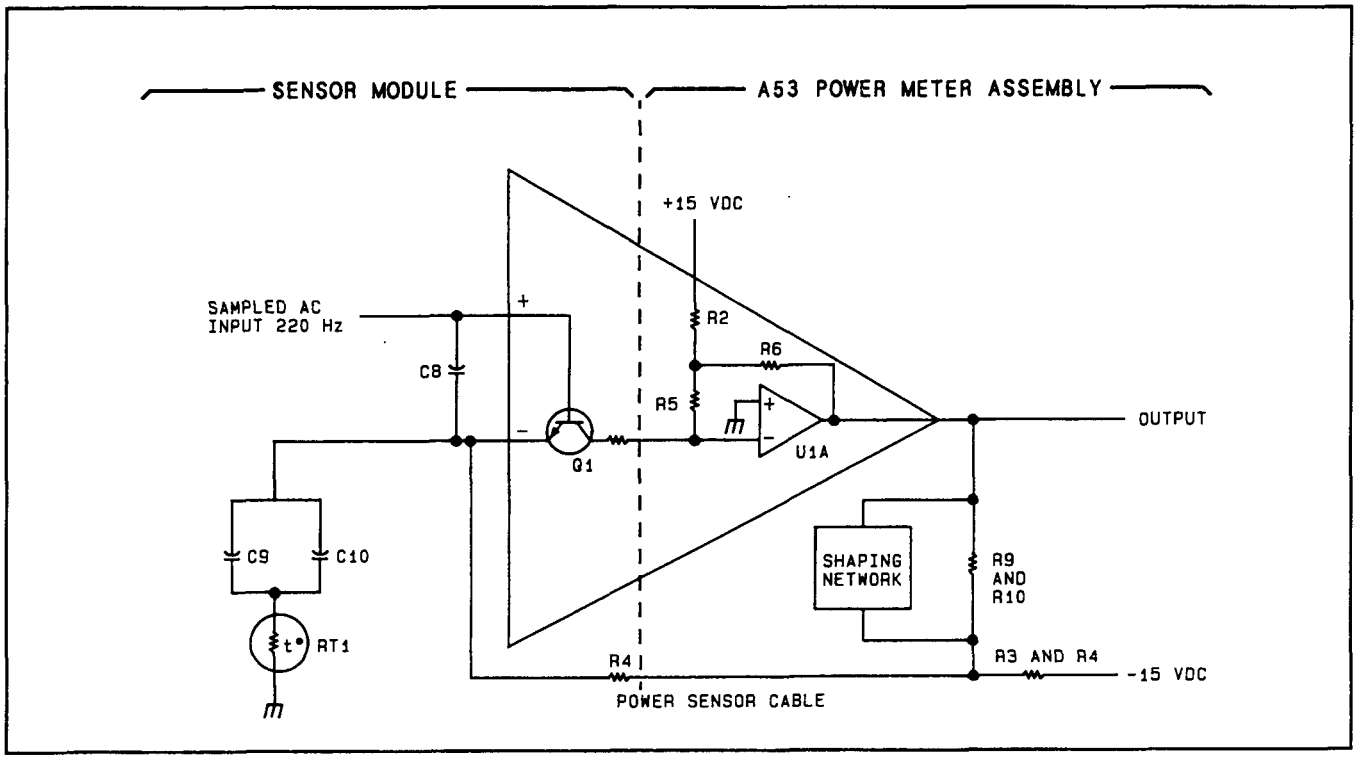


Figure 8F-1. *First Amplifier Stage of the RF Power Meter*

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The combination of C10, R9, and R10 determines, in part, the upper cutoff frequency (240 Hz) of the bandpass response of the ac amplifiers; C14, R19, and R20 determine, in part, the lower cutoff frequency (200 Hz). C1, C5, and C13 filter line noise.

Ground Regulator

U17 and U1B are connected as a voltage follower between the GND REGULATOR line from the Sensor Module and ANALOG GND 1 of the RF Power circuits. This circuit ensures that a minimum voltage difference exists between the grounds to eliminate error-creating voltage difference between measurement ground and instrument ground.

Attenuators 1 and 2 and Amplifiers 2 and 3

Attenuators 1 and 2 operate as shown in Table 8F-1. (The attenuation indicated is voltage attenuation.)

Table 8F-1. *Attenuation vs. Range of Attenuators 1 and 2*

Range	Attenuation (dB)		
	Attenuator 1	Attenuator 2	Total
1	0	0	0
2	0	20	20
3	0	40	40
4	40	20	60
5	40	40	80

Amplifier 2 has a gain of 21. Amplifier 3 has a gain of 19. The two combinations of C18 and R21 and of C27 and R31 determine, in part, the upper cutoff frequency (240 Hz) of the bandpass response of the ac amplifiers; C19, R24, R25, and R26 and C22 and R27 determine, in part, the lower cutoff frequency (200 Hz).

Synchronous Detector

The 220 Hz Multivibrator drives the Synchronous Detector in the same way it drives the sampling gate (chopper) in the external power sensor. The 220 Hz switching signal is applied through Q5 and Q6 to the gate of FET Q4 which causes Q4 to turn on and off. When Q4 is on, the gain of amplifier U3 is −1. When Q4 is off, the gain of U3 is +1. Since the 220 Hz drive signal is in synchronism with the ac signal originating in the power sensor's chopper, the output of U3 is full-wave rectified. The average dc level of the signal from U3 is proportional to the power dissipated in the power-sensing element of the external power sensor.

220 Hz Multivibrator

The 220 Hz Multivibrator drives both the chopper in the external power sensor and the gain switch (Q4) of the Synchronous Detector. Q8, Q9, and associated components form an astable multivibrator. Q11 and Q12 are drivers. R40 (FREQ) allows fine adjustment of the multivibrator's frequency. R40 is adjusted for minimum phase shift through the bandpass filter response of the ac amplifiers. The point of minimum phase shift gives the maximum and most drift-immune power indication.

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TROUBLESHOOTING

General

Procedures for checking the RF Power Assembly are given below. The circuits to check are marked on the schematic diagram by a hexagon with a check mark and a number inside, for example, ⟨√3⟩. In addition, any points outside the labeled circuit area that must be checked are also identified. Fixed signals are also shown on the schematic inside a hexagon, for example, ⟨+1.9 TO +2.1 VDC⟩.

Extend the board assembly where necessary to make measurements. Extending the assembly will require freeing the two multi-conductor cables atop the assembly so that they may be reconnected. Freeing the cables will require disconnecting several RF cables. The RF cables need not be reconnected while troubleshooting the assembly.

CAUTION

Tighten SMC connectors to 0.6 N·m (5 in·lb). Hand tightening of connectors is insufficient. Hand-tightened connectors can work loose and cause reduced performance or malfunctions.

Equipment

Oscilloscope ..... HP 1740A
Range Calibrator ..... HP 11683A

⟨√1⟩ Amplifier 1 and Ground Regulator Check

NOTE

Failure of the Ground Regulator may make Amplifier 1 appear to fail.

1. Remove any connection to the SENSOR connector.
2. Connect one channel of a high-impedance, dc coupled oscilloscope to pin 6 of U17. Connect the other channel to pin 7 of U1B. Connect pin 3 of U17 through a 100 kΩ resistor to the supply indicated in the table below. After connecting the resistor to the supply, briefly short pin 2 of U17 to chassis ground and observe the oscilloscope display. The voltages should be as indicated in Table 8F-2.

NOTE

U17 and U1B will be operating with nearly short-circuited outputs, which they should be able to withstand indefinitely. It is a good practice, however, to be as brief as possible. The +15V Supply is easily accessed at the + end of C2, the −15V Supply at the − end of C4.

Table 8F-2. *Voltage Limits for ⟨√1⟩ Step 2*

Supply Connection	Limits (Vdc) on U17 Pin 6	Limits (Vdc) on U1B Pin 7
+15V	+0.2 to +1.0	+0.1 to +0.3
−15V	−1.0 to −0.2	−0.3 to −0.1

Hint: If the short on pin 2 of U17 is removed, the outputs of U17 and U1B will normally drift towards the corresponding supply and, for the +15V Supply, will begin pulsing. If this change

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does not occur, the Ground Regulator is working properly but its load (the devices connected to Analog Ground 1) requires more current than the regulator is able to supply.

3. Remove the short from pin 2 of U17. Connect the oscilloscope to A53TP6 (A GND). Connect the 100 kΩ resistor to chassis ground. The level at A53TP6 should slowly drift to between −50 and +50 mVdc.
4. Ground pin 3 of U1A. (Shorting R1 with a cliplead may be the simplest way to do this.)
5. Connect the oscilloscope to pin 1 of U1A. The voltage should be between −15 and −12 Vdc.

   Hint: U1A, R2, and R6 form an inverting amplifier with the +15V Supply as the input. The gain is high enough to drive U1A into limiting by the −15V Supply.
6. Connect a 42.2 kΩ resistor between the + end of C5 and the −15V Supply. The voltage should be between −0.5 and +0.5 Vdc. (Ignore any ac ripple.)
7. Remove all jumpers. Leave the oscilloscope connected to pin 1 of U1A.
8. Connect the range calibrator to the SENSOR input. Set the calibrator's range to 1 mW, function to calibrate, and polarity to normal.
9. Press RF POWER. The waveform on the oscilloscope display should appear as shown in Figure 8F-2.

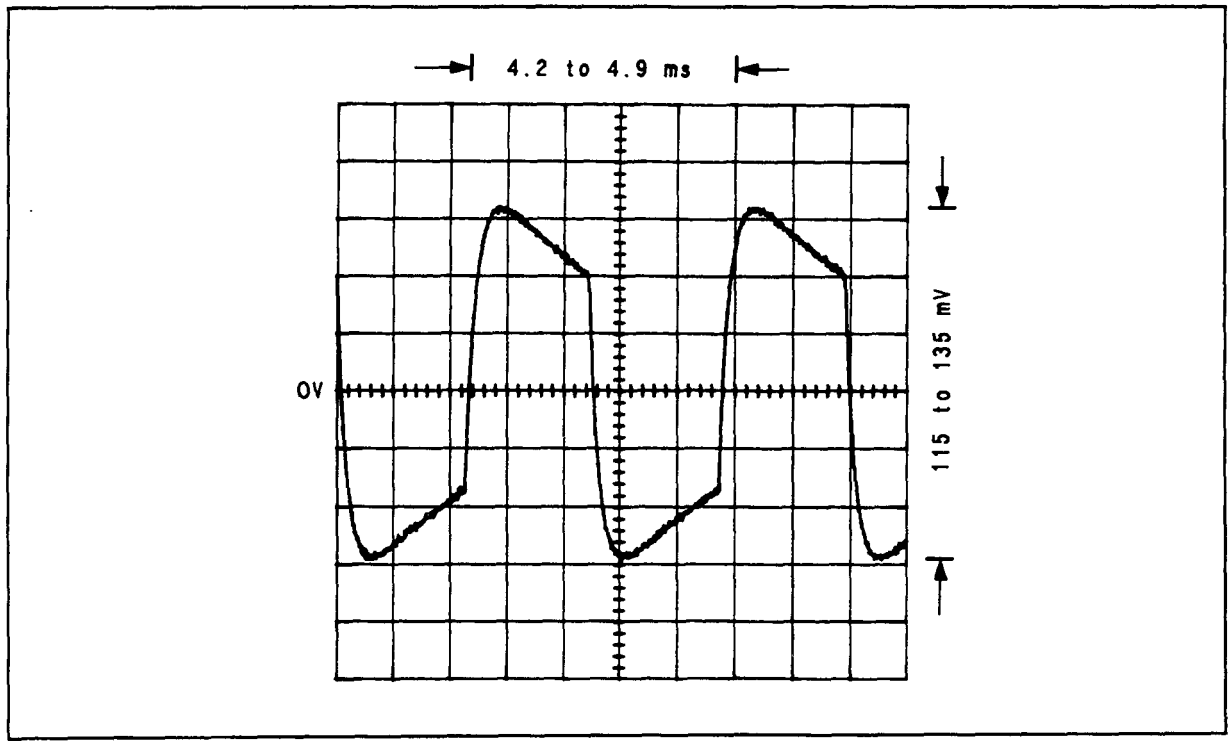


Figure 8F-2. *Waveform for* ⟨√1⟩ *Step 9*

Hint: If the period is out of limits, see ⟨√4⟩ 220 Hz Multivibrator Check. Improper operation of the Zeroing Control circuit can alter the input to Amplifier 1 and cause an erroneous output. If this is suspected, short R65 (see Service Sheet 2) and recheck the waveform.

10. Set the calibrator's range to 10 mW. Reduce the oscilloscope's vertical gain by a factor of 10. The waveform should appear as in the figure for step 9 with the voltage limits multiplied by 10.

    Hint: If faulty, check the components associated with the Range 4 shaping circuit (R13, CR1, CR2, etc.).

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11. Set the calibrator's range to 100 mW. Reduce the oscilloscope's vertical gain by a factor of 10. The waveform should appear as in the figure for step 9 with the voltage limits multiplied by 100.

    Hint: If faulty, check the components associated with the Range 5 shaping circuit (R16, VR1, VR2, etc.).

⟨√2⟩ Attenuator 1, Amplifier 2, Attenuator 2, and Amplifier 3 Check

1. Connect the range calibrator to the SENSOR input. Set the calibrator's range to 1 mW, function to calibrate, and polarity to normal.
2. Connect a high-impedance, ac coupled oscilloscope to pin 1 of U1A. The display should be as shown in the figure for step 9 of the ⟨√1⟩ Amplifier 1 and Ground Regulator Check.

    Hint: If faulty, perform ⟨√1⟩ above.
3. Connect the oscilloscope to pin 2 of U4A. Key in 0.209 SPCL to switch U4A on and U4B off. The waveform on the oscilloscope display should appear as shown in Figure 8F-3.

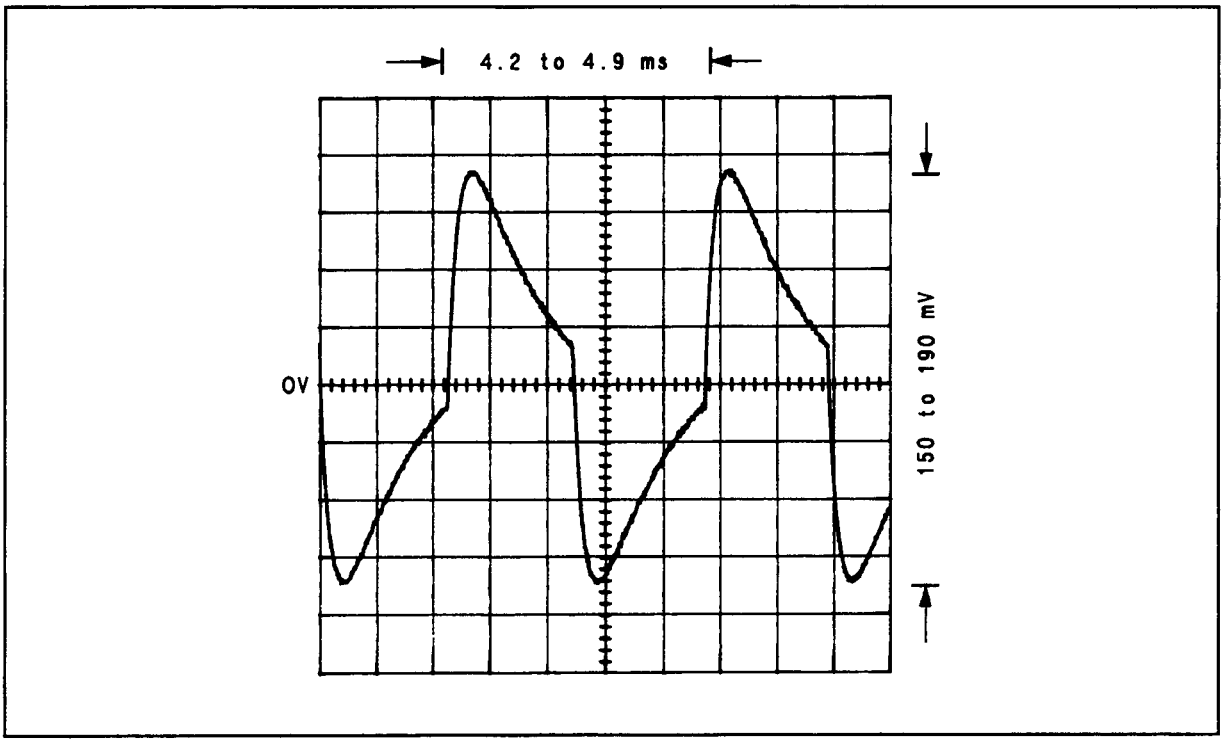


Figure 8F-3. *Waveform for ⟨√2⟩ Step 3*

Hint: Pin 1 of U4A should be a TTL low. Pin 8 of U4B should be high.

4. Key in 0.208 SPCL to switch U4A off and U4B on. Switch the calibrator's range to 100 mW. The waveform should appear as in the figure for step 3.

    Hint: Pin 1 of U4A should be high. Pin 8 of U4B should be low.
5. Connect the oscilloscope to pin 11 of U4C. Switch the calibrator's range to 1 mW. Key in 0.202 SPCL to switch U4C on and U4D and U8A off. The waveform should appear as shown in Figure 8F-4.

    Hint: Pin 9 of U4C should be low. Pin 16 of U4D and pin 1 of U8A should be high.

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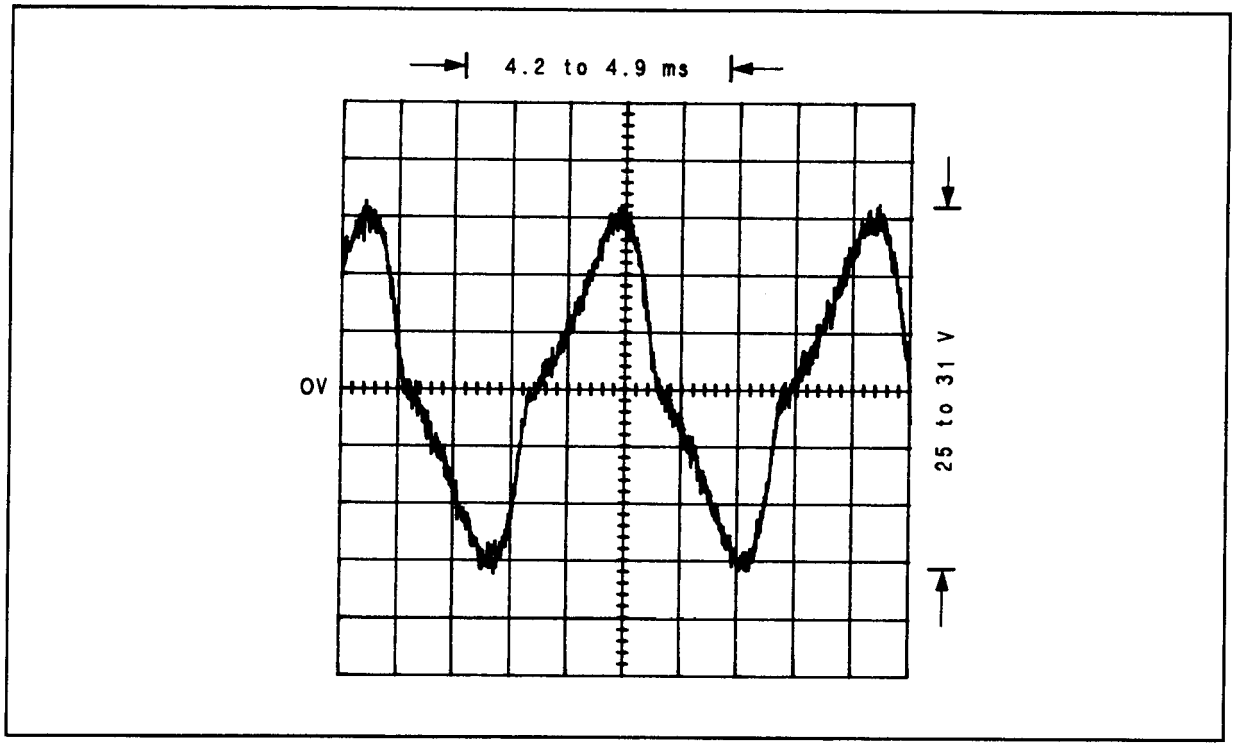


Figure 8F–4. *Waveform for* ⟨√2⟩ *Step 5*

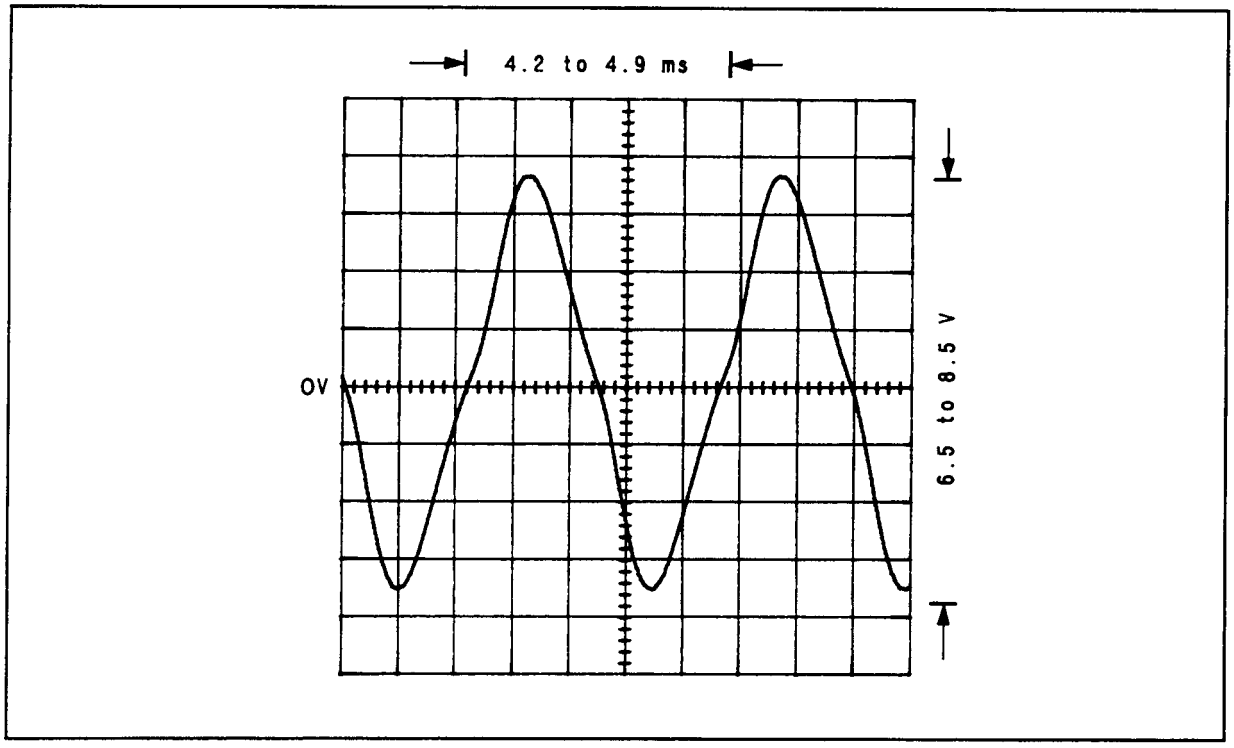


Figure 8F–5. *Waveform for* ⟨√2⟩ *Step 8*

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6. Key in 0.204 SPCL to switch U4D on and U4C and U8A off. Switch the calibrator's range to 10 mW. The waveform should appear as in the figure for step 5.

   Hint: Pin 16 of U4D should be low. Pin 9 of U4C and pin 1 of U8A should be high.

7. Key in 0.208 SPCL to switch U8A on and U4C and U4D off. Switch the calibrator's range to 100 mW. The waveform should appear as in the figure for step 5.

8. Connect the oscilloscope to A53TP1 (AC). The waveform should appear as shown in Figure 8F-5.

   Hint: The waveform at pin 7 of U2B should have a similar shape and an amplitude of approximately 600 mVpp.

⟨√3⟩ Synchronous Detector Check

1. Connect the range calibrator to the SENSOR input. Set the calibrator's range to 1 mW, function to calibrate, and polarity to normal. Press RF POWER.

2. Connect a high-impedance, ac coupled oscilloscope to A53TP1 (AC). The display should be as shown in the figure for step 8 of the ⟨√2⟩ Amplifier 1, Attenuator 2, Amplifier 2, and Amplifier 3 Check.

   Hint: If faulty, perform ⟨√2⟩ above.

3. DC couple the oscilloscope and connect it to A53TP2 (Φ DET). The waveform should appear as shown in Figure 8F-6.

   Hint: The collector of Q6 should be switching between 0 and approximately −15V with a period between 4.2 and 4.9 ms. The gain of operational amplifier based on U3 switches from +1 to −1 as Q4 switches from off to on. Non-uniform half-cycles indicates unequal gain for the two states of U3.

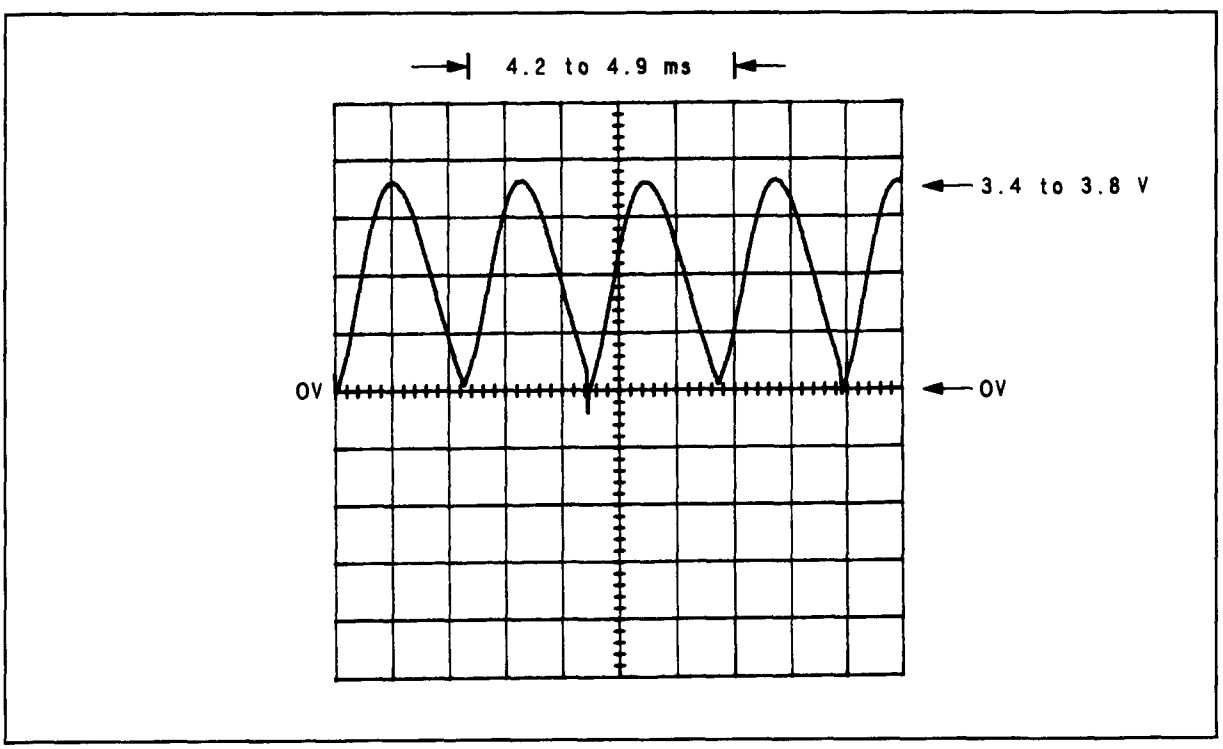


Figure 8F-6. *Waveform for* ⟨√3⟩ *Step 3*

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⟨√4⟩ 220 Hz Multivibrator Check

1. Connect a high-impedance, dc coupled oscilloscope to A53TP4 (MULTVIB or MV1). The waveform should be a square wave switching between 0V and 10 to 11V with a period between 4.2 and 4.9 ms.

   Hint: A more accurate way of measuring the multivibrator's frequency and adjusting it if necessary is found in *Adjustment 20—Power Meter.*

2. Connect the oscilloscope to A53TP5 (MV2) and repeat step 1.

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Service Sheet 2

ASSEMBLY

- **A53 RF Power (Control Circuits)**

PRINCIPLES OF OPERATION

General

This Service Sheet documents the circuits that filter the signal from the Synchronous Detector, zero the Power Sensor, and control the Power Meter and external Sensor Module.

Noise Filter

The dc voltage from the Synchronous Detector (see Service Sheet 1) is filtered to remove noise and improve measurement readability. U13 and associated components form an active, three-pole, low-pass filter. The noise bandwidth is 10 Hz with switch U8B closed and 1 Hz with U8B open. The 10 Hz bandwidth is used in ranges 5, 4, and 3 (refer to Table 8F-1); the 1 Hz bandwidth is used in ranges 2 and 1. (In addition, in range 1, the Controller effectively increases filtering by averaging several successive readings.)

The Voltmeter reads the Noise Filter output (RF PWR/SENSOR TYPE) via switch U8C to display RF power. The Voltmeter also reads the Noise Filter output via U8D to identify the type of sensor connected to the front-panel SENSOR input connector. By reading the voltage developed at the junction of R68, R69, and the SENSOR-TYPE READBACK line the type of sensor is determined. Each sensor type has a unique resistor value with one end of the resistor connected to ground. (In the HP 11722A Sensor Module, the resistor is 1.62 kΩ.)

Zeroing Control

Power offsets (positive or negative readings from the Power Meter when no power is actually applied) come primarily from the Power Sensing Element in the external Power Sensor. The offset is cancelled by the Zeroing Control DAC (U10) when the Power Meter is zeroed. To zero the Power Meter, the Controller removes the power from the external Power Sensor using the Input Switch in the Sensor Module. (If a sensor is used which is not part of a Sensor Module, the RF power source must be manually removed before zeroing is attempted.) With no power into the Power Sensor, the Controller takes an RF power reading and adjusts the Zeroing Control DAC to cancel the reading; more than one attempt may be required to bring the reading within limits.

The Zeroing Control DAC outputs a current proportional to the binary-weighted input. This output current, flowing through R65 develops a negative voltage. Another current, originating from Q15, flows through R67 to develop a constant positive voltage across R65. The combination of the currents from the DAC and Q15 thus permits a positive or negative offset. The offsetting voltage is fed to the Power Sensing Element of the external Power Sensor. To minimize drift of the offset, reference diodes VR3, VR4, and VR5 are biased by thermally compensated current sources (Q14 and Q15) to produce the reference voltage to the DAC and R67.

Sensor Module Switch Control

The Switch Drive One-Shot permits control of latching-type RF switches in the Sensor Module which can have either automatic breaking or non-breaking solenoid drive contacts. For either case, one-shot U16 provides an energizing pulse for 30 ms which is sufficient to throw the switch's plunger.

Switch Q3 actually energizes the RF switch solenoid. The collector resistor (R77) of Q3 provides sufficient drive current for the types of RF switches commonly used in the external Sensor Module.

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CR3 suppresses the emf generated by the RF switch solenoid when the drive current is interrupted. Q3 is driven from U16 via Q13.

Relays K1 and K2, activated by U14A and U14B, route the switch drive to the proper solenoid contacts. The Controller then activates the RF switch via the Switch Drive One-Shot.

Power Reference Oscillator Control

The RF Power Reference Oscillator (see Service Sheet 3) is activated by the Controller via Q7 and Q2. When Q2 is on, −15V is supplied to the reference circuitry.

Frequency Offset Control

Gates U15A and U15B provide a three-level (0, +3, and +5V) output to indicate to an external down-converter the status and frequency range of frequency offset. (See Table 8D-4 for status information.)

Select Decoder and Data Latches

Refer to the general discussion under *Instrument Bus* in Service Sheet BD5. R53 and C35 for the Power-Up Reset circuit that sets the front-end components of the instrument to the most-protected state at power-up; that is, input attenuation is set to maximum and the external Power Sensor is switched out.

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TROUBLESHOOTING

General

Procedures for checking the RF Power Assembly are given below. The circuits to check are marked on the schematic diagram by a hexagon with a check mark and a number inside, for example, ⟨√3⟩. In addition, any points outside the labeled circuit area that must be checked are also identified. Fixed signals are also shown on the schematic inside a hexagon, for example, ⟨+1.9 TO +2.1 VDC⟩.

Extend the board assembly where necessary to make measurements. Extending the assembly will require freeing the two multi-conductor cables atop the assembly so that they may be reconnected. Freeing the cables will require disconnecting several RF cables. The RF cables need not be reconnected while troubleshooting the assembly.

CAUTION

Tighten SMC connectors to 0.6 N·m (5 in·lb). Hand tightening of connectors is insufficient. Hand-tightened connectors can work loose and cause reduced performance or malfunctions.

Equipment

Oscilloscope	HP 1740A
Range Calibrator	HP 11683A

⟨√1⟩ Noise Filters Check

1. Connect the range calibrator to the SENSOR input. Set the calibrator's range to 1 mW, function to calibrate, and polarity to normal. On the Measuring Receiver, press RF POWER.
2. Connect a high-impedance, dc coupled oscilloscope to A53TP2 (Φ DET). (See Service Sheet 1.) The waveform should appear as in Figure 8F-7.

   Hint: If the waveform is faulty, see Service Sheet 1 and check the Synchronous Detector.

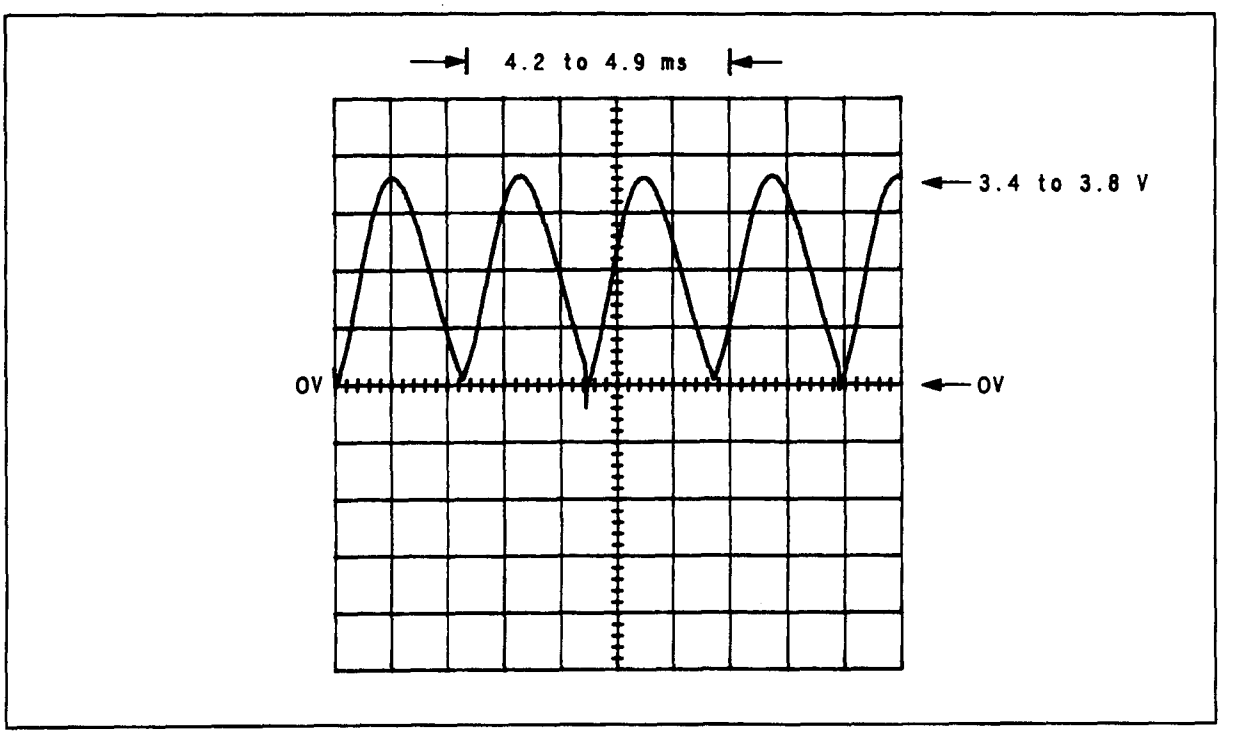


Figure 8F-7. *Waveform for* ⟨√1⟩ *Step 2*

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3. Connect the oscilloscope to A53TP3 (FLTR). Key in 0.231 SPCL to set the Noise Filters to wide. The waveform should be dc at a level between 700 and 900 mV.

   Hint: Pin 8 of U8B should be a TTL high.

4. Key in 0.230 SPCL to set the Noise Filters to narrow. The waveform should be between 700 and 900 mV.

   Hint: Pin 8 of U8B should be a TTL low.

⟨√2⟩ RF Power and Sensor-Type Readback Switches Check

1. Connect the range calibrator to the SENSOR input. Set the calibrator's range to 1 mW, function to calibrate, and polarity to normal. On the Measuring Receiver, press RF POWER.
2. Connect a high-impedance, dc coupled oscilloscope to A53TP3 (FLTR). The waveform should be dc at a level between 700 and 900 mV.

   Hint: If the waveform is faulty, perform ⟨√1⟩ above.

3. Key in 0.21A SPCL to enable the RF Power Readback Switch. Key in 49.F SPCL to read back the output of the switch. The display should read between 0.7 and 0.9.

   Hint: Pin 9 of U8C should be a TTL low. Pin 16 of U8D should be a TTL high.

4. Key in 0.219 SPCL to enable the Sensor-Type Readback Switch. Key in 49.F SPCL. The display should read between −0.01 and +0.01. (The sensor-type resistor in the range calibrator is a short circuit.)

   Hint: Pin 9 of U8C should be a TTL high. Pin 16 of U8D should be a TTL low.

⟨√3⟩ Power Reference Oscillator Control Check

1. Connect a high-impedance, dc coupled oscilloscope to the collector of Q2.
2. Key in 0.21E SPCL to switch Q2 on. The dc waveform should be between −15 and −14 Vdc.

   Hint: Pin 10 of U6 should be a TTL high.

3. Key in 0.21A SPCL to switch Q2 off. The dc waveform should be between +1 and +2 Vdc.

   Hint: Pin 10 of U6 should be a TTL low.

⟨√4⟩ Sensor Module Switch Control Check

1. Disconnect any connection to the SENSOR input.
2. Connect a high-impedance, dc coupled oscilloscope to pin 6 of U16.
3. Key in 0.24 SPCL to trigger the Switch Drive One-Shot. The waveform on the oscilloscope should be a square wave with a period of approximately 60 ms and a level alternating between a TTL high and a TTL low.

   Hint: Pin 1 of U16 should be low-going TTL pulses with a width of approximately 30 ms and a period of approximately 60 ms.

4. Connect the oscilloscope to pin 14 of K1. Connect a 10 kΩ resistor between pin 14 of K1 and ground. The waveform should be a square wave with a period of approximately 60 ms and a level alternating between approximately −15 and 0V.
5. Move the oscilloscope and resistor to pin 8 of the relay indicated in Table 8F-3. Key in the Direct Control Special Functions indicated in the table. For each step, the waveform should be as described. If faulty, also check the logic level on the pin on U14 indicated.

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Table 8F–3. *Levels at Relays,* ⟨√4⟩ *Step 5*

Relay	Direct Control Special Functions	Waveform	Level (TTL) at U14	
			Pin 2	Pin 7
K1	0.212, 0.24	as in step 4	L	H
K1	0.21A, 0.24	0 Vdc	H	L
K2	0.21A, 0.24	as in step 4	H	L
K2	0.212, 0.24	0 Vdc	L	H

⟨√5⟩ Zeroing Control Check

1. Connect the range calibrator to the SENSOR input. Set the calibrator's function to standby.
2. On the Measuring Receiver, press RF POWER.
3. Connect a high-impedance, dc coupled oscilloscope to the collectors of Q14 then Q15. The dc voltage should be between +6.0 and +6.4 Vdc. (The two voltages may differ from each other.)

   Hint: If the voltage at the collector of Q15 is faulty, check the anode of VR5; if the voltage is not 0V, there may be a fault in the Ground Regulator. (See Service Sheet 1.)

5. Connect the oscilloscope to pin 4 of U10. Successively key in the following Direct Control Special Functions to clear the latches of U11: 0.220 SPCL, 0.222 SPCL, 0.224 SPCL, 0.226 SPCL, 0.228 SPCL, 0.22A SPCL, 0.22C SPCL, and 0.22E SPCL. (Note that each suffix is even.) The oscilloscope should read approximately 15 mVdc.

   Hint: Pins 4, 5, 6, 7, 9, 10, 11, and 12 of U11 should be TTL low.

6. Successively key in 0.221 SPCL, 0.223 SPCL, 0.225 SPCL, 0.227 SPCL, 0.229 SPCL, 0.22B SPCL, 0.22D SPCL, and 0.22F SPCL. (Note that each suffix is odd.) As each Direct Control Special Function is entered, the voltage should drop is successively larger steps until the voltage is approximately −15 mVdc.

   Hint: As each Special Function is entered, the pins of U11 mentioned in the previous hint should successively go to a TTL high.

⟨√6⟩ Select Decoder and Data Latches Check

1. Key in the Direct Control Special Functions indicated in Table 8F-4. For each setting, check the pins on U12 indicated.

Table 8F–4. *Levels at U12,* ⟨√6⟩ *Step 1*

Direct Control Special Function	Level (TTL) at U12 Pin				
	11	12	13	14	15
0.200	H	H	H	H	*
0.210	H	H	H	*	H
0.220	H	H	*	H	H
0.230	H	*	H	H	H
0.240	*	H	H	H	H
* Low-going TTL pulses, ≈60 ms period.					

2. Key in the Direct Control Special Functions indicated in Table 8F-5. For each setting, check the pins on U9 and U15 indicated.

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Table 8F–5. *Levels at U9 and U15,* ⟨√6⟩ *Step 2*

Direct Control Special Function	Level (TTL) at U9 Pin				Level at U15 Pin	
	2	7	10	15	3	5
0.230	L	L	L	L	TTL L	TTL L
0.23E	H	H	H	H	TTL H	TTL H
0.232	L	H	L	L	2.6 to 3.2 Vdc	TTL L

3. Key in the Direct Control Special Functions indicated in Table 8F-6. For each setting, check the pins on U5 indicated.

Table 8F–6. *Levels at U5,* ⟨√6⟩ *Step 3*

Direct Control Special Function	Level (TTL) at U5 Pin				
	2	3	6	11	14
0.200	L	H	H	H	H
0.20F	H	L	L	L	L

4. Key in the Direct Control Special Functions indicated in Table 8F-7. For each setting, check the pins on U6 indicated.

Table 8F–7. *Levels at U6,* ⟨√6⟩ *Step 4*

Direct Control Special Function	Level (TTL) at U6 Pin				
	3	6	10	14	15
0.210	H	H	L	H	L
0.21F	L	L	H	L	H

5. Key in 0.0 SPCL to disable the current Direct Control Special Function. Momentarily ground pin 1 of U9 to reset the latches. Measure all the IC pins in steps 2, 3, and 4. For each pin, the level should be the same as those given for the Direct Control Special Function code 0.230 in step 2, 0.200 in step 3, and 0.210 in step 4.

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Service Sheet 3

ASSEMBLY

- **A32 Power Reference Oscillator**

PRINCIPLES OF OPERATION

General

The Power Reference Oscillator generates a 50 MHz signal which maintains a constant output level over a wide range of environmental conditions. The oscillator is adjusted to deliver 1 mW (0 dBm) into a 50Ω load.

50 MHz Oscillator

The tank circuit of the 50 MHz Oscillator is a pi-network consisting of C11, L1, and the series combination of C13 and C14. (Since C13 has much less capacitance than C14, it predominates over C14 in determining the frequency of oscillation.) At 50 MHz, the tank circuit produces 180° phase shift. Another 180° phase shift is generated between the base and collector of Q1. The output of the tank circuit is fed to the base of Q1 through a capacitive voltage divider—C4 and varactor diode CR3. Thus, at 50 MHz, an in-phase signal fed back to the base of Q1 re-enforces the oscillation.

Voltage divider R12 and R13 sets the bias voltage at the base of Q1. Emitter resistors R14 and R15 establish the quiescent emitter current. The frequency of oscillation is adjusted by L1 (FREQ). The output of the oscillator is taken from the tap of capacitive divider C13 and C14. L2 is an RF choke which sets the dc collector voltage of Q1 at ground potential.

ALC Loop

The Automatic Leveling Control (ALC) Loop is a negative-feedback loop which assures that the oscillator output level remains constant. CR2 detects the positive peak of the signal at the output of the tank circuit. The detected peak voltage is stored in C7 and is compared to a dc reference voltage by comparator U2. If the detected signal level differs from the reference, U2 alters the reverse bias on varactor diode CR3 which changes the junction capacitance of the diode and thus the division ratio of the capacitive divider C9 and CR3. If the capacitance of CR3 decreases (due to an increase of reverse bias), the positive feedback to the base of Q1 is increased and the output level of the oscillator is increased.

DC Reference and Level Adjust

The reference to which the detected oscillator signal is compared in the ALC Loop originates with voltage reference diode VR1. VR1, when biased with a specified current, has a breakdown voltage that is constant with temperature. Q2 supplies a constant current to VR1. VR2 sets the emitter current of Q2 and has a temperature coefficient that tracks the base-emitter junction of Q2.

U1 inverts and slightly attenuates the reference voltage from VR1. R4 (LEVEL ADJ) permits fine adjustment of the reference and hence the output power of the oscillator. CR1 adds a temperature coefficient to the reference input of U2 which matches the temperature coefficient of the detector diode CR2. The Power Reference Oscillator is switched off by interrupting the −15V supply via the PWR REF OSC ON/OFF −15V line.

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TROUBLESHOOTING

General

Procedures for checking the Power Reference Oscillator Assembly are given below. The circuits to check are marked on the schematic diagram by a hexagon with a check mark and a number inside, for example, ⟨√3⟩ . Fixed signals are also shown on the schematic inside a hexagon, for example, ⟨+1.9 TO +2.1 VDC⟩ . Remove the assembly, the assembly cover, and RF cables where necessary to make measurements.

CAUTION

When removing the RF power calibrator assembly, take care that the power supply terminals do not short against the metal chassis parts.

Tighten SMC connectors to 0.6 N· m (5 in· lb). Hand tightening of connectors is insufficient. Hand-tightened connectors can work loose and cause reduced performance or malfunctions.

If a fault in the Power Reference Oscillator is isolated and repaired, the correct output level (1 mW) must be set by a very accurate power measurement system. To see what this entails, review Adjustment 18 or 19—Power Reference *in Section 5.*

Equipment

Oscilloscope ..... HP 1740A

⟨√1⟩ Power Reference Oscillator Check

1. Connect a high-impedance, dc coupled oscilloscope to C3 (where the violet wire connects). Press RF POWER, and switch CALIBRATE on and off. The dc waveform should read between +1 and +2 Vdc when off and between −15 and −14 Vdc when on.

   Hint: If faulty, see Service Sheet 2 and check the Power Reference Oscillator Control.

2. Switch CALIBRATE on. Connect the oscilloscope to A32TP1. The voltage should read between +3.5 and +5.5 Vdc.

   Hint: The voltage at the collector of Q2 should be between −6.4 and −6.0 Vdc.

3. Connect the oscilloscope to A32TP2. The voltage should read between −5 and −1 Vdc.

   Hint: If the oscillator does not oscillate and the voltage at A23TP2 is more negative than −5 Vdc, U2 is working properly. If the oscillator output is very large and the voltage at A23TP2 is more positive than −1 Vdc, U2 is working properly.

   Hint: Modulation or spurious signals on the oscillator output may be caused by a fault in R9, R10, R11, or C8.

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Service Sheet 4

ASSEMBLIES

RF Input (A15)

PRINCIPLES OF OPERATION

General.

The RF Input Assembly contains the Input Attenuator, Overpower Protection, RF Level and Overpower Detector, and 5.25 MHz High-Pass Filter. Together, these circuits provide a suitable input signal for the Input Mixer (see Service Sheet 5).

5.25 MHz High-Pass Filter.

The 5.25 MHz High-Pass filter must be switched in by entering user Special Function 3.3 or 3.4 SPCL. Its function is to prevent the IF from responding to low-frequency, spurious signals which may be present along with a higher frequency input signal. The filter is a diplexer type which presents a 50Ω termination to all frequencies present at its output (whether above or below the cutoff frequency). An example of such a signal is the IF itself. The 50Ω termination improves the RF flatness of the Input Mixer over the wide range of input frequencies. The filter is switched in by relay K2 via driver transistor Q2.

Input Attenuator.

The Input Attenuator is composed of two 20 dB pads and one 10 dB pad for a range of 0 to 50 dB in 10 dB steps. Each pad is a resistive pi network. The first shunt arm of 20 dB No. 1 has two resistors (R15 and R19) in parallel to handle the brunt of high-level RF power. The pads are switched in by relays K3, K4, and K5 driven by transistors Q6, Q7, and Q8 respectively.

RF Level Detector.

The RF Level Detector (CR1 and CR2) senses the positive peak of the input signal. The detected dc voltage is used to initially set the Input Attenuator, to give an indication of RF level when the RF LEVEL measurement mode is selected, and to de-activate the Overpower Protection relay. Because the detector can introduce a slight amount of clipping on the input signal, it is switched slightly off after the instrument is tuned to the input signal except when measuring Rf level. The detector is shut off when Q10 is on.

Detector Amplifier.

U1 and U2 from a unity-gain amplifier and peak detector with offset. U2 detects the peaks of the signal from the RF Level Detector when AM is present on the signal. Whenever the voltage at the non-inverting (+) input of U2 exceeds that of the inverting input (−), the output transistor of U2 (see Note 2 on the schematic) turns on and charges C22 from its emitter until the voltage across C22 equals the input voltage at the inverting input plus the constant drop across CR7, R34, CR8, and R42. U1 is simply a unity-gain buffer amplifier. When the input voltage drops the output of U2 shuts off, and C22 remains charged to its previous level. R39 and R41 slowly discharge C22 when the input signal level is lowered or removed. CR7 and CR8 are biased on by R26 which acts as a current source. CR7 and CR8 are hot carrier diodes whose offset voltage tracks that of CR1 and CR3 with temperature. Fine adjustment of the offset is made with R42 which is set for zero output from U1 when no input signal is present.

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Overpower Detector.

The Overpower Detector amplifier U3 senses when the output from the RF Level Detector and voltage divider R36, R54, and R37 exceeds +2.7V (set by R43, R44, and hysteresis resistor R56) which corresponds to 1W of input power. The output of U3A then goes low and deactivates the Overpower Protection relay K1 via the LO Control circuits (see Service Sheet 21.) K1 remains de-activated until reset by the operator pressing any front-panel key.

The OVERPOWER(L) output line from U3A is also an input line from the LO Control circuit which perfroms two other functions. First the line is used to discharge the storage capacitor C22 of the Detctor Amplifier between RF LEVEL measurements. Second, the line is used to turn off the RF Level Detector when RF LEVEL is not being measured after the instrument is tuned. To accomplish these two tasks, a qausi-low is put on the line by the LO Control circuits. The low does not trip the overpower circuit but is low enough to set the Detector Amplifier Discharge comparator U3B low which discharges C22. It also turns off the RF Level Detector by turning on Q11, Q9, and Q10. In this state the RF Level Detector can still sense an overpower condition and trip the Overpower Protection.

Relay Drivers.

The drivers for the five relays are similar. A TTL low at the base of a driver transistor (Q1, Q2, Q6, Q7, or Q8) turns the transistor on and energizes the relay. The relay contacts move in the direction of the arrow. The capacitors across the relay coils suppress the flyback voltage when the coil is de-energized and improve switching speed. Control of the relays is via the LO Control circuits (see Service Sheet 21).

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TROUBLESHOOTING

General

Procedures for checking the RF Input Assembly are given below. The circuits to check are marked on the schematic diagram by a hexagon with a check mark and a number inside, e.g. ⟨√3⟩ . In addition, any points outside the labeled area that must be checked are also identified. Fixed signals are shown on the schematic inside a hexagon, e.g. ⟨+1.9 to +2.1 Vdc⟩ . Extend the board assembly and its input and output cables where necessary to make measurements.

CAUTION

Tighten SMC connectors to 0.6 N-m (5 in. lb). Hand tightening of connectors is insufficient. Hand tightened connectors can work loose and cause reduced performance, malfunctions, or damage to the instrument.

Equipment

Oscilloscope ..... HP 1740A
Power Supply ..... HP 6215A
Signal Generator ..... HP 8640B
Voltmeter ..... HP 3455A

⟨√1⟩ Input Attenuator Check

1. Set the signal generator to 11 MHz CW at +13 dBm. Connect int Rf output to the input of an ac coupled oscilloscope. Switch the input impedance of the oscilloscope to 50Ω or terminate the input in 50Ω using a tee.

2. Fine adjust the signal generator's level for an oscilloscope display of 3 Vpp.

3. Reconnect the signal generator's output to the Modulation Analyzer's INPUT. (The input cable, W1 or W3, should be connected to A15J2 with an extender cable.) Reconnect the oscilloscope to A15J2 (RF OUT).

4. Key in 41.0 SPCL to initialize the instrument. Key in the Direct Control Special Functions and check the signals indicated in Table 8F-8.

Hint: If the oscilloscope display reads low for all above conditions, check the 5.25 MHz High-Pass Filter, Overpower Protection, and input cable (W1 or W36).

Table 8F-8. *Levels at XA15, Q6c, Q7c, and Q8c,* ⟨√1⟩ *Step 4*

Check	Direct Control Special Function	Level (TTL) at						Oscilloscope Display (Vpp)
		A28XA15 Pin			Transistor			
		18	19	20	Q6-c	Q7-c	Q8-c	
Thru Path	0.047	L	L	L	H	H	H	2.75 to 3.00
10 dB	0.045	L	H	L	H	L	H	0.83 to 1.00
20 dB No. 1	0.043	H	L	L	L	H	H	0.26 to 0.31
20 dB No. 2	0.046	L	L	H	H	H	L	0.26 to 0.31

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⟨√2⟩ 5.25 MHz High-Pass Filter Check

1. Set the signal generator to 5.25 MHz CW at +3 dBm. Connect its RF output to the input of an ac coupled oscilloscope. Switch the input impedance of the oscilloscope to 50Ω or terminate the input in 50Ω using a tee.
2. Fine adjust the signal generator's level for an oscilloscope display of 1 Vpp.
3. Reconnect the signal generator's output to the Modulation Analyzer's INPUT. (Connect the input cable, W1 or W36, to A15J1 with an extender cable.) Reconnect the oscilloscope to A15J2 (RF OUT).
4. Key in 41.0 SPCL and 0.047 SPCL to initialize the instrument and set the attenuator to the thru path. Key in the Direct Control Special Functions and check the signals indicated in Table 8F-9.

Table 8F-9. *Levels at XA15, and Q2c ⟨√2⟩ Step 4*

Check	Direct Control Special Function	Level (TTL) at A28XA15 Pin 28	Level (TTL) at Q2-c	Oscilloscope Display (Vpp)
Thru Path	0.024	L	H	0.76 to 1.00
5.25 MHz HPF	0.02C	H	L	0.59 to 0.73

Hint: If the oscilloscope display reads low for both above conditions, check the Input Attenuator, Overpower Protection, and input cable (W1 or W36).

⟨√3⟩ Overpower Protection Check

1. Set the signal generator to 11 MHz CW at +13 dBm. Connect its RF output to the Modulation Analyzer's INPUT.
2. Connect an ac coupled oscilloscope to A15J2 (RF OUT). Switch the input impedance of the oscilloscope to 50Ω or terminate the input in 50 Ω using a tee.
3. Key in 41.0 SPCL to initialize the instrument. Key in 1.1 SPCL to set the input attenuation to 0 dB. Check the signals indicated in Table 8F-10 for the thru path only.

Table 8F-10. *Levels at XA15 and Q1c ⟨√3⟩ Step 3*

Check	Level (TTL) at A28XA15 Pin 17	Level (TTL) at Q1-c	Oscilloscope Display (Vpp)
Thru Path	L	H	2.75 to 3.00
Overpower	H	L	0

Hint: If the oscilloscope display reads low, check the Input attenuator, 5.25 MHz High-Pass Filter, and input cable (W1 or W36).

4. Remove signal generator from INPUT. Set power supply to 20 Vdc. Touch the +20V lead to the Modualtion Analyzer's INPUT (the minus side should be at ground).
5. Reconnect the signal generator. Check the signals indicated in the table under step 3 for the condition of overpower. The display should also show E06.
6. Repeat step 3 to check the recovery from the overpower condition.

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NOTE

If step 4 is repeated, it is usually necessary to first discharge the input dc blocking capacitor by connecting a 50Ω termination to the INPUT. Discharge it also after completing this check.

⟨√4⟩ Overpower Detector Check

1. Key in 41.0 SPCL to initialize the instrument.
2. Connect a high-impedance, dc coupled oscilloscope or a dc voltmeter to A28XA15 pin 21. The node should be a TTL high.
3. Induce an overpower transient by touching the +20V lead to the Modulation Analyzer's INPUT (the minus side should be at ground). The node should show a momentary low. The display should also show E06.

NOTE

If steps 1 to 3 are to be repeated, it is necessary to first discharge the input dc blocking capacitor by connecting a 50 Ω termination to the INPUT. Discharge it also after completing this check.

⟨√5⟩ Detector Amplifier Check

1. Set the signal generator to 11 MHz CW at +13 dBm. connect its RF OUTPUT to the Modualtion Analyzer's INPUT. (Connect the input cable, W1 or W36, to A15J1 with an extender cable.)
2. Key in 41.0 SPCL to initialize the instrument. Press RF LEVEL.
3. Key in 0.024 SPCL and 49.31 SPCL to turn the detector on and to connect the internal voltmeter to the output of the Detector Amplifier. Change the level of the signal generator as indicated in Table 8F-11 and note the display. Alternatively, measure A15TP1 (RF DET) with a dc voltmeter.

Table 8F-11. *Detector Amplifier Limits*

RF Level (dBm)	Display Limits	Voltage Limits at A15TP1 (Vdc)
+13	1.05 to 1.25	1.05 to 1.25
+3	0.27 to 0.33	0.27 to 0.33
Off	−0.003 to +0.003	−0.008 to +0.008

Hint: If the off condition above is slightly out of limit, perform the RF Detector Offset Adjustment.

⟨√6⟩ RF Level Detector Offset Check

1. Remove the cable (W1 or W36) from A15J1. Key in 0.024 SPCL to turn the detector on.
2. Measure the dc voltage at the junction of CR4 and C13. It should be between −0.5 and −0.2 Vdc. (The input impedance of the voltmeter must be at least 10 MΩ.)
3. Measure the dc voltage at pin 2 of U2. It should be 50 to 70 mV more negative than the voltage read in step 2.
4. Key in 0.020 SPCL to turn the detector off.
5. Measure the dc voltage at the junction of CR4 and CR13. It should be between +8.5 and +10.0 Vdc.
6. Measure the dc voltage at pin 2 of U2. It should be between +13.0 and +14.5 Vdc.

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⟨√7⟩ Detector Amplifier Discharge Check

1. Set the signal generator to 11 MHz CW at +13 dBm. Connect its RF output to the Modulation Analyzer's INPUT. (Connect the input cable, W1 or W36, to A15J1 with an extender cable.
2. Key in 41.0 SPCL to initialize the instrument. Press RF LEVEL.
3. Key in 0.020 SPCL to turn the detector off. Key in 49.31 SPCL to connect the internal voltmeter to the output of the Detector Amplifier. The display should read between −0.0200 and +0.0200.
4. Key in 0.024 SPCL to turn the detector on. Key in 49.31 SPCL. The display should read between 1.0000 and 1.3000.
5. Set the signal generator for 50% AM at a 20 Hz rate. The display should vary no more than ±0.1V from its average value.
6. Press RF LEVEL. Switch the signal generator's AM off, then turn the RF off and note the Modualtion Analyzer's display as the reading decreases. The reading should decrease to less than 0.010 −03 watts by the second reading after the RF is switched off.

⟨√8⟩ SWR Check

1. Perform the SWR portion of the RF Level Performance Test.

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Service Sheet 5

ASSEMBLIES

- **A17 Input Mixer**
- **A16 Buffer Amplifier**
- **A18 IF Amplifier**
- **S2 LO Input Switch (Option Series 030)**

PRINCIPLES OF OPERATION

General—A17 Input Mixer Assembly

The Input Mixer Assembly down-converts the input signal to an intermediate frequency (IF). For input signals above 2.5 MHz, the IF is equal to the LO frequency minus the signal frequency. The IF is normally 1.5 MHz for frequencies above 10 MHz and 455 kHz for frequencies between 2.5 and 10 MHz. Below 2.5 MHz the input signal passes directly through the Mixer into the IF Amplifier without down-conversion.

The Input Mixer Assembly contains the Mixer, LO Amplifier, and two IF filters (a 455 kHz Bandpass Filter and a 4 MHz Low-Pass Filter). The 4 MHz Low-Pass Filter is followed by a 2.5 MHz Low-Pass Filter in the AM Demodulator Assembly which determines the frequency response of the 1.5 MHz IF (see Service Sheet 8).

LO Amplifier

The input to the LO Amplifier is a 1.25 to 1301.5 MHz signal which comes from the LO Divider Assembly (see Service Sheet 17). The amplifier has a gain of approximately 10 dB and drives the L port of the Mixer (U1) at about +10 dBm. The amplifier has two stages, stripline transistors Q4 and Q6, which are actively biased by Q5 and Q7 respectively. Using Q4 and Q5 to illustrate the biasing, notice that for dc levels the emitter of Q5 is connected directly to the collector of Q4. (L3 is an RF choke.) The base of Q5 is fixed at the voltage determined by voltage divider R1 and R2. The emitter of Q5 is normally a junction drop above this. The collector of Q5 is the source of dc base current for Q4. Changes in the collector voltage of Q4 alter the collector current of Q5, which regulates the collector voltage of Q4.

The gain of each stage is inversely proportional to the total emitter resistance and directly proportional to the collector load. C3 increases the gain slightly at high frequencies.

Mixer

Mixer U1 is a single-balanced type (that is, signals at the L port are balanced out at the R and I ports, but signals at the R port are not balanced at the I port). This permits low-frequency input signals to pass into the IF without down-conversion. The LO signal is coupled into the Mixer by U1T2. IF is coupled out from the center tap of the same transformer. U1C1 is the first element of the IF filters that follow. U1T1 optimizes the impedance seen by the IF Amplifier. The Input Pad ahead of the Mixer's R port improves the flatness over the wide range of input frequencies by presenting a constant impedance to the IF at the R port. The Limiter adds protection to the Mixer.

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IF Filters *(2314A to 2636A)*

The 455 kHz Wide Bandpass Filter has seven poles and a 3 dB bandwidth of 200 kHz. L8 is adjusted for best passband flatness to minimize incidental AM (AM generated in the IF as the result of FM). L11 is adjusted primarily for best phase linearity vs. frequency to minimize FM distortion generated in the IF. The filter is switched in by Q3 and Q1 which forward-bias CR3 and CR6 when the output of U2B goes low. This also turns on DS1.

The 4 MHz Low-Pass Filter has three poles ***(2314A to 2332A)*** or five poles ***(2333A to 2636A)***. It is switched in by Q2 which forward-biases CR4 and CR5 when U2A goes low. Control of the filters is via the LO Control Assembly (see Service Sheet 21).

The IF is routed in one of two ways depending upon the option installed. For instruments without Option 030, the IF is routed directly to the A18 IF Amplifier Assembly. For instruments with Option 030 installed, the IF is routed to the A16 Buffer Amplifier Assembly.

IF Filters *(2642A and Above)*

The down-converted (IF) signal from the Input Mixer is filtered by the three-pole, 4 MHz Low-Pass Filter 1. (U1C2 in the Input Mixer is the first reactive component of the filter.) When the 455 kHz IF is selected, C32 is switched in (by Q13 turning on CR8 and CR9) to improve the conversion efficiency of the Input Mixer for low-frequency input signals. The IF is then amplified by the First IF Amplifier. The amplifier has a gain of 5 to the input of Q9 (the input to the 455 kHz Wide Bandpass Filter) and 2.3 to the input of Q8 (the through-path). C18, R13, and L7 add a slight slope to the IF frequency response to compensate for slope in the 4 MHz Filters 1 and 2.

Transistor Q12B controls the routing of the IF to the 455 kHz Wide Bandpass Filter or the through path. When Q12B goes on, Q12C goes on and Q12D goes off. Q12C forward-biases CR3 and CR4, activates Q9 and Q1, and switches the 455 kHz Wide Bandpass Filter in. At the same time CR5 and Q8 go off and switch the through-path out. This also turns on DS1. Control of the filters is via the LO Control Assembly (see Service Sheet 21).

The seven-pole, 455 kHz Wide Bandpass Filter has 3 dB bandwidth of 200 kHz. L8 is adjusted for best passband flatness to minimize incidental AM (AM generated in the IF as the result of FM). L11 is adjusted primarily for best phase linearity vs. frequency to minimize FM distortion generated in the IF.

NOTE

In Selective Power (Option Series 030) measurement modes, a second 455 kHz IF bandpass filter is inserted into the IF path. For Selective Power measurements, the filter bandwidth depends on the particular measurement mode and option installed.

The IF is routed to the A72 IF Channel Filter Assembly through the Second IF Amplifier, which has a gain of 2.8 at the output to J4 and unity gain at the output to Q1. The IF is also routed through 4 MHz Low-Pass Filter 2 on to the A18 IF Amplifier Assembly. The 4 MHz Low-Pass Filter 2 has three poles.

General — A16 IF Buffer Amplifier Assembly (Opt. 030 only) *(2314A to 2636A)*

The signal from the Input Mixer is split and amplified by two descrete non-inverting operational amplifiers. One is a 0 dB gain buffer for the A18 IF Amplifier and the other a 9 dB gain amplifier for the Opt. 030 circuitry.

IF Buffer Amplifier

Transitors Q3, Q2, and Q1 form a non-inverting operational amplifier with an ac gain of 2 (6 dB). The non-inverting input is the base of Q3 and the inverting input is the emitter of Q3. The voltage divider formed by R10 and R9 supplies base bias for both Q3 and Q6. The gain of the amplifier is 1+(R14/R12). The output from the emitter of Q1 is divided by 2 (6 dB) by the voltage divider formed by R17 and the input impedance of the following circuitry. This results in a overall gain of 1 (0 dB).

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IF Amplifier

Transistors Q6, Q5, and Q4 form a non-inverting operational amplifier with an ac gain of approximately 5.6 (15 dB) . The operation of the amplifier is identical to that of the IF Buffer Amplifier. The gain determining resistors are R5 and R3. Resistor R8 forms a voltage divider with the input impedance of the following circuitry, which also divides the output from the emitter of Q4 by 2 (6dB). This results in a overall gain of 2.8 (9 dB).

General—A18 IF Amplifier Assembly

The signal from the Input Mixer, whether down-converted or not, is amplified by the IF Amplifier. The amplifier is a low-noise type with 33 dB of gain and a phase compensation network to reduce FM distortion. The IF Amplifier has three stages.

IF Input Amplifier

The first stage, Q7 and Q5, is low noise and has 20 dB of gain. An active input impedance, the result of feeding signal back to the input through R6, generates a lower source noise than would be generated by a strictly passive resistance. The input impedance is essentially equal to R6 divided by the amplifier gain. The gain is approximately R9 divided by R7.

Inverting Amplifier

The second stage is a unity-gain amplifier with a phase-shift characteristic that can be adjusted to compensate for phase shifts generated in the 1.5 MHz IF system. This compensation improves FM distortion. The IF shape can also be adjusted to minimize incidental AM.

A simplified diagram of this stage is shown in Figure 8F-8. Q1 is shown as an amplifier with a gain of −1, Q2 with a gain of +1. The voltage gain for the circuit is

$$\frac{V_2}{V_1} = \frac{R - jX}{R + jX}.$$

which has a constant magnitude (+1) and a variable phase shift. The impedance jX is formed by L1, L2, C15, and C16. R is formed by the combination of R17, R23, and R24. R is fine adjusted by R23 for optimum phase shift (minimum FM distortion) at 1.5 MHz. R19 fine adjusts the gain of Q1 for best flatness (minimum incidental AM) at 1.5 MHz.

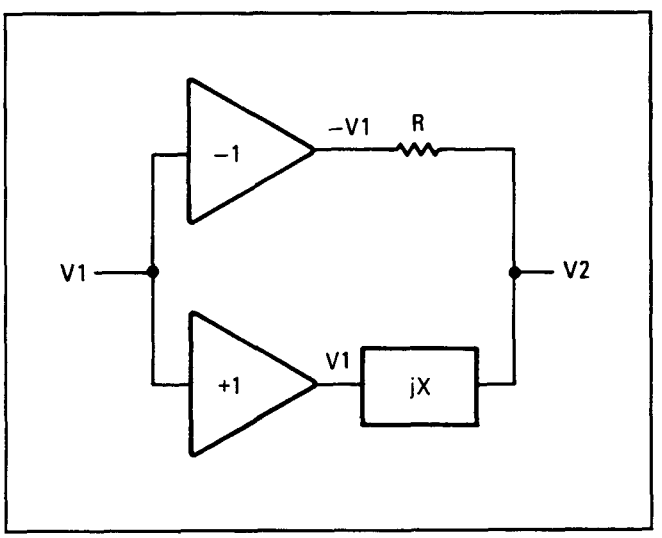


Figure 8F-8. *Simplified Diagram of Phase Compensation Amplifier*

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IF Output Amplifier

The third stage is a 13 dB amplifier which drives the AM Demodulator. Its gain is approximately one plus R29 divided by R27.

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TROUBLESHOOTING

General

Procedures for checking the Input Mixer and IF Amplifier Assemblies are given below. The circuits to check are marked on the schematic diagram by a hexagon with a check mark and a number inside, for example, ⟨√3⟩ . In addition, any points outside the labeled area that must be checked are also identified. Fixed signals are also shown on the schematic inside a hexagon, for example, ⟨+1.9 TO +2.1 VDC⟩ . Extend the board assemblies and their input and output cables where necessary to make measurements.

CAUTION

Tighten SMC connectors to 0.6 N·m (5 in·lb). Hand tightening of connectors is insufficient. Hand-tightened connectors can work loose and cause reduced performance, malfunctions, or damage to the instrument.

Equipment

Oscilloscope	HP 1740A
Signal Generator	HP 8640B
Spectrum Analyze	HP 8559A/182T
Test Probe	HP 1250-1598
Voltmeter	HP 3455A

⟨√1⟩ LO Amplifier General Check

NOTE

This test checks only the LO Amplifier at a low frequency but will easily localize a catastrophic failure. ⟨√2⟩ LO Amplifier Check *is more thorough and will detect more subtle failures; however, more time and equipment are required.*

1. Key in 5 and press MHz to set the LO to 5.455 MHz.
2. Connect a high-impedance oscilloscope to the base of A17Q4. The waveform should be a square wave with a period of approximately 180 ns and an amplitude of 0.5 Vpp or greater excluding ringing.

   Hint: If the signal is faulty, check the output from the A19 LO Divider Assembly (see Service Sheet 17).
3. Connect the oscilloscope to the collector of A17Q4. The waveform should be a square wave of 1.2 Vpp or greater excluding ringing.
4. Connect the oscilloscope to the collector of A17Q6. The waveform should be a square wave of 1 Vpp or greater excluding ringing overshoot on the falling edge.

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⟨√2⟩ LO Amplifier Check

NOTE

To check for a catastrophic failure of the LO Amplifier, use the ⟨√1⟩ LO Amplifier General Check *above.*

1. Unplug A17U1 Mixer. Gently pry it from its socket with a screwdriver blade.
2. Set the spectrum analyzer to measure a +20 dBm, 0 to 1400 MHz signal. Connect its input to pins 8 and 9 of the Mixer socket using the test probe. The probe center goes on pin 9.
3. Key in 57.0 SPCL to cause the LO to sweep sequentially across bands DBLR through 3. The LO signal should sweep slowly from above 1300 MHz to below 40 MHz. The sweep will occur over five bands. As the low end of a band is reached, the sweep will stop, jump up slightly in frequency, then continue to sweep. Throughout the sweep, the fundamental of the LO should be between +7 and +15 dBm.

   Hint: A faulty level may also be the result of a faulty output from the A19 LO Divider Assembly.

   Hint: The sweep can be halted by pressing the SPCL key. Use manual tune to manually set the LO frequency.
4. Set the spectrum analyzer to view a 0 to 40 MHz signal.
5. Key in 56.0 SPCL to cause the LO to sweep sequentially across bands 4 through 8. The LO should sweep slowly from above 50 to below 1.25 MHz in the manner described in step 3 above.

NOTE

The test probe will cause a low-frequency rolloff to about +4 dBm at 1.25 MHz.

The low-frequency bands can also be viewed on an oscilloscope. The oscilloscope should have a 50Ω termination. The signal should be a square wave with an amplitude of approximately 2 Vpp excluding ringing and the rolloff due to the probe.

⟨√3⟩ Input and Mixer Check

1. Set the signal generator to 18 MHz CW at 0 dBm. Connect its RF output to the input of an ac coupled oscilloscope. Switch the input impedance of the oscilloscope to 50Ω or terminate the input in 50Ω using a tee.
2. Fine adjust the signal generator's level for an oscilloscope display of 800 mVpp.
3. Reconnect the signal generator's output to A17J2 (RF IN). Reconnect the oscilloscope to A17J1 (IF OUT).
4. Press the blue key, then press INSTR PRESET (the AUTOMATIC OPERATION key) to preset the instrument. Key in 18 and press MHz to set the LO to 19.5 MHz. The waveform should be a sine wave with an amplitude of 70 to 110 mVpp and a period of approximately 670 ns. A slight fuzziness on the waveform is normal; it is the partially filtered sum frequency. The 455 kHz IF annunciator (A17DS1) should be off.

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⟨√4⟩ Filter Switching Check *(2314A to 2636A)*

NOTE

Filter frequency response is tested along with the IF Amplifier in ⟨√6⟩ IF Filter Check.

1. Disconnect any signal at the Measuring Receiver's INPUT connector. Key in the Direct Control Special Functions indicated in Table 8F-12a. For each setting note the reading on the dc voltmeter connected to the points indicated. Also observe the 455 kHz IF annunciator (A17DS1).

Table 8F-12a. *Levels at A17U2, Q1, Q2, and Q3,* ⟨√4⟩ *Step 1*

Direct Control Special Function	Voltage Limits (Vdc) at A17				State of A17DS1
	U2A-1	U2B-7	Q1-c and Q3-c	Q2-c	
0.030	0 to +1	+10 to +15	−5.4 to −4.5	+1 to +2	Off
0.031	+12 to +15	0 to +1	+0.5 to +1	−5.4 to −4.5	On

⟨√4⟩ Filter Switching, First and Second IF Amplifiers Check *(2642A and Above)*

NOTE

Filter frequency response is tested along with the IF Amplifier in ⟨√6⟩ IF Filter Check.

1. Set the signal generator to 455 kHz CW at 0 dBm. Connect its RF output to A17J2 (RF IN). (The internal LO should be connected to A17J3 (LO IN).)
2. On the Measuring Receiver, key in 1300 MHz to manually tune the LO. (LO signal must be present at the mixer even though no down-conversion will be used.)
3. Connect a high-impedance, ac coupled oscilloscope to the base of A17Q11. The oscilloscope should have a low-capacitance 10:1 divider probe. The waveform should be a sine wave with an amplitude between 200 and 500 mVpp and a period of approximately 2.2 μs. (Depending upon the bandwidth of the oscilloscope, the LO signal may also be visible in the form of fuzz.)

   Hint: If the waveform is faulty, perform ⟨√3⟩ *Input Mixer Check.*
4. Set the signal generator level for a waveform of 300 mVpp. Connect the oscilloscope to the collector of A17Q10. The waveform should have an amplitude of 1.2 to 1.6 Vpp.
5. Connect the oscilloscope to the base of A17Q8. The waveform should have an amplitude of 500 to 800 mVpp.
6. Connect the oscilloscope to the emitter of A17Q1 and Q3 as indicated in Table 8F-12b. Key in the Direct Control Special Functions indicated in the table. For each setting, the reading on the oscilloscope should be as indicated. If faulty, also check the voltages indicated and observe the 455 kHz IF annunciator (A17DS1).

Table 8F-12b. *Levels at A17Q3, Q8, Q12, and Q13,* ⟨√4⟩ *Step 6*

Direct Control Special Function	Voltage Limits (mVpp) at A17		Voltage Limits (Vdc) at A17				State of A17DS1
	Q3-e	Q8-e	Q12B-7	Q12C-8	Q12D-13	Q13-c	
0.030	<10	600 to 700	+12 to +15	0 to +0.2	+9 to +11	0 to +0.2	Off
0.031	500 to 700	300 to 400	0 to +0.2	+8 to +10	0 to +0.1	+9 to +11	On

7. Key in 0.030 SPCL. Connect the oscilloscope to A17J1 (IF OUT). (The cable to A17J1 should not be connected.) The waveform should have an amplitude of 600 to 800 mVpp.

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8. Key in 0.031 SPCL. Connect the oscilloscope to A17J4. (The cable to A17J4 should not be connected.) The waveform should have an amplitude of 1.4 to 1.6 Vpp.

⟨√5⟩ IF Amplifier Check

1. Set the signal generator to 1.5 MHz CW at −23 dBm. Connect its RF output to Al8J2 (IF IN).
2. Connect a high-impedance, ac coupled oscilloscope to the base of A18Q7. The oscilloscope should have a low-capacitance 10:1 divider probe.
3. Fine adjust the signal generator's level for an oscilloscope display of 100 mVpp.
4. Connect the oscilloscope to the emitter of A18Q5. The waveform of the 1.5 MHz signal should be sinusoidal with an amplitude of 0.9 to 1.1 Vpp.
5. If necessary, readjust the signal generator's level for an oscilloscope display of 1.0 Vpp.
6. Connect the oscilloscope to the collector of A18Q4. The waveform should be sinusoidal and have an amplitude of 4.6 to 5.0 Vpp.

   Hint: The gain of the IF Output Amplifier is 4.8 open circuit. The Phase Compensation Amplifier has a gain of 1, but capacitive loading of the oscilloscope prevents measuring the gain separately.
7. Vary the signal generator frequency from 0.15 to 2.5 MHz. The amplitude of the waveform should remain constant within 200 mV.

   Hint: The collectors of A18Q6 and Q1 should be flat with frequency also. The phase difference between the emitter of A18Q5 and collector of A18Q4 should be 180° at 4.4 MHz and 1.03 MHz and 0° at a frequency between 2.0 and 2.5 MHz and between 70 and 130 kHz. If the signal generator frequency does not extend to 70 kHz, use an audio source.

⟨√6⟩ IF Filters Check *(2314A to 2636A)*

NOTE

This check assumes that ⟨√5⟩ IF Amplifier Check *gives positive results.*

1. Set the signal generator to 18.00 MHz CW at −27 dBm. Connect its RF output to the Measuring Receiver's INPUT.
2. Connect an ac coupled oscilloscope to A18J1 (IF OUT). Switch the input impedance of the oscilloscope to 50Ω or terminate the input in 50Ω using a tee.
3. Press the blue key, then press INSTR PRESET (the AUTOMATIC OPERATION key) to preset the instrument. Key in 18 and press MHz to set the LO to 19.5 MHz and generate a 1.5 MHz IF. The waveform should be a sinusoidal signal with a period of approximately 670 ns and an amplitude between 200 and 300 mVpp.

   Hint: If the signal is faulty, perform the checks above.
4. Fine adjust the signal generator's level for an oscilloscope display of 200 mVpp. Key in 20.5 and press MHz to generate a 4 MHz IF. The waveform frequency should increase, and its amplitude drop to between 120 and 160 mVpp.

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NOTE

The partially filtered sum signal may cause the waveform to appear slightly fuzzy.

5. Key in 18 and press MHz. Key in 3.1 SPCL to set the IF to 455 kHz. The waveform should be a sinusoidal signal with a period of approximately 2.2 μs and an amplitude between 150 and 190 mVpp.
6. If necessary, fine adjust the signal generator's level for an oscilloscope display of 200 mVpp. Key in 18.1 and press MHz to generate a 355 kHz IF. The waveform should have an amplitude between 120 and 160 mVpp.
7. Key in 17.9 and press MHz to generate a 555 kHz IF. The waveform should have an amplitude between 120 and 160 mVpp.

   Hint: If the amplitude in steps 6 or 7 is slightly out of limit, perform the *Adjustment 16—FM Distortion and Incidental AM—455 kHz IF.*

⟨√6⟩ IF Filters Check *(2642A and Above)*

NOTE

This check assumes that ⟨√5⟩ IF Amplifier Check *gives positive results.*

1. Set the signal generator to 18.00 MHz CW at −27 dBm. Connect its RF output to the Measuring Receiver's INPUT.
2. Connect an ac coupled oscilloscope to A18J1 (IF OUT). Switch the input impedance of the oscilloscope to 50Ω or terminate the input in 50Ω using a tee.
3. Press the blue key, then press INSTR PRESET (the AUTOMATIC OPERATION key) to preset the instrument. Key in 18 and press MHz to set the LO to 19.5 MHz and generate a 1.5 MHz IF. The waveform should be a sinusoidal signal with a period of approximately 670 ns and an amplitude between 200 and 300 mVpp.

   Hint: If the signal is faulty, perform the checks above.
4. Fine adjust the signal generator's level for an oscilloscope display of 200 mVpp. Key in 20.5 and press MHz to generate a 4 MHz IF. The waveform frequency should increase, and its amplitude drop to between 140 and 180 mVpp.
5. Key in 18 and press MHz. Key in 3.1 SPCL to set the IF to 455 kHz. The waveform should be a sinusoidal signal with a period of approximately 2.2 μs and an amplitude between 170 and 210 mVpp.
6. If necessary, fine adjust the signal generator's level for an oscilloscope display of 200 mVpp. Key in 18.1 and press MHz to generate a 355 kHz IF. The waveform should have an amplitude between 130 and 170 mVpp.
7. Key in 17.9 and press MHz to generate a 555 kHz IF. The waveform should have an amplitude between 120 and 150 mVpp.

   Hint: If the amplitude in steps 6 or 7 is slightly out of limit, perform the *Adjustment 16—FM Distortion and Incidental AM—455 kHz IF.*

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⟨√7⟩ LO Switch (Option Series 030) Check

1. Set the signal generator to 10 MHz CW at 0 dBm. Connect its RF output to the Measuring Receiver's rear-panel LO INPUT (chassis part J14).
2. Connect an ac coupled oscilloscope to the rear-panel LO OUTPUT (chassis part J13). Switch the input impedance of the oscilloscope to 50Ω or terminate the input in 50Ω using a tee.
3. On the Measuring Receiver, key in 23.0 SPCL to set the LO to internal. The waveform should be a sinusoidal signal with a period of approximately 100 ns and an amplitude approximately 630 mVpp.

   Hint: Terminal C+ (red wire) on the LO Input Switch (S2) should be between +4.8 and +5.2 Vdc. See *LO Switch Control Check* on Service Sheet 33.
4. Connect the oscilloscope to the end of cable W55 which connects to A17J3 (LO IN). No signal should be present.
5. On the Measuring Receiver, key in 23.1 SPCL to set the LO to external. As the special function is entered, an audible click should be heard. The waveform should be approximately 630 mVpp.

   Hint: The click indicates that the switch drive circuitry is probably good and S2 probably faulty.
6. On the Measuring Receiver, key in 23.0 SPCL to set the LO back to internal. An audible click should be heard as in step 5.

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Service Sheet 6 *(2314A to 2636A)*

ASSEMBLY

- **A55 IF Channel Filter Assembly (Option Series 030)**

PRINCIPLES OF OPERATION

General

The channel filters determine the passband characteristics of the IF for the high-selectivity measurement mode. The shape of the IF passband is dependent on the specific option pair (any two of Options 032, 033, 035, and 037) installed.

Channel Filters

The A55 Channel Filter Assembly contains two selectable IF Channel Filters, associated buffer amplifiers, a programmable 20 dB Amplifier, and associated switches. Transformer T1 steps up the IF level 12 dB. FETs Q1 and Q2 select the IF path through the two Channel Filters (FL1 and FL2). The FETs are controlled by the output of U5. For example, if U5 is low (−15V), diode CR1 switches on and CR2 off; FET Q2 is off and Q1 is on. Thus, the secondary winding of T1 is grounded on the low end, and the IF signal appearing at the upper end couples into FL1 via emitter follower Q6. Resistors R5 and R9 present the proper impedance to drive and terminate the crystal filters. (The resistor values vary to match the specific requirements of the Channel Filters.)

The output of the selected Channel Filter is amplified approximately 6 dB depending on filter loss. Diodes CR3 and CR4 steer the signal from the selected channel to the switchable 20 dB pad (R24, R25, and U1) and into the 20 dB output amplifier.

Digital Circuits

Transistors Q3 and Q4 drive coaxial RF switch S2 which switches the LO to either internal or external. (Refer to Service Sheet 5 for serial prefixes 2642A and above.) For a general discussion of instrument control, see *Instrument Bus* in Service Sheet BD5.

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TROUBLESHOOTING

General

Procedures for checking the IF Channel Filter Assembly is given below. The circuits to check are marked on the schematic diagram by a hexagon with a check mark and a number inside, for example, ⟨√3⟩. In addition, any points outside the labeled circuit area that must be checked are also identified. Fixed signals are also shown on the schematic inside a hexagon, for example, ⟨+1.9 TO +2.1 VDC⟩. Extend the board assembly where necessary to make measurements.

CAUTION

Tighten SMC connectors to 0.6 N·m (5 in·lb). Hand tightening of connectors is insufficient. Hand-tightened connectors can work loose and cause reduced performance or malfunctions.

Equipment

Oscilloscope ..... HP 1740A
Signal Generator ..... HP 8640B

⟨√1⟩ First Channel 1 Filter Check

1. Set the signal generator to between 454 and 456 kHz CW at −10 dBm (70.7 mVrms into 50Ω). Connect its RF output to A55J2 (IF IN) on the Measuring Receiver.
2. Press the blue key, then press INSTR PRESET (the AUTOMATIC OPERATION key) to preset the instrument.
3. Connect a high-impedance, ac coupled oscilloscope to the emitter of Q6. The 455 kHz signal should have an amplitude between 1.0 and 1.5 Vpp.

   Hint: The gate of Q2 should be approximately −9 Vdc. Pin 7 of U4 should be a TTL low.
4. Set the oscilloscope gain for a display of 6 divisions peak-to-peak.
5. Connect the oscilloscope to the base of Q11. Fine tune the signal generator for an amplitude peak. The amplitude should be between 1.5 and 2.5 divisions peak-to-peak.
6. Set the oscilloscope gain for a display of 6 divisions peak-to-peak. Tune the signal generator up and down and note the frequencies at which the waveform drops to 3 divisions. The difference between the highest and lowest frequencies should be within the limits listed in Table 8F-13.

   Hint: R5 and R9 are supplied with FL1 when FL1 is replaced.

Table 8F-13. *Bandwidth of First Channel 1 Filter,* ⟨√1⟩ *Step 6*

Option Combination	Frequency Difference Limits (kHz)	
	Minimum	Maximum
032 and 035 033 and 035 035 and 037	25.0	35.0
032 and 033 033 and 037	12.4	16.9
032 and 037	6.4	10.4

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7. Tune the signal generator back to the amplitude peak. Adjust the oscilloscope gain for a display of 2 divisions peak-to-peak. Connect the oscilloscope to the collector of Q12. The waveform should have an amplitude between 5 and 6 divisions peak-to-peak.
8. Connect the oscilloscope to pin 8 of U1A. The waveform should have the same amplitude as in step 7.

⟨√2⟩ First Channel 2 Filter Check

1. Set the signal generator to between 454 and 456 kHz CW at −10 dBm (70.7 mVrms into 50Ω). Connect its RF output to A55J2 (IF IN) on the Measuring Receiver.
2. Press the blue key, then press INSTR PRESET (the AUTOMATIC OPERATION key) to preset the instrument.
3. Connect a high-impedance, ac coupled oscilloscope to the emitter of Q5. Key in 0.3D3 SPCL to select channel 2. The 455 kHz signal should have an amplitude between 1.0 and 1.5 Vpp.

   Hint: The gate of Q1 should be approximately +9 Vdc. Pin 7 of U4 should be a TTL high.
4. Set the oscilloscope gain for a display of 6 divisions peak-to-peak.
5. Connect the oscilloscope to the base of Q9. Fine tune the signal generator for an amplitude peak. The amplitude should be between 1.0 and 1.6 divisions peak-to-peak.
6. Set the oscilloscope gain for a display of 4 divisions peak-to-peak. Tune the signal generator up and down and note the frequencies at which the waveform drops to 2 divisions. The difference between the highest and lowest frequencies should be within the limits listed in Table 8F-14.

   Hint: R6 and R10 are supplied with FL2 when FL2 is replaced.

Table 8F-14. *Bandwidth of First Channel 2 Filter,* ⟨√1⟩ *Step 6*

Option Combination	Frequency Difference Limits (kHz)	
	Minimum	Maximum
032 and 037 033 and 037 035 and 037	3.0	7.0
032 and 033 032 and 035	6.4	10.4
033 and 035	12.4	16.9

7. Tune the signal generator back to the amplitude peak. Adjust the oscilloscope gain for a display of 2 divisions peak-to-peak. Connect the oscilloscope to the collector of Q10. The waveform should have an amplitude between 6 and 9 divisions peak-to-peak.
8. Connect the oscilloscope to pin 8 of U1A. The waveform should have the same amplitude as in step 7.

⟨√3⟩ Channel Output Circuit Check

1. Set the signal generator to between 454 and 456 kHz CW at −10 dBm (70.7 mVrms into 50Ω). Connect its RF output to A55J2 (IF IN) on the Measuring Receiver.
2. Press the blue key, then press INSTR PRESET (the AUTOMATIC OPERATION key) to preset the instrument.
3. Connect a high-impedance, ac coupled oscilloscope to pin 8 of U1A. Fine tune the signal generator for an amplitude peak. The 455 kHz signal should have an amplitude between 1.0 and 1.2 Vpp.

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Hint: If the signal is faulty, perform ⟨√1⟩ *First Channel 1 Filter Check.*

4. Set the oscilloscope gain for a display of 6 divisions peak-to-peak. Connect the oscilloscope to pin 9 of U1A. Key in 0.3D1 SPCL to switch out the Channel Output Attenuator. The waveform should have the same amplitude as in step 3.

   Hint: Pin 1 of U1A should be a TTL low, pin 2 of U1B a TTL high.

5. Key in 0.3D0 SPCL to switch in the Channel Output Attenuator. The waveform should have an amplitude between 0.5 and 0.7 divisions peak-to-peak.

   Hint: Pin 2 of U1B should be a TTL low, pin 1 of U1A a TTL high.

6. Connect the oscilloscope to the collector of Q7. The waveform should have an amplitude between 6 and 7 divisions peak-to-peak.

⟨√4⟩ LO Input Switch Control Check

1. Check that W55 is connected to A55J3.
2. Key in the Direct Control Special Functions listed in Table 8F-15. For each setting, connect a high-impedance, dc coupled oscilloscope to the points listed in the table. The voltages should be within the limits indicated.

Table 8F-15. *LO Input Switch Control Levels,* ⟨√4⟩ *Step 2*

Direct Control Special Function	Level (TTL) on U2 Pin		Level (Vdc) on Collector of		DS1
	6	2	Q3	Q4	
0.3D0	H	L	L	H	Off
0.3D4	L	H	H	L	On

⟨√5⟩ Select Decoder and Data Latch Check

1. Key in the Direct Control Special Functions listed in Table 8F-16. For each setting, check the pins on U3 indicated.

Table 8F-16. *Levels at U3,* ⟨√5⟩ *Step 1*

Direct Control Special Function	Level (TTL) at U3 Pin			
	14	10	9	7
0.390	*	H	H	H
0.3D0	H	*	H	H
0.3E0	H	H	*	H
0.3F0	H	H	H	*
* Low-going TTL pulses, ≈60 ms period.				

2. Key in the Direct Control Special Functions listed in Table 8F-17. For each setting, check the pins on U4 indicated.

Table 8F-17. *Levels at U4,* ⟨√5⟩ *Step 2*

Direct Control Special Function	Level (TTL) at U4 Pin				
	2	3	7	15	14
0.3D0	L	H	L	L	H
0.3DF	H	L	H	H	L

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Service Sheet 7 *(2314A to 2636A)*

ASSEMBLY

- **A54 IF Amplifier/Detector (Option Series 030)**

PRINCIPLES OF OPERATION

General

The IF Amplifier/Detector Assembly (A54) contains three stages of IF amplification, four stages of attenuation, two selectable bandpass filters, and an IF rms detector. The IF gain is selectable in 5 dB steps over a range of 0 to 60 dB.

IF Amplifiers and Attenuators

IF Amplifiers 1, 2, and 3 are nearly identical and have between 21 and 24 dB gain each. IF Amplifier 4 has 33 dB gain. Gain stability is more critical than the accuracy. Using IF Amplifier 1 as an example, the gain is 1+(R7/R6). Schottky diodes CR1 through CR4 prevent saturation of Q3, Q1, Q6, and Q8 respectively during overloads to speed up recovery time.

Switches U2, U1, and U3 select three, 20 dB voltage dividers. Switch U4 select one of four, 5 dB taps of a 20 dB voltage divider. The divider resistors are high-precision, low-drift types. Voltage follower Q7 prevents the bandpass filters from loading IF Attenuator 3.

IF Filters and RMS Detector

FL1 and FL2 are crystal-type, bandpass filters. They are switched in by Q11 and Q12 which are driven by switch U5. The filters have a passband loss of approximately 14 dB.

The amplified and filtered IF signal at the output of Q8 is detected by the IF RMS Detector (U6). U6 is a true-rms detector which produces a dc output equal to the rms level of the IF signal. The output of U6 goes to the Voltmeter.

The output of IF Amplifier 4 is also made available at J1 for testing and troubleshooting purposes.

Digital Circuits

Transistor Q14 provides a means of identifying the installation of Option Series 030. For a general discussion of instrument control, see *Instrument Bus* in Service Sheet BD5.

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TROUBLESHOOTING

General

Procedures for checking the IF Amplifier/Detector Assembly is given below. The circuits to check are marked on the schematic diagram by a hexagon with a check mark and a number inside, for example, ⟨√3⟩ . In addition, any points outside the labeled circuit area that must be checked are also identified. Fixed signals are also shown on the schematic inside a hexagon, for example, ⟨+1.9 TO +2.1 VDC⟩ . Extend the board assembly where necessary to make measurements.

CAUTION

Tighten SMC connectors to 0.6 N·m (5 in·lb). Hand tightening of connectors is insufficient. Hand-tightened connectors can work loose and cause reduced performance or malfunctions.

Equipment

Oscilloscope ..... HP 1740A
Signal Generator ..... HP 8640B

⟨√1⟩ Programmable IF Amplifier Check

1. Set the signal generator to between 454 and 456 kHz CW at −7 dBm (100 mVrms into 50Ω). Connect its RF output to A54J2 (IF IN) on the Measuring Receiver.
2. Press the blue key, then press INSTR PRESET (the AUTOMATIC OPERATION key) to preset the instrument. Connect a high-impedance, ac coupled oscilloscope to pin 5 of U2B. Set the oscilloscope gain for a display of 6 divisions peak-to-peak.
3. Key in 0.391 SPCL to set Attenuator 1 to 0 dB and Attenuators 2 and 3 to 20 dB. Key in 0.3EE SPCL to set Attenuator 4 to 15 dB. Connect the oscilloscope to pin 4 of U2B. The waveform should have the same amplitude as in step 2.

   Hint: Pin 2 of U2B should be a TTL low, pin 1 of U2A a TTL high.
4. Key in 0.390 SPCL to set Attenuators 1, 2, and 3 to 20 dB. The waveform should have an amplitude between 0.5 and 0.7 divisions peak-to-peak.

   Hint: Pin 2 of U2B should be a TTL high, pin 1 of U2A a TTL low.
5. Connect the oscilloscope to pin 5 of U1B. The waveform should have an amplitude between 6.0 and 7.2 divisions peak-to-peak.
6. Adjust the signal generator level for a display of 6 divisions peak-to-peak. Key in 0.392 SPCL to set Attenuator 2 to 0 dB and Attenuators 1 and 3 to 20 dB. Connect the oscilloscope to pin 4 of U1B. The waveform should have the same amplitude as in step 5.

   Hint: Pin 2 of U1B should be a TTL low, pin 1 of U1A a TTL high.
7. Key in 0.390 SPCL. The waveform should have an amplitude between 0.5 and 0.7 divisions peak-to-peak.

   Hint: Pin 2 of U1B should be a TTL high, pin 1 of U1A a TTL low.
8. Connect the oscilloscope to pin 9 of U3A. The waveform should have an amplitude between 6.0 and 7.2 divisions peak-to-peak.
9. Adjust the signal generator level for a display of 6 divisions peak-to-peak. Key in 0.394 SPCL to set Attenuator 3 to 0 dB and Attenuators 1 and 2 to 20 dB. Connect the oscilloscope to pin 8 of U3B. The waveform should have the same amplitude as in step 8.

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Hint: Pin 1 of U3A should be a TTL low, pin 2 of U3B a TTL high.

10. Key in 0.390 SPCL. The waveform should have an amplitude between 0.5 and 0.7 divisions peak-to-peak.

    Hint: Pin 1 of U3A should be a TTL high, pin 2 of U3B a TTL low.

11. Connect the oscilloscope to pin 2 of U4. Decrease the oscilloscope gain by a factor of 2. The waveform should have an amplitude between 4.4 and 5.0 divisions peak-to-peak.

12. Adjust the signal generator level for a display of 6 divisions peak-to-peak. Key in the Direct Control Special Functions listed in Table 8F-18. For each setting, the waveform amplitude should be within the limits indicated. If faulty, also check the logic level of the pins on U4 indicated.

Table 8F-18. *Levels on U4,* ⟨√1⟩ *Step 12*

Direct Control Special Function	Waveform Amplitude (div pk-pk)	Level (TTL) at U4 Pin			
		1	8	9	16
0.3E7	5.9 to 6.0	L	H	H	H
0.3EB	3.3 to 3.5	H	L	H	H
0.3ED	1.8 to 2.0	H	H	L	H
0.3EE	1.0 to 1.2	H	H	H	L

13. Key in 0.3E7 SPCL. Connect the oscilloscope to A71TP1. The waveform amplitude should be 5.4 to 6.0 divisions peak-to-peak.

⟨√2⟩ Channel Filters, Output Amplifier, and IF RMS Detector Check

1. Set the signal generator to between 454 and 456 kHz CW at −7 dBm (100 mVrms into 50Ω). Connect its RF output to A71J2 (IF IN) on the Measuring Receiver.

2. Press the blue key, then press INSTR PRESET (the AUTOMATIC OPERATION key) to preset the instrument. Connect a high-impedance, ac coupled oscilloscope to A54TP1.

3. Key in 0.390 SPCL to set Attenuators 1, 2, and 3 to 20 dB and switch in FL1. Key in 0.3EE SPCL to set Attenuator 4 to 15 dB. The waveform should have an amplitude between 300 and 400 mVpp.

   Hint: If the signal is faulty, perform ⟨√1⟩ *Programmable IF Amplifier Check.*

4. Set the oscilloscope gain for a display of 6 divisions peak-to-peak. Connect the oscilloscope to the base of Q10. Fine tune the signal generator to peak the display on the oscilloscope. The waveform should be between 1 and 2 divisions peak-to-peak.

   Hint: The amplitude at this point is quite sensitive to the capacitive loading of the oscilloscope. This step is mainly a check of continuity. Pin 2 of U5B should be a TTL low, pin 1 of U5A a TTL high. Q11 should be on, Q12 off.

5. Key in 0.398 SPCL to switch in FL2. Fine tune the signal generator to peak the display on the oscilloscope. The waveform should be between 1 and 2 divisions peak-to-peak.

   Hint: Pin 2 of U5B should be a TTL high, pin 1 of U5A a TTL low. Q11 should be off, Q12 on.

6. Set the oscilloscope gain for a display of 1 division peak-to-peak. Connect the oscilloscope to the A71TP2. Decrease the oscilloscope gain by a factor of 10. The waveform should have an amplitude between 3 and 8 divisions peak-to-peak.

   Hint: The change in loading on the base of Q10 makes this an inexact measurement.

6. Set the oscilloscope for a calibrated level measurement. Adjust the signal generator level for a display of 2 Vpp. Connect the oscilloscope to pin 9 of U6. Set the oscilloscope to read dc. The oscilloscope should read between 0.69 and 0.73 Vdc.

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7. Key in 49.C SPCL to measure the IF level with the IF RMS Detector. The Measuring Receiver should display between 0.69 and 0.73.

   Hint: If the reading is faulty, see Service Sheet 15.

8. Adjust the signal generator level for a Measuring Receiver display of 0.60, then tune the signal generator up and down and note the frequencies at which the level drops to 0.30. The difference between the highest and lowest frequencies should be between 3 and 7 kHz.

9. Key in 0.390 SPCL to switch in FL1. Key in 49.C SPCL. Fine tune the signal generator to peak the Measuring Receiver's display. Adjust the signal generator level for a Measuring Receiver display of 0.60, then tune the signal generator up and down and note the frequencies at which the level drops to 0.30. The difference between the highest and lowest frequencies should be between 33 and 55 kHz.

⟨√3⟩ Data Latches and Option Series 030 Indicator Check

1. Key in the Direct Control Special Functions listed in Table 8F-19. For each setting, check the pins on U8 indicated.

Table 8F-19. *Levels at U8, ⟨√3⟩ Step 1*

Direct Control Special Function	Level (TTL) at U8 Pin							
	2	3	7	6	10	11	15	14
0.390	L	H	L	H	L	H	L	H
0.39F	H	L	H	L	H	L	H	L

2. Key in the Direct Control Special Functions listed in Table 8F-20. For each setting, check the pins on U7 indicated.

Table 8F-20. *Levels at U7, ⟨√3⟩ Step 2*

Direct Control Special Function	Level (TTL) at U7 Pin			
	2	7	10	15
0.3E0	L	L	L	L
0.3EF	H	H	H	H

3. Key in 0.3F0 SPCL to read back the Option Series 030 Installed Indicator. The Measuring Receiver should display 000001.0000.

   Hint: The waveform at the collector and the emitter of Q14 should be low-going TTL pulses with a period of approximately 60 ms.

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Service Sheet 8

ASSEMBLY

- **A6 AM Demodulator (ALC Loop)**

PRINCIPLES OF OPERATION

General

AM is demodulated by rectifying the IF signal and by forcing the average of the IF signal to be a constant level using an automatic level control (ALC) loop. The rectified IF (after the IF carrier is filtered) accurately represents the carrier average plus its AM envelope. In fact, the % AM equals the level of the ac component divided by the level of the dc component times 100%. Since the average carrier level is forced to be constant, the % AM is proportional to the level of the ac component alone. The demodulation process is illustrated in Figure 8F-11.

2.5 MHz Low-Pass Filter and AM IF Buffer

The 2.5 MHz Low-Pass Filter determines the IF frequency response when using the 1.5 MHz IF or when the input signal is not down-converted. The filter has six poles and is designed for best flatness up to 2.5 MHz. At 2.5 MHz the flatness can be fine adjusted with C8 (IF FLATNESS) for minimum incidental AM. After passing through the AM IF Buffer and an FM IF Buffer (see Service Sheet 9), the filtered IF is routed to the FM Demodulator, IF Level and IF Present Detectors, and the rear-panel OUTPUT IF connector.

Current-Variable Amplifier

The Current-Variable Amplifier adjusts its gain in response to the dc output from the AM and IF Average Detector. The amplifier is then the "leveler" of the ALC loop and, as shown in Figure 8F-10, is an ac coupled, variable-gain, non-inverting operational amplifier.

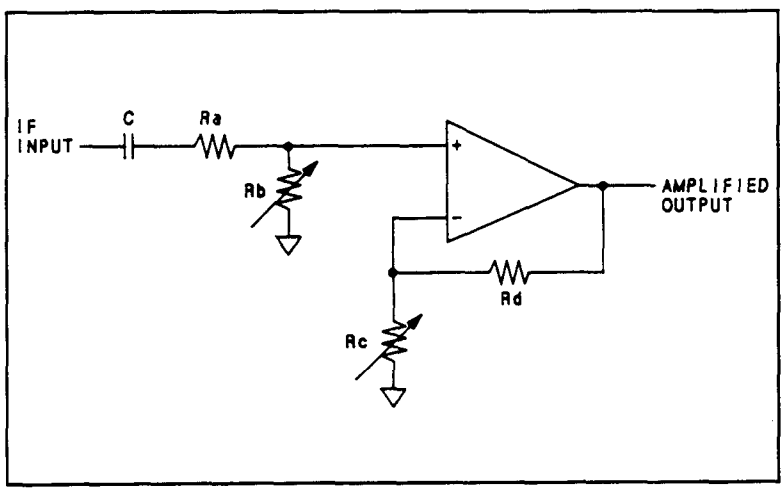


Figure 8F-10. *Simplified Diagram of the Current-Variable Amplifier*

The gain of the Current-Variable Amplifier is

$$\frac{R_b}{R_a + R_b} \times \frac{R_c + R_d}{R_c}.$$

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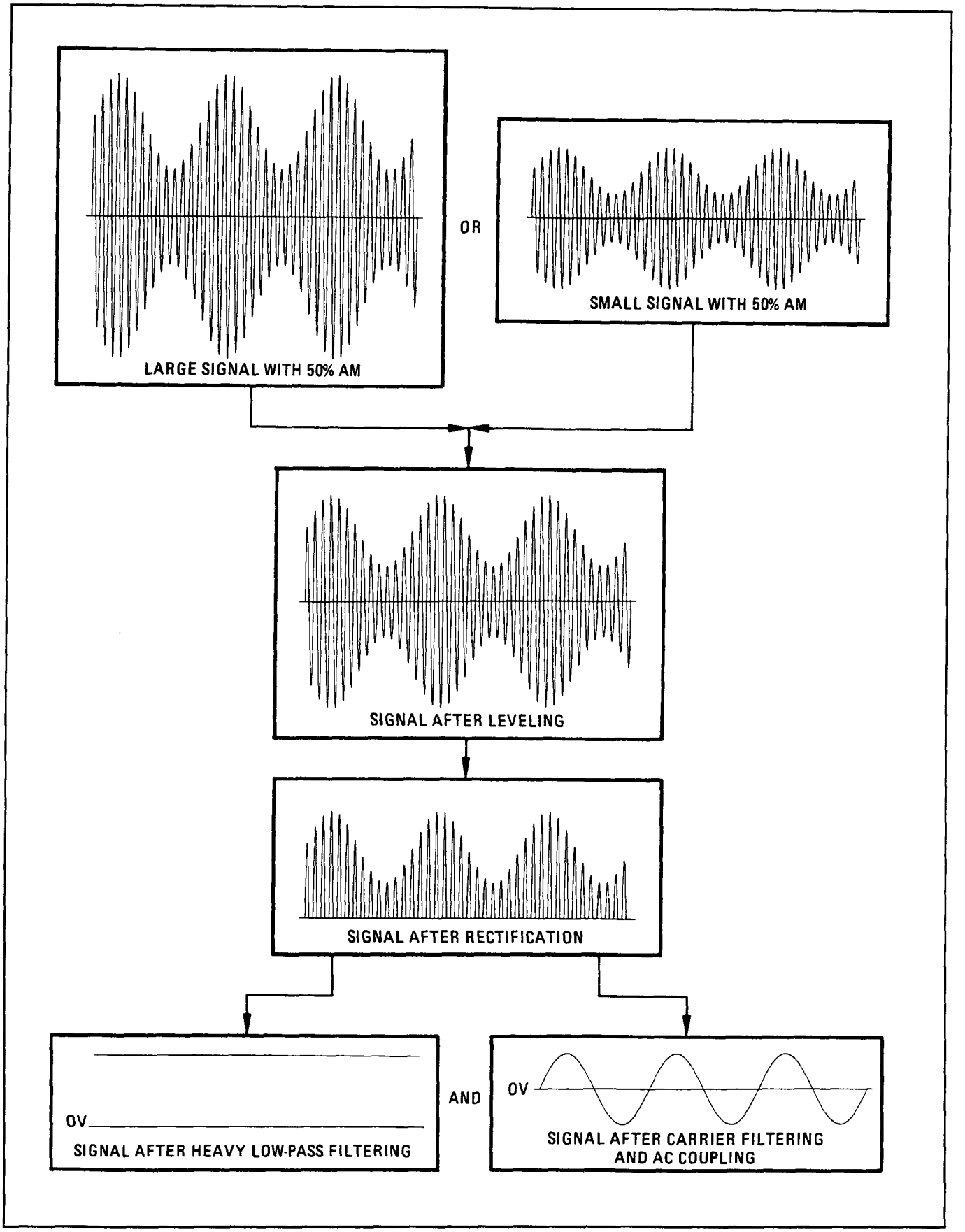


Figure 8F–11. *AM Demodulation Process*

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R_a is R10. R_b is the parallel combination of R16 and the resistance of the channel of FET Q7, which predominates. R_d is R34. R_c is the parallel combination of R37, R22, R21, and the resistance of Q6, which predominates.

The R-Setting (that is, Resistance-Setting) Circuit adjusts the input attenuation and feedback division ratio of the Current-Variable Amplifier in proportion to the output voltage of U2. The output of U2, in turn, is proportional to the amplitude error of the IF signal.

The variable resistors (FETs Q6 and Q7), which set the gain of the Current-Variable Amplifier, are controlled by two matched current sources Q2C and Q2D and two local-feedback amplifiers U4A and U4B. U4A drives n-channel FET Q6 in such a way as to hold the FET's dc drain voltage at the same potential as the reference voltage at the inverting input of U4A. The reference voltage, determined by the voltage divider R23 and R25, is approximately +50 mV. If the current from the collector of Q2D changes, the voltage at the drain of Q6 changes proportionally. The change is sensed by U4A. U4A then drives Q6 to change the channel resistance and bring the drain voltage back to +50 mV. The operation of Q2C, Q7, and U4B is similar to that of Q2D, Q6, and U4A except: (1) Q7 is a p-channel FET, (2) U4A is referenced to −50 mV, and (3) Q2C must supply the current to R13 as well as to Q7. Thus the FETs work in opposition—the resistance of Q6 decreases when Q7 increases (resulting in an increase in gain of the Current-Variable Amplifier).

The following example should clarify the action of the R-Setting Circuit: suppose that a change in IF level (in this case a decrease) causes the output of U2 to decrease. The reduction in voltage at the bases of transistors Q2C and Q2D causes an increase in their collector currents. As the drain voltage of Q6 rises, U4A responds by increasing the gate voltage of Q6 (that is, making it less negative) which reduces the resistance of the FET's channel and brings the drain voltage back to a nominal +50 mV. At the same time, as the drain voltage of Q7 rises (that is, becomes less negative), U4B responds by increasing the gate voltage of Q7 (making it more positive) which increases the resistance of the FET's channel and brings the drain voltage back to a nominal −50 mV.

The reduction in channel resistance of Q6 reduces the negative feedback around the amplifier formed by Q4 and Q5 and increases its gain. The increase in channel resistance of Q7 decreases the attenuation of the voltage divider between the output of Q8 and the base of Q5. Thus the gain of the overall Current-Variable Amplifier is increased which is the desired effect since in this example, the IF level was too low.

The Current-Variable Amplifier is designed to operate over a gain ranging from unity (0 dB) to at least 16 (24 dB). Q4 and Q5 provide the forward gain of the amplifier with well-defined performance at 1.5 MHz. Two RC networks, R14 and C16 and R28 and C23, aid in canceling distortion created in the FET channels by the IF frequency. The networks inject a small amount of IF signal into the gates of the FETs. C17 and C21 set the response time of the local feedback amplifiers U4B and U4A.

Q21 and Q20 form a unity-gain, IF buffer amplifier which drives the AM and IF Average Detector. Q31 improves the symmetry of the overdrive characteristics of the buffer amplifier. This is necessary since the ALC loop initially receives signals when its ALC gain is maximum (the no-signal condition).

AM and IF Average Detector

The AM and IF Average Detector rectifies the IF carrier. Q13 to Q16, CR9 and CR10, and associated components form a precision, active, half-wave rectifier. A simplified diagram of the rectifier is shown in Figure 8F-12. The circuit is essentially an inverting operational amplifier with two parallel feedback paths which each conduct current in a different direction as determined by CR9 and CR10. The path through CR9 can produce only negative voltages at the output to the Level Amplifier and Carrier Filter. This feedback path, which contains the network R73, R74, C43, and L8, acts as a constant resistance (equal to R73) between CR9 and the amplifier's inverting (−) input, and low-pass filters the IF going to the AM Output Buffer.

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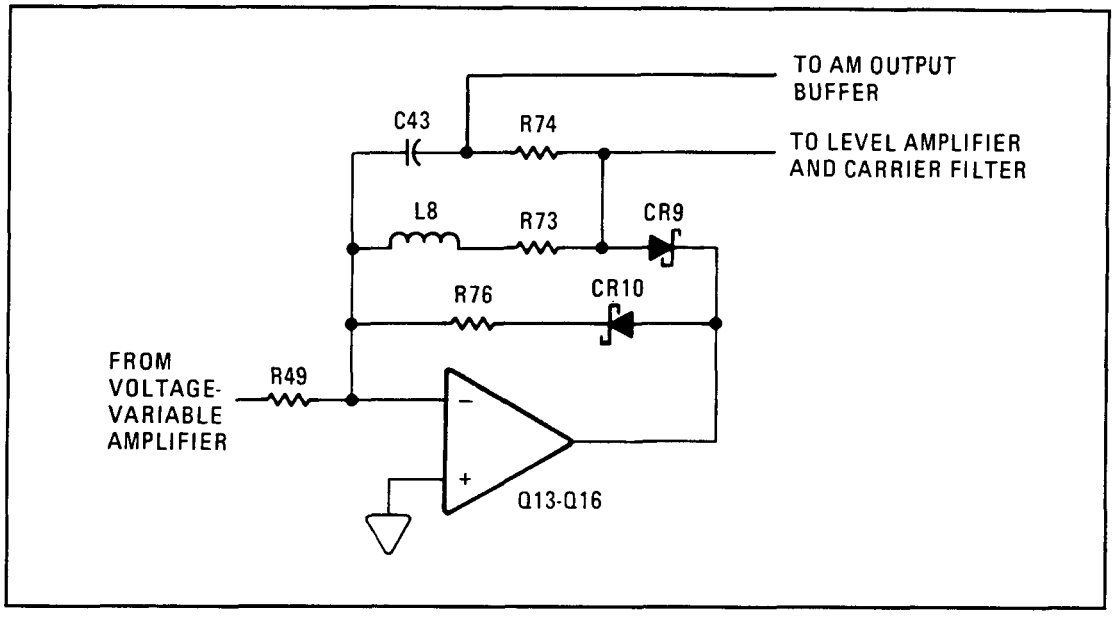


Figure 8F–12. *Simplified Diagram of the AM and Average IF Level Detector*

The emitter of Q13 is the amplifier's common-base inverting input. The base of Q13 is the ac grounded, non-inverting input of the amplifier. Q13 is followed by a cascode stage (a common-emitter transistor driving a common-base transistor) Q15 and Q14. R58 and C40 frequency compensate the amplifier. Q16 is a +13.8V regulator and RF decoupling circuit. CR6 and CR7 protect the amplifier in the event of unusual conditions at the input.

AM Output Buffer

Q17, Q18, and Q19 form a unity-gain buffer amplifier which interfaces the demodulated AM with the rear-panel AM OUTPUT connector and the audio circuits. R87 and C50 further filter the IF carrier. R88 and C51 form the first two elements of a complex 260 kHz Low-Pass Filter (see Service Sheet 12).

Level Amplifier and Carrier Filter

U3 and associated components form an inverting amplifier and IF carrier and AM ripple filter. Note that the non-inverting (+) input of U3 connects through R75 to the inverting input (namely, the emitter of Q13) of the AM and Level Detector which is its "virtual" ground. Thus the two amplifiers have a common signal-ground reference.

BW Control and Level Comparison Amplifier

The dc output of U3 represents the IF carrier's average level. This output is compared against a stable reference voltage. Differences between the two voltages are amplified by U1 to alter the drive voltage (via U2) to the bases of Q2C and Q2D of the R-Setting Circuit. U1 adds more filtering to the detected IF and determines the response time of the ALC loop to variations in IF level (that is, it determines the ALC bandwidth). U5B permits selection of the 0.1 dB bandwidth of either 20 Hz when open or 200 Hz when closed. When U5B is closed, the time constant of the integrator U1 is the product of R55 and C31. When U5B is open, the time constant is the product of C31 and R51+R54+R55; C36 adds even more filtering.

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ALC Reference

The very stable voltage reference for the ALC loop is supplied by the voltage-reference diode VR3. VR3 is biased on by a regulated current source formed by Q1, VR4, and associated components. The reference output is divided by the combined value of R69, R65, and R66. Fine adjustment of the ALC Reference is via R65 (ALC REF).

Resistor Drive Amplifier

U2 amplifies (with a gain of 1.1) and inverts the output of U1. Switch U5A is normally closed, and U5C is normally open. U2 then normally drives the bases of Q2C and Q2D of the R-Setting Circuit. The output of U2 works against the +15V supply through R26, R31, R32, and Q2A, which is wired as a diode to temperature compensate the base-emitter voltages of Q2C and Q2D.

Q2B produces a voltage at its collector that is proportional to the control currents of Q2C and Q2D. This voltage is monitored by the Voltmeter to check that the ALC loop is operating within its proper range. The automatic leveling can be defeated, if desired, by opening U5A and closing U5C (user Special Function 6.2). The bases of Q2C and Q2D are then biased by voltage divider R26, Q2A, and R27.

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TROUBLESHOOTING

General

Procedures for checking the AM Demodulator Assembly are given below. The circuits to check are marked on the schematic diagram by a hexagon with a check mark and a number inside, for example, ⟨✓3⟩. In addition, any points outside the labeled circuit area that must be checked are also identified. Fixed signals are also shown on the schematic inside a hexagon, for example, ⟨+1.9 TO +2.1 VDC⟩. Extend the board assembly where necessary to make measurements.

CAUTION

Tighten SMC connectors to 0.6 N·m (5 in·lb). Hand tightening of connectors is insufficient. Hand-tightened connectors can work loose and cause reduced performance or malfunctions.

Equipment

Oscilloscope	HP 1740A
Signal Generator	HP 8640B
Voltmeter	HP 3455A

⟨✓1⟩ 2.5 MHz Low-Pass Filter and AM IF Buffer Amplifiers Check

1. Set the signal generator to 1.5 MHz CW at −7 dBm. Connect its RF output to A6J2 (IF IN).
2. Connect an ac coupled oscilloscope to A6J3 (IF OUT). (A6J3 is shown on Service Sheet 9.) Switch the input impedance of the oscilloscope to 50Ω or terminate the input in 50Ω using a tee. The waveform of the 1.5 MHz signal should be sinusoidal with an amplitude of 300 to 360 mVpp.

   Hint: If the signal is faulty, trace the signal from A6J1 through Q9. (See Service Sheet 9 for the schematic.)
3. Connect the oscilloscope to A6J4 (IF OUT). (A6J4 is shown on Service Sheet 9.) The waveform should be sinusoidal with an amplitude of 50 to 60 mVpp.

   Hint: If the signal is faulty, check Q10. (See Service Sheet 9 for the schematic.)
4. Connect a high-impedance, ac coupled oscilloscope to the emitter of Q8. The oscilloscope should have a low-capacitance 10:1 divider probe. The waveform should be sinusoidal with an amplitude of 180 to 200 mVpp.
5. If necessary, fine adjust the signal generator level for an oscilloscope display of 200 mVpp.
6. Set the signal generator to 3 MHz. The waveform should have an amplitude of 120 to 160 mVpp.

   Hint: The 3 dB frequency of the 2.5 MHz Low-Pass Filter is approximately 3 MHz.

⟨✓2⟩ Current-Variable Amplifier Check

1. Set the signal generator to 1.5 MHz CW at −7 dBm. Connect its RF output to A6J2 (IF IN).
2. Connect a high-impedance, ac coupled oscilloscope to the emitter of Q8. The oscilloscope should have a low-capacitance 10:1 divider probe. Adjust the signal generator level for a waveform of 200 mVpp.
3. Key in 0.0D0 SPCL to switch the ALC off.
4. Measure pin 11 of U5C with a dc voltmeter. The voltage should be between −15 and −13 Vdc.

   Hint: U5C should be on. U5A should be off. Pin 9 of U5C should be a TTL low.

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5. Measure pin 7 (the collector) of Q2B with a dc voltmeter. The voltage should be between +1.66 and +1.69 Vdc.
6. Connect the oscilloscope (with divider probe) to the collector of Q4. The waveform of the 1.5 MHz signal should be sinusoidal with an amplitude between 400 and 600 mVpp.

   Hint: If this step fails, check the R-Setting Circuits as follows:

   a. Measure the drains of Q6 and Q7 with a dc voltmeter. The voltages should be within the limits shown in the schematic.

      Hint: The voltage at pins 2 and 6 of U4 should be within the limits shown in the schematic. The polarity at the output of U4A (pin 1) should conform to the polarity of its differential inputs. (For example, if pin 3 is more positive than pin 2, pin 1 should be positive and may be as high as +15V.) Similarly for U4B.

   b. Connect the oscilloscope (with divider probe) to the base of Q5 and observe the ac waveform on the oscilloscope. Momentarily ground pin 8 (the collector) of Q2C and observe the waveform. Then momentarily place a 1 kΩ resistor in parallel with R8 and observe the waveform. The amplitude of the waveform should be as shown in Table 8F-21.

Table 8F-21. *Amplitude Limits on the base of Q5,* ⟨√2⟩ *Step 6b*

Condition	Waveform Amplitude Limits (mVpp)	
	Minimum	Maximum
Unmodified circuit	20	50
Pin 8 of Q2C grounded	10	30
1 kΩ resistor in parallel with R8	150	200

   c. Connect the oscilloscope to the collector of Q4 and observe the ac waveform on the oscilloscope. Momentarily ground pin 14 (the collector) of Q2D and observe the ac waveform on the oscilloscope. Momentarily place a 1 kΩ resistor in parallel with R20 and observe the waveform. The amplitude of the waveform should be as shown in Table 8F-22.

Table 8F-22. *Amplitude Limits on the collector of Q4,* ⟨√2⟩ *Step 6c*

Condition	Waveform Amplitude Limits (mVpp)	
	Minimum	Maximum
Unmodified circuit	200	400
Pin 14 of Q2D grounded	30	70
1 kΩ resistor in parallel with R20	2000	3000

   Hint: Check the bias of Q4 and Q5.

7. If necessary, fine adjust the signal generator level for a waveform of 500 mVpp.
8. Connect the oscilloscope to the collector of Q20. The waveform should be sinusoidal with an amplitude between 450 and 550 mVpp.

⟨√3⟩ AM and IF Average Detector and Level Amplifier and Carrier Filter Check

1. Set the signal generator to 1.5 MHz CW at 0 dBm. Connect its RF input to A6J2 (IF IN).
2. Key in 0.0D0 SPCL to switch the ALC off.
3. Connect a high-impedance, ac coupled oscilloscope to the collector of Q20. The oscilloscope should have a low-capacitance 10:1 divider probe. Adjust the signal generator level for a waveform of 1 Vpp.

   Hint: If the level is unadjustable, see ⟨√2⟩ *Current-Variable Amplifier Check.*

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4. Connect the oscilloscope to the anode of CR9. The waveform should be a negative, half-wave rectified sine wave with an amplitude of 2.3 to 2.7 Vpp. Some distortion of the waveform and droop of the no-conduction voltage is normal.
5. Connect the oscilloscope to the cathode of CR10. The waveform should be a positive, half-wave rectified sine wave with an amplitude of 2.3 to 2.7 Vpp. Some distortion of the waveform is normal.
6. Measure the dc voltage between the emitter of Q13 and the gate of Q17. Multiply that voltage by 2.63. Now measure the dc voltage at A6TP2 (DEMOD CARR LVL) which should be within ±7% of the calculated voltage (ignoring the polarity).

⟨√4⟩ ALC Reference, BW Control and Level Comparison Amplifier, Inverting Amplifier, and Resistor Drive Amplifier Check

NOTE

This test assumes that the ⟨√3⟩ AM and Level Detector and Level Amplifier and Carrier Filter Check *gives positive results.*

1. Measure pin 3 of U1 with a dc voltmeter. The voltage should be between 2.095 and 2.105 Vdc. Record the voltage for future reference.

   Hint: If the voltage is only slightly out of limits and if the AM Demodulator is only slightly in error, perform *Adjustment 8—ALC Reference.*
2. Set the signal generator for 1.5 MHz CW at 0 dBm. Connect its RF output to A6J2 (IF IN).
3. Key in 0.0D2 SPCL to switch the ALC off and set the response time to fast (200 Hz bandwidth).
4. Connect a high-impedance, dc coupled oscilloscope to pin 6 of U1.
5. Connect the dc voltmeter to A6TP2 (DEMOD CARR LVL).
6. Slowly vary the signal generator level such that the voltage at A6TP2 varies between +2.0 and +2.2 Vdc. When the voltage at A6TP2 approaches +2.2 Vdc, the voltage at pin 6 of U1 should rapidly drift to a level that is between −15 and −12 Vdc. When the voltage at A6TP2 approaches +2.0 Vdc, the voltage at pin 6 of U1 should rapidly drift to a level that is between +9 and +11 Vdc.
7. Adjust the signal generator level until the voltage at pin 6 of U1 holds steady at 0 Vdc. The voltage at A6TP2 should be within ±20 mV of the voltage measured in step 1.
8. Key in 0.0D0 SPCL to set the ALC response time to slow. Vary the signal generator level as in step 6. The drift rate should be about ten times slower. It should take about 8 seconds for the level at A6TP2 to drift from the negative to the positive extreme when the signal level is rapidly switched from −3 to −1 Vdc at pin 6 of U1.

   Hint: U5B should be off. Pin 8 of U5B should be a TTL high.
9. Set the oscilloscope to view two channels. Connect the second channel of the oscilloscope (dc coupled with a divider probe) to pin 6 of U2. Set its input to invert the signal. Set both channels to the same range. Check that the 0V reference is the same for both channels. Repeat step 6 and verify that the two channels track. The voltage at pin 6 of U2 should be larger in magnitude by about 10% as the signals drift.
10. Key in 0.0D1 SPCL to close the ALC loop with slow ALC response time. Set the signal generator level to 0 dBm.
11. Measure the dc voltage at pin 3 of U5A. The voltage should be greater than +12 Vdc.

    Hint: U5A should be on with a TTL low at pin 1. U5C should be off.
12. Measure the dc voltage at A6TP2 with a dc voltmeter. The voltage should equal the voltage measured in step 1 within ±20 mV.

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Hint: Checks ⟨√1⟩ to ⟨√3⟩ above and this check up to step 9 verify all the circuits which demodulate the AM without the ALC loop being closed. Step 10 above closes the loop. If the loop is working properly, the voltage at A6TP2 should equal the ALC Reference present on pin 3 of U1. The 1.5 MHz signal at the collector of Q4 should be between 900 and 1100 mVpp.

13. Set the signal generator level to −17 dBm. Measure A6TP2 with a dc voltmeter. The voltage should equal the voltage of step 1 within ±20 mV.

    Hint: This verifies the dynamic range of the ALC loop. If the range is inadequate, the fault probably is with the R-Setting Circuit.

⟨√5⟩ AM Output Buffer Check

NOTE

This check assumes that all checks above give positive results (in other words, the AM Demodulator is known to work).

1. Set the signal generator to 1.5 MHz at 0 dBm. Set up 50% AM at a 1 kHz rate. Connect its RF output to A6J2 (IF IN).
2. Press the blue key, then press INSTR PRESET (the AUTOMATIC OPERATION key) to preset the instrument.
3. Connect a high-impedance, ac coupled oscilloscope to the gate of Q17. Note the amplitude of the half-wave rectified signal.
4. Connect the oscilloscope to the collector of Q19. The amplitude should be the same within ±5%.

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Service Sheet 9

ASSEMBLY

- **A6 AM Demodulator (Control Circuits)**

PRINCIPLES OF OPERATION

General

The filtered IF signal is buffered and detected by two peak detectors. The output of the IF Level Detector is measured by the Voltmeter for use in determining the setting of the input attenuation and for Special Function 36, Peak Tuned RF Level. The output of the IF Present Detector is used in the automatic tuning mode to sense the presence of an IF signal as the LO is swept through its ranges. Its output stops the LO sweep, bypassing the Controller, but can also be read by the Controller as needed.

FM IF Buffer

Q9 is an emitter-follower amplifier which drives the input to the FM Demodulator and the IF Detector Amplifier. Q10 is an emitter-follower amplifier which drives the rear-panel IF OUTPUT connector. Q10 receives its input from the output of Q9 which is divided down by R92 and R93.

IF Detector Buffer

Q11 and Q12 and associated components form an active 50 kHz high-pass filter with approximately 16 dB of passband gain. It suppresses a phantom signal that can appear in the IF as the result of the LO sweep even when no input signal is present.

IF Level Detector

CR15 detects the positive peaks of the IF signal. The detected peak is stored on C65. Q29 is a momentary switch to quickly discharge C65 upon request from the Controller. C70 charges C65 to a slightly negative value after being discharged by Q29. U6 and associated components form a unity-gain amplifier. A dc offset is generated by CR16 that thermally compensates CR15. The output is attenuated by R117 and R118 to make it compatible with the Voltmeter.

IF Present Detector

CR14 detects the negative peaks of the IF signal. The detected peak is stored on C63. The value of C63 is small enough to allow rapid charging. U7 compares the output of the detector with a reference at its inverting (−) input. The reference is established by the +15V and −15V supplies, R104, R105, R109, and CR13 which thermally compensates CR14. When an IF signal is sensed, the output of U7 goes to a TTL low. R112 provides hysteresis.

IF Present Latch

U10C and U10D form a set-reset flip-flop. When the IF Present Detector senses an IF signal, the flip-flop is set; that is, the output of U10C goes low and U10D goes high. This condition remains until the Controller resets the flip-flop by momentarily causing a low on pin 9 of U8. Readback of the IF Present Latch is via Q30. Q30 is enabled when the Controller, via U9, places a low on the emitter. CR17 prevents Q30 from becoming an active transistor in the inverted mode (that is, the roles of collector and emitter are reversed) when the emitter is high and the collector is low. (For a discussion of the readback operation, see *Direct Control Special Functions,* paragraph 8-7.)

Select Decoder and Data Latch

See the general discussion under *Instrument Bus* in Service Sheet BD5.

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TROUBLESHOOTING

General

Procedures for checking the AM Demodulator Assembly are given below. The circuits to check are marked on the schematic diagram by a hexagon with a check mark and a number inside, for example, ⟨√3⟩. In addition, any points outside the labeled circuit area that must be checked are also identified. Fixed signals also are shown on the schematic inside a hexagon, for example, ⟨+1.9 TO +2.1 VDC⟩. Extend the board assembly and its input and output cables where necessary to make measurements.

CAUTION

Tighten SMC connectors to 0.6 N·m (5 in·lb). Hand tightening of connectors is insufficient. Hand-tightened connectors can work loose and cause reduced performance or malfunctions.

Equipment

Oscilloscope	HP 1740A
Signal Generator	HP 8640B
Voltmeter	HP 3455A

⟨√1⟩ FM IF Buffer Check

1. See *2.5 MHz Low-Pass Filter and IF Buffer Amplifiers Check* on Service Sheet 8.

⟨√2⟩ IF Detectors and IF Present Latch Check

1. Set the signal generator to 1.5 MHz CW at 0 dBm. Connect its RF output to A6J2 (IF IN). (A6J2 is shown on Service Sheet 8.)
2. Press the blue key, then press INSTR PRESET (the AUTOMATIC OPERATION key) to preset the instrument. Press RF POWER to halt automatic tuning.
3. Connect an ac coupled, high-impedance oscilloscope to the emitter of Q9. The oscilloscope should have a low-capacitance 10:1 divider probe. Adjust the signal generator level for a waveform of 1 Vpp.

   Hint: If the level is unadjustable, see the *2.5 MHz Low-Pass Filter and IF Buffer Amplifiers Check* on Service Sheet 8.
4. Connect the oscilloscope to the collector of Q11. The 1.5 MHz waveform should be sinusoidal with an amplitude between 6.0 and 7.2 Vpp. A small amount of distortion is normal.
5. If necessary, adjust the signal generator level for a waveform of 6 Vpp. Measure the voltage at pin 2 of A25XA6 with a dc voltmeter. The voltage should be between +1.1 and +1.3 Vdc.
6. Connect the voltmeter to pin 7 of U7. The voltmeter should read a TTL low.
7. Slowly decrease the signal generator level until the voltmeter reading jumps to a TTL high. The amplitude of the waveform should be between 800 and 1000 mVpp when the voltmeter level switches.
8. Slowly increase the signal generator level until the voltmeter reading jumps to a TTL low. The amplitude of the waveform should be between 1000 and 1200 mVpp.
9. Key in 0.0F0 SPCL and 0.0E0 SPCL to disable resetting the IF Present Latch to enable readback of it. The display should read 000001.0000.
10. Reduce the signal generator level until the voltmeter reads a TTL high. The display should read 000000.0000.

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11. Key in 0.0F1 SPCL and 0.0E0 SPCL to reset the IF Present Latch and enable readback of it. The display should read 000000.0000.
12. Increase the signal generator level until the voltmeter reads a TTL high. The display should remain 000001.0000.
13. Reduce the signal generator level until the voltmeter reads a TTL high. The display should remain 000001.0000.
14. Connect the oscilloscope to the collector of Q29. Adjust the signal generator level for approximately +2 Vdc on the oscilloscope display.
15. Key in 0.0F0 to momentarily activate Q29. The voltage on the oscilloscope should momentarily discharge to 0V then recharge to its previous level within a few milliseconds.

⟨√3⟩ Select Decoder and Date Latch Check

1. Key in the Direct Control Special Functions indicated in Table 8F-23. For each setting, check the pins indicated on U9 with a high-impedance, dc coupled oscilloscope.

Table 8F-23. *Levels at U9, ⟨√3⟩ Step 1*

Direct Control Special Function	Level (TTL) at U9 Pin		
	7	9	10
0.0D0	H	H	*
0.0E0	H	*	H
0.0F0	*	H	H
*Low-going TTL pulses, ≈60 ms period.			

2. Key in the Direct Control Special Functions indicated in Table 8F-24. For each setting, check the pins indicated on U8.

Table 8F-24. *Levels at U8, ⟨√3⟩ Step 2*

Direct Control Special Function	Level (TTL) at U8 Pin	
	1	14
0.0D0	H	H
0.0D3	L	L

3. Key in the Direct Control Special Functions indicated in Table 8F-25. For each setting, check the pins indicated on U8.

Table 8F-25. *Levels at U8, ⟨√3⟩ Step 3*

Direct Control Special Function	Level (TTL) at U8 Pin	
	8	9
0.0F0	H	L
0.0F3	L	H

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Service Sheet 10

ASSEMBLY

- **A4 FM Demodulator (Limiters)**

PRINCIPLES OF OPERATION

General

The IF signal to be FM demodulated is first passed through three amplifier/limiter stages to remove amplitude fluctuations. A buffer amplifier is also provided to drive the Counter and to isolate the demodulator from the digital noise on the line to the Counter.

Limiters

The three limiter stages are nearly identical, non-saturating differential amplifiers. Stage 2 is discussed here in detail. The low-level differential gain is about 22 dB and is stabilized by the negative-feedback resistors R14 and R22. The feedback resistors also extend the small-signal bandwidth so that the small-signal delay is equal to the large-signal delay. C10 compensates for phase changes with level. The high-signal, output level is determined by the current from current source Q19E being switched back and forth between differential transistors Q19A and Q19B. This switching develops an output voltage across load resistors R19 and R21. Emitter followers Q19D and Q19C drive the next stage. Stage 3 drives the FM discriminator with its differential outputs and the Counter IF Buffer with one of its emitters.

Counter IF Buffer

Transistors Q2 and Q1 amplify and limit the IF signal to TTL levels. DC feedback through R40 and R39 sets the operating point. This amplifier also performs an isolating function.

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TROUBLESHOOTING

General

Procedures for checking the FM Demodulator Assembly are given below. The circuits to check are marked on the schematic diagram by a hexagon with a check mark and a number inside, for example, ⟨√3⟩ . In addition, any points outside the labeled circuit area that must be checked are also identified. Fixed signals are also shown on the schematic inside a hexagon, for example, ⟨+1.9 TO +2.1 VDC⟩ . Extend the board assembly and its input and output cables where necessary to make measurements.

CAUTION

Tighten SMC connectors to 0.6 N·m (5 in·lb). Hand tightening of connectors is insufficient. Hand-tightened connectors can work loose and cause reduced performance or malfunctions.

Equipment

Oscilloscope	HP 1740A
Signal Generator	HP 8640B
Voltmeter	HP 3455A

⟨√1⟩ IF Limiters and Counter IF Buffer Check

1. Set the signal generator to 1.5 MHz CW at −60 dBm. Connect its RF output to A4J1 (IF IN) with a 50Ω termination in parallel with it.
2. Connect oscilloscope to A4TP2 (DISC IN). The oscilloscope input should have a low-capacitance 10:1 divider probe. The waveform of the 1.5 MHz signal should be sinusoidal with an amplitude of 0.17 to 0.34 Vpp and an offset of +9.6 to +10.0 Vdc.

   Hint: Each limiter has a gain of 22 dB.
3. Increase the signal generator level to 0 dBm. The waveform should be a square wave with an amplitude of 0.9 to 1.1 Vpp and an offset of +9.6 to +10.0 Vdc.
4. Check A4J2 (IF OUT). The waveform should be slightly asymmetrical "square wave" with an amplitude of 3 to 4 Vpp.

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Service Sheet 11

ASSEMBLY

- **A4 FM Demodulator (Discriminator)**

PRINCIPLES OF OPERATION

General

The IF signal is FM demodulated by a "charge-count" discriminator. Operation is similar to a "pulse-count" discriminator except that pulses of constant charge are formed directly and averaged instead of voltage or current pulses of constant amplitude and width (that is, duration). For each cycle of IF signal, a large, amplitude-stable square wave charges and discharges a small capacitor. Steering diodes on the other side of the capacitor direct the negative discharge pulses to the inverting input of an operational amplifier which also partially smooths the charge pulses. In actual operation, two capacitors are charged and discharged on opposite phases of the IF signal. This doubles the sensitivity of the discriminator and doubles the frequency of the charge pulses.

The discriminator output is lightly filtered and is utilized in three places. A dc coupled signal goes to the rear-panel FM OUTPUT connector. Another dc coupled signal is fed back to the LO tune input to form an automatic frequency control loop when in the track-tune mode. The main, ac coupled signal goes to the FM Output Amplifier and is then processed by the audio circuits. A Squelch Switch at the input to the FM Output Amplifier cuts off the FM output when the IF signal level is too low for good noise performance.

FM Discriminator (Simplified)

Figure 8F-13 shows a simplified schematic of the FM discriminator. The differential IF inputs from the IF Limiters alternately cause the collectors of Q12 and Q13 to clamp to one diode drop above a +6V reference and one diode drop below a −10V reference. The two collectors move out of phase with each other. Thus the left end of C27 swings 16 Vpp plus two diode drops. Diodes CR10 and CR12 clamp the right end of C27 to within one diode drop of −10V. Thus C27 is alternately charged to 16V and discharged to 0V. A fixed amount of charge flows through CR12 from the inverting (−) input of the operational amplifier each time the collector of Q12 drops from +6V to −10V, namely, once per cycle of the IF signal. The value of the charge is CV, where C is the value of C27 and V=16V. The average current flowing through CR12 is CVf, where f is the IF signal frequency. The operational amplifier forces this current to flow through R69 and R71, thus producing a voltage which is directly proportional to capacitance, voltage, resistance, and frequency. Since the first three quantities are held constant, the discriminator output is a linear function of frequency.

Exactly the same behavior happens in connection with C28, but 180° out of phase, with the result that the discriminator output voltage is doubled and the ripple frequency is doubled (twice the IF). C31 and C33 smooth the ripple as do R85, R87, and C42. The high-frequency response of the entire FM system is adjusted with R85.

Upper Clamp, Lower Clamp Regulator, and Upper Clamp Buffer

Refer now to the schematic diagram of Service Sheet 11. The Upper and Lower Clamp voltages (nominally +6V and −10V) must be very stable and quiet since they directly affect FM demodulator sensitivity and noise. The basic reference is a temperature-stable reference diode VR1. The reference is fed from current source Q8, which itself is temperature stable because its base-emitter junction and its reference (LED DS1) have similar thermal behavior. The Upper Clamp voltage is taken directly from VR1 through emitter-followers Q9 and Q10 whose thermal variations cancel. The Lower Clamp voltage is referenced to VR1 with the Lower Clamp Regulator composed of comparison transistors Q4 and Q3 and pass transistor Q5, and is adjustable with R50. This adjustment changes the sensitivity of the demodulator and is used to calibrate the FM system. C24 and C25 reduce noise.

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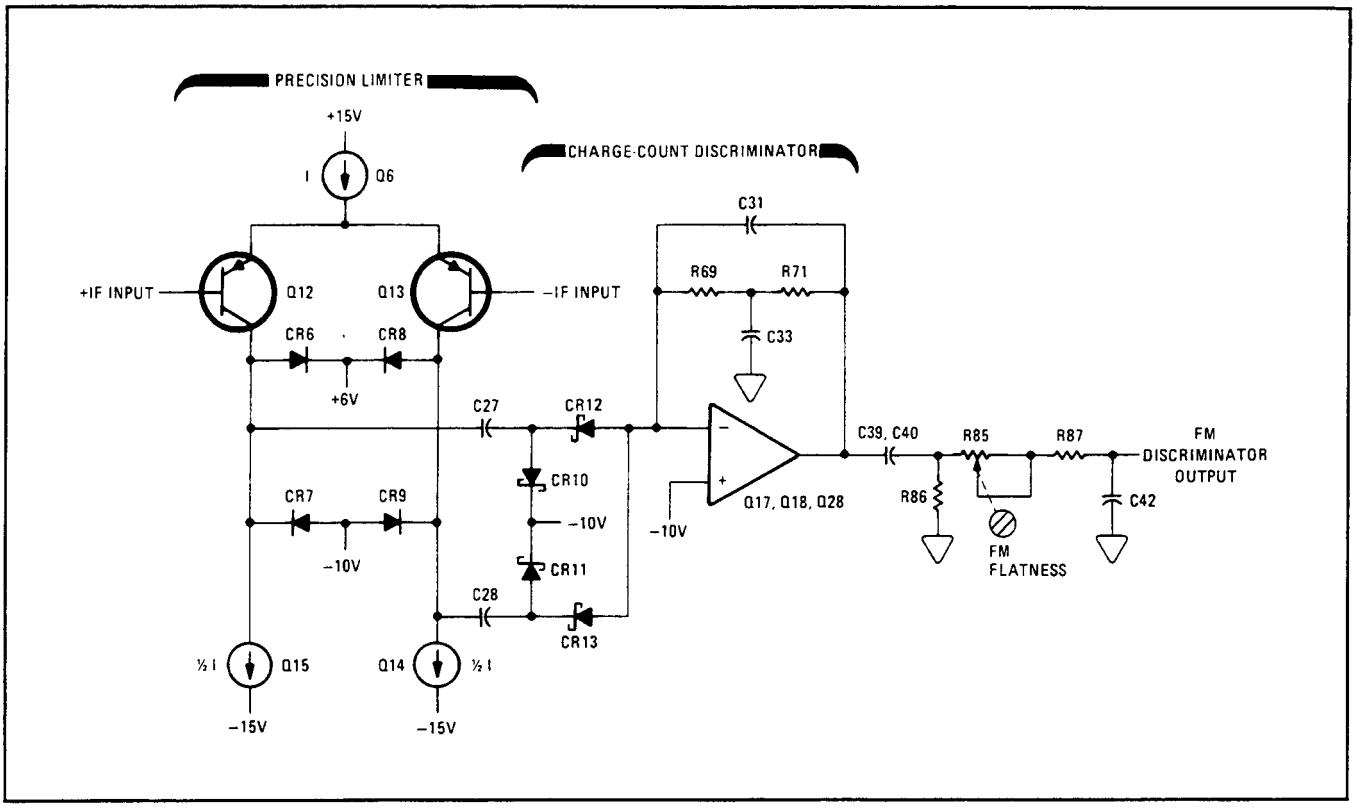


Figure 8F–13. *Simplified Schematic Diagram of FM Discriminator*

Precision Limiter and Charge-Count Discriminator

Figure 8F-13 shows the three temperature-compensated current sources, Q6, Q14, and Q15. On the schematic diagram, Service Sheet 11, these current sources consist of transistors Q6, Q14, Q15, and voltage references (LEDs) DS1 and DS2. Q7 and C26 filter the −15V supply. RL networks R64 and L1 and R65 and L2 speed up shut-off of charge steering diodes CR10 and CR11 by means of a controlled amount of overshoot to improve linearity. R66 and C29 improve linearity by introducing a small frequency-dependent voltage in series with charge steering diodes CR10 and CR11.

The discriminator amplifier, a discrete operational amplifier, consists of amplifier transistors Q18, Q17, and Q28 and current-source transistors Q29, Q34, and Q33. Q34 and Q33 comprise a conventional two-transistor current source in which negative feedback causes the voltage drop across the emitter resistor (R81) of Q33 to equal the base-emitter voltage of Q34. The voltage that is thus established at the base of Q33 (two junction drops above the −15V supply) is also used as the reference for three other current source transistors (Q29, Q27, and Q26). R75 is added to reduce the sensitivity of the latter three current sources to power supply ripple.

R69 and R71 are feedback resistors mentioned above and, in combination with C31 and C33, form a bridged-T network in the feedback path of the discriminator operational amplifier, producing the complex pole pair of a three-pole, low-pass filter. The third pole is produced later in the signal chain (see Service Sheet 13). The bridged-T network also produces a real-axis zero which is cancelled by the pole introduced by R85, R87, and C42. C35 and RC network R68 and C32 frequency-compensate the amplifier.

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FM Output Amplifier

The FM Output Amplifier is an FET input, non-inverting amplifier with a voltage gain of 3.3 that is determined by feedback resistors R95 and R93. C43 and C44 are compensation elements. R97 and R99 establish the output impedance of the amplifier in order to properly drive the 260 kHz Low-Pass Filter which is at the amplifier's output (see Service Sheet 12). C45 is the first element of that filter.

Squelch Circuits

The squelch circuits short the signal path to ground by means of FET switch Q21 when the IF signal is too weak for proper operation of the instrument. Q21 is controlled by the Squelch Detector at the output of the IF Limiters and by the Controller through Squelch Switch Drive transistors Q32 and Q31. Q21 is a low-impedance short when its gate-to-source voltage is zero (Q32 and Q31 off).

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TROUBLESHOOTING

General

Procedures for checking the FM Demodulator Assembly are given below. The circuits to check are marked on the schematic diagram by a hexagon with a check mark and a number inside, for example, ⟨√3⟩. In addition, any points outside the labeled circuit area that must be checked are also identified. Fixed signals are also shown on the schematic inside a hexagon, for example, ⟨+1.9 TO +2.1 VDC⟩. Extend the board assembly and its input and output cables where necessary to make measurements.

CAUTION

Tighten SMC connectors to 0.6 N·m (5 in·lb). Hand tightening of connectors is insufficient. Hand-tightened connectors can work loose and cause reduced performance or malfunctions.

Equipment

Oscilloscope ..... HP 1740A
Signal Generator ..... HP 8640B
Voltmeter ..... HP 3455A

⟨√1⟩ Squelch Detector Check

NOTE

This check assumes that the IF Limiters and Counter IF Buffer Check *on Service Sheet 10 gives positive results.*

1. Set the signal generator to 1.5 MHz CW at −51 dBm. Connect its RF output to A4J1 (IF IN) with a 50Ω termination in parallel with it. (A4J1 is shown on Service Sheet 10.)
2. Check the gate (can) of Q21 with a dc voltmeter. The voltage should be −0.1 to +0.1 Vdc (that is, squelched).
3. Key in 0.152 SPCL to unsquelch. The voltage should not change. (It is still squelched by the lack of adequate signal.)
4. Increase the signal generator's level to −45 dBm. The gate of Q21 should be −15 to −14 Vdc (that is, unsquelched).
5. Key in 0.150 SPCL to squelch. The gate of Q21 should be −0.1 to +0.1 Vdc.

⟨√2⟩ Precision Limiter Check

NOTE

This check assumes that the IF Limiters and Counter IF Buffer Check *on Service Sheet 10 gives positive results.*

1. Set the signal generator to 1.5 MHz CW at 0 dBm. Connect its RF output to A4J1 (IF IN) with a 50Ω termination in parallel with it. (A4J1 is shown on Service Sheet 10.)
2. Check the collectors (cans) of Q12, Q13, Q14, and Q15 with an oscilloscope. The oscilloscope input should have a low-capacitance 10:1 divider probe. The 1.5 MHz waveform should be a trapezoidal wave with an amplitude of 15 to 19 Vpp.

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⟨√3⟩ Charge-Count Discriminator Check

NOTE

This check assumes that the ⟨√2⟩ Precision Limiter Check *gives positive results.*

1. Set the signal generator to 1.5 MHz CW at 0 dBm. Connect its RF output to A4J1 (IF IN) with a 50Ω termination in parallel with it. (A4J1 is shown on Service Sheet 10.)
2. Check A4TP3 (DISC OUT) with an oscilloscope. The oscilloscope input should have a low-capacitance 10:1 divider probe. The waveform should be a 3 MHz (that is, a doubled 1.5 MHz) triangle wave with an amplitude of 3 to 4 Vpp and an offset of −1 to +1 Vdc. The triangle may be slightly asymmetrical and adjacent cycles may be uneven.
3. Check A4TP4 (+ INPUT) and A4TP6 (− INPUT) with an oscilloscope. The offset voltages should be the same within ±10 mVdc. In addition, A4TP6 will have a superimposed 3 MHz "square wave" with an amplitude of 25 to 40 mVpp. The square wave may be asymmetrical and adjacent cycles may be uneven.
4. Decrease the signal generator frequency to 500 kHz. Check A4TP3 again. The offset level should be −7 to −5 Vdc.

⟨√4⟩ FM Output Amplifier Check

NOTE

This check assumes that the ⟨√3⟩ Charge-Count Discriminator Check *gives positive results.*

1. Set the signal generator to 1.5 MHz CW at 0 dBm. Connect its RF output to A4J1 (IF IN) with a 50Ω termination in parallel with it. (A4J1 is shown on Service Sheet 10.)
2. Key in 0.152 SPCL to unsquelch. Check A4TP5 (FM OUT) with an oscilloscope. The waveform should be a 3 MHz (that is, a doubled 1.5 MHz) sine wave with an amplitude of 0.4 to 0.8 Vpp and an offset of −1.9 to −1.3 Vdc. The waveform will be distorted and adjacent cycles may not be even.
3. Key in 0.150 SPCL to squelch. The ac component of the signal should decrease markedly.

   Hint: Pin 10 of A25XA4 should be a TTL low.

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Service Sheet 12

ASSEMBLY

- **A2 Audio Filters**

PRINCIPLES OF OPERATION

General

The Audio Filter Assembly contains some of the circuits that process the audio signal: low-pass filters, attenuators, and amplifiers. The inductors of all filters are carefully oriented and shielded to minimize mutual coupling and pickup of stray powerline fields.

260 kHz Low-Pass Filters and 20 dB Attenuator 1

The two 260 kHz Low-Pass Filters remove any IF carrier remaining on the demodulated AM or FM. Both are seven-pole, Butterworth filters with a nominal 3 dB cutoff frequency of 260 kHz. The filters determine the high-frequency response of the audio system when LP FILTER is set to ALL OFF. For each filter the first shunt capacitor is on the previous assembly (see Service Sheets 8 and 11). Filter switching is via U1. An additional range of FM is provided by 20 dB Attenuator 1 (R8 and R9) at the output of its 260 kHz Low-Pass Filter. R5 and C12 form a real-axis zero to equalize for a real-axis pole found later in the audio chain (see Service Sheet 13) when in AM only. In FM the pole is utilized in determining the overall frequency response. C11 is a dc blocking capacitor. R6 permits adjustment of the AM sensitivity.

Amplifier 1

Amplifier 1 is a low-noise, high slew-rate, non-inverting amplifier with a gain of 2.8. It must pass 200 kHz signals with minimum loss of fidelity. Amplifier transistors Q1, Q3, Q6, and Q7 and current source transistors Q2, Q5, and Q4 form a discrete operational amplifier. The overall amplifier gain is determined by feedback resistors and is equal to 1+(R27/R22). The bases of differential pair Q1A and Q1B are respectively the non-inverting and inverting inputs of the amplifier. Q4 and Q5 comprise a conventional two-transistor current source in which negative feedback causes the voltage drop across the emitter resistor (R24) of Q4 to equal the base-emitter voltage of Q5. The voltage that is thus established at the base of Q4 (two junction drops above the −15V supply) is also used as a reference for current-source transistor Q2. Complementary transistors Q6 and Q7 provide the current necessary to drive the output load at high modulation rates or levels. R11 and C14 frequency compensate the amplifier.

15 kHz and >20 kHz Low-Pass Filters

The 15 kHz Low-Pass Filter is selected when LP FILTER is set to 15 kHz or when the 455 kHz IF is being used (unless overridden). It is also switched in whenever the 3 kHz Low-Pass Filter (see Service Sheet 13) is selected to improve stopband rejection. The filter is a five-pole, Butterworth type with a 3 dB frequency of 15 kHz.

The >20 kHz Low-Pass Filter has nine poles and approximates a Bessel response for minimize overshoot. The 3 dB frequency is approximately 110 kHz.

The filters are switched by U2 and U4D. Since each filter has a 6 dB loss in the passband, the 6 dB Attenuator is inserted into the through path. Thermistors RT2 and RT3 compensate for thermal changes in the resistance of the filter inductors (and hence the insertion loss). The passband gain of the filters is adjusted by means of R40 and R44. When the 15 kHz Low-Pass Filter is selected, the outputs of the 6 dB Attenuator and >20 kHz Low-Pass Filter are grounded to minimize leakage through the output switches.

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Amplifiers 2 and 3 and 20 dB Attenuator 2

Amplifier 2 is non-inverting and has a gain of 4.84. Thermistor RT1 compensates for thermal changes in the resistance of the filter inductors of the 260 kHz Low-Pass Filters.

Two of the audio gain ranges are determined by 20 dB Attenuator 2 and the through path as set by the Audio Gain Selectors U4C and U4B.

Amplifier 3 is non-inverting and has a gain of 10 overall (including the attenuation due to R46 and R47). R47, R48, and the amplifier load (on Service Sheet 13) are grounded in such a way as to minimize the effect of ground loops.

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TROUBLESHOOTING

General

Procedures for checking the Audio Filter Assembly are given below. The circuits to check are marked on the schematic diagram by a hexagon with a check mark and a number inside, for example, ⟨√3⟩. In addition, any points outside the labeled circuit area that must be checked are also identified. Fixed signals are also shown on the schematic inside a hexagon, for example, ⟨+1.9 TO +2.1 VDC⟩. Extend the board assembly and its input cables where necessary to make measurements.

CAUTION

Tighten SMC connectors to 0.6 N·m (5 in·lb). Hand tightening of connectors is insufficient. Hand-tightened connectors can work loose and cause reduced performance or malfunctions.

If the Measuring Receiver is to be turned off, disconnect the audio synthesizer first to prevent damage to the FET switches by the large signal present.

Equipment

Audio Synthesizer	HP 3336C
Capacitor, 620 pF	HP 0160-3536
Oscilloscope	HP 1740A
Resistor, 909Ω	HP 0757-0422
Resistor, 1210Ω	HP 0757-0274
Resistor, 2150Ω	HP 0698-0084
Resistor, 4640Ω	HP 0698-3155
Voltmeter	HP 3455A

⟨√1⟩ 260 kHz Low-Pass Filters and Modulation Selectors Check

1. Disconnect the cables from A2J1 (AM IN) and A2J2 (FM IN). Extend the A2 Audio Filter Assembly. Jumper a lead between chassis ground and the cover of the A2 assembly.
2. Construct the input load for the AM input as shown in Figure 8F-14. The 775Ω resistor can be constructed from a 2150Ω resistor in parallel with a 1210Ω resistor.

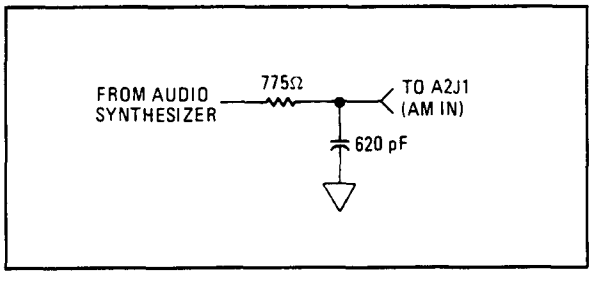


Figure 8F-14. *Filter for ⟨√1⟩ Step 2*

3. Set the audio synthesizer to 1 kHz at +13 dBm. Connect its 50Ω output to the input of the load. Connect the output of the load directly to A2J1 (AM IN). An intervening cable will add too much capacitance to the load.
4. Key in 0.120 SPCL and 0.111 SPCL to select low audio gain and AM.

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5. Connect a high-impedance, ac coupled oscilloscope to the input of the load. The oscilloscope should have a low-capacitance 10:1 divider probe. Adjust the synthesizer lever for a waveform of 5 Vpp.
6. Connect the oscilloscope to pin 3 of U1A. The 1 kHz waveform should have an amplitude between 450 and 500 mVpp.

   Hint: Pin 1 of U1A should be a TTL low. If for any reason the signal into the Audio Overvoltage Detector is too high, the Modulation Selectors will be latched open (see Service Sheet 13).
7. If necessary, adjust the synthesizer level for a waveform of 500 mVpp. Increase the synthesizer frequency to 50 kHz. The 50 kHz waveform should have an amplitude between 500 and 530 mVpp.
8. Increase the synthesizer frequency until the waveform amplitude is 355 mVpp. The synthesizer frequency should be between 240 and 280 kHz.
9. Increase the synthesizer frequency to 1.5 MHz. The waveform should drop into the noise.
10. Construct the input load for the FM input as shown in Figure 8F-15. The 760Ω resistor can be constructed from a 909Ω resistor in parallel with a 4640Ω resistor.

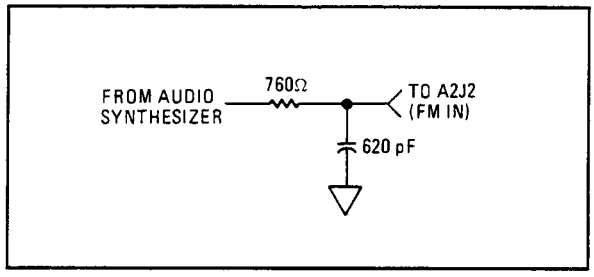


Figure 8F-15. *Filter for* ⟨√1⟩ *Step 10*

11. Set the synthesizer to 1 kHz. Connect its 50Ω output to the input of the load. Connect the output of the load directly to A2J2 (FM IN).
12. Key in 0.118 SPCL to select high-gain FM.
13. Connect the oscilloscope to the input of the load. Adjust the sythesizer for a waveform of 5 Vpp.
14. Connect the oscilloscope to pin 14 of U1D. The 1 kHz waveform should have an amplitude between 1.8 and 2.0 Vpp.

    Hint: Pin 16 of U1D should be low.
15. Adjust the level for a waveform of 2 Vpp. Increase the synthesizer frequency to 150 kHz. The 150 kHz waveform should have an amplitude between 1.95 and 2.05 Vpp.
16. Increase the synthesizer frequency until the waveform amplitude is 1.4 Vpp. The synthesizer frequency should be between 240 and 280 kHz.
17. Increase the synthesizer frequency to 1.5 MHz. The waveform should drop into the noise.
18. Set the synthesizer frequency to 1 kHz.
19. Key in 0.112 SPCL to select low-gain FM. The waveform should have an amplitude between 195 and 205 mVpp.

    Hint: Pin 9 of U1C should be a TTL low.

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⟨√2⟩ Amplifiers 1, 2, and 3, 15 kHz and >20 kHz LPFs, and Audio Gain Selectors Check

NOTE

This check assumes that the ⟨√1⟩ 260 kHz Low-Pass Filters and Modulation Selectors Check *above gives positive results.*

1. Disconnect the cables from A2J1 (AM IN) and A2J2 (FM IN). Extend the A2 Audio Filter Assembly. Jumper a lead between chassis ground and the cover of the A2 assembly.
2. Construct the input load for the FM input as described in step 10 of the ⟨√1⟩ *260 kHz Low-Pass Filters and Modulation Selectors Check* above.
3. Set the audio synthesizer to 1 kHz at +10 dBm. Connect its 50Ω output to the input of the load. Connect the output of the load directly to A2J2 (FM IN). An intervening cable will add too much capacitance to the load.
4. Key in 0.120 SPCL and 0.118 SPCL to select low audio gain and high-gain FM.
5. Connect a high-impedance, ac coupled oscilloscope to the base of Q1A. Adjust the synthesizer level for a waveform of 1.5 Vpp.

   Hint: If for any reason the signal into the Audio Overvoltage Detector is too high, the Modulation Selectors will latch open (see Service Sheet 13).
6. Connect the oscilloscope to A2TP2 (AMPL 1 OUT). The 1 kHz waveform should have an amplitude between 4.1 and 4.3 Vpp.
7. Adjust the synthesizer level for a waveform of 4 Vpp.
8. Key in 0.139 SPCL to select the 6 dB Attenuator. Connect the oscilloscope to pin 14 of U4D. The 1 kHz waveform should have an amplitude between 1.9 and 2.1 Vpp.

   Hint: Pin 1 of U2A should be a TTL low.
9. Key in 0.13C SPCL to select the 15 kHz Low-Pass Filter. The waveform should have an amplitude between 1.9 and 2.1 Vpp.

   Hint: Pin 16 of U4D and pins 8 and 16 of U2 should be a TTL low.
10. Increase the synthesizer frequency to 10 kHz. The waveform should have an amplitude between 1.9 and 2.1 Vpp.
11. Increase the synthesizer frequency until the waveform amplitude is 1.4 Vpp. The synthesizer frequency should be between 14 and 16 kHz.
12. Increase the synthesizer frequency to 150 kHz. The waveform should drop into the noise.
13. Set the synthesizer frequency to 1 kHz. Key in 0.13A SPCL to select the >20 kHz Low-Pass Filter. The 1 kHz waveform should have an amplitude between 1.9 and 2.1 Vpp.

    Hint: Pin 9 of U2C should be a TTL low.
14. Increase the synthesizer frequency to 10 kHz. The waveform should have an amplitude between 1.9 and 2.1 Vpp.
15. Increase the synthesizer frequency until the waveform amplitude is 1.4 Vpp. The synthesizer frequency should be between 100 and 120 kHz.
16. Increase the synthesizer frequency to 450 kHz. The waveform should drop into the noise.
17. Key in 0.139 SPCL to set all filters off. Set the synthesizer frequency to 1 kHz. If necessary, adjust the level for a waveform amplitude of 2 Vpp.
18. Connect the oscilloscope to A2TP3 (AMPL 2 OUT). The 1 kHz waveform should have an amplitude between 9.5 and 9.9 Vpp.

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19. Adjust the synthesizer level for a waveform of 10 Vpp.
20. Connect the oscilloscope to A2TP4 (AMPL 3 OUT). The 1 kHz waveform should have an amplitude between 9.9 and 10.1 Vpp.

    Hint: Pin 8 of U4B should be a TTL low.
21. Reduce the synthesizer level by exactly 20 dB.
22. Key in 0.121 SPCL to set audio gain to high. The waveform should have an amplitude between 9.9 and 10.1 Vpp.

    Hint: Pin 9 of U4C should be a TTL low.
23. Increase the synthesizer frequency until the waveform amplitude is 7.1 Vpp. The synthesizer frequency should be between 240 and 280 kHz.

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Service Sheet 13

ASSEMBLY

- **A3 Audio De-emphasis and Output**

PRINCIPLES OF OPERATION

General

The Audio De-emphasis and Output Assembly contain some of the circuits that process the audio signal: high- and low-pass filters, amplifiers, and an integrator for phase demodulation. It also contains the Instrument Bus decoding logic for itself, the Audio Filter Assembly, and the FM Demodulator Assembly.

300 Hz and 50 Hz High-Pass Filters and High-Pass Filter Switching

The 300 Hz and 50 Hz High-Pass Filters are active, two-pole, Butterworth filters with unity passband gain. Selection of the filter outputs or the through line is via U12A, U12B, and U12C.

3 kHz Low-Pass Filter, Low-Pass Filter Switching, and 300 kHz Pole

The 3 kHz Low-Pass Filter is an active, five-pole, Butterworth filter with unity passband gain. U4A is a unity-gain input buffer to the filter; R7 and C24 at its output form a real-axis pole. The R8, R9, C25, C26 and U4D form a pair of complex poles, and R11, R12, C33, C34, and U4C form another pair. Selection of the filter output of the through line is via U13A and U12D. R18 and C42 form a real-axis pole at 300 kHz that completes the filter for the Charge-Count Discriminator in the FM Demodulator (see Service Sheet 11). U3 is a unity-gain buffer amplifier.

De-emphasis Networks and Phase Modulation Integrator

The de-emphasis networks can be selected only in FM. They are simple single-pole, low-pass filters with 3 dB frequencies as shown in Table 8F-26.

Table 8F-26. *De-Emphasis Network 3 dB Frequencies*

Time Constant (μs)	3 dB Frequency (Hz)
25	6366
50	3183
75	2122
750	212.2

The 750 μs de-emphasis network is followed by an amplifier (U9A, R32, and R34) with a gain of 10. The gain is needed because 750 μs FM de-emphasis is normally used in situations where more resolution is desired because of low deviation and noise.

The Phase Modulation Integrator, U9B, converts the voltage from the FM Demodulator, which is proportional to frequency deviation, into a voltage proportional to phase deviation. Mathematically, the instantaneous phase deviation is equal to the time integral of the instantaneous frequency deviation (see *Modulation Basics* in the *Operation and Calibration Manual*). VR2 and VR3 limit the integrator output for large inputs and low frequencies. The integrator sensitivity is adjusted using R27.

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Switching of the de-emphasis networks and Phase Modulation Integrator is via the switches at their outputs. U14A and U14B select the input to the amplifiers that drive the Voltmeter, whether the input is before or after the de-emphasis. When de-emphasis is used, the de-emphasized signal is present at the MODULATION OUTPUT/AUDIO INPUT connector when the Modulation Output function has been selected.

Output Amplifiers

U10, U8, and associated resistors form two, closely matched amplifiers with a gain of two. U11 inverts the output of U10 and drives the MODULATION OUTPUT/AUDIO INPUT connector through 600Ω impedance (R54 and A25R1) when the Modulation Output function has been selected. U7 either inverts or does not invert the output of U8 depending on its configuration determined by the states of U14C and U14D. When U14C is active, the amplifier is non-inverting. When U14D is active, the amplifier is inverting.

Absolute Peak Detector

The input level to the assembly is sensed by the Absolute Peak Detector to determine if audio ranging is necessary. Range sensing is normally done by the Peak Detector (see Service Sheet 14). However, large signals of stopband frequency at the input to an active filter may go undetected by the Peak Detector and overdrive the filter. The Absolute Peak Detector and the Peak Detector are both read by the Voltmeter to determine the proper setting of audio gain.

The Absolute Peak Detector consists of an inverting, negative-peak detector (U6) and a non-inverting, positive-peak detector (U5) driving a common hold capacitor C44. The voltage across C44, then, is never negative. When the input voltage is negative, CR4 is off. The action of U5 is to turn on CR2 and reverse bias CR6 because the voltage across C44 is positive and the output of U5 is at least one junction drop more negative than the negative input voltage. Ignoring those components that have no effect, the detector can be simplified as shown in Figure 8F-16. The circuit shown is a conventional inverting, negative-peak detector.

When the input voltage is positive, CR2 is off. The action of U6 is to turn on CR4 and reverse bias CR5 because the voltage across C44 is positive and the output of U6 is one junction drop below ground. Ignoring those components that have no effect, the detector can be simplified as shown in Figure 8F-17. The circuit shown is a conventional, non-inverting, positive-peak detector.

CR1 and CR7 are protection diodes. The hold capacitor can be discharged by switching on Q1 via U15D at the request of the Controller. The detector's output goes to the Voltmeter.

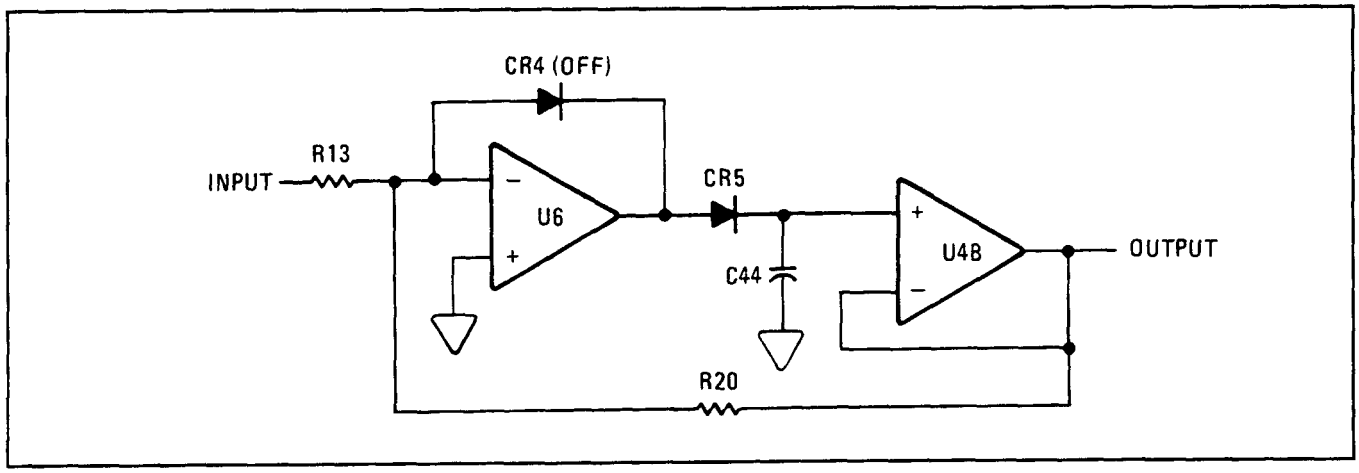


Figure 8F-16. *The Absolute Peak Detector Shown as an Inverting, Negative-Peak Detector*

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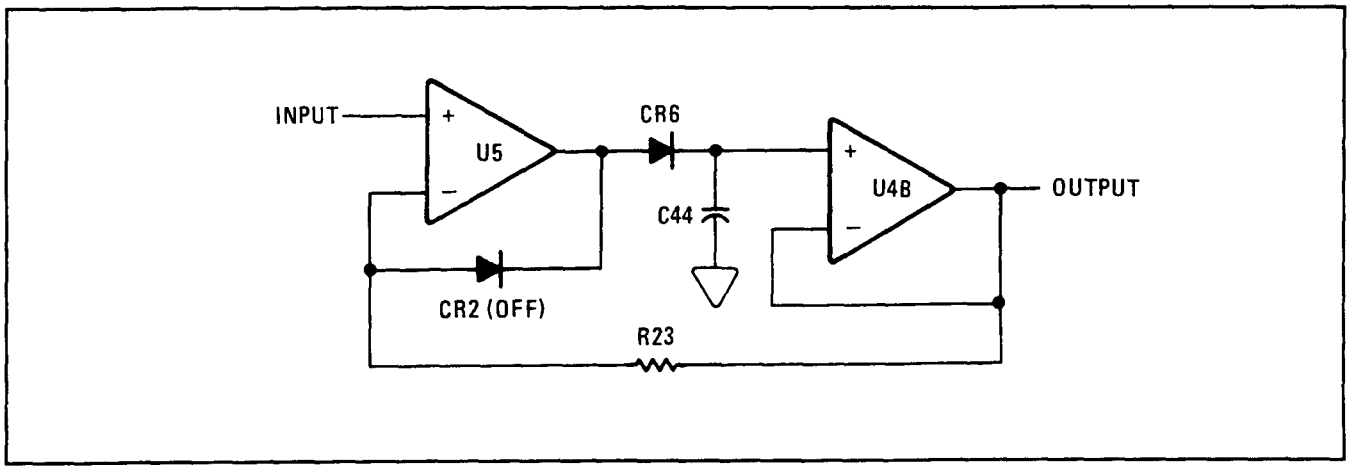


Figure 8F–17. *The Absolute Peak Detector Shown as a Non-Inverting, Positive-Peak Detector*

Audio Overvoltage Detector

The Audio Overvoltage Detector is a positive-peak detector followed by a comparator. If the peak input level should exceed +3.6V, U9D goes low and resets register U19. This opens up the audio path from the 260 kHz Low-Pass Filters via the Modulation Selectors (see Service Sheet 12). The status of the detector is read by the Controller via gates U21D and U21C.

Digital Circuits

Some of the digital circuits on this assembly also control circuits on the FM Demodulator and Audio Filter Assemblies (see Service Sheet 11 and 12). For a general discussion of instrument control, see *Instrument Bus* in Service Sheet BD5.

The FM SQUELCH (L) line going to the FM Demodulator is both an input and an output line. FM is squelched when either the Squelch Detector (see Service Sheet 11) senses a low IF level or when the Controller requests squelch. In the former case the line goes low and resets flip-flop U22B. The status of squelch can then be read by the Controller via gates U21B and U21C. The Controller can reset squelch by clocking a low into U22B which pulls the FM SQUELCH (L) line low. (For a discussion of the readback operation, see *Direct Control Special Functions* in paragraph 8-7.)

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TROUBLESHOOTING

General

Procedures for checking the Audio De-emphasis and Output Assembly are given below. The circuits to check are marked on the schematic diagram by a hexagon with a check mark and a number inside, for example, ⟨√3⟩. In addition, any points outside the labeled circuit area that must be checked are also identified. Fixed signals are also shown on the schematic inside a hexagon, for example, ⟨+1.9 TO +2.1 VDC⟩. Extend the board assembly where necessary to make measurements.

CAUTION

If the Measuring Receiver is to be turned off, disconnect the audio systhesizer first to prevent damage to the FET switches by the large signal present.

Equipment

Audio Synthesizer	HP 3336C
Oscilloscope	HP 1740A

⟨√1⟩ High-Pass and Low-Pass Filters and Filter Switching Check

1. Unplug the A2 Audio Filter Assembly.
2. Set the audio synthesizer to 1 kHz at +4 dBm. Connect its 50Ω output to pin 2 of A25XA3.
3. Connect a high-impedance, dc coupled oscilloscope to pin 2 of A25XA3. Adjust the synthesizer level for a waveform of 2 Vpp.
4. Key in 0.141 SPCL to select no high-pass filter.
5. Connect the oscilloscope to pin 2 of U12A. The 1 kHz waveform should be between 1.95 and 2.05 Vpp.

   Hint: Pin 8 of U12B should be a TTL low.
6. Key in 0.144 SPCL to select the 300 Hz High-Pass Filter. The waveform should be between 1.95 and 2.05 Vpp.

   Hint: Pin 9 of U12C should be a TTL low.
7. Decrease the synthesizer frequency to 300 Hz. The waveform should be between 1.3 and 1.5 Vpp.
8. Increase the synthesizer frequency to 1 kHz. Key in 0.142 SPCL to select the 50 Hz High-Pass Filter. The waveform should be between 1.95 and 2.05 Vpp.

   Hint: Pin 1 of U12A should be a TTL low.
9. Decrease the synthesizer frequency to 50 Hz. The waveform should be between 1.3 and 1.5 Vpp.
10. Key in 0.141 SPCL and 0.139 SPCL to select no high-pass or low-pass filters.
11. Increase the synthesizer frequency to 1 kHz. Connect the oscilloscope to A3TP4 (FLTR OUT). The waveform should be between 1.95 and 2.05 Vpp.

    Hint: Pin 16 of U12D should be a TTL low.

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12. Key in 0.130 SPCL to select the 3 kHz Low-Pass Filter. The waveform should be between 1.95 and 2.05 Vpp.

    Hint: Pin 1 of U13A should be a TTL low.

13. Increase the synthesizer frequency to 3 kHz. The waveform should be between 1.3 and 1.5 Vpp.

⟨√2⟩ De-Emphasis and Output Amplifiers Check

1. Unplug the A2 Audio Filter Assembly.

2. Set the audio synthesizer to 1 kHz at +4 dBm. Connect its 50Ω output to pin 2 of A25XA3.

3. Key in 0.139 SPCL, 0.149 SPCL, and 0.100 SPCL to select no high-pass or low-pass filters or FM de-emphasis.

4. Connect a high-impedance, dc coupled oscilloscope to A3TP4 (FLTR OUT). Adjust the synthesizer level for a waveform of 2 Vpp.

    Hint: If the level is faulty, see ⟨√1⟩ High-Pass and Low-Pass Filters and Filter Switching Check.

5. Connect the oscilloscope to A3TP2 (MOD OUT). The waveform should be between 3.9 and 4.1 Vpp.

    Hint: Pin 1 of U15A should be a TTL low. The gain of the Output Amplifier should be +2 followed by −1.

6. Key in the Direct Control Special Functions indicated in Table 8F-27. For each setting, set the synthesizer frequency as indicated. The waveform amplitude at A3TP2 should be as indicated.

Table 8F-27. *Levels at A3TP2, ⟨√2⟩ Step 6*

Direct Control Special Function	Synthesizer Frequency (Hz)	Waveform Amplitude (Vpp)	Level (TTL) at		
			U13-16	U13-9	U15-9
0.101	6366	2.6 to 3.0	H	H	L
0.104	3183	2.6 to 3.0	H	L	H
0.102	2122	2.6 to 3.0	L	H	H

7. Set the synthesizer frequency to 212.2 Hz and reduce its level exactly 20 dB.

8. Key in 0.103 SPCL to select 750 μs de-emphasis. The waveform should be between 2.6 and 3.0 Vpp.

    Hint: Pin 8 of U13B should be a TTL low. The in-band gain of the 750 μs amplifier is 10.

9. Key in 0.105 SPCL to select ΦM.

10. Set the synthesizer frequency to 1 kHz and increase its level exactly 20 dB. The waveform should be between 3.8 and 4.2 Vpp.

11. Increase the synthesizer frequency to 10 kHz and increase its level exactly 20 dB. The waveform should be between 380 and 420 mVpp.

12. Key in 0.100 SPCL.

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13. Decrease the synthesizer frequency to 2122 Hz. Connect the oscilloscope to A3TP3 (DE-EM OUT). Set the oscilloscope to trigger on the synthesizer output. The waveform should be between 3.9 and 4.1 Vpp.

    Hint: Pin 8 of U14B and pin 16 of U14D should be a TTL low.

14. Key in 0.108 SPCL to select a non-inverting output. The waveform should invert and have an amplitude between 3.9 and 4.1 Vpp.

    Hint: Pin 9 of U14C should be a TTL low.

15. Key in 0.102 SPCL and 0.141 SPCL to select 75 μs de-emphasis with pre-display on. The waveform should be between 2.6 and 3.0 Vpp.

    Hint: Pin 1 of U14A should be a TTL low.

16. Key in 0.100 SPCL. Increase the synthesizer frequency to 311 kHz. The waveform should be between 2.5 and 3.1 Vpp.

    Hint: This rolloff is due to R18 and C42. No other device should contribute to the rolloff.

⟨√3⟩ Detectors Check

1. Unplug the A2 Audio Filter Assembly.

2. Set the audio synthesizer to 1 kHz at +4 dBm. Connect its 50Ω output to pin 2 of A25XA3.

3. Key in 0.141 SPCL to select no high-pass filters and to assure that Q1 is off.

4. Connect a high-impedance, dc coupled oscilloscope to pin 2 of A25XA3 also. Adjust the synthesizer for a waveform of 2 Vpp.

5. Connect the oscilloscope to A3TP5 (AUDIO RANGE). The voltage should be between +0.9 and +1.1 Vdc.

6. Reduce the synthesizer level by 10 dB. The voltage at A3TP5 should discharge to 0.3V in about 2s.

7. Key in 0.160 SPCL to enable the discharge of the Absolute Peak Detector.

8. Increase then decrease the synthesizer level by 10 dB. The voltage at A3TP5 should discharge to 0.3V in about 0.5s.

   Hint: Low-going TTL pulses should appear at pin 16 of U15D.

9. Key in 0.111 SPCL and 0.150 SPCL to select AM and reset the Audio Overvoltage Detector and to enable readback of the audio overvoltage.

10. Connect the oscilloscope to pin 3 of U19. It should be a TTL low. The display should show 000000.0000.

    Hint: Low-going TTL pulses should appear at pin 12 of U21D. Pin 11 of U21D should be a TTL high. Pin 10 of U21C should be a TTL high.

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11. Set the synthesizer to +24 dBm or, if the synthesizer cannot deliver +24 dBm, set it to +19 dBm and connect its output to the anode of CR3. The voltage at pin 3 of U19 should be a TTL high. The display should show 000001.0000.

    Hint: Pin 11 of U21D should be a TTL low. Low-going TTL pulses should appear at pin 10 of U21C.

12. Reduce the synthesizer level by 10 dB. The voltage at pin 3 of U19 and the display should remain unchanged.

13. Connect the oscilloscope to pin 12 of U9D. The voltage should be between +3.4 and +3.8 Vdc.

⟨√4⟩ Select Decoder, Data Latches, and FM Squelch Checks

1. Key in the Direct Control Special Functions indicated in Table 8F-28. For each setting, check the pins on U20 indicated.

Table 8F-28. *Levels at U20, ⟨√4⟩ Step 1*

Direct Control Special Function	Level (TTL) at U20 Pin							
	7	9	10	11	12	13	14	15
0.100	H	H	H	H	H	H	H	*
0.110	H	H	H	H	H	H	*	H
0.120	H	H	H	H	H	*	H	H
0.130	H	H	H	H	*	H	H	H
0.140	H	H	H	*	H	H	H	H
0.150	H	H	*	H	H	H	H	H
0.160	H	*	H	H	H	H	H	H
0.170	*	H	H	H	H	H	H	H
*Low-going TTL pulses, approximately 60 ms period.								

2. Key in the Direct Control Special Functions indicated in Table 8F-29. For each setting, check the indicated pins.

Table 8F-29. *Levels at U18 and U17, ⟨√4⟩ Step 2*

Direct Control Special Function	Level (TTL) at U18 Pin					Level (TTL) at U17 Pin					
	2	7	10	14	15	1	2	3	4	5	6
0.100	L	L	L	H	L	L	H	H	H	H	H
0.101	H	L	L	H	L	H	L	H	H	H	H
0.102	L	H	L	H	L	H	H	L	H	H	H
0.103	H	H	L	H	L	H	H	H	L	H	H
0.104	L	L	H	H	L	H	H	H	H	L	H
0.105	H	L	H	H	L	H	H	H	H	H	L
0.108	L	L	L	L	H	H	H	H	H	H	H

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3. Key in the Direct Control Special Function indicated in Table 8F-30. For each setting, check the pins indicated on U19.

Table 8F-30. *Levels at U19,* ⟨√4⟩ *Step 3*

Direct Control Special Function	Level (TTL) at U19 Pin			
	3	6	11	15
0.111	L	H	H	H
0.112	H	L	H	H
0.114	H	H	H	H
0.118	H	H	L	H

4. Key in the Direct Control Special Functions indicated in Table 8F-31. For each setting, check the pins indicated on U22A.

Table 8F-31. *Levels at U22A,* ⟨√4⟩ *Step 4*

Direct Control Special Function	Level (TTL) at U22A Pin	
	5	6
0.120	L	H
0.121	H	L

5. Key in the Direct Control Special Functions indicated in Table 8F-32. For each setting, check the pins indicated on U23.

Table 8F-32. *Levels at U23,* ⟨√4⟩ *Step 5*

Direct Control Special Function	Level (TTL) at U23 Pin			
	3	6	11	15
0.131	L	H	H	H
0.132	H	L	H	H
0.134	H	H	L	H
0.138	H	H	H	L

6. Key in the Direct Control Special Functions indicated in Table 8F-33. For each setting, check the pins indicated on U16.

Table 8F-33. *Levels at U16,* ⟨√4⟩ *Step 6*

Direct Control Special Function	Level (TTL) at U16 Pin				
	3	6	11	14	15
0.141	L	H	H	H	L
0.142	H	L	H	H	L
0.144	H	H	L	H	L
0.148	H	H	H	L	H

7. Unplug the A4 FM Demodulator Assembly.

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8. Key in 0.152 SPCL and 0.170 SPCL to unsquelch then read squelch. The display should read 000000.0000.

   Hint: Pin 9 of U22B should be a TTL high. Pin 4 of U21B should be a TTL low. Pin 10 of U21C should be a TTL high.

9. Key in 0.150 SPCL to 0.170 SPCL to squelch then read squelch. The display should read 000001.0000.

   Hint: Pin 9 of U22B should be a TTL low. Pin 4 of U21B should be high-going TTL pulses. Pin 10 of U21C should be low-going TTL pulses.

10. Key in 0.152 SPCL and 0.170 SPCL, then momentarily ground pin 13 of U22B. The display should go from 000000.0000 to 000001.0000.

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Service Sheet 14

ASSEMBLY

- **A5 Voltmeter (Audio Detectors)**

PRINCIPLES OF OPERATION

General

The Voltmeter Assembly contains two ac-to-dc converters: the Audio Peak Detector and the Audio Average Detector. The input to the detectors is the output of the audio system and is a voltage proportional to AM depth, frequency deviation, or phase deviation. (An audio signal applied to the MODULATION OUTPUT/AUDIO INPUT connector cannot be measured by these detectors.)

Audio Peak Detector Circuits

The peak-detecting circuitry consists of the Peak Detector, the Sample-and-Hold Switch, and the Buffer Amplifier. U4 and Q2 comprise a high-gain comparison amplifier. The inverting (−) input of U4 is the non-inverting input of the overall comparator. If the inverting input of U4 is equal to or more positive than the voltage at the non-inverting (+) input, the output drives the collector of Q2 to follow the inverting input of U4. In doing this, Q2 must charge C18. When the inverting input of U4 lowers, the output of U4 goes high and shuts off Q2. Since C18 has no path to rapidly discharge, it remains at its previous potential, which was the peak value of the input voltage.

FET Q5 is a Sample-and-Hold Switch which is periodically (every 100 ms) switched on to transfer the voltage on C18 to C19. U8 is a high-impedance, unity-gain buffer amplifier which minimizes bleeding of C19 when Q5 is off (in its hold mode). Astable multivibrator U9 controls the switching of Q5. Q5 is switched on by Q6 when the output of U9 goes low. The transfer frequency is determined primarily by R19 and C8. The transfer time is determined by C8 and either R17 (when Q7 is off) or R17 in parallel with R14 (when Q7 is on). Also, when U9 goes high, Q3 is momentarily turned on to rapidly discharge C18. (At this time Q5 is off.) Thus, C18 must be recharged by the Peak Detector after each charge-transfer cycle.

The result of the sample-and-hold sequence is to control the response time of the peak-detector circuit and to make it respond equally well to an increasing or decreasing input level. This is illustrated in Figure 8F-18 where the response to a step increase and decrease in input level is shown.

Normally, Q7 is off, and the charge-transfer time is long enough for C19 to be charged completely. This gives the fastest response time. To slow down the peak-detector response, Q7 is switched on (by issuing 5.1 SPCL). R14 then is switched in parallel with R17, which shortens the time U9 is low. (See schematic Note 3 for timing information.) R36 now prevents C19 from charging completely in one sample period. This slows down the response time and smooths the output if the signal is noisy. When DETECTOR is set to PEAK HOLD, U9 is reset to switch Q5 into a permanent sample (on) mode. The voltage across C19 is then equal to the peak of the peaks. (In this mode the Controller also digitally holds the peak of the peaks read by the Voltmeter.)

Offset resistor R38 for U8 is adjusted under a no-signal condition to produce an output equal to the typical peak-detected noise level.

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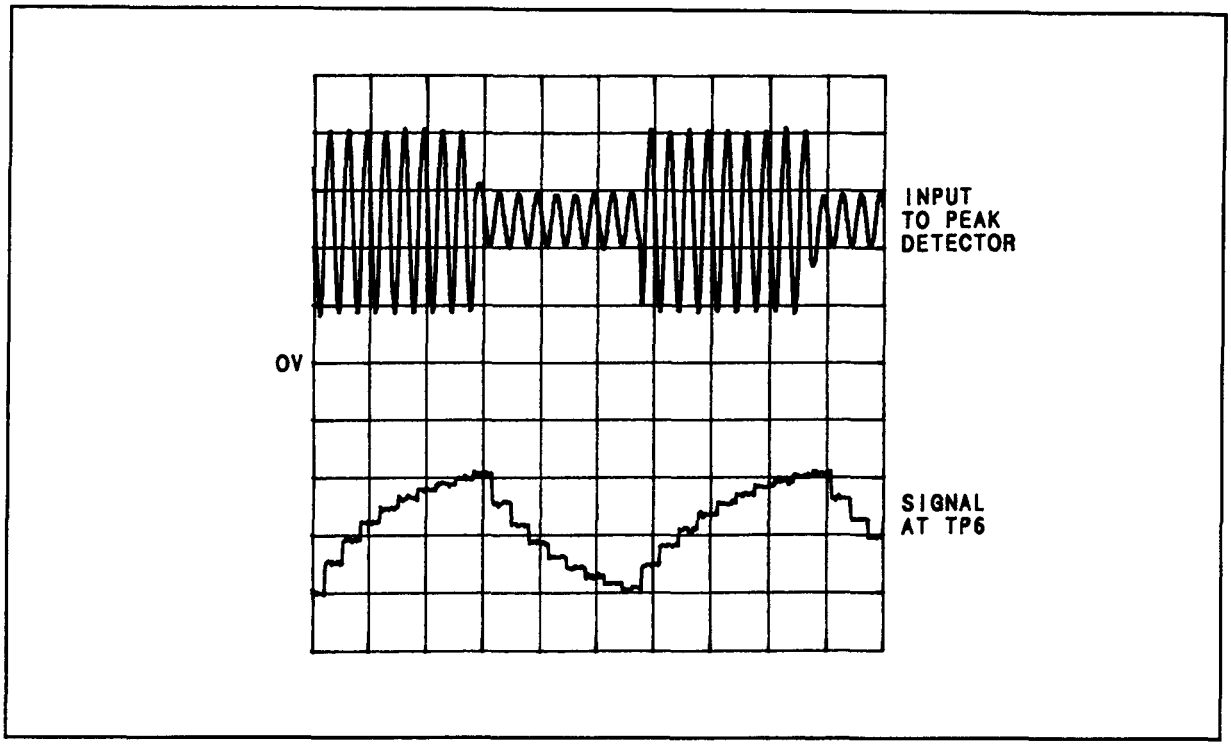


Figure 8F–18. *Action of the Peak Detector Sample-and-Hold Filter*

Audio Average Detector

The Audio Average Detector consists of the Half-Wave Rectifier followed by the Summer and Filter. The voltages and currents in the detector, for a sine wave input, are shown in Figure 8F-19. The input voltage produces a current in R5. This current is summed with the current in R8, also produced by the input voltage, which has been half-wave rectified and inverted. Since R8 is approximately half the value of R5 (and has a very stable resistance), the half-wave current is weighted by a factor of two when summed. The sum current, then, is proportional to the full-wave-rectified input voltage. After filtering, the sum current produces a dc voltage equal to the "absolute" average value of the input voltage. (The "actual" average of a sine wave is, of course, always zero.)

U3 is an inverting amplifier with two feedback paths (one for each direction of current flow). For a positive input voltage, current flows through R3, R6, and CR5. Since the values of R3 and R6 are equal, the output from R6 is opposite and equal to the input voltage. For a negative input voltage, the current flows through R3 and CR8. Since no current flows through R6 (because CR5 is shut off), the output from R6 is zero.

U1 sums the currents in R5 and R8. The sum current flows through the feedback resistors R22 and R23 and filter capacitor C12 to produce a negative dc voltage proportional to the sum current. R24, C14, R26, and C15 add further filtering. The Audio Average Detector has two offset adjustments. R18 is adjusted under a no-signal condition so that the detector output is zero with the Half-Wave Rectifier R2 adjusted to shut it off. R2 is then adjusted for a detector output equal to one half of the least-significant digit normally displayed. (This compensates for the fact that this undisplayed digit is dropped and not rounded off.)

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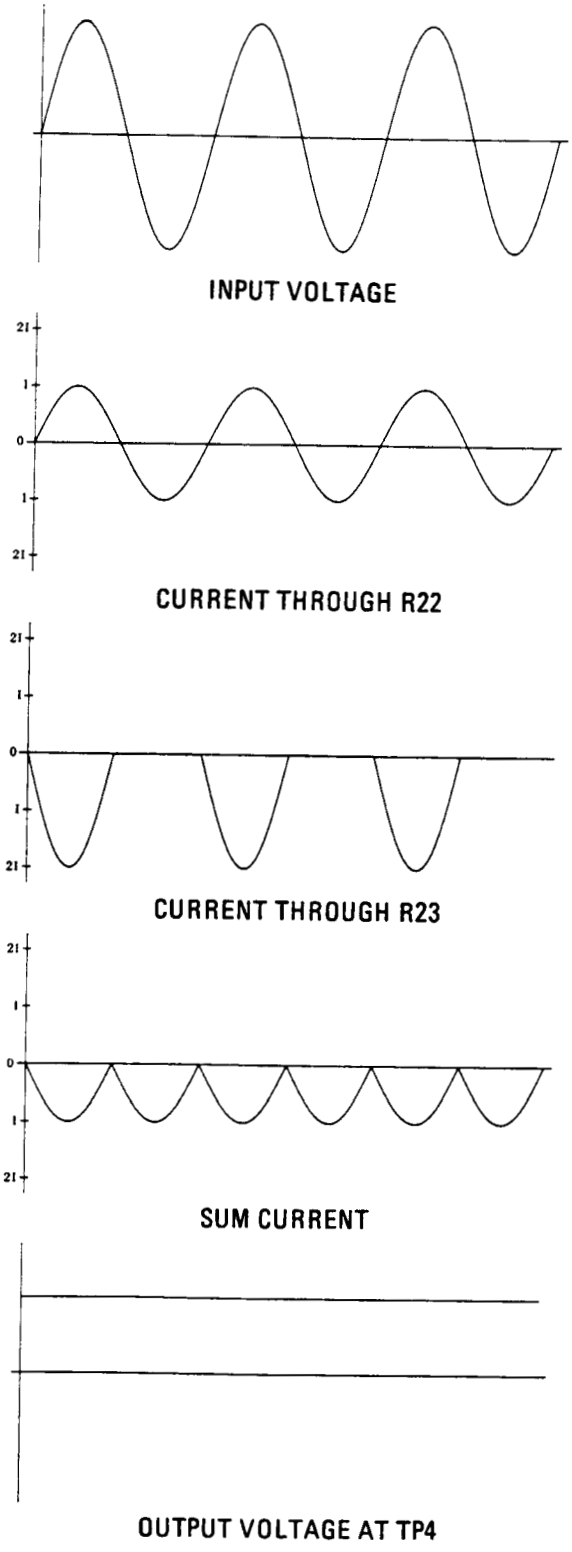


Figure 8F–19. *Waveforms in the Audio Average Detector*

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TROUBLESHOOTING

General

Procedures for checking the Voltmeter Assembly are given below. The circuits to check are marked on the schematic diagram by a hexagon with a check mark and a number inside, for example, ⟨√3⟩ . In addition, any points outside the labeled circuit area that must be checked are also identified. Fixed signals are also shown on the schematic inside a hexagon, for example, ⟨+1.9 TO +2.1 VDC⟩ . Extend the board assembly where necessary to make measurements.

CAUTION

CMOS circuits can be damaged by static charges and circuit transients. Do not remove this assembly from the instrument while power is applied. Discharge the board, replacement device, and soldering iron to the same potential. (Use the conductive foam pad provided in the Service Accessory Kit HP 08901-60287.)

Equipment

Audio Source	HP 8903B
Oscilloscope	HP 1740A
Voltmeter	HP 3455A

⟨√1⟩ Sample and Hold Drive Check

1. Key in 49.0 SPCL to set up the Voltmeter to measure ground.
2. Key in the Direct Control Special Functions indicated in Table 8F-34. For each setting, check the points indicated with a high-impedance, dc coupled oscilloscope. For each setting, the oscilloscope should read as indicated.

⟨√2⟩ Peak Detector Check

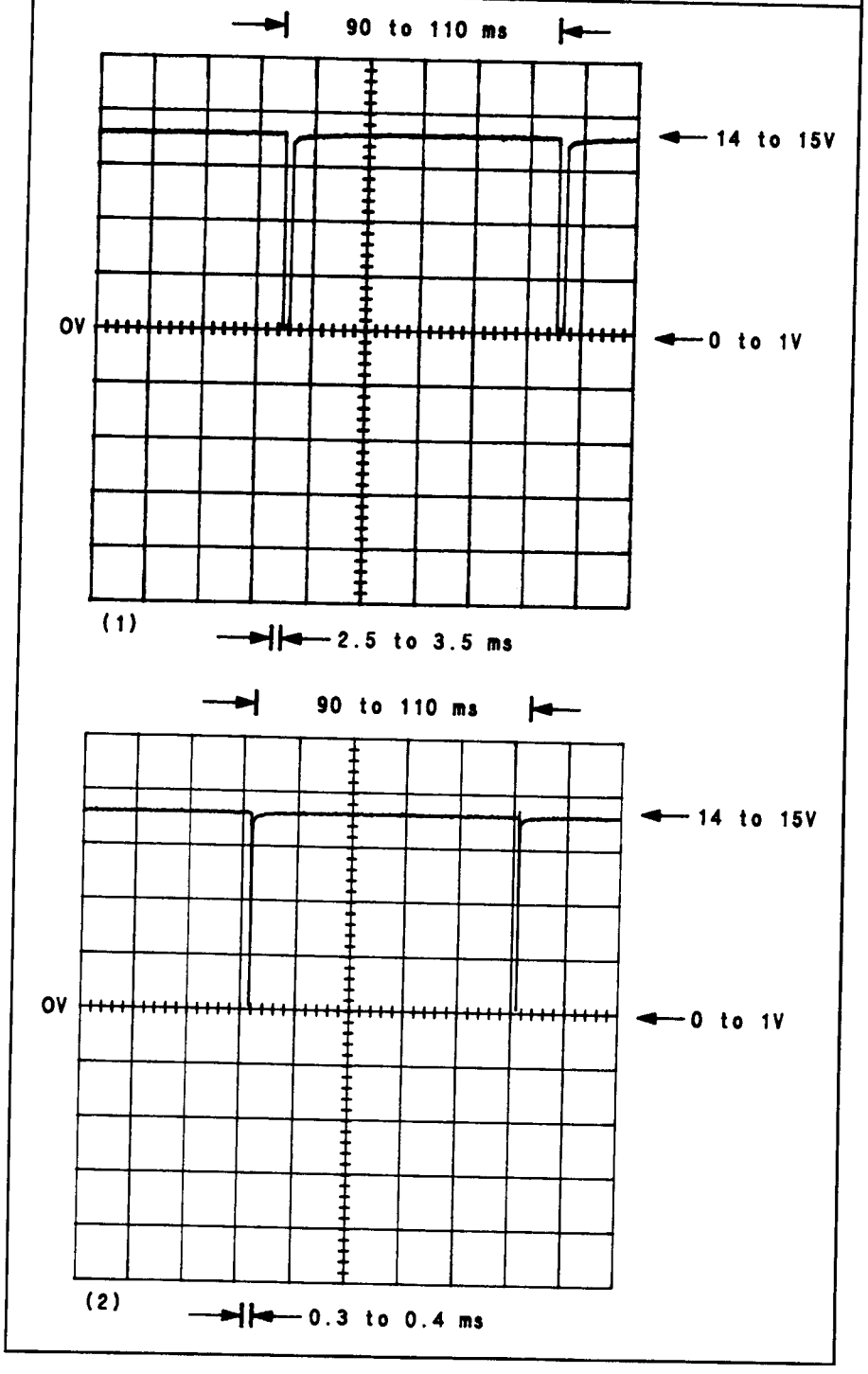
1. Unplug the A3 Audio De-Emphasis and Output Assembly.
2. Set the audio source to 1 kHz at 0.7 Vrms. Connect its output to pin 9 of A25XA5.
3. Connect an ac voltmeter also to pin 9 of A26XA5. Adjust the level of the source to 707.1 mVrms.
4. Key in 0.1E0 SPCL to set the peak detector discharge mode to hold.
5. Connect the voltmeter to A5TP7 (PK DET CAP). Set the voltmeter to measure dc. The voltmeter should read between +990 and +1010 mVdc or if the level of setup 3 could not be set exactly, 1.414 times the reading of step 3 ±1%.
6. Connect the voltmeter to A5TP6 (PK DET OUT). The voltmeter should read within ±1% of the reading in step 5.

   Hint: The collector of Q6 should be between +14 and +15 Vdc. Q5 should be on. If the reading is only slightly in error, perform the Voltmeter Offset and Sensitivity Adjustment. In normal operation the Peak Detector should be accurate to ±0.1% ±1 mV from 20 Hz to 200 kHz and to 4 Vpk. When testing the detector, the distortion of the source must be less than −70 dB.
7. Key in 0.1E1 SPCL to set the peak detector discharge mode to fast.

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Table 8F-34. *Waveform Levels on U15A and U9,* ⟨✓1⟩ *Step 2*

Direct Control Special Function	Level (TTL) on U15A		Voltage Limits (Vdc) on U9 Pin 3
	Pin 15	Pin 16	
0.1E1	L	H	See (1).
0.1E3	H	H	See (2).
0.1E0	L	L	0 to 1



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8. Connect a high-impedance, dc coupled oscilloscope to A5TP7. The waveform should be as in Figure 8F-20.

   Hint: If the waveform is faulty, see ⟨√1⟩ *Sample and Hold Drive Check.*

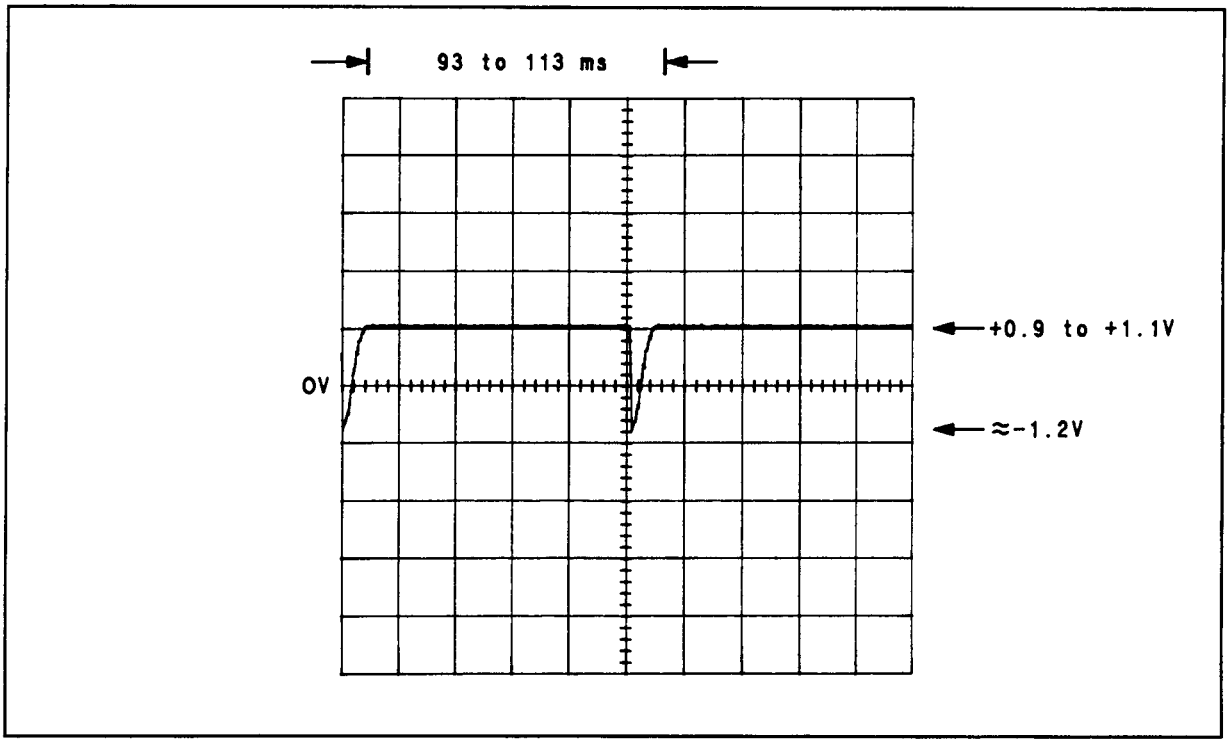


Figure 8F–20. *Waveform for* ⟨√2⟩ *Step 8*

⟨√3⟩ Average Detector Check

1. Unplug the A3 Audio De-emphasis and Output Assembly.

2. Set the audio source to 1 kHz at 0.7 Vrms. Connect its output to pin 9 of A26XA5.

3. Connect an ac voltmeter also to pin 9 of A25XA5. Adjust the level of the source to 707.1 mVrms as read by the voltmeter.

4. Connect a high-impedance, dc coupled oscilloscope to A5TP5 (RECT OUT). The waveform should be as in Figure 8F-21.

5. Increase the source frequency to 100 kHz (or preferably 150 kHz) without altering the amplitude. The waveform should appear as in step 4 except for the increase in frequency, and the level of the negative peak should be unchanged.

6. Decrease the source frequency to 1 kHz.

7. Connect a dc voltmeter to A5TP4 (AVG OUT). The voltage should be between +700 and +714 mVdc.

   Hint: If the reading is only slightly in error or if the Average Detector is known to be inaccurate at low levels, perform the Voltmeter Offset and Sensitivity Adjustment. In normal operation the Average Detector should be accurate to ±0.1testing the detector, the distortion of the source must be less than −70 dB.

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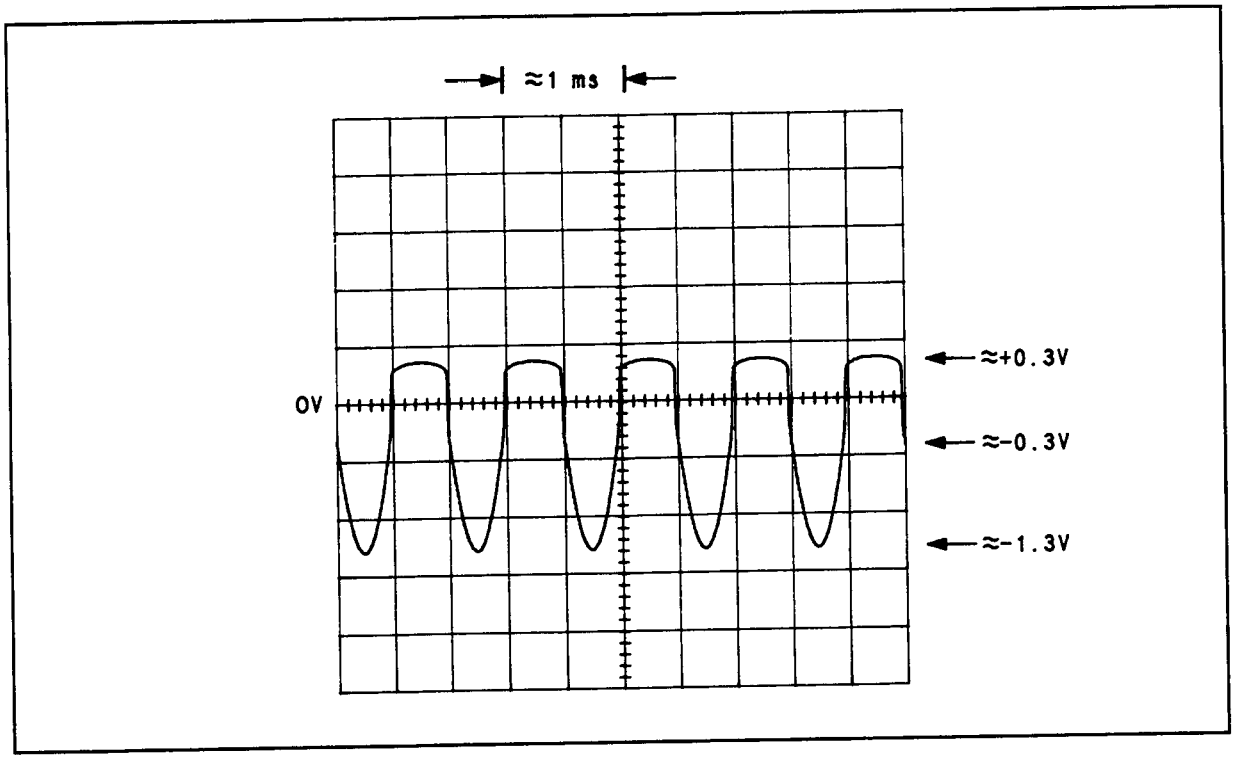


Figure 8F–21. *Waveform for* ⟨√3⟩ *Step 4*

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Service Sheet 15

ASSEMBLY

- **A5 Voltmeter (Voltmeter Circuits)**

PRINCIPLES OF OPERATION

General

The Voltmeter Assembly contains the Input Selectors and the Voltage-to-Time Converter portion of a digital dc voltmeter. It also contains a true RMS to DC Converter, which is utilized in the Tuned RF Level measurement mode, and a Parity Check circuit.

Input Selectors

Multiplexers U10, U11, and U12 form a 24 pole, single-throw switch. The individual multiplexers are enabled by a low on the G8 input. The selecting of U11 or U10 and U12 is via register U15B and exclusive-OR gate U14D. U10 or U11 is enabled when the code $esd = 1C0$ is issued on the Instrument Bus. (Note that $d2 = 0$. The D2 input to U15B is low.) After that, a code of the form $esd = 1Fd$ is issued to select a given input line. If $d3 = 1$, U11 is enabled. If $d3 = 0$, U10 is enabled. U12 is enabled when the code $esd = 1C4$ is issued. After that, a code of the form $esd = 1Fd$ is issued to select a given input line ($d3 = 0$ is not allowed here, for it would also enable U11). On the significance of the Instrument Bus codes, see *Instrument Bus* in Service Sheet BD5.

Voltage-to-Time Converter

The dc voltage at the output of the Input Selectors is converted to a pulse, with a duration proportional to the magnitude of the voltage, by the Voltage-to-Time Converter. The pulse length is then measured by the Counter (see Service Sheet 23), digitally processed by the Controller, and displayed. The converter consists of the Comparator, Ramp Generator, and Voltage Reference.

The Voltage Reference supplies a voltage of known temperature stability to the input to the Ramp Generator. The basic reference is a temperature-stable reference diode VR4. The reference is fed from current source Q1, which itself is temperature stable because its base-emitter junction and its reference (VR3) have matching thermal behavior. The negative Voltage Reference supplies current to the inverting (−) input of U6 through R73 and R74. CR13, R69 and R70 add a slight temperature coefficient to the current to cancel the effect of the temperature coefficient of integrating capacitor C31. The Voltmeter sensitivity is adjusted by means of R73.

U6 (with C31) integrates the negative input current to produce an increasing voltage ramp. The ramp is generated only when Q4 is off (when the RAMP GATE(H) line is high). The Controller initiates the ramp. When on, Q4 supplies a positive current to the inverting input of U6, which overrides the current from the reference and turns on CR15. Thus the output of U6 is clamped one PN junction drop below ground. Since the ramp begins at a rather imprecise voltage, each voltage measurement includes a measurement of ground which the Controller subtracts from the voltage measurement.

The ramp begins when the RAMP GATE(H) line goes high. The output of comparator U5 at this time is low because the positive (or zero) voltage at its inverting (−) input is higher than the voltage at its non-inverting (+) input. The Counter now begins clocking the duration of the ramp. When the ramp input of U5 reaches the voltage at the inverting input, the output goes high to inhibit the clocking of the Counter. R77 and R79 add a small amount of hysteresis to the Comparator to assure a complete transition of the output once it begins to change.

U17 is a unity-gain, non-inverting buffer amplifier, which drives the rear-panel RECORDER OUTPUT connector. This feature permits continuous monitoring of the voltmeter input. (See *Service Special Functions 49 and 50,* in paragraph 8-7, for information on the practical uses of this output.)

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Parity Check

The Parity Check circuit allows the Controller to test the integrity of the data lines of the Instrument Bus. To check parity, the Controller sends out the sixteen codes $esd = 1F0$ to $esd = 1FF$. For each code, the output of exclusive-OR gate U14C is read back by the Controller. The output of U14C is low when $d0 + d1 + d2 + d3$ is even, or high when it is odd. On the significance of the Instrument Bus codes, see *Instrument Bus* in Service Sheet BD5.. Parity is checked only during instrument power up (see *Power-Up Checks,* paragraph 8-9).

Digital Circuits

For a general discussion of instrument control, see *Instrument Bus* Service Sheet BD5. For a discussion of the readback operation, see *Direct Control Special Functions* in paragraph 8-7.

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TROUBLESHOOTING

General

Procedures for checking the Voltmeter Assembly are given below. The circuits to check are marked on the schematic diagram by a hexagon with a checkmark and a number inside, for example, ⟨√3⟩. In addition, any points outside the labeled circuit area that must be checked are also identified. Fixed signals are also shown on the schematic inside a hexagon, for example, ⟨+1.9 TO +2.1 VDC⟩. Extend the board assembly where necessary to make measurements.

CAUTION

CMOS circuits can be damaged by static charges and circuit transients. Do not remove this assembly from the instrument while power is applied. Discharge the board, replacement device, and soldering iron to the same potential. (Use the conductive foam pad provided in the Service Accessory Kit HP 08901-60287.)

Equipment

Oscilloscope ..... HP 1740A
Voltmeter ..... HP 3455A

⟨√1⟩ Input Selectors Check

1. Key in 0.1C0 SPCL to enable U10 or U11.
2. Key in the Direct Control Special Functions indicated in Table 8F-35. For each setting, compare the dc voltage at A5TP1 (SW OUT) to the pin on U11 or U10 indicated. The two voltages should be the same to within the repeatability of the voltmeter. If faulty, also check the logic level of the pins indicated.

Table 8F-35. *Levels on U10 and U11, ⟨√1⟩ Step 2*

Direct Control Special Function	Check Voltage at	Level (TTL) at				
		U10-1	U10-16	U10-15	U10-2	U11-2
0.1F0	U10-4	L	L	L	H	L
0.1F1	U10-5	H	L	L	H	L
0.1F2	U10-6	L	H	L	H	L
0.1F3	U10-7	H	H	L	H	L
0.1F4	U10-12	L	L	H	H	L
0.1F5	U10-11	H	L	H	H	L
0.1F6	U10-10	L	H	H	H	L
0.1F7	U10-9	H	H	H	H	L
0.1F8	U11-4	L	L	L	L	H
0.1F9	U11-5	H	L	L	L	H
0.1FA	U11-6	L	H	L	L	H
0.1FB	U11-7	H	H	L	L	H
0.1FD	U11-11	H	L	H	L	H
0.1FE	U11-10	L	H	H	L	H
0.1FF	U11-9	H	H	H	L	H

Hint: Pin 10 of U15B should be a TTL low. The logic state of pin 13 of U14D should be the same as pin 2 of U11.

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Hint: If a selector switch of U10, U11, or U12 is stuck shut, it may be difficult to isolate the faulty multiplexer. Try selecting a switch position which gives a non-zero voltage reading at A5TP1 then vary each of the input lines and see if the measured level follows it. (The labels on the input lines in the schematic diagram indicate what each input is.) Also try taping over a suspected input on the edge connector; if that input is causing the fault, the fault will go away. (See steps 3 and 4 for selecting the inputs of U12.)

3. Key in 0.1C4 SPCL to enable U12.
4. Key in the Direct Control Special Functions indicated in Table 8F-36. For each setting, compare the dc voltage at A5TP1 to the pin on U12 indicated. The two voltages should be the same within the repeatability of the voltmeter. If faulty, also check the logic level of the pins indicated.

Table 8F-36. *Levels on U12,* ⟨√1⟩ *Step 4*

Direct Control Special Function	Check Voltage at U12 Pin	Level (TTL) at U12 Pin			
		1	16	15	2
0.1F8	4	L	L	L	H
0.1F9	5	H	L	L	H
0.1FA	6	L	H	L	H
0.1FB	7	H	H	L	H
0.1FC	12	L	L	H	H
0.1FD	11	H	L	H	H
0.1FE	10	L	H	H	H
0.1FF	9	H	H	H	H

Hint: Pin 10 of U15B should be a TTL high. Pin 11 of U14D should be a TTL low.

⟨√2⟩ Voltage-to-Time Converter Check

1. Measure A5TP2 (REF) with a dc voltmeter. The voltage should be between −6.5 and −5.9 Vdc.
2. Key in 50.4 SPCL to set the instrument to measure the +15V Supply.
3. Connect a high-impedance, dc coupled oscilloscope to A5TP3 (RAMP). The waveform should be as in Figure 8F-22.

   Hint: Pin 2 of U6 should be between ±10 mV. The base of Q4 should be approximately +4V except for a pair of pulses which raise it to +5V approximately each 20 ms.
4. Connect the oscilloscope to A11TP6 (VM GATE). (A11TP6 is shown on Service Sheet 23.) The waveform should be as in Figure 8F-23.

   Hint: Step 4 assumes that the Input Selectors are able to select the input for the +15V Check.

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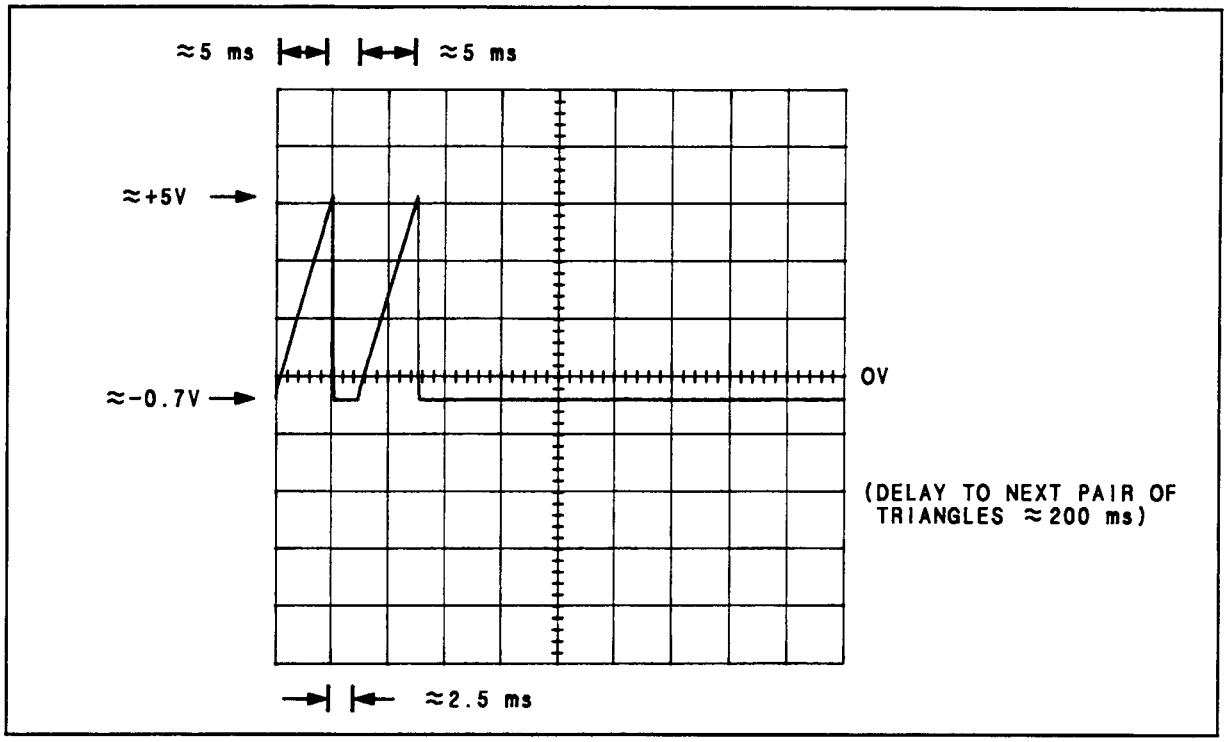


Figure 8F–22. *Waveform for* ⟨√2⟩ *Step 3*

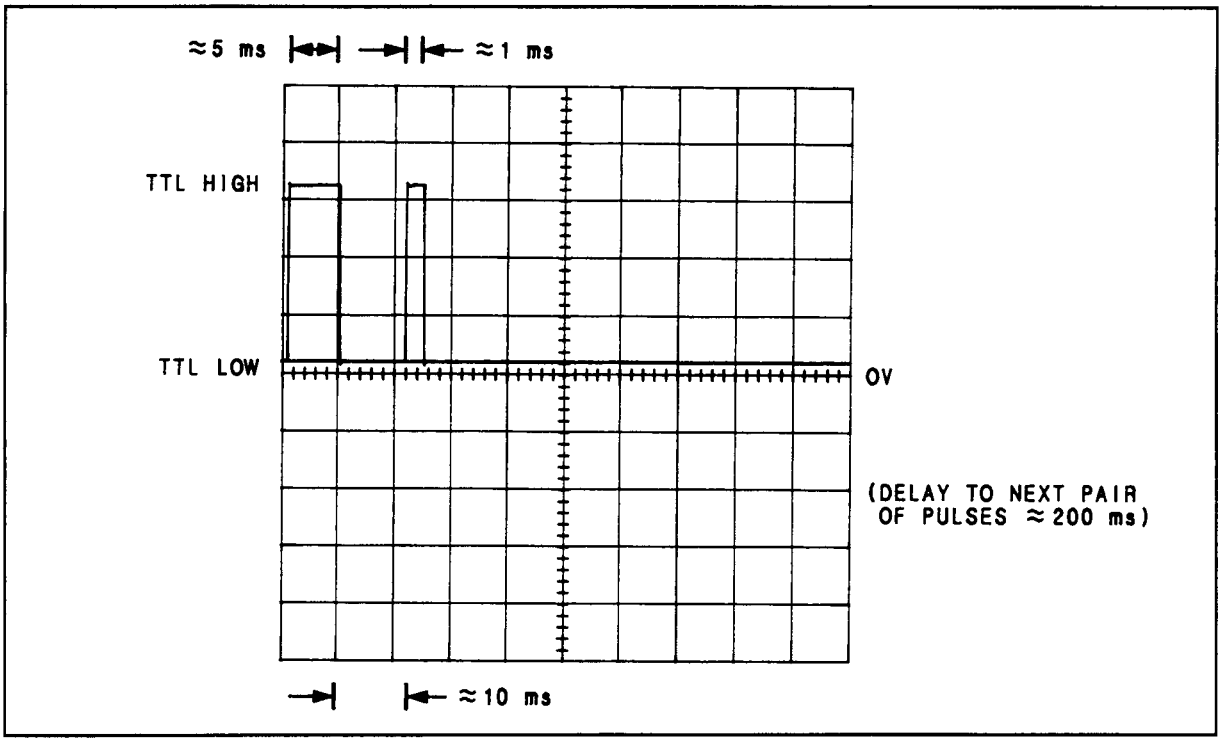


Figure 8F–23. *Waveform for* ⟨√2⟩ *Step 4*

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⟨3⟩ Parity Check

1. Key in the Direct Control Special Functions indicated in Table 8F-37, then key in 0.1D0 SPCL to enable parity readback. The display should be as indicated. If faulty, also check the logic level of the pins indicated.

Table 8F-37. *Levels on U14 and U16, ⟨3⟩ Step 1*

Direct Control Special Function	Display	Level (TTL) at			
		U14A-3	U14B-6	U14C-8	U16D-11
0.1F0	000000.0000	L	L	L	H
0.1F1	000001.0000	H	L	H	*
0.1F2	000001.0000	H	L	H	*
0.1F3	000000.0000	L	L	L	H
0.1F4	000001.0000	L	H	H	*
0.1F5	000000.0000	H	H	L	H
0.1F6	000000.0000	H	H	L	H
0.1F7	000001.0000	L	H	H	*
0.1F8	000001.0000	L	H	H	*
0.1F9	000000.0000	H	H	L	H
0.1FA	000000.0000	H	H	L	H
0.1FB	000001.0000	L	H	H	*
0.1FC	000000.0000	L	L	L	H
0.1FD	000001.0000	H	L	H	*
0.1FE	000001.0000	H	L	H	*
0.1FF	000000.0000	L	L	L	H
* Low-going TTL pulses, approximately 60 ms period.					

⟨4⟩ Select Decoder and Data Latch Check

1. Key in the Direct Control Special Functions indicated in Table 8F-38. For each setting, check the pins indicated.

Table 8F-38. *Levels on U16 and U18, ⟨4⟩ Step 1*

Direct Control Special Function	Level (TTL) at					
	U18-11	U18-10	U18-9	U18-7	U16B-6	U16C-8
0.1C0	*	H	H	H	**	L
0.1D0	H	*	H	H	L	**
0.1E0	H	H	*	H	L	L
0.1F0	H	H	H	*	L	L
* Low-going TTL pulses, approximately 60 ms period. ** High-going TTL pulses, approximately 60 ms period.						

2. Key in the Direct Control Special Functions indicated Table 8F-39. For each setting, check the pins on U13 indicated.

Table 8F-39. *Levels on U13, ⟨4⟩ Step 2*

Direct Control Special Function	Level (TTL) at U13 Pin				
	2	3	7	10	15
0.1F0	L	H	L	L	L
0.1FF	H	L	H	H	H

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Service Sheet 16

ASSEMBLY

- **A52 Audio Counter and Distortion Analyzer**

PRINCIPLES OF OPERATION

NOTE

The following discussions require an understanding of the operation of the Instrument Bus (see Instrument Bus *in Service Sheet BD5) and the Instrument Bus readback (see* Direct Control Special Functions, *paragraph 8-7).*

General

The Audio Counter and Distortion Analyzer Assembly makes measurements on internal or external audio signals. The signal comes internally from the Audio De-emphasis and Output Assembly (A3) or externally from the MODULATION OUTPUT/AUDIO INPUT connector. The measurements on the signal include ac voltage (true RMS), distortion (or the related measurement SINAD), and frequency. The measuring circuits include audio amplifiers, an RMS-to-DC converter, a notch filter, an audio counter, and control circuits.

Internal/External Source Switch and Audio Input Buffer

The four bi-directional switches of U19 determine whether the audio input signal into the Audio Counter and Distortion Analyzer circuits is from the Audio De-emphasis and Output Assembly (see Service Sheet 13) or from the MODULATION OUTPUT/AUDIO INPUT connector (used as an input). When switches U19A, U19B, and U19C are closed and U19D is open, the signal from the Audio De-emphasis and Output Assembly is routed into the Audio Input Buffer (U3D) and out to the MODULATION OUTPUT/AUDIO INPUT connector. With the switches of U19 in the opposite configuration, the signal from MODULATION OUTPUT/AUDIO INPUT connector is routed into U3D.

Amplifier U3D buffers the audio input signal. The amplifier is an ac coupled, inverting, unity-gain amplifier. Diodes VR1 and VR2 offer some degree of input-overload protection. The output of U3D goes to the RMS-to-DC Converter (via Amplifier 1), the Notch Filter, and the Audio Counter (via Schmitt Trigger U3A and U13B).

Amplifier 1

Amplifier 1 has two switched inputs: one from the Audio Input Buffer (U3D) and one from the output of the Notch Filter via Amplifier 2. U2A and U2B are the respective input switches. U4A is a non-inverting, unity-gain input stage of Amplifier 1.

U4B is configured as a non-inverting amplifier with a gain of 10 (20 dB). At its input is a switched 0 or 20 dB attenuator. The overall gain of Amplifier 1 is thus 0 or 20 dB. The output of Amplifier 1 is the input to the RMS-to-DC Converter (U1). The input is limited to approximately 4 Vrms. The sensitivity of the RMS-to-DC Converter is set by R38 (RMS SENS) at the output of U4B.

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RMS-to-DC Converter

The RMS-to-DC Converter converts the ac inputs signal into a dc voltage equal to the rms level of the input. The conversion is accomplished by U1. U1 converts the ac signal to its dc equivalent by a method called implicit conversion. The implicit equation for rms value is

$$V_{rms} = \text{avg of } \frac{\text{square of input voltage}}{V_{rms}}.$$

Note that V_{rms} appears on both sides of the equation.

The Absolute Value Detector of U1 converts the input to a full-wave rectified current. The rectified current is squared and then divided by the current at the Squarer/Divider's other input which comes from the Current Mirror (a device that produces two output currents equal to the input current). The current into the Current Mirror is filtered (that is, averaged) by C34. The current I from the Squarer/Divider is

$$I = \frac{\text{square of current from Absolute Value Detector}}{\text{current from Current Mirror}},$$

$$I = \frac{\text{square of current from Absolute Value Detector}}{\text{avg of } I}.$$

I_{OUT} from the Current Mirror also equals the average value of I, so

$$I_{OUT} = \text{avg of } I,$$

$$I_{OUT} = \text{avg of } \frac{\text{square of current from Absolute Value Detector}}{\text{avg of } I},$$

$$I_{OUT} = \text{avg of } \frac{\text{square of current from Absolute Value Detector}}{I_{OUT}}.$$

This is the implicit definition of the rms value of the input current. I_{OUT} flows through U1RL and produces a voltage which is buffered. R38 (RMS SENS) adjusts this buffered voltage equal to the rms value of the voltage at the input of U3D. R47 (RMS OFS) adjusts the output of the RMS-to-DC Converter to 0V when there is no input signal.

Ripple Filter

The dc output of the RMS-to-DC Converter is low-pass filtered, to remove ripple and noise, before being read by the Voltmeter. This smooths the displayed readings for audio distortion or SINAD. The Ripple Filter, consisting of U17A and associated components, generates a complex impedance across the line from the RMS-to-DC Converter and gives three poles of rolloff. The output is buffered by U17B.

Notch Filter

The Notch Filter has three active stages with two poles and two zeros generated by each stage. Each stage itself has a notch-filter frequency response. Jumpers W1 and W2 permit testing of the notch stages individually. The composite notch filter must have a notch depth of at least 50 dB over its nominal center frequency ±5%. The center frequency of the notch can be switched to either 400 or 1000 Hz by switches U5A, U5B, U5C, U5D, U6C, and U6D. The switches are closed when the notch center frequency is 400 Hz.

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Amplifier 2

Amplifier 2 is a 0 or 20 dB, switched attenuator followed by a 20 dB amplifier (U4D). Amplifier 2 amplifies the output from the Notch Filter. R44 (NOTCH FLTR GAIN) is adjusted to correct for stopband gain errors in the Notch Filter.

Schmitt Trigger and Audio Counter

The audio signal to be counted is conditioned by Schmitt Trigger U13A and U13B. Hysteresis in the Schmitt Trigger is provided by positive-feedback resistors R59 and R60 which cause the output to set the trigger reference voltage.

The output of U13B goes to three places: through U10C and on to an input of the input selector of the Counter (A11), through U9B and U9A and on to the first stage (U8A) of the Audio Counter, and to U12B to initiate the count after the flip-flop has been armed. (The output to the Counter (A11) is not used in normal instrument operation but the function is useful for checking operation of the Schmitt Trigger. See *Service Special Function 46.B,* paragraph 8-7.)

The count sequence is as follows: When the frequency of the audio signal is to be measured, the Controller resets all counter stages by placing a low on RDY(H)—and thus a high on RDY(L)—and then releasing it. Counters U8 and U16 are thus reset and readied to count, although the count does not actually begin at this time.

To initiate the count, the Controller sets GET SET(H) high and thus puts a high on input D1 of U12B. The first low-to-high transition from the Schmitt Trigger clocks the high at the D1 input of U12B into its output which enables U9B to pass the audio signal to the counter stages (U8 and U16). During the count, PLS LSB (pulse least-significant byte), PLS MSB (pulse most-significant byte), and CARRY ON(L) are all low. The transition of the output of U12B also sets STOP COUNT(H) low which enables the 10 MHz Selected Time Base Reference Oscillator to be counted by the Counter (A11, see Service Sheet 23).

During the count, the Controller continues to participate by counting the overflows of U16B via NAND gate U10D, which has been enabled by a high on the READBACK line. (The Controller also counts overflows from the Counter (A11).) After 100 ms, the Controller terminates the count.

To terminate the count, the Controller puts a low on GET SET(H). On the next low-to-high transition from the Schmitt Trigger, the output of U12B changes state which inhibits the count to the Audio Counter via U9B and stops the count of the Time Base Reference via U13A. If no transition of the Schmitt Trigger occurs, the Controller stops the the count by setting RDY(H) low to reset U12B and abort the count.

To read the count accumulated in counter U16, the Controller sets CARRY ON(L) high. This enables U9D regardless of the state of the FF(8) output of counter U8B. The Controller then rapidly pulses the PLS MSB line while it looks for a high-to-low transition from the FF(8) output of counter U16B via U10D which has been enabled (READBACK is high). The readback line to the Controller is d0(L). When the transition occurs, the Controller, which has kept track of the pulses it sent out, momentarily ceases pulsing PLS MSB.

The Controller next sends 255 pulses on the PLS MSB line to fill counter U16 (which was at count 0) to its maximum count then sets PLS MSB low. The count accumulated in U8 can now be read back. The Controller rapidly pulses the PLS LSB line while it looks for a high-to-low transition from U16B as before. When the transition occurs, the Controller, which has again kept track of the pulses, ceases pulsing PLS LSB.

The Controller now processes the count information (including the count it reads back from the main counter) and displays the audio frequency. The information included in the frequency calculation includes the accumulated count in U8 and U16, the number of carries from U16B during the count sequence, the number of 10 MHz pulses counted by the main counter, and the frequency of the time base (10 MHz).

Select Decoder and Data Latches

See the general discussion under *Instrument Bus* in Service Sheet BD5.

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TROUBLESHOOTING

General

Procedures for checking the Audio Counter/Distortion Analyzer Assembly are given below. The circuits to check are marked on the schematic diagram by a hexagon with a check mark and a number inside, for example, ⟨√3⟩. Fixed signals are also shown on the schematic inside a hexagon, for example, ⟨+1.9 TO +2.1 VDC⟩. Extend the board assembly where necessary to make measurements.

CAUTION

Tighten SMC connectors to 0.6 N·m (5 in·lb). Hand tightening of connectors is insufficient. Hand-tightened connectors can work loose and cause reduced performance or malfunctions.

Equipment

Audio Source ..... HP 3336C
Oscilloscope ..... HP 1740A

⟨√1⟩ Internal/External Source Switch Check

1. Set the audio source to 1 kHz at 1 Vrms. Connect its output to A52J1 (AUDIO IN).
2. Connect a high-impedance, ac coupled oscilloscope to pin 3 of U18 (or to A52J1). The oscilloscope should show the 1 kHz sinusoidal waveform with an amplitude between 2.7 and 2.9 Vpp
3. Adjust the audio source level for an amplitude of 3 Vpp as observed on the oscilloscope.
4. Key in the Direct Control Special Functions indicated in Table 8F-40. For each setting, connect the oscilloscope as shown. The waveform should be within the limits indicated. If faulty, also check the logic level at the pins indicated.

Table 8F-40. *Levels on A52TP4 and A52J2, ⟨√1⟩ Step 4*

Direct Control Special Function	Waveform Amplitude (Vpp) at A52TP4 and A52J2	Level (TTL) at U19 Pin	
		1, 8, and 9	16
0.2B0	2.9 to 3.1	L	H
0.2B1	<0.03	H	L

5. Connect the audio source to A52J2 (AUDIO OUT) and repeat step 4 using Table 8F-41.

Table 8F-41. *Levels on A52TP4, ⟨√1⟩ Step 5*

Direct Control Special Function	Waveform Amplitude (Vpp) at A52TP4 and A52J2	Level (TTL) at U19 Pin	
		1, 8, and 9	16
0.2B0	<0.03	L	H
0.2B1	2.9 to 3.1	H	L

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⟨√2⟩ Notch Filter Check

1. Set the audio source to 1 kHz at 1 Vrms. Connect its output to A52J1 (AUDIO IN).
2. Connect a high-impedance, ac coupled oscilloscope to A52TP4 (BUF OUT).
3. Key in 0.2B0 SPCL to route the signal to A54TP4. The oscilloscope should show the 1 kHz waveform with an amplitude between 2.7 and 2.9 Vpp.

   Hint: If the waveform is faulty, see ⟨√1⟩ *Internal/External Source Switch Check.*
4. Adjust the audio source level for an amplitude of 3 Vpp as observed on the oscilloscope.
5. Key in 0.2A4 SPCL to switch in the 1 kHz notch filter. Connect the oscilloscope as shown in Table 8F-42. The amplitude should be as indicated. In addition, for each display, momentarily increase the frequency of the signal to 1.1 kHz. In each case the signal level should increase.

Table 8F-42. *Levels on U3 and U4,* ⟨√2⟩ *Step 5*

Pin to Check	Amplitude Limits (mVpp)
U3C Pin 8	<300
U3B Pin 7	<30
U4C Pin 8	<10

   Hint: Pins 1, 8, 9, and 16 of U5 and pins 9 and 16 of U6 should be TTL high.
6. Key in 0.2AC SPCL to switch in the 400 Hz notch filter. Set the frequency of the audio source to 400 Hz. Repeat step 5 using Table 8F-43 and increasing the frequency to 440 Hz.

Table 8F-43. *Levels on U3 and U4,* ⟨√2⟩ *Step 6*

Pin to Check	Amplitude Limits (mVpp)
U3C Pin 8	<300
U3B Pin 7	<30
U4C Pin 8	<10

   Hint: Pins 1, 8, 9, and 16 of U5 and pins 9 and 16 of U6 should be TTL low.
7. Increase the audio source frequency slowly until the amplitude observed on the oscilloscope at pin 8 of U4C is 100 mVpp.
8. Connect the oscilloscope to A52TP3 (NOTCH FLTR OUT). The amplitude should be between 3.3 and 4.6 Vpp.

   Hint: The gain of Amplifier 2 has a wide range of adjustment. The adjustment potentiometer (R44) will normally be near its center. If adjustment is needed to correct a small distortion accuracy problem, perform *Adjustment 21—Audio True RMS Detector and Notch Filter Gain* in Section 5.

   Hint: Pin 16 of U2D should be a TTL low. Pin 9 of U2C should be a TTL high.
9. Key in 0.2A8 SPCL to set Amplifier 2 to low gain. The amplitude should be be 0.1 times the level noted in step 8.

   Hint: Pin 16 of U2D should be a TTL high. Pin 9 of U2C should be a TTL low.
10. Key in 0.2A9 SPCL to switch the notch input into Amplifier 1. Connect the oscilloscope to pin 3 of U4A. The amplitude should be the same as in step 9.

    Hint: Pin 8 of U2B should be a TTL low. Pin 1 of U2A should be a TTL high.

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⟨√3⟩ Amplifier 1, RMS-to-DC Converter, and Ripple Filter Check

1. Set the audio source to 1 kHz at 100 Vrms. Connect its output to A52J1 (AUDIO IN).
2. Connect a high-impedance, ac coupled oscilloscope to A52TP4 (BUF OUT).
3. Key in 0.2B0 SPCL to route the signal to A54TP4. The oscilloscope should show the 1 kHz waveform with an amplitude between 270 and 290 mVpp.

   Hint: If the waveform is faulty, see ⟨√1⟩ *Internal/External Source Switch Check.*
4. Adjust the audio source level for an amplitude of 300 mVpp as observed on the oscilloscope.
5. Key in 0.2A0 SPCL to switch the signal into Amplifier 1 and to set it to minimum gain. Connect the oscilloscope to pin 1 of U4A. The signal displayed on the oscilloscope should have an amplitude between 290 and 310 mVpp.

   Hint: Pin 1 of U2A should be a TTL low. Pin 8 of U2B should be a TTL high.
6. Connect the oscilloscope to A52TP2 (AMPL 1 OUT). The amplitude should be between 290 and 310 mVpp.

   Hint: Pin 1 of U6A should be a TTL high. Pin 8 of U6B should be a TTL low.
7. Key in 0.2A2 SPCL to set the gain of Amplifier 1 to 10. The amplitude should be between 2.9 and 3.1 Vpp.

   Hint: Pin 1 of U6A should be a TTL low. Pin 8 of U6B should be a TTL high.
8. DC couple the oscilloscope and connect it to pin 6 of U1. The voltage should be between 1.0 and 1.2 Vdc and should contain no ripple.

   Hint: If the level is only slightly out of limits, perform *Adjustment 21—Audio True RMS Detector and Notch Filter Gain* in Section 5.
9. Connect the oscilloscope to A52TP1 (RMS OUT). The voltage should be between 1.0 and 1.2 Vdc.
10. Change the source frequency to 20 Hz without changing the level. AC couple the oscilloscope. The ac ripple should be between 20 and 100 mVpp.

⟨√4⟩ Audio Counter Check

1. Set the audio source to 100 kHz at 20 Vrms. Connect its output to A52J1 (AUDIO IN).
2. Connect a high-impedance, ac coupled oscilloscope to A52TP4 (BUF OUT).
3. Key in 0.2B0 SPCL to route the signal to A54TP4. The oscilloscope should show the 100 kHz waveform with an amplitude between 55 and 58 mVpp.

   Hint: If the waveform is faulty, see ⟨√1⟩ *Internal/External Source Switch Check.*
4. DC couple the oscilloscope and connect it to pin 6 of U13B. The 100 kHz signal displayed on the oscilloscope should be a TTL squarewave.

   Hint: The signal at pin 1 of U3A should be a rounded squarewave with an amplitude between 500 and 700 mVpp.
5. Follow the instructions in the steps below and observe the results listed in Table 8F-44. (All levels listed are TTL.)
   a. Key in 0.296 SPCL and 0.282 SPCL to reset the counter.
   b. Key in 0.28A SPCL to release the counter reset.
   c. Remove (momentarily) the signal from A52J1. Key in 0.28E SPCL to ready the counter.
   d. Reconnect the signal to A52J1 to initiate the count.
   e. Remove (momentarily) the signal from A52J1. Key in 0.28A SPCL to ready the count stop.

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f. Reconnect the signal to A52J1 to initiate the count stop.

g. Key in 0.288 SPCL to enable pulsing of counter U16.

h. Key in 0.292 SPCL to disable U9D.

i. Key in 0.28C SPCL and 0.294 SPCL to disable U9A and pulse it (to verify that it is disabled).

Table 8F–44. *Levels on Various ICs on A52,* ⟨√4⟩ *Step 5*

Step	U11 Pin					U12 Pin		U9 Pin				U8 and U16 Pins 3, 4, 5, 6, 8, 9, 10, and 11
	3	2	5	10	14	6	8	4	1	10	13	
a	L	H	L	L	L	L	H	L	H	H	L	L
b	H	L	L	L	L	L	H	L	H	H	L	L
c	H	L	H	L	L	L	H	L	H	H	L	L
d	H	L	H	L	L	L	L	*	*	*	*	*
e	H	L	L	L	L	L	L	-	-	-	-	-
f	H	L	L	L	L	L	H	L	H	-	-	-
g	H	L	L	L	L	H	H	L	H	L	H	-
h	H	L	L	L	H	H	H	L	H	L	L	-
i	H	L	H	H	L	H	L	*	L	L	H	-

* Indicates a squarewave signal. The frequency is 100 kHz divided by 2 for each counter in U8 and U16. The output of U9A (pin 1) should be 100 kHz; the FF(1) output of U8A (pin 3) should be 50 kHz; etc.; the output of FF(8) of U16B (pin 8) should be 1.5 Hz (100 kHz divided by 65536).

\- Indicates a don't care situation. (It may be either high or low.) The logic level will be the state of the counter at the moment the count was stopped.

6. Key in 0.314 SPCL to inhibit the ramp gate (see Service Sheet 23). Key in 0.280 SPCL to input a high into U13A. Pin 1 of U13A should be a TTL high.

   Hint: The Stop Count line (pin 1 of U13A) is shared by the Comparator of the Voltmeter (see Service Sheet 15).

7. Key in 0.28C SPCL to input a low into U13A. Pin 1 of U13A should be a TTL low.

8. Connect the oscilloscope to pin 11 of U10D. Key in 0.28E SPCL and 0.296 SPCL to initiate the count and enable readback of the audio count. The waveform should alternate sporadically between a TTL high and a TTL low. (The waveform is the Audio Count as gated by the FF(8) output of U16B. The Audio Count should be narrow, high-going TTL pulses with a period of approximately 60 ms.)

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⟨√5⟩ Select Decoder and Data Latches Check

NOTE

U11 is checked by the ⟨√4⟩ Audio Counter Check.

1. Key in the Direct Control Special Functions indicated in Table 8F-45. For each setting, check the pins on U7 indicated.

Table 8F-45. *Levels on U7,* ⟨√5⟩ *Step 1*

Direct Control Special Function	Level (TTL) at U7 Pin			
	15	14	13	12
0.280	*	H	H	H
0.290	H	*	H	H
0.2A0	H	H	*	H
0.2B0	H	H	H	*
* Low-going TTL pulses, ≈60 ms period.				

2. Key in the Direct Control Special Functions indicated in Table 8F-46. For each setting, check the pins on U14 indicated.

Table 8F-46. *Levels on U13,* ⟨√5⟩ *Step 2*

Direct Control Special Function	Level (TTL) at U14 Pin						
	2	3	7	6	10	11	14
0.2A0	L	H	L	H	L	H	H
0.2AF	H	L	H	L	H	L	L

3. Key in the Direct Control Special Functions indicated in Table 8F-47. For each setting, check the pins on U15 indicated.

Table 8F-47. *Levels on U15,* ⟨√5⟩ *Step 3*

Direct Control Special Function	Level (TTL) at U15 Pin	
	2	3
0.2B0	L	H
0.2B1	H	L

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Service Sheet 17

ASSEMBLY

- **A19 LO Divider**

PRINCIPLES OF OPERATION

General

The LO Divider Assembly converts the nominal 320 to 650 MHz signal from the High Frequency VCO to the appropriate range required to down-convert an RF input signal to the IF frequency. The circuits consist of one frequency doubler, one through path, and eight binary dividers (that is, divide-by-twos) for a total of ten ranges. The first two dividers and a separate third divider are always enabled to provide a 40 to 81.25 MHz signal for the Counter. Figure 8F-24 shows the divider scheme.

Input Buffer and Doubler Circuits

U2 is a non-saturating, high-frequency limiter which interfaces the High-Frequency VCO with the dividers and Frequency Doubler. The non-inverted output drives the first divider (U8). When in Band 0, the inverted output (the DIV 0 line) drives the LO output connector (J3) via U10, U5, and CR9. The inverted output also drives the Frequency Doubler through the Doubler Input Filter.

The Doubler Input Filter is a five-pole, tuneable, low-pass filter which removes the odd-ordered harmonics of the High Frequency VCO input to maximize the signal output and minimize subharmonics which could cause spurious IF responses. The filter is tuned by varactor diodes CR2 to CR5 which are driven by the same voltage that tunes the High Frequency VCO (see Service Sheet 18). The tune voltage is filtered by R1 and C1, attenuated by R1, R20, R22, and R23, then offset and buffered by U3.

The Frequency Doubler (U4) is an active, full-wave rectifier. The input transformer (U4T1) produces two out-of-phase signals in its secondary windings which drive the two inputs of differential amplifier (U4Q1 and Q2). The two differential output amplifiers (U4Q3 and Q4) conduct current flowing only in one direction; their outputs are wired-OR and produce a train of negative, full-wave rectified pulses. R41 can be adjusted to improve the balance (that is, minimize the fundamental and odd-harmonic feed-through) and minimize the possibility of the $^1/_2$ and $^3/_2$ harmonics of the doubled signal causing an IF response.

The Doubler Output Gate and High-Pass Filter aids in further eliminating the $^1/_2$ harmonic of the doubled signal. PIN diodes CR7, CR8, and CR9 switch the signal either from the doubler or the dividers to the LO output connector. For the Band Doubler, CR7 and CR8 are on and CR9 is off.

Divider Circuits

The first two dividers (U8 and U7) are EECL devices; all others are ECL. Signal routing is done via gates, switchable limiters (for example, U10 and U11), and PIN diodes. Except for Bands Doubler (Dblr), 0, and 1, the divider following the output divider is turned off to eliminate subharmonics which would be generated by leaving all dividers on. In the case of Band 2, U1A only is disabled. This is not apparent in Figure 8F-24. Figure 8F-24 does show that on Band 5, for example (where the output is taken from Divider 5, U6B), U8, U7, U1A, U6A, and U6B are all enabled and U12A is disabled (by setting it). The output of U6B is routed to the LO output connector via U13A, U14B, U9B, U11, U5, and CR9.

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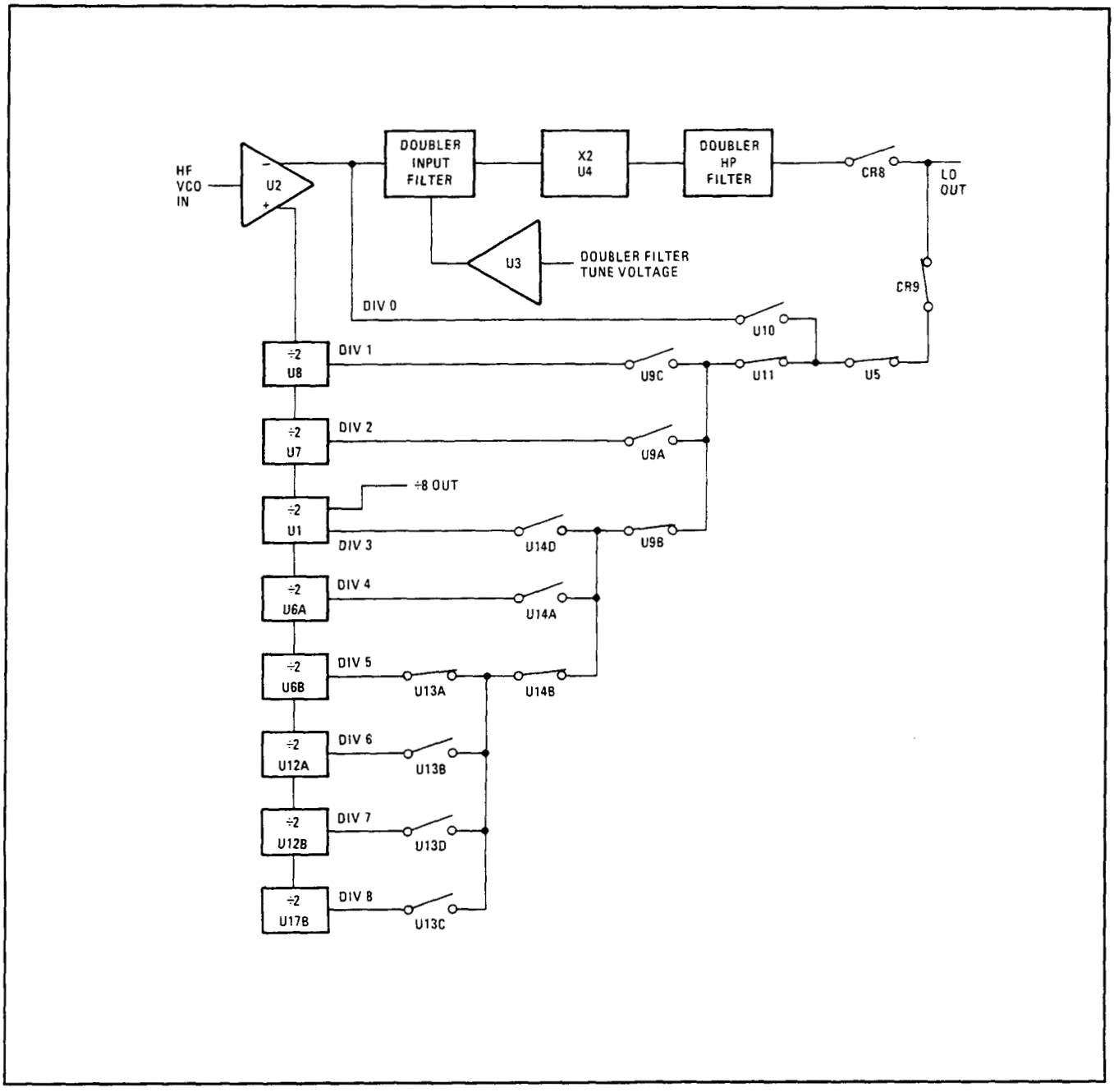


Figure 8F–24. *LO Divider Scheme (Shown for Band 5)*

Divider and Gate Decoders

Band enabling and signal routing is controlled by the Divider-Disable/Gate-Enable Decoder (U15 and U18). The decoder simply demultiplexes the *esd* = 00*d* code generated by the Instrument Bus and latched by the LO Control circuitry (see Service Sheet 21). The *d* is unique for each band. Further decoding for the added switching complexity that arises on the higher-frequency bands is accomplished by the Gate-Enable Decoders and Divider Output and Doubler Gate Drive circuits. For a general discussion of instrument control, see *Instrument Bus* in Service Sheet BD5.

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TROUBLESHOOTING

General

Procedures for checking the LO Divider Assembly are given below. The circuits to check are marked on the schematic diagram by a hexagon with a check mark and a number inside, for example, ⟨√3⟩. In addition, any points outside the labeled circuit area that must be checked are also identified. Fixed signals are also shown on the schematic inside a hexagon, for example, ⟨+1.9 TO +2.1 VDC⟩. Extend the board assembly where necessary to make measurements.

CAUTION

Tighten SMC connectors to 0.6 N·m (5 in·lb). Hand tightening of connectors is insufficient. Hand-tightened connectors can work loose and cause reduced performance or malfunctions.

Equipment

Oscilloscope ..... HP 1740A
Signal Generator ..... HP 8640B Opt 002
Spectrum Analyzer ..... HP 8559A/182T
Test Probe ..... HP 1250-15988
Voltmeter ..... HP 3455A

⟨√1⟩ LO Divider and Control Check

1. Set the signal generator to 512 MHz CW at 0 dBm. Connect its RF output to A19J2 (HF VCO IN).
2. Set the signal generator's counter to external. Connect its counter input to A19J3 (LO OUT).
3. Key in the Direct Control Special Functions indicated in Table 8F-48. For each setting, check the LO frequency on the signal generator's counter. If a fault is detected, also check the logic control lines indicated in the table. (All logic levels are ECL.)

   Hint: If only one of the bands 1 through 8 has a failure, check the last divider of that band noting that separate outputs drive the output gates and the next divider.

Table 8F-48. *LO Frequency, ⟨√1⟩ Step 3 (1 of 2)*

Band	Direct Control Special Function	Frequency (MHz)	U15 Pin											
			2	14	9	7	6	5	4	3	13	12	11	10
Dblr	0.00A	See ⟨√3⟩.	H	L	H	L	L	L	L	L	L	L	L	L
0	0.009	512	H	L	L	H	L	L	L	L	L	L	L	L
1	0.008	256	H	L	L	L	L	L	L	L	L	L	L	L
2	0.007	128	L	H	H	H	L	L	L	L	L	L	L	H
3	0.006	64	L	H	H	L	L	L	L	L	L	L	H	L
4	0.005	32	L	H	L	H	L	L	L	L	L	H	L	L
5	0.004	16	L	H	L	L	L	L	L	L	H	L	L	L
6	0.003	8	L	L	H	H	L	L	L	H	L	L	L	L
7	0.002	4	L	L	H	L	L	L	H	L	L	L	L	L
8	0.001	2	L	L	L	H	L	H	L	L	L	L	L	L
None	0.000	0	L	L	L	L	H	L	L	L	L	L	L	L

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Table 8F–48. *LO Frequency,* ⟨√1⟩ *Step 3 (2 of 2)*

Band	U18 Pin			U19 Pin				U16 Pin				U10-3	U11-3	U5-3
	13	12	11	9	3	14	2	14	3	9	2			
Dblr	L	L	H	H	L	H	L	H	H	L	H	H	H	H
0	L	H	L	H	H	L	L	H	H	L	H	L	H	L
1	H	L	L	H	H	L	H	H	H	H	L	H	L	L
2	L	L	L	H	H	L	H	H	L	H	H	H	L	L
3	L	L	L	L	H	L	H	L	H	L	H	H	L	L
4	L	L	L	L	H	L	H	L	H	L	H	H	L	L
5	L	L	L	L	H	L	H	H	H	L	H	H	L	L
6	L	L	L	L	H	L	H	H	H	L	H	H	L	L
7	L	L	L	L	H	L	H	H	H	L	H	H	L	L
8	L	L	L	L	H	L	H	H	H	L	H	H	L	L
None	L	L	L	L	L	H	L	H	H	L	H	H	H	H

4. Connect either a spectrum analyzer (for high frequencies) or an ac coupled oscilloscope terminated in 50Ω (for low frequencies) to A19J3 (LO OUT).

5. Repeat the keying in of the Direct Control Special Functions of step 3 (except the doubler band). For each step, vary the signal generator frequency between 320 and 650 MHz and note the output signal level. The level should be between 0 and +3 dBm or 500 and 700 mVpp (square wave).

⟨√2⟩ HF VCO÷8 Output Check

1. Set the signal generator to 512 MHz CW at 0 dBm. Connect its RF output to A19J2 (HF VCO IN).

2. Set the signal generator's counter to external. Connect its counter input to A19J1 (÷8 OUT). The signal generator's counter should read 64 MHz.

3. Connect either a spectrum analzyer or an ac coupled oscilloscope terminated in 50Ω to A19J1 (÷8 OUT).

4. Tune the signal generator frequency between 320 and 650 MHz. The measured signal level should be between 0 and +4 dBm or 500 and 800 mVpp (square wave).

⟨√3⟩ LO Doubler Band General Check

1. Set the signal generator to 512 MHz CW at 0 dBm. Connect its RF output to A19J2 (HF VCO IN).

2. Connect a spectrum analyzer to A19J3 (LO OUT).

3. Key in 0.0FF SPCL to inhibit LO sweep. Key in 0.01E SPCL to connect the DAC to the HF VCO. Key in 0.08F SPCL and 0.09F SPCL to set the eight most significant DAC bits to maximum. Key in 0.00A SPCL to switch to the doubler band.

4. Tune the signal generator frequency between 320 and 650 MHz. The signal level should be +1 dBm or more and the frequency should vary between 640 and 1300 MHz. Also, the $^1/_2$ and $^3/_2$ harmonics should be at least 30 dB below the fundamental over the frequency range.

   Hint: If the subharmonics are only slightly high, perform *Adjustment 5—LO Doubler Balance* in Section 5. If all bands but the doubler band work, start diagnosis by checking the control logic levels denoted in the table of step 3 of the ⟨√1⟩ *LO Divider and Control Check* above. Further diagnose the doubler band by checking the individual circuits using the following checks.

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⟨√4⟩ Doubler Input Filter and Filter Driver Check

1. Connect a dc voltmeter to A19TP1 (DBLR FLTR TUNE).
2. Set the signal generator to 320 MHz CW at 0 dBm. Connect its RF output to A19J2 (HF VCO IN).
3. Unplug U4.
4. Connect a spectrum analyzer between pin 11 of the socket for U4 and ground. An RF test probe will assist in making good contact.
5. Key in 0.0FF SPCL to inhibit LO sweep. Key in 0.01E SPCL to connect the DAC to the HF VCO. Key in 0.00A SPCL to switch to the doubler band. Key in 0.080 SPCL, 0.090 SPCL, 0.0A0 SPCL, and 0.0B0 SPCL to set the DAC output to zero.
6. Key in the Direct Control Special Functions indicated in Table 8F-49. For each setting, note the voltmeter reading then tune the signal generator until the signal drops by 6 dB and note the generator's frequency. In the filter passband the signal level should be approximately 0 dBm.

Table 8F-49. *Doubler Input Filter Signals,* ⟨√4⟩ *Step 6*

Direct Control Special Function	Voltage Limits (Vdc)		Frequency Limits (MHz)	
	Minimum	Maximum	Minimum	Maximum
As in step 5	+0.5	+1.6	330	430
0.088, 0.098	+6.2	+8.3	540	640
0.08F, 0.09F	+12.0	+15.0	700	>700

⟨√5⟩ Frequency Doubler and Doubler Output Circuit Check

NOTE

This check assumes that the ⟨√4⟩ Doubler Input Filter and Filter Driver Check *gives positive results.*

1. Key in the Direct Control Special Functions indicated in Table 8F-50. For each setting check the points indicated with a dc voltmeter.

Table 8F-50. *Doubler Output Signals,* ⟨√5⟩ *Step 1*

Direct Control Special Function	Voltage Limits (Vdc) at		
	Q1 Collector	U4 Pin 2	U4 Pins 4 and 6
0.00A	−15.2 to −14.4	−10.4 to −8.6	−4.2 to −1.8
0.000	+0.6 to +0.85	−2.6 to 0.0	+0.6 to +0.85

2. Check pins 2 and 8 of U4 with a dc voltmeter. The voltage should be between −2.6 and −2.2 Vdc.
3. Set the signal generator to 320 MHz CW at 0 dBm. Connect its RF output to A19J2 (HF VCO IN).
4. Key in 0.0FF SPCL to inhibit LO sweep. Key in 0.00A SPCL to switch to the doubler band.
5. Terminate A19J3 (LO OUT) in 50Ω.
6. Probe the output of U4 (pin 5) and the path through the Doubler Output Gate and High-Pass Filter. An RF test probe will assist in making good contact. The doubler signal will vary somewhat in amplitude along the path but it should be approximately 0 dBm when loaded by the probe.

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Service Sheet 18

ASSEMBLIES

- **A23 Sampler**
- **A24 High Frequency VCO**

PRINCIPLES OF OPERATION

General—A23 Sampler Assembly

The Sampler Assembly contains the Sampler and the HF VCO Tune Integrator and Amplifier. The assembly's output tunes the HF VCO and the Doubler Input Filter (see Service Sheet 17). Except for the track tune mode, the Sampler is used to phase lock the HF VCO to a tuneable, low-noise reference oscillator (the Low Frequency VCXO) when the LO has been tuned to the proper frequency. The Sampler is the phase detector of the phase-lock loop.

Sampler

The Sampler consists of the 2 MHz Limiter Amplifier, Impulse Generator, Sampling Bridge, and Sampler Amplifier. The Sampling Bridge is driven from the LF VCXO through the Impulse Generator. Once each cycle of the LF VCXO, the Impulse Generator produces a pulse which turns on the diodes of the Sampling Bridge for about 1 ns. At that time the signal from the HF VCO is sampled, and the sampled voltage is stored on a capacitor. If the HF VCO is frequency-coherent with a harmonic of the LF VCXO, the HF VCO will be sampled at the same point each time, and the output from the Sampling Bridge will be a dc voltage equal to the signal amplitude at the sample point. If the two signals are not frequency coherent, the output from the Sampling Bridge will be a sine wave with a frequency equal to the difference between the HF VCO and the nearest harmonic of the LF VCXO. This is illustrated in Figure 8F-25.

The nominal 2 MHz signal from the LF VCXO is first squared by the 2 MHz Limiter Amplifier. The limiter keeps the drive level to the Impulse Generator constant to keep the sample time of the Sampling Bridge constant. The limiter consists of Q1 and Q2—a non-saturating, differential amplifier.

The limiter drives switch Q6. When Q6 is off (that is, when Q2 is off), step-recovery diode CR3 is forward biased by R16, L7 and L8. When Q6 goes on, it quickly reverse biases CR3. CR3 then begins to conduct current in the reverse direction until the minority carriers, which had accumulated near the diode junction when forward biased, have been removed. The diode current then snaps off. Since this same current is flowing in L7 and L8, a large pair of impulses are produced when the current ceases. C16 is a high-frequency ac short. L7, L8, R19, R20, and the capacitance of CR3 form a carefully damped, parallel-resonant circuit to control the ringing of the impulses. C18, L10, and C21 and C19, L11, and C22 form two high-pass filters to pass the impulse pair but filter out any low-frequency 2 MHz signal. T1 is a balun which forces the impulse currents going to the Sampling Bridge to be opposite and equal to maintain balance in the bridge.

The Sampling Bridge consists of four matched, hot carrier diodes (CR6 to CR9). Normally, the diodes are reverse biased at approximately 4V (through R27 and R28). When a sample pulse occurs, the current impluses from T1 simultaneously forward bias all four diodes. This momentarily closes the signal path from the HF VCO to the gate of Q9B and charges C25 to the level of the waveform at that instant. The 700 MHz Low-Pass Filter removes the third harmonic of the HF VCO which influences the gain of the phase lock loop by altering the slope of the waveform at the zero crossing.

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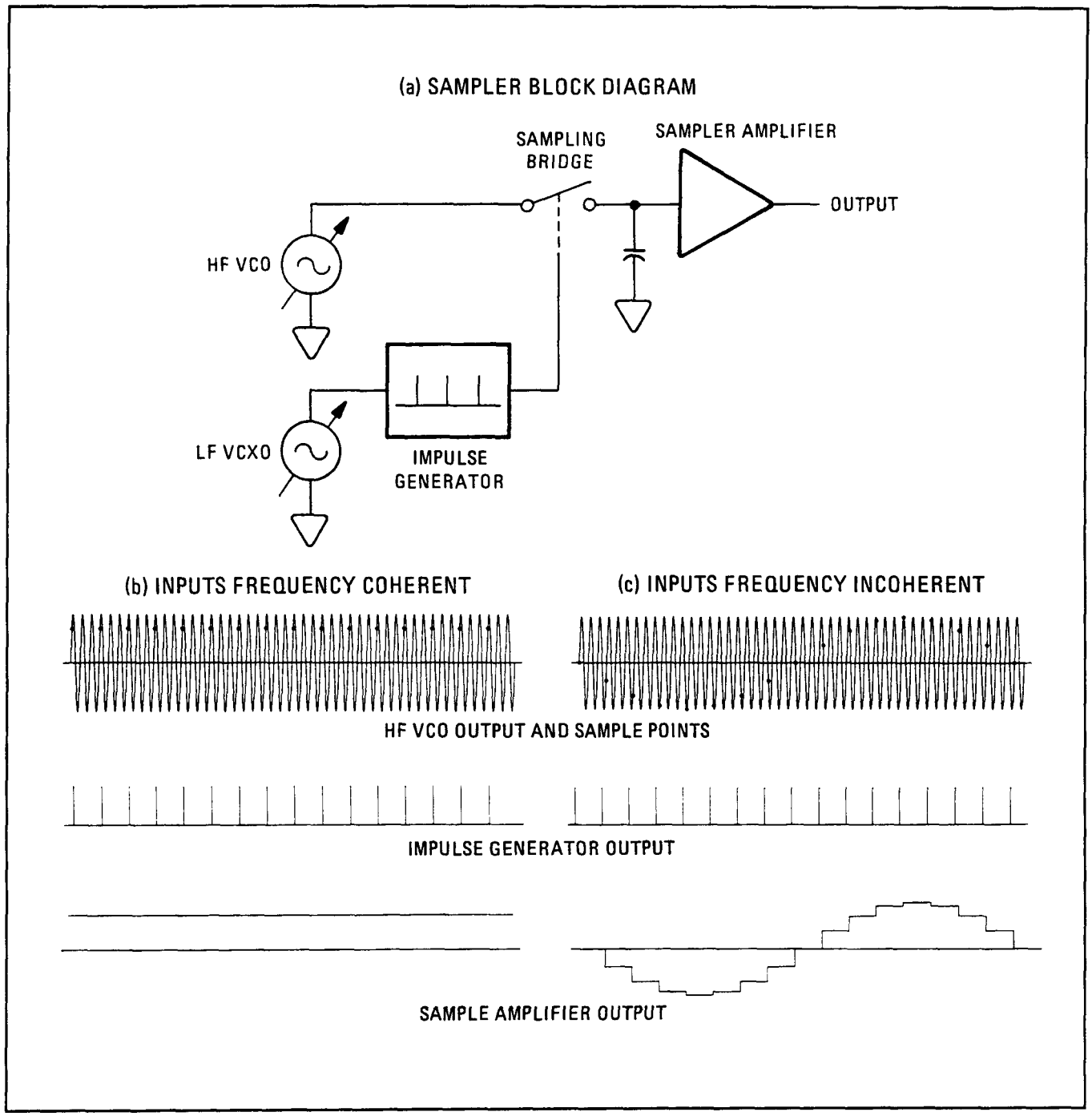


Figure 8F-25. *Sampler Operation*

The Sampler Amplifier is a dc to 5 MHz follower with feedback to automatically maintain a reverse bias of 4V on the Sampling Bridge diodes regardless of the output from the bridge itself. A simplified schematic of the Sampler Amplifier is shown in Figure 8F-26. Zener diodes VR2 and VR3 (represented as batteries in Figure 8F-26), produce the bias reference which is divided by R51, R54, R55, and R48. The junction of VR2 and VR3 is driven from the output of the unity-gain amplifier whose input is the output from the Sampling Bridge. Thus, as the level of the sampled voltage moves, the top and bottom of the Sampling Bridge move along with it, but the bias across the bridge is unchanged. The bias across the bridge is adjusted by R54.

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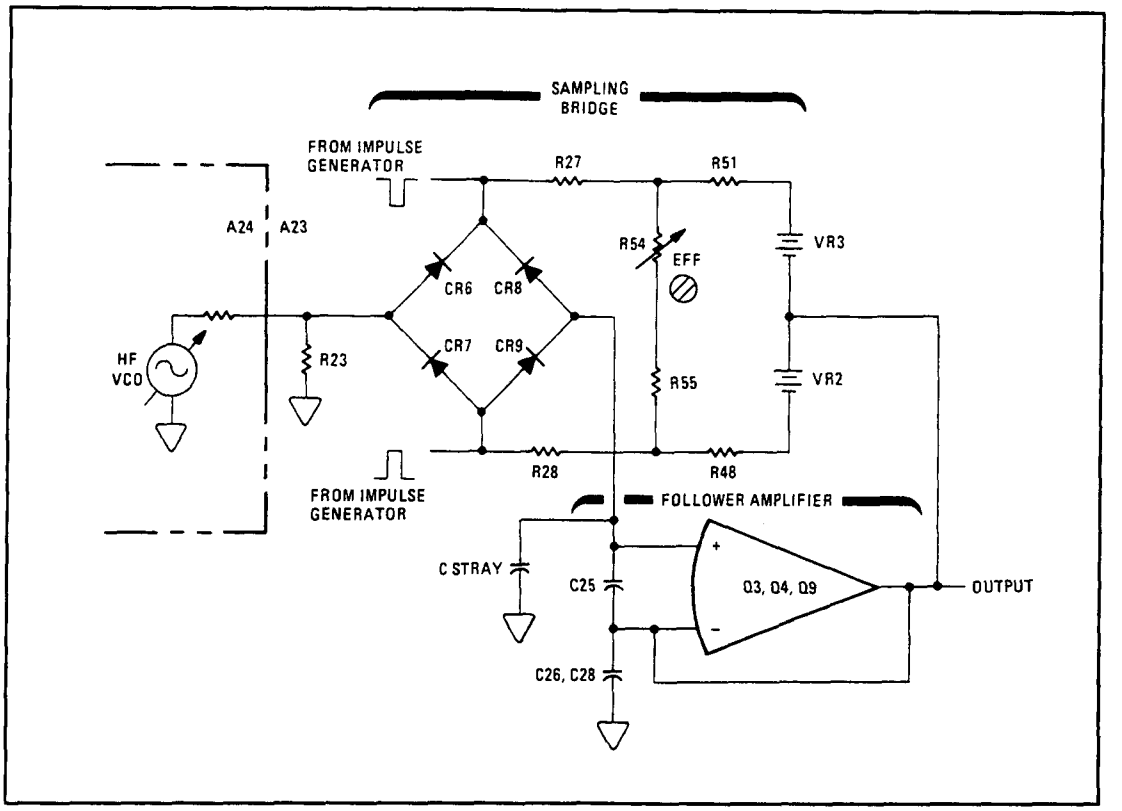


Figure 8F–26. *Simplified Schematic of Sampler Amplifier*

Because of the short duration of the sampling pulse and the finite drive impedance of the HF VCO, the capacitance at the input to the Sampler Assembly normally fails to charge completely to the level of the HF VCO in one sample. (The input capacitance is the parallel combination of the stray capacitance and C25; C26 and C28 together are much larger than C25 and can be considered an ac short.) During the sample period, however, a voltage develops across C25 and thus across the differential input of the follower amplifier. This large differential error causes the output of the amplifier to rapidly discharge C25 to zero and, in doing so, it continues to charge the stray capacitance (and C26 and C28). The additional charging created by C25 thus compensates for the inefficiency of the Sampling Bridge. R54 adjusts the sampling efficiency (by altering the bias across the bridge diodes) to match the sampling compensation and produce the optimum frequency response. R33 is adjusted to produce an output of zero volts when the phase error is zero.

HF VCO Tune Integrator and Amplifier and Bandwidth Loop Switching

The HF VCO Tune Integrator and Amplifier tunes the HF VCO and the Doubler Input Filter. It is configured in one of four different ways depending on the LO tune mode and the state of the mode. For a detailed discussion of the tuning modes, see Service Sheet BD1.

When the LO is configured with the DAC connected to the HF VCO, Q11 is off. (Q12 is on, but this is of little consequence here.) The HF VCO Tune Integrator and Amplifier and the DAC-to-VCO Loop Amplifier (A20U4B) of Service Sheet 14 form a unity-gain feedback amplifier. See Figure 8F-27.

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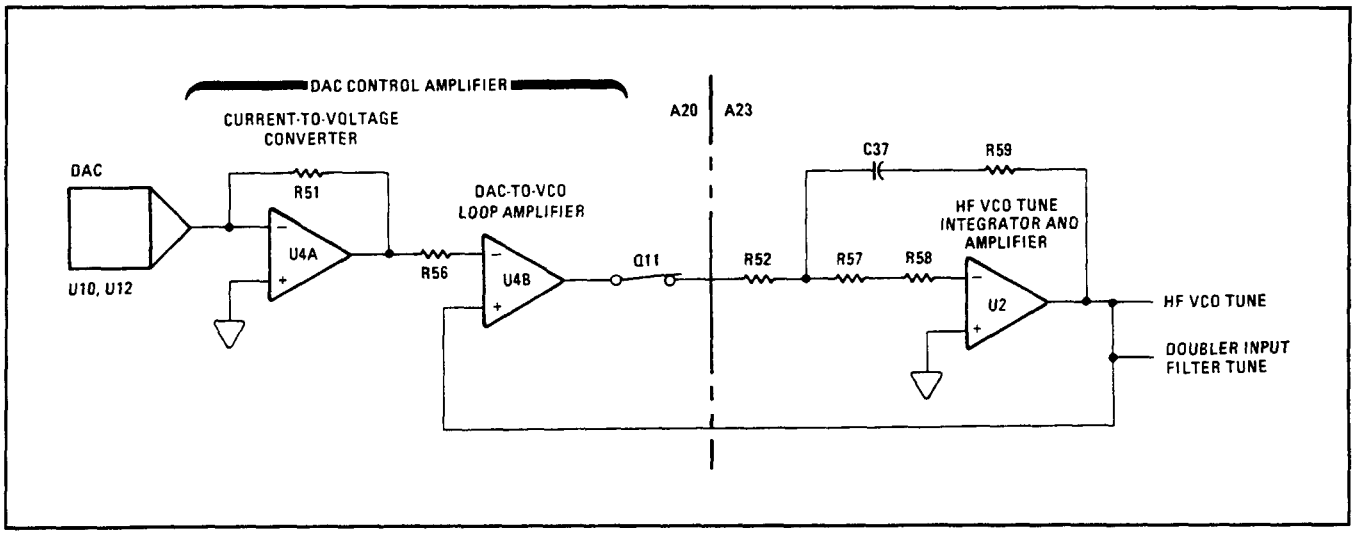


Figure 8F–27. *Simplified Schematic of LO Configuration: DAC to HF VCO*

When the LO is configured as a phase lock loop, with the DAC connected to the LF VCXO, Q11 is on. While phase lock is being acquired and while tuning the LF VCXO, Q12 is on to provide a wide (fast) tuning bandwidth. Initially, the LF VCXO is low in frequency. R46 produces a small current which causes the HF VCO to drift down into lock. After the HF VCO is locked and tuned, Q12 is turned off to narrow the bandwidth of the loop. The configuration is shown in Figure 8F-28 (the DAC connection is not shown).

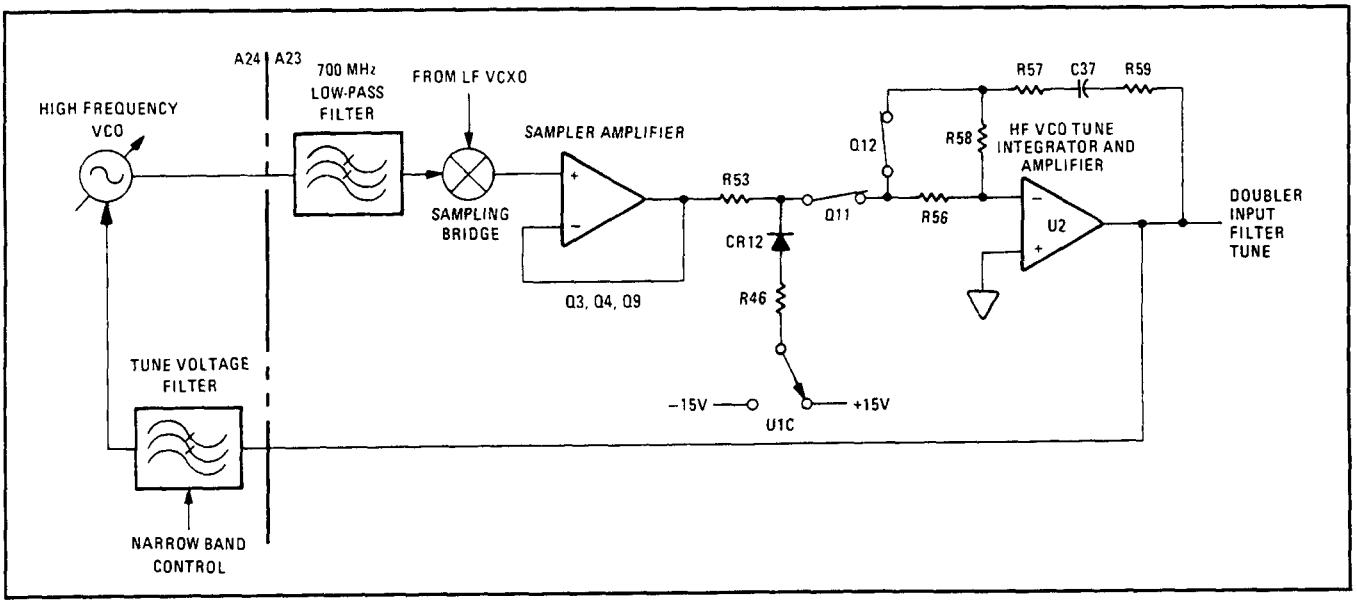


Figure 8F–28. *Simplified Schematic of LO Configuration: DAC to LF VCXO (DAC Connection Not Shown)*

When the LO is configured for HF VCO sweep, Q11 is off, (Q12 is on, but this is of little consequence here). The input to the HF VCO Tune Integrator and Amplifier is the Sweep Up and Sweep Down Current Sources (see Service Sheet 20). The current is integrated and produces a voltage ramp down (for sweep down) or up (for sweep up) at the output of U2.

When the LO is configured for track tuning, Q11 and Q12 are off. The input to the HF VCO Tune Integrator and Amplifier is the Track Loop Amplifier (see Service Sheet 20). The configuration forms

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a frequency-lock loop with a dc voltage (proportional to the IF frequency) from the FM Demodulator tuning the HF VCO.

Q10 shorts the output of the Sampler Amplifier when not connected to U2. Since the Sampler is always on, Q10 prevents any beat frequency from leaking into U2 and frequency modulating the HF VCO.

No-HF-VCO and Out-of-Lock Detectors

CR15 peak detects the RF signal from the HF VCO. If the detected level goes below the reference set by CR4 at the inverting input of U1A, the output of U1A goes low and turns on the NO HF VCO annunciator (DS1).

CR5 will peak detect an ac beat frequency on the output of the Sampler Amplifier. The beat frequency represents an out-of-lock condition. If the detected level exceeds the reference at the non-inverting input of U1B, the output of U1B goes low and turns on the OUT OF LOCK annunciator (DS2). When the Narrow Band control line is high (that is, not narrow band), the high output of U1C causes DS2 to light. The phase lock loop is not considered to be locked in its final state until the narrow-band filter has been switched in.

Power Supply Decoupling

Q5 multiplies the effect of C12 to assist in decoupling RF on the +15V supply. Q7 and Q8 multiply the effect of C13 to assist in decoupling the −15V supply.

General—A24 High Frequency VCO Assembly

The High Frequency Voltage Controlled Oscillator (VCO) is tuneable over the minimum range 320 to 650 MHz. It drives the LO Divider which produces the LO signal and the high-frequency input to the Sampler when the LO is locked to the LF VCXO.

High Frequency VCO and Output Buffer Amplifiers

The High Frequency VCO is a negative-resistance oscillator. At the frequency of operation, the inductor (L9) in the base of Q1, together with the collector-base capacitance of Q1, creates a negative resistance at the emitter port which is in parallel with a parallel-resonant Tank Circuit (L7 and the capacitance of the series-connected varactor diodes CR3 and CR4). The negative resistance cancels the losses in the Tank Circuit and sets up RF oscillations at the tank circuit's resonant frequency.

Varactor diodes CR3 and CR4 permit voltage tuning of the oscillator. Increasing the reverse bias on CR3 and CR4, decreases the junction capacitance and increases the resonant frequency. L6 and L8 are RF chokes.

U1 and U2 are limiter amplifiers that buffer the HF VCO output and drive the LO Divider and Sampler respectively.

Tune Voltage Filter and Filter Switch

The Tune Voltage Filter is switched in when the LO is tuned to the RF input signal and the HF VCO has been locked to the LF VCXO. It is also switched in the track-tune mode. The filter prevents noise in the tuning circuits from frequency modulating the HF VCO. It must be switched gently so as to not perturb the tune voltage.

The filter is out when current source Q4 is on (which switches Q2 and Q3 on). The input voltage is sensed by follower amplifier U3B which drives the varactor diodes through switch Q3. R3 has no filtering effect.

To switch the filter in, Q2 and Q3 are switched off by Q4 (which is now off). U3B has no effect, but it has pre-charged C10 to the present dc level. The filter is formed by R3, R17, and C10 in a lead-lag configuration. C9, which is charged by Q4, controls the turn on rate so that the filter switches in slowly without causing phase lock to break. C31, C32, and C33 are RF decoupling capacitors.

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VCO Tune Voltage Clamp

The VCO Tune Voltage Clamp prevents the tune voltage from forward biasing the varactor diodes (CR3 and CR4) whose anodes are biased at approximately −7.5 Vdc. The clamp reference is supplied by follower amplifier U3A which is referenced approximately one diode junction drop (CR6) above the varactor anode voltage. Clamp diode CR2 comes on when the tune voltage drops one PN junction drop below the output of U3A. If U3B were in the tune circuit, U3A would be supplying current to its output also. CR1 limits the current into the output of U3B by creating a current mirror—the current through CR1 and R2 is "mirrored" in CR2 and R3 since U3B is a voltage follower. CR5 sharpens the turn on characteristic of CR2. CR5 begins to conduct slightly when CR2 begins to conduct. The feedback action of U3A then causes its output to go more positive, which turns CR2 on harder.

Power Supply Decoupling

Q7 and Q8 multiply the effect of C7 and C8 respectively to assist in decoupling the +15 and −15V supplies.

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TROUBLESHOOTING

General

Procedures for checking the Sampler and High Frequency VCO Assemblies are given below. The circuits to check are marked on the schematic diagram by a hexagon with a check mark and a number inside, for example, ⟨√3⟩. In addition, any points outside the labeled circuit area that must be checked are also identified. Fixed signals are also shown on the schematic inside a hexagon, for example, ⟨+1.9 TO +2.1 VDC⟩. Extend the board assembly where necessary to make measurements.

CAUTION

Tighten SMC connectors to 0.6 N·m (5 in·lb). Hand tightening of connectors is insufficient. Hand-tightened connectors can work loose and cause reduced performance or malfunctions.

To avoid heat damage to the monoblock capacitors on the A24 High Frequency VCO Assembly, use low-temperature silver solder (HP 8090-0022). Apply silver solder to the printed circuit board at the appropriate pads, and apply just enough heat to solder the capacitor to the board. To remove a monoblock capacitor, apply heat to the trace to melt the solder holding the capacitor in place, then lift the capacitor off the board.

Equipment

Audio Source	HP 8903B
Oscilloscope	HP 1740A
Signal Generator	HP 8640B Opt 002
Spectrum Analyzer	HP 8559A/182T
Voltmeter	HP 3455A

⟨√1⟩ High Frequency VCO and Output Buffer Amplifiers Check

1. Connect a spectrum analyzer to A24J1 (HF VCO OUT).
2. Key in 55.0 SPCL to cause the HF VCO to sweep slowly back-and-forth across its range. The oscillator should sweep from below 310 to above 660 MHz at a power level between 0 and +4 dBm.
3. Connect the spectrum analyzer to A24J2 (HF VCO OUT). The signal should be the same as in step 2 except the level should be between −1 and +2 dBm.

   Hint: If only one output of step 2 or 3 is low, the Output Buffer Amplifier is probably faulty. If there is no signal, or if the signal drops out at certain frequencies, the High Frequency VCO is probably faulty but may also be the result of improper varactor bias (see ⟨√2⟩ *Varactor Bias Check*).

⟨√2⟩ Varactor Bias Check

1. Key in 0.0FF SPCL to inhibit LO sweep. Key in 0.01E SPCL to connect the DAC to the HF VCO.
2. Key in the Direct Control Special Functions indicated in Table 8F-51. For each setting, measure the points indicated with a dc voltmeter. When measuring the voltage between A24TP1 (TUNE) and A24TP2, connect the positive input to TP1 and the negative input to TP2. Neither side should be grounded.

   Hint: The VCO Tune Clamp is active for Direct Control Special Functions 0.080, 0.090, etc. A24CR2 is then on, clamping the tune line to the negative voltage.

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Table 8F–51. HF VCO Tuning, (√2) Step 2

Direct Control Special Functions	Voltage Limits (Vdc) at		Frequency (MHz)
	A24TP1 to A24TP2	A28XA24 Pin 5	
0.080, 0.090, 0.0A0, 0.0B0	+0.50 to +0.75	−11.2 to −10.6	>650
0.08F, 0.09F, 0.0AF, 0.0BF	+15 or more	+10.1 to +10.4	280 to 305

(√3) Tune Voltage Filter and Switch Check

1. Key in 0.0F8 SPCL to switch the filter on. Key in 0.01E SPCL to connect the DAC to the HF VCO. Key in 0.088 SPCL and 0.098 SPCL to set the DAC to its midrange.
2. Key in the Direct Control Special Functions indicated in Table 8F-52. For each setting, connect a dc voltmeter to the points indicated. (The voltmeter input impedance must be 10 MΩ or greater and neither side of the input should be grounded.)

Table 8F–52. Levels on A24Q4 and A24U3B, (√3) Step 2

Direct Control Special Functions	Voltage Limits (Vdc) at	
	A24Q4 Collector	A24U3B Pins 5 to 7
As in step 1	−15 to −11	−0.01 to +0.01
0.0FA	0.4 to 0.6 above A24TP1	−0.01 to +0.01

Hint: The voltage at pin 5 of A28XA24 should be between −4 and +5 Vdc. If the voltage across A24R2 is greater than 10 mV, A24CR1 may be leaky.

3. Key in 0.0F8 SPCL.
4. Connect an ac voltmeter to A24TP1 (TUNE).
5. Set the audio source (in the audio analyzer) to 10 kHz at 0.1 Vrms. If the output of the source is not 50Ω, put a 50Ω load in parallel with the output using a tee. Insert a 0.1 μF non-electrolytic capacitor in series with the (loaded) output. Connect the ac coupled output to the junction of A24R2 and R3 or to pin 5 of A28XA24.
6. Adjust the audio source level for a voltmeter reading of 10 mVrms.
7. Key in 0.0FA SPCL to remove the filter. The voltmeter should read between 140 and 170 mVrms.

(√4) Sampler Check

1. Disconnect W17 from A23J2 (HF VCO IN).
2. Set the signal generator to 2 MHz CW at −2 dBm. Connect its RF output to A23J1 (LF VCXO IN).
3. Check the collector (can) of A23Q2 with a dc coupled oscilloscope. The oscilloscope input should have a low-capacitance, 10:1 divider probe. The signal should be at the signal generator's frequency with the waveform shown in Figure 8F-29.
4. Check the emitter of Q6 with the oscilloscope. The waveform should be as shown in Figure 8F-30.

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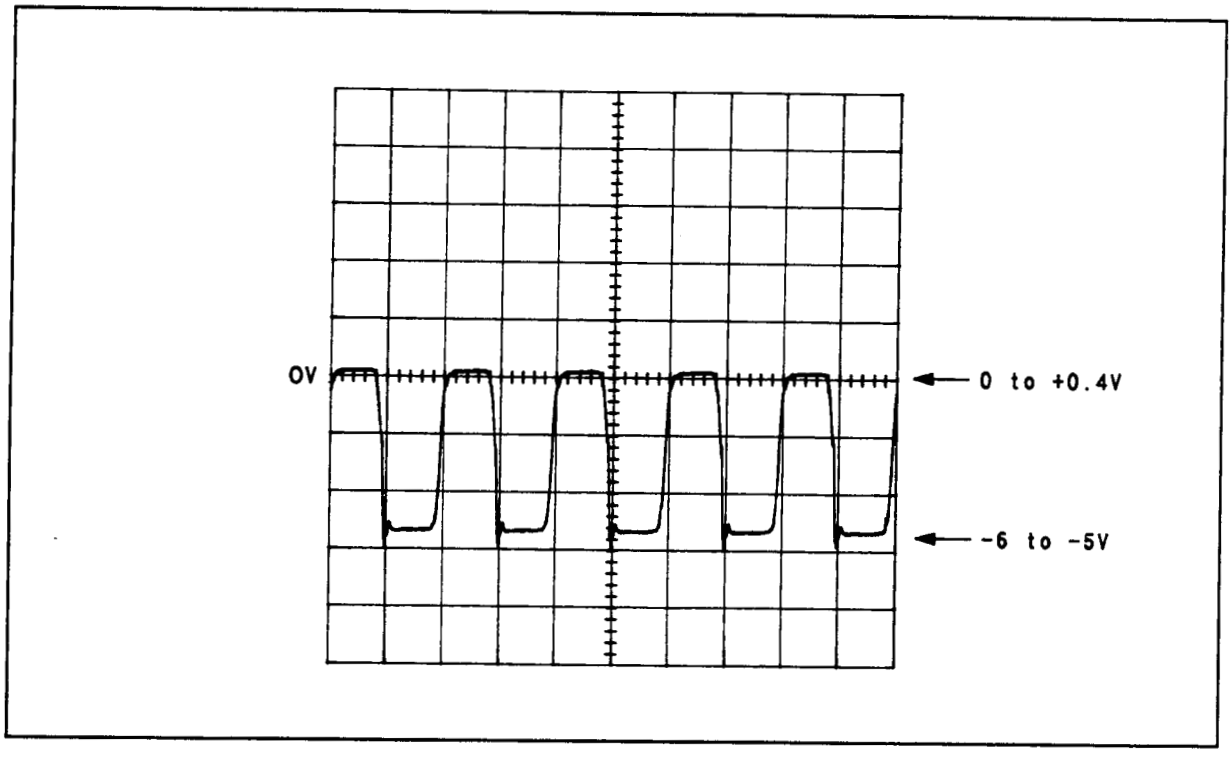


Figure 8F–29. *Waveform for* ⟨√4⟩ *Step 3*

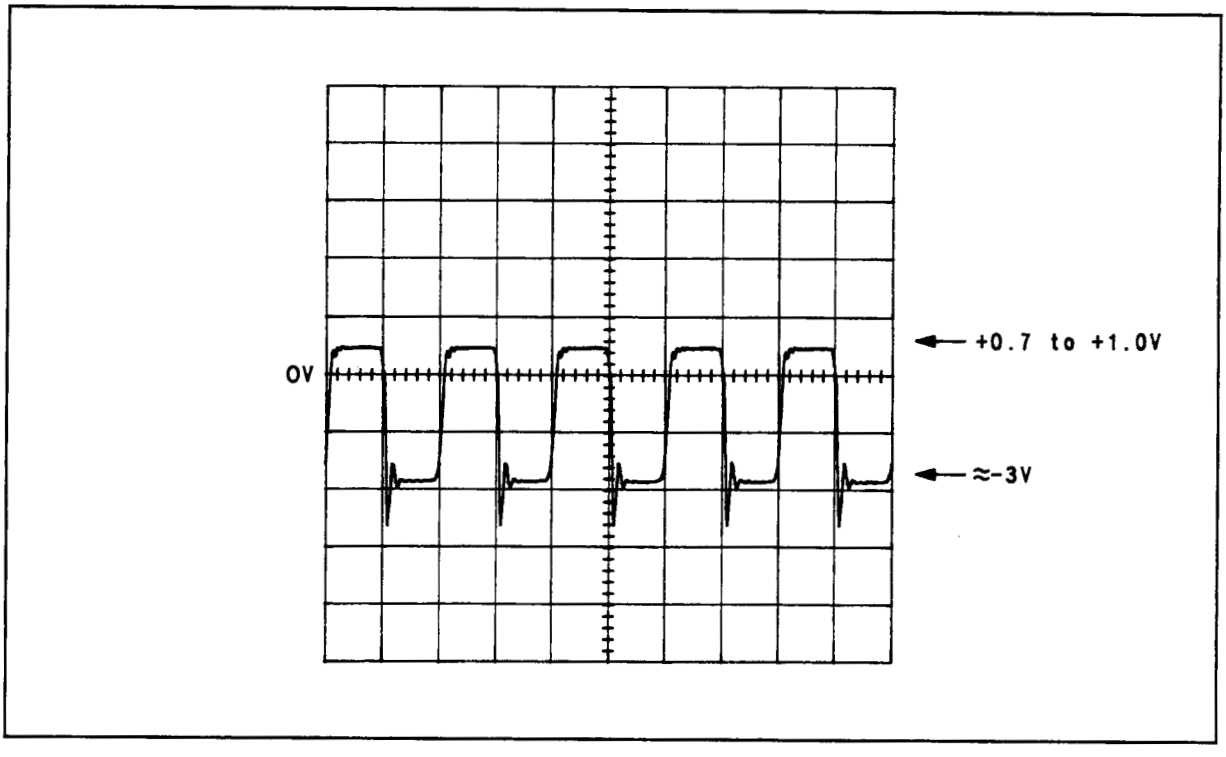


Figure 8F–30. *Waveform for* ⟨√4⟩ *Step 4*

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5. Check the junction of A23CR6, CR8, R27 with the oscilloscope. The waveform should be narrow, negative-going pulses at the signal generator frequency. The pulse width will depend on the capacitive loading of the oscilloscope but should be approximately 15 ns.
6. Check the junction of A23CR7, CR9, and R28 with the oscilloscope. The waveform should be as in step 5 except that the pulses will be positive going.
7. Connect a dc coupled oscilloscope to A23TP1 (SAMP AMPL).
8. Slowly vary A23R34 (OFS) through its range. The voltage should vary smoothly over the minimum range of −1 to +1V.

   Hint: If the voltage at A23TP1 jumps rapidly through OV as adjustment is made, the Sampling Bridge is probably not being gated on by the Impulse Generator. If the voltage doesn't adjust at all, the Sampler Amplifier may be at fault.
9. After the repair has been completed, perform *Adjustment 4—Sampler Efficiency and Offset.* For this adjustment, the Sampler Assembly must be inserted in its extrusion.

⟨√5⟩ Bandwidth and Loop Switching HF VCO Tune Integrator and Amplifier Check

1. Disconnect any signal at the INPUT connector. Connect a high-impedance, dc coupled oscilloscope to pin 9 of A28XA23.
2. Key in 0.017 SPCL to open the loops. Key in 0.0F2 SPCL to turn on the Sweep Up Current Source. The voltage should be +10.1 to +11.2 Vdc.

   Hint: The voltage at pin 8 of A28XA23 should be between −12 and −11 Vdc.
3. Key in 0.0FF SPCL to turn off the Sweep Up Current Source and turn on the Sweep Down Current Source. The voltage should be −11.2 to −10.1 Vdc.

   Hint: The voltage at pin 8 of A28XA23 should be between +1.8 and +2.2 Vdc.
4. Press AUTOMATIC OPERATION. The waveform should be as shown in Figure 8F-31.

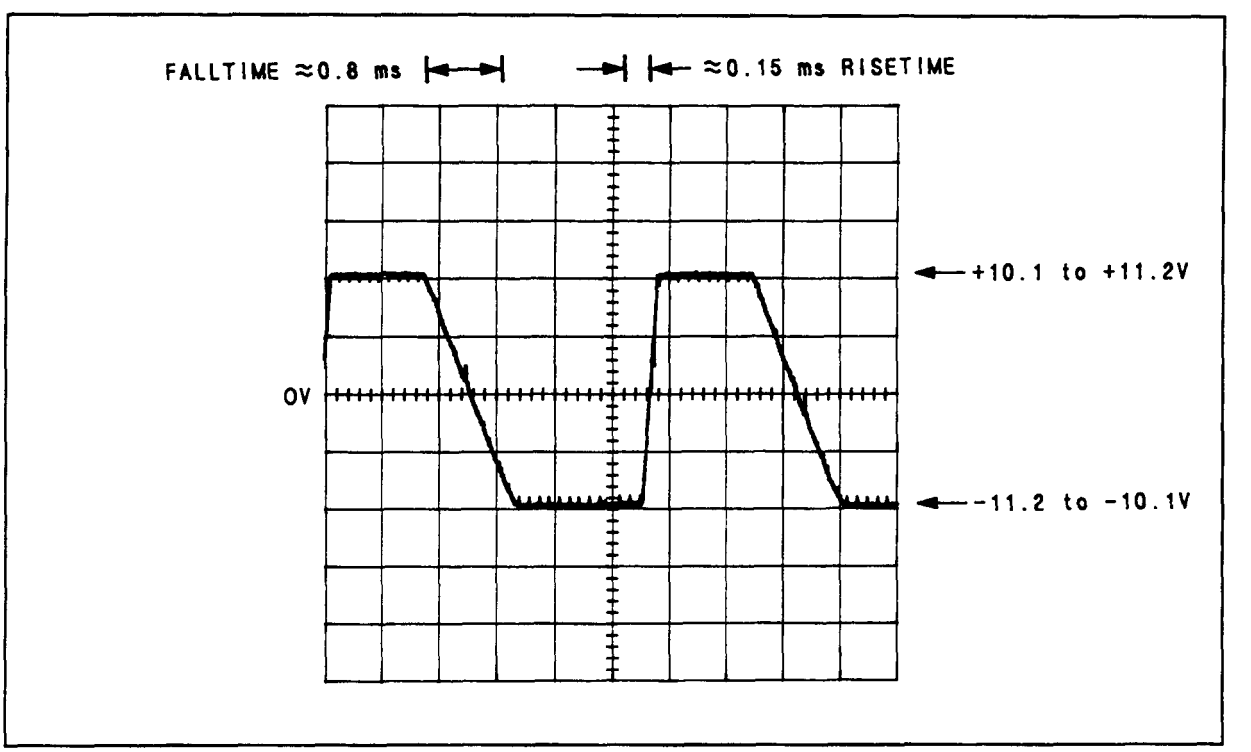


Figure 8F–31. *Waveform for* ⟨√5⟩ *Step 4*

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5. Key in the Direct Control Special Functions indicated in Table 8F-53. For each setting, make the measurements indicated with a dc voltmeter.

Table 8F-53. *Levels on A23Q11 and A23Q10,* ⟨√5⟩ *Step 5*

Direct Control Special Function	Voltage Limits (Vdc) at	
	A23Q11 Gate	A23Q10 Base
0.013	0 to +0.2	+0.3 to +0.8
0.019	−15 to −12	−0.8 to −0.5

6. Key in the Direct Control Special Functions indicated in Table 8F-54. For each setting, make the measurements indicated with a dc voltmeter.

Table 8F-54. *Levels on A23Q12 Gate,* ⟨√5⟩ *Step 6*

Direct Control Special Function	Voltage Limits (Vdc) at A23Q12 Gate
0.0FA	0 to +0.2
0.0F8	−15 to −12

⟨√6⟩ No-HF-VCO Detector and Out-of-Lock Detector Check

1. Set the signal generator to 500 MHz CW at −2 dBm. Connect its RF output to A23J2 (HF VCO IN). A23DS1 (NO HF VCO) should be off.
2. Reduce the signal level to −10 dBm. A23DS1 should be on.
3. Key in 0.0FA SPCL. A23DS2 (OUT OF LOCK) should be on.
4. Key in 0.0F8 SPCL. A23DS2 should be off.

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Service Sheet 19

ASSEMBLIES

- **A22 Low Frequency VCXO**
- **A21 Low Frequency VCXO Filter**

PRINCIPLES OF OPERATION

General—A22 Low Frequency VCXO Assembly

The output of the Low Frequency VCXO Assembly is a tuneable, but frequency-stable, 2 MHz signal used as a reference to stabilize the HF VCO. The 2 MHz signal is obtained by mixing the outputs of two higher frequency, voltage controlled crystal oscillators (VCXOs), one at a nominal 9.26 MHz, the other at 11.26 MHz. The oscillators tune in opposite directions. The resultant difference frequency from the mixer is a 2 MHz signal with a tuning range of ±6.25 kHz. This tuning scheme permits a wide tuning range (at least for a crystal oscillator) and yet retains the high stability inherent in a crystal source. On the other hand, great care must be taken to filter out spurious mixing products, which can create residual FM tones on the LO.

9.26 and 11.26 MHz Crystal Oscillators

The two crystal oscillators are similar in design. The 9.26 MHz oscillator will be discussed here in detail. L2, C15, and C16 shift the phase at the collector of Q8 by 180°. The divider formed by R17 and the resistance of CR1 and CR5 routes the in-phase signal (positive feedback) to the base of Q8 to reinforce oscillation. L1 is an RF choke which biases the collector of Q8.

The emitter of Q8 contains the crystal (Y1) and a tuneable, series resonant LC circuit (L3, CR9, and CR11). The high Q circuit in the emitter of Q8 resonates near the resonant frequency of its collector circuit. Since the gain of Q8 is highest and the phase shift of the emitter is zero when the emitter circuit goes series resonant, the emitter resonator determines the frequency of oscillation. Varactor diodes CR9 and CR11 are in ac parallel and dc series. Changing the reverse bias on the diodes tunes the oscillator. Increasing the reverse bias increases the frequency. The varactor diodes (CR10 and CR12) in the emitter circuit of Q7 tune the 11.26 MHz oscillator in the direction opposite to 9.26 MHz oscillator.

The amplitude of the signal from the oscillators is stabilized in a manner that prevents the transistor from either saturating or cutting off at any time during the cycle of oscillation to maintain optimum Q and noise. The positive and negative peaks of each cycle are limited by passive diodes—CR6 limits the positive peak at the collector of Q8, CR2 limits the negative peak. In addition when the diodes conduct, C10 and C6 are charged to the value of the positive and negative peak respectively. The peak-to-peak voltage across the two capacitors then slowly leaks off through CR5 and CR1. The leakage current determines the resistance of the diodes and, hence, the amount of positive feedback to the base of Q8. The action of the peak-to-peak detector is to stabilize the amplitude of oscillation and maintain it at a level that is optimum for good noise performance.

Double Balanced Mixer

The output of the 9.26 MHz Crystal Oscillator is amplified and limited by Q5 and Q6 and drives the L (or high-level) port of the Double Balanced Mixer. T1 provides a dc return for the collectors of Q5 and Q6 and a return for the X (or broadband) port of the mixer. The output of the 11.26 MHz Crystal Oscillator drives the R (or low-level) port of the mixer through amplifier Q4. Both amplifiers minimize loading of the respective oscillators. The High-Frequency Termination (C21, L7, and R29) maintains a constant 50Ω impedance at frequencies where the 2 MHz Low-Pass Filter appears as a high impedance and provides a place for high-frequency spurious signals to dissipate.

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2 MHz Low-Pass Filter and Output Amplifier

The 2 MHz Low-Pass Filter is one of two filters that eliminate spurious mixing products from the LF VCXO. The other filter is in a separate housing (A21 Low Frequency VCXO Filter Assembly). The Output Amplifier isolates the two filters. It is a low-noise amplifier with an active input impedance created by the feedback resistor R31.

General—A21 Low Frequency VCXO Filter Assembly

The Low Frequency VCXO Filter is a 2 MHz bandpass filter. In conjunction with the 2 MHz Low-Pass Filter on the A22 Low Frequency VCXO Assembly, the filter eliminates spurious mixing products on the LF VCXO. This filter is in an isolated compartment to minimize pickup from the other assembly. The first two elements of the filter are at the output of the other assembly (A22L10 and C28).

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TROUBLESHOOTING

General

Procedures for checking the Low Frequency VCXO and Filter Assemblies are given below. The circuits to check are marked on the schematic diagram by a hexagon with a check mark and a number inside, for example, ⟨√3⟩. In addition, any points outside the labeled circuit area that must be checked are also identified. Fixed signals are also shown on the schematic inside a hexagon, for example, ⟨+1.9 TO +2.1 VDC⟩. Extend the board assembly where necessary to make measurements.

CAUTION

Tighten SMC connectors to 0.6 N·m (5 in·lb). Hand tightening of connectors is insufficient. Hand-tightened connectors can work loose and cause reduced performance or malfunctions.

Equipment

Counter ..... HP 8640B
Oscilloscope ..... HP 1740A
Voltmeter ..... HP 3455A

⟨√1⟩ Low Frequency VCXO General Check

1. Connect a dc voltmeter to A20TP3 (LF VCXO TUNE). (A20TP3 is shown on Service Sheet 14.)
2. Connect a high-impedance, ac coupled oscilloscope to A22J1 (LF VCXO OUT).
3. Key in 0.01B SPCL to connect the DAC to the LF VCXO.
4. Key in the Direct Control Special Functions indicated in Table 8F-55. For each setting, note the reading on the voltmeter and the waveform level on the oscilloscope. The waveform should be sinusoidal with a period of approximately 500 ns. The readings should be within the limits shown.

Table 8F-55. *LF VCXO Levels, ⟨√1⟩ Step 4*

Direct Control Special Functions	Limits	
	Voltmeter (Vdc)	Oscilloscope (Vpp)
0.080, 0.090, 0.0A0, and 0.0B0	0 to +2	0.36 to 0.52
0.08F, 0.09F, 0.0AF, and 0.0BF	+37 to +40	0.36 to 0.52

5. Connect a counter (in the signal generator) in place of the oscilloscope. Key in the Direct Control Special Functions indicated in Table 8F-56. For each setting, observe the frequency which should be as shown.

Table 8F-56. *Frequencies at A22J1, ⟨√1⟩ Step 5*

Direct Control Special Functions	Frequency Limits (MHz)
0.08F, 0.09F, 0.0AF, 0.0BF	2.0063 or higher
0.080, 0.090, 0.0A0, 0.0B0	1.9937 or lower

Hint: If the signal at A22J1 is not correct, but the tuning voltage is, perform the ⟨√2⟩ *9.26 and 11.26 MHz Xtal Oscillators and Double Balanced Mixer Check.*

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⟨√2⟩ 9.26 and 11.26 MHz Xtal Oscillators and Double Balanced Mixer Check

NOTE

This check assumes that the VCXO tune line works properly. See step 4 of the ⟨√1⟩ Low Frequency VCXO General Check.

1. Connect a counter (in the signal generator) to A22TP2.
2. Key in 0.01B SPCL to connect the DAC to the LF VCXO.
3. Key in the Direct Control Special Functions indicated in Table 8F-57. For each setting, note the counter reading.

Table 8F-57. *Frequencies at A22TP2,* ⟨√2⟩ *Step 3*

Direct Control Special Functions	Frequency Limits (MHz)
0.080, 0.090, 0.0A0, 0.0B0	9.2628 or higher
0.08F, 0.09F, 0.0AF, 0.0BF	9.2572 or lower

4. Connect the counter to A22TP1.
5. Key in the Direct Control Special Function indicated in Table 8F-58. For each setting, note the counter reading.

Table 8F-58. *Frequencies at A22TP1,* ⟨√2⟩ *Step 5*

Direct Control Special Functions	Frequency Limits (MHz)
0.08F, 0.09F, 0.0AF, 0.0BF	11.2637 or higher
0.080, 0.090, 0.0A0, 0.0B0	11.2563 or lower

Hint: With A22Y1 unplugged the voltage at A22TP1 should be 0.6 to 0.8 Vpp (sinusoidal) as measured with a high-impedance ac coupled oscilloscope.

⟨√3⟩ Low Frequency VCXO Filter Check

NOTE

This check assumes that the ⟨√1⟩ Low Frequency VCXO General Check *gives positive results.*

1. Connect a high-impedance, ac coupled oscilloscope either in parallel with A21J2 (LF VCXO OUT) with W13 connecting to A23J1 or directly to A21J2 with a 511Ω resistor in parallel with it. The signal should be sinusoidal with an amplitude of 0.5 to 1.0 Vpp and a period of approximately 500 ns.

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Service Sheet 20 *(2314A to 2622A)*

ASSEMBLY

- **A20 LO Control (Analog Circuits)**

NOTE

For instruments with serial prefixes 2627A and above, see the following Service Sheet 20.

PRINCIPLES OF OPERATION

General

The LO Control Assembly contains various circuits related to the tuning of the LO. The circuits include: the Digital-to-Analog Converters with associated amplifiers, the Sweep Up and Sweep Down Current Sources, and the Track Loop Amplifier. The interaction of these circuits to accomplish tuning of the LO is most easily understood by referring to the discussion for Service Sheet BD1.

Digital-to-Analog Converters

The Digital-to-Analog Converters (DACs) tune the HF VCO and the LF VCXO. U10 and U12 convert the binary code on the inputs to an output current with a magnitude proportional to the weighting of the bits. Conventional current flows in the direction indicated by the arrow in the current source of the DAC symbol. The DACs are referenced from a common Voltage Reference (Q9) through current-setting resistors R17 and R33 which have the same value. U10 and U12 thus produce equal outputs for equal digital inputs. R29, R30 and R31 form a current divider which attenuates the current from U12 before being summed with the current from U10. The weighting given to the current from U12 by the attenuator is such that a change in the most significant bit (input 128) has the same effect as a change in the second least-significant bit (input 2) of U10. Thus the outputs of the two DACs overlap by two bits.

The summed currents from the converter are routed either through switch Q18 into the LF VCXO Tune Amplifier or through switch Q13 into the DAC Control Amplifier (which tunes the HF VCO). Normally, the voltage at the output of the DACs is near ground potential but is clamped by CR8 and CR11 if an abnormal condition occurs (such as both Q18 and Q13 off).

LF VXCO Tune Amplifier and Filter

Transistors Q19 to Q24 form a transresistance amplifier which converts the negative input current from the DACs (through switch Q18) into a positive voltage which tunes the LF VCXO. Its output range is 0 to +40V. The input stage is the differential pair Q19 and Q21. Q20 is an intermediate stage. Complementary pair Q22 and Q23 is the output driver stage. Q24B is a current source which very slightly biases on Q22 and Q23 with the voltage drop across CR20. The current in Q24B is approximately equal to the current flowing in Q24A (which is a current mirror to Q24B). Q24A is connected as a diode. C14 is for frequency compensation.

The tune voltage to the LF VCXO is filtered by a 0.7 Hz low-pass filter. The filter reduces the phase noise caused by the tuning circuits and determines the response time of the LO when locked. The filter is normally not switched in until lock has been acquired. The filter consists of R68 and C18. C18 is switched in by opto-isolator switch U14. When C18 is not in, it is being pre-charged through R62 and opto-isolator switch U13 to the level present on the output node of R68. This prevents a transient on the tune voltage which would cause a frequency error with a long settling time when C18 is switched in. R64, R65, R66, and R67 simulate the bias condition of the varactor diodes which tune the LF VCXO (see Service Sheet 19), but the components are scaled down by a factor of ten because R62 is one-tenth the resistance of R68.

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DAC Control Amplifier

The DAC Control Amplifier is used during the preliminary tuning of the LO when the DAC tunes the HF VCO. During that time, both Q13 and Q11 are switched on and the DAC Control Amplifier is configured as part of a feedback loop (see Figure 8D-1). The DAC Control Amplifier consists of transresistance amplifier (Current-to-Voltage Converter) U4A and comparison amplifier (DAC-to-VCO Loop Amplifier) U4B. The negative current from the DACs generates a positive voltage at the output of U4A. In addition, R46 adds a negative offset to center the output range about 0V.

Track Loop Amplifier

The Track Loop Amplifier is used principally in the track tune mode. Track mode functions only with the 1.5 MHz IF. The amplifier receives a dc tune voltage from the FM Demodulator. The voltage is proportional to the IF frequency and is offset (as adjusted by R1) to produce a 1.5 MHz IF when the tuning error is zero. The tune voltage is buffered by U1 and attenuated by the resistor (R19 through R26) selected by demultiplexor U2. The variable attenuation compensates for the difference in LO tuning sensitivity caused by the different bands of the LO Divider. The Track Loop Amplifier couples onto the tune line via switch Q10.

Sweep Up and Sweep Down Current Sources

In the automatic signal seeking tune mode, the LO is swept down over each band. The Sweep Down Current Source supplies a current that is integrated by the HF VCO Tune Integrator and Amplifier (see Service Sheet 18) to produce a voltage ramp which tunes the HF VCO. The Sweep Up Current Source produces a quick retrace ramp.

The Sweep Down Current Source is designed to produce a constant current which can be stopped abruptly when an IF response is produced. The Stop Sweep signal comes from the IF Present Detector (see Service Sheet 9). The current source (Q7) is biased from divider R52 and R53 through buffer Q6, which also thermally compensates the base-emitter junction of Q7. When sweeping, Q4 is off. When Q4 goes on, it diverts the emitter current of Q7 and shuts Q7 off. Q5 is normally off, but when Q4 is switched on, it too is switched on momentarily by the pulse of current through C12. Q5 then discharges the capacitance on the tune line.

To retrace the sweep, Q1 is switched on. This essentially connects R77 to the −15V supply and discharges the integrating capacitor on the HF VCO Tune Integrator and Amplifier.

Power Supply Decoupling

Q26 and Q27 multiply the effect of C5 to assist in decoupling the +40V supply.

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TROUBLESHOOTING

General

Procedures for checking the LO Control Assembly are given below. The circuits to check are marked on the schematic diagram by a hexagon with a check mark and a number inside, for example, ⟨√3⟩. In addition, any points outside the labeled circuit area that must be checked are also identified. Fixed signals are also shown on the schematic inside a hexagon, for example, ⟨+1.9 TO +2.1 VDC⟩. Extend the board assembly where necessary to make measurements.

CAUTION

CMOS circuits can be damaged by static charges and circuit transients. Do not remove this assembly from the instrument while power is applied. Discharge the board, replacement device, and soldering iron to the same potential. (Use the conductive foam pad provided in the Service Accessory Kit HP 08901-60287.)

Equipment

Audio Source ..... HP 8903B
Oscilloscope ..... HP 1740A
Voltmeter ..... HP 3455A

⟨√1⟩ Sweep Down and Sweep Up Current Sources Check

1. Key in 0.01F SPCL to open the LO loops.

2. Key in the Direct Control Special Functions indicated in Table 8F-59. For each setting, check the pins indicated with a dc voltmeter or a high-impedance, dc coupled oscilloscope.

Table 8F-59. *Levels, ⟨√1⟩ Step 2*

Direct Control Special Function	Voltage Limits (Vdc) at			Condition of Base-Emitter Junction of				
	U3C-8	U3B-6	A28XA20-32	Q4	Q7	Q5	Q1	Q2
0.0FE	+4.5 to +5.4	0 to +0.8	+1.8 to +2.3	Off	On	Off	Off	Off
0.0F2	0 to +0.8	+1.2 to +1.6	−12 to −11	On	Off	Off	On	On

Hint: For this check Q10 and Q11 must be off. The voltage at the gates of Q10 and Q11 should be +11 to +15 Vdc.

3. Press AUTOMATIC OPERATION.

4. Check the voltage at the collector of Q5 with a high-impedance, dc coupled oscilloscope. The waveform should be a square wave with an amplitude of approximately 1.6 Vpp and a period of approximately 2.8 ms, but more importantly, observe the falling edge. Set the oscilloscope to trigger on a negative slope with a sweep time of 2 μs per division. The waveform will be intermittently stable and very faint but the falling edge should be as in Figure 8F-32.

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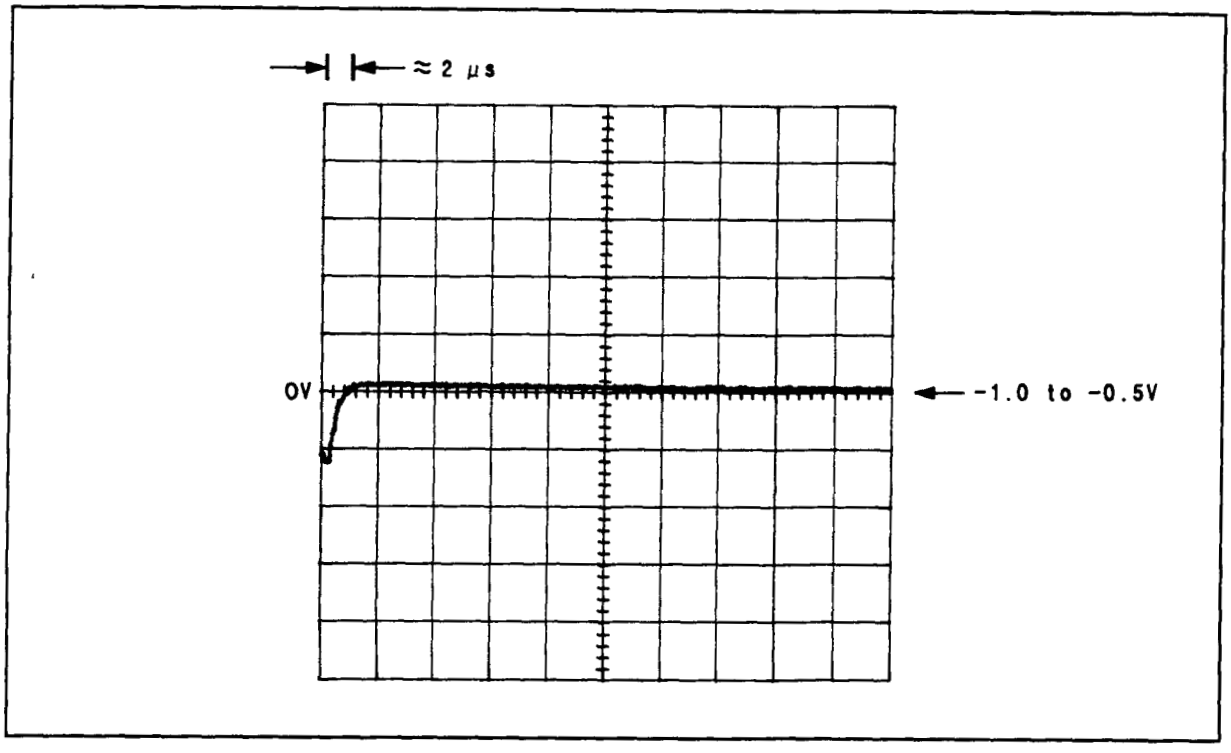


Figure 8F–32. *Waveform for* ⟨√1⟩ *Step 4*

⟨√2⟩ Digital-to-Analog Converters and DAC Control Amplifier Check

1. Key in 0.0FF SPCL to inhibit LO sweep. Key in 0.01E SPCL to connect the DAC to the HF VCO.
2. Key in the Direct Control Special Functions indicated in Table 8F-60. For each setting, measure U4B pin 6 and A20TP4 (HF VCO TUNE) with a dc voltmeter.

Table 8F–60. *Level at A20TP4,* ⟨√2⟩ *Step 2*

Direct Control Special Functions	Voltage Limits (Vdc)
0.080, 0.090, 0.0A0, 0.0B0	−10 to −8
0.08F, 0.09F, 0.0AF, 0.0BF	+9 to +12

Hint: For this check Q18 must be off and Q13 on. The gate of Q18 should be between −15.4 and −11 Vdc. The gate of Q13 should be between −0.1 and +0.02 Vdc.

Hint: If pin 6 of U4B is correct but TP4 is not, check the components in the loop formed by A20U4B, A20Q11, A23Q11, and A23U2. (See Service Sheet 12). A20Q11 must be on.

Hint: To test U4A independent of the DAC, key in 0.013 SPCL to open switch Q13, then connect a 10 kΩ resistor between the +15V supply and pin 2 of U4A. Pin 1 of U4A, pin 6 of U4B, and TP4 should be the same voltage (which should be between +4 and +7 Vdc.)

Hint: Since the output of the DAC is a current source, it is difficult to test the DAC independent of the DAC Control Amplifier (which is a transconductance amplifier).

3. Key in 55.0 SPCL to cause the LO to sweep slowly back and forth across its range. The voltage at TP4 should sweep slowly between the limits given in step 2.

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⟨√3⟩ LF VCXO Tune Amplifier and LF VCXO Tune Filter Check

NOTE

This check assumes that the ⟨√2⟩ Digital-to-Analog Converter and DAC Control Amplifier Check *gives positive results.*

1. Key in the Direct Control Special Functions indicated in Table 8F-61. For each setting, measure the dc resistance indicated.

Table 8F-61. *Resistances,* ⟨√3⟩ *Step 1*

Direct Control Special Functions	Resistance (Ω) Between	
	U13 Pins 2 and 3	U14 Pins 2 and 3
0.0FA	<600	>10 000
0.0F8	>10 000	<600

Hint: When U13 is low resistance, the voltage across R69 should be between 3 and 7 Vdc; when high, the voltage should be between 0 and 50 mVdc. When U14 is low resistance, the voltage across R74 should be between 11 and 14 Vdc; when high, the voltage should be between 0 and 50 mVdc.

2. Connect a dc voltmeter to A20TP3 (LF VCXO TUNE).
3. Key in 0.01B SPCL to connect the DAC to the LF VCXO.
4. Key in the Direct Control Special Functions indicated in Table 8F-62. For each setting, note the reading on the voltmeter.

Table 8F-62. *Level at A20TP3,* ⟨√3⟩ *Step 4*

Direct Control Special Functions	Voltage Limits (Vdc)
0.080, 0.090, 0.0A0, 0.0B0	0 to +2
0.08F, 0.09F, 0.0AF, 0.0BF	+37 to +40

Hint: For this check, Q18 must be on and Q13 off. The gate of Q18 should be between −0.02 and +0.1 Vdc. The gate of Q13 should be between −15.4 and −14.0 Vdc.

⟨√4⟩ Track Loop Amplifier Check

1. Key in 0.01D SPCL to switch on the track loop.
2. Check pin 14 of U5D with a dc voltmeter. The voltage should be between −15.4 and −11 Vdc.
3. Check Q10. The gate-to-source voltage should be between −0.02 and 0 Vdc.
4. Turn the instrument to STBY. Unplug A4 FM Demodulator Assembly. Turn the instrument back to ON.
5. Key in 0.0FF SPCL to inhibit LO sweep. Key in 0.01D SPCL.
6. Set the audio source to 1 kHz at 0.5 Vrms. Connect its output to pin 3 of A28XA20.
7. Connect a high-impedance, ac coupled oscilloscope to pin 3 of A28XA20.
8. Fine adjust the audio source level for 2 Vpp as read on the oscilloscope.
9. Connect the oscilloscope to the source of FET Q10.
10. Key in the Direct Control Functions indicated in Table 8F-63. For each setting, the oscilloscope should read as indicated.

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Table 8F-63. *Level at Q10,* ⟨√4⟩ *Step 10*

Direct Control Special Function	Voltage Limits (mVpp)	Resistor Selected
0.004	600 to 880	R22
0.005	300 to 440	R21
0.006	150 to 220	R20
0.007	75 to 110	R19
0.008	38 to 58	R26
0.009	19 to 28	R25
0.00A	10 to 14	R24
0.00B	1200 to 1760	R23

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Service Sheet 20 *(2627A and Above)*

ASSEMBLY

- **A20 LO Control (Analog Circuits)**

NOTE

For instruments with serial prefixes between 2314A and 2622A, see the previous Service Sheet 20.

PRINCIPLES OF OPERATION

General

The LO Control Assembly contains various circuits related to the tuning of the LO. The circuits include: the Digital-to-Analog Converters with associated amplifiers, the Sweep Up and Sweep Down Current Sources, and the Track Loop Amplifier. The interaction of these circuits to accomplish tuning of the LO is most easily understood by referring to the discussion for Service Sheet BD1.

Digital-to-Analog Converters

The Digital-to-Analog Converters (DACs) tune the HF VCO and the LF VCXO. U10 and U12 convert the binary code on the inputs to an output current with a magnitude proportional to the weighting of the bits. Conventional current flows in the direction indicated by the arrow in the current source of the DAC symbol. The DACs are referenced from a common Voltage Reference (U5A) through voltage divider resistors R7 and R8 which have the same value. U10 and U12 thus produce equal outputs for equal digital inputs. R29, R30 and R31 form a current divider which attenuates the current from U12 before being summed with the current from U10. The weighting given to the current from U12 by the attenuator is such that a change in the most significant bit (input 128) has the same effect as a change in the second least-significant bit (input 2) of U10. Thus the outputs of the two DACs overlap by two bits.

The summed currents from the converter are routed either through switch U14D into the LF VCXO Tune Amplifier or through switch U14A into the DAC Control Amplifier (which tunes the HF VCO). Normally, the voltage at the output of the DACs is near ground potential but is clamped by CR6 and CR7 if an abnormal condition occurs (such as both U14A and U14D off).

LF VXCO Tune Amplifier and Filter

Transistors Q19 to Q24 form a transresistance amplifier which converts the negative input current from the DACs (through switch U14D) into a positive voltage which tunes the LF VCXO. Its output range is 0 to +40V. The input stage is the differential pair Q19A and Q19B. Q20 and Q21 form an intermediate differential stage. Complementary pair Q22 and Q23 is the output driver stage. Q24B is a current source which very slightly biases on Q22 and Q23 with the voltage drop across CR20. The current in Q24B is approximately equal to the current flowing in Q24A (which is a current mirror to Q24B). Q24A is connected as a diode. C14 is for frequency compensation.

The tune voltage to the LF VCXO is filtered by an automatic-switching 340/34 Hz low-pass filter. The 34 Hz filter (with a bandwidth determined by R74, R73, and C18) reduces the phase noise caused by the tuning circuits and determines the response time of the LO when locked; the 340 Hz filter (R73 and C18) determines the tuning speed when unlocked. When the LF VCXO is locked (not tuning), no current flows through R74 to turn Q12 or Q13 on. When the DAC tunes the LF VCXO (in either direction), enough current flows through R74 to turn Q12 or Q13 on, and, in effect bypasses R74.

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DAC Control Amplifier

The DAC Control Amplifier is used during the preliminary tuning of the LO when the DAC tunes the HF VCO. During that time, both U14A and U23D are switched on and the DAC Control Amplifier is configured as part of a feedback loop (see Figure 8D-1). The DAC Control Amplifier consists of transresistance amplifier (Current-to-Voltage Converter) U4A and comparison amplifier (DAC-to-VCO Loop Amplifier) U4B. The negative current from the DACs generates a positive voltage at the output of U4A. In addition, R46 adds a negative offset to center the output range about 0V.

Track Loop Amplifier

The Track Loop Amplifier is used principally in the track tune mode. Track mode functions only with the 1.5 MHz IF. The amplifier receives a dc tune voltage from the FM Demodulator. The voltage is proportional to the IF frequency and is offset (as adjusted by R1) to produce a 1.5 MHz IF when the tuning error is zero.

LED's DS3 and DS4 act as 1.3V limiter diodes to reduce the effects of tuning transients and no-signal conditions on the tuning circuits. FET Q9 is non-functional (always off).

The tune voltage is buffered by U1 and attenuated by the resistor (R19 through R26) selected by demultiplexor U2. The variable attenuation compensates for the difference in LO tuning sensitivity caused by the different bands of the LO Divider. The Track Loop Amplifier couples onto the tune line via switch U23.

Sweep Up and Sweep Down Current Sources

In the automatic signal seeking tune mode, the LO is swept down over each band. The Sweep Down Current Source supplies a current that is integrated by the HF VCO Tune Integrator and Amplifier (see Service Sheet 18) to produce a voltage ramp which tunes the HF VCO. The Sweep Up Current Source produces a quick retrace ramp.

The Sweep Down Current Source is designed to produce a constant current which can be stopped abruptly when an IF response is produced. The Stop Sweep signal comes from the IF Present Detector (see Service Sheet 9). The current source (Q7) is biased from divider R52 and R37B in parallel with R37C through buffer Q6, which also thermally compensates the base-emitter junction of Q7. When sweeping, Q4 is off. When Q4 goes on, it diverts the emitter current of Q7 and shuts Q7 off. Q5 is normally off, but when Q4 is switched on, it too is switched on momentarily by the pulse of current through C12. Q5 then discharges the capacitance on the tune line.

To retrace the sweep, Q1 is switched on. This essentially connects R71 to the −15V supply and discharges the integrating capacitor on the HF VCO Tune Integrator and Amplifier.

Power Supply Decoupling

Q26, Q27, and U5B regulate the +40V supply and drastically reduce supply noise coupling onto the LO tune lines. Q26 is the series-pass regulator; Q27 is its driver. The supply's reference is the +40V (actually, +42V) input divided by the voltage divider R6 and the series combination of R7 and R8. The +40V output, divided by R10 and the series combination of R9 and R14, is compared to the reference by U5B, which drives Q27. C5 filters the supply's reference; C6 widens the bandwidth of the regulator.

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TROUBLESHOOTING

General

Procedures for checking the LO Control Assembly are given below. The circuits to check are marked on the schematic diagram by a hexagon with a check mark and a number inside, for example, ⟨√3⟩. In addition, any points outside the labeled circuit area that must be checked are also identified. Fixed signals are also shown on the schematic inside a hexagon, for example, ⟨+1.9 TO +2.1 VDC⟩. Extend the board assembly where necessary to make measurements.

CAUTION

CMOS circuits can be damaged by static charges and circuit transients. Do not remove this assembly from the instrument while power is applied. Discharge the board, replacement device, and soldering iron to the same potential. (Use the conductive foam pad provided in the Service Accessory Kit HP 08901-60287.)

Equipment

Audio Source ..... HP 8903B
Oscilloscope ..... HP 1740A
Voltmeter ..... HP 3455A

⟨√1⟩ Sweep Down and Sweep Up Current Sources Check

1. Key in 0.01F SPCL to open the LO loops.

2. Key in the Direct Control Special Functions indicated in Table 8F-64. For each setting, check the pins indicated with a dc voltmeter or a high-impedance, dc coupled oscilloscope.

Table 8F-64. *Levels, ⟨√1⟩ Step 2*

Direct Control Special Function	Voltage Limits (Vdc) at			Condition of Base-Emitter Junction of				
	U3C-8	U3B-6	A28XA20-32	Q4	Q7	Q5	Q1	Q2
0.0FE	+4.5 to +5.4	0 to +0.8	+1.8 to +2.3	Off	On	Off	Off	Off
0.0F2	0 to +0.8	+1.2 to +1.6	−12 to −11	On	Off	Off	On	On

Hint: For this check U23A and U23D must be off. The control inputs should be TTL highs.

3. Press AUTOMATIC OPERATION.

4. Check the voltage at the collector of Q5 with a high-impedance, dc coupled oscilloscope. The waveform should be a square wave with an amplitude of approximately 1.6 Vpp and a period of approximately 2.8 ms, but more importantly, observe the falling edge. Set the oscilloscope to trigger on a negative slope with a sweep time of 2 μs per division. The waveform will be intermittently stable and very faint but the falling edge should be as in Figure 8F-32.

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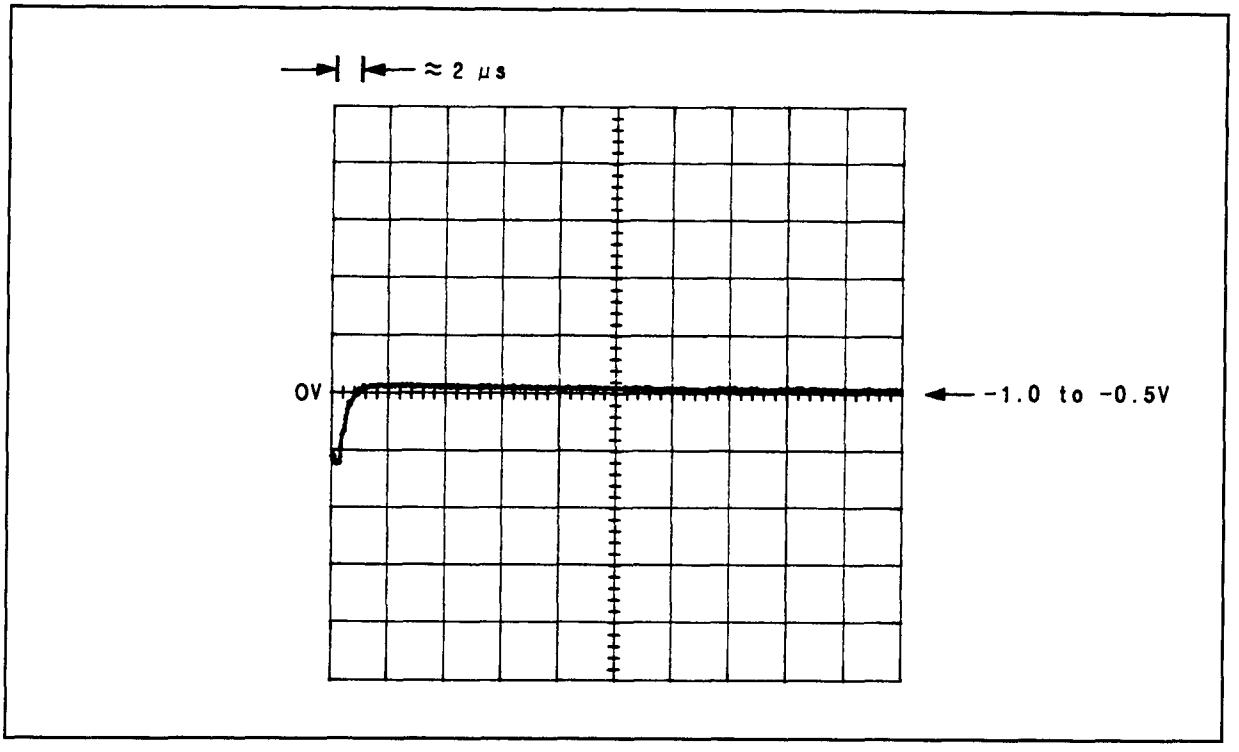


Figure 8F–32. *Waveform for* ⟨√1⟩ *Step 4*

⟨√2⟩ Digital-to-Analog Converters and DAC Control Amplifier Check

1. Key in 0.0FF SPCL to inhibit LO sweep. Key in 0.01E SPCL to connect the DAC to the HF VCO.
2. Key in the Direct Control Special Functions indicated in Table 8F-65. For each setting, measure U4B pin 6 and A20TP4 (HF VCO TUNE) with a dc voltmeter.

Table 8F–65. *Level at A20TP4,* ⟨√2⟩ *Step 2*

Direct Control Special Functions	Voltage Limits (Vdc)
0.080, 0.090, 0.0A0, 0.0B0	−10 to −8
0.08F, 0.09F, 0.0AF, 0.0BF	+9 to +12

Hint: For this check U14D must be off and U14A on. The control input of U14D should be a TTL high. The control input of U14A should be a TTL low.

Hint: If pin 6 of U4B is correct but TP4 is not, check the components in the loop formed by A20U4B, A20U23D, A23Q11, and A23U2. (See Service Sheet 12). A20U23D must be on.

Hint: To test U4A independent of the DAC, key in 0.013 SPCL to open switch U14A, then connect a 10 kΩ resistor between the +15V supply and pin 2 of U4A. Pin 1 of U4A, pin 6 of U4B, and TP4 should be the same voltage (which should be between +4 and +7 Vdc.)

Hint: Since the output of the DAC is a current source, it is difficult to test the DAC independent of the DAC Control Amplifier (which is a transconductance amplifier).

3. Key in 55.0 SPCL to cause the LO to sweep slowly back and forth across its range. The voltage at TP4 should sweep slowly between the limits given in step 2.

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⟨√3⟩ LF VCXO Tune Amplifier and LF VCXO Tune Filter Check

NOTE

This check assumes that the ⟨√2⟩ Digital-to-Analog Converter and DAC Control Amplifier Check *gives positive results.*

1. Connect one channel of a high-impedance, ac coupled oscilloscope to the emitter of Q22 or Q23. Connect the other channel to A20TP3 (LF VCXO TUNE).
2. Key in 0.01B SPCL to connect the DAC to the LF VCXO. Key in 0.080 SPCL, 0.090 SPCL, 0.0A0 SPCL, and 0.0B0 SPCL to set the DAC to its lowest state.
3. Key in 0.08F, then observe the two waveforms on the oscilloscope while pressing SPCL. This causes the DAC to increment a large part of its range. The waveform at TP3 should not noticeably lag the waveform at Q22. Both waveforms should rise to 39 to 41 Vdc.

   Hint: See the hint for step 4.

   Hint: For this check U14A must be off and U14D on. The control input of U14A should be a TTL high. The control input of U14D should be a TTL low.
4. Key in 0.080 and again observe the two waveforms on the oscilloscope while pressing SPCL. This causes the DAC to decrement back. The waveforms should fall together. The voltage at Q22 should be between 2 and 3 Vdc; the voltage at TP3 should be approximately 0.5 Vdc higher.

   Hint: Repeat steps 3 and 4 as needed to check for waveform lag. A noticeable lag in either direction indicates that Q12 (increasing) or Q13 (decreasing) is faulty.

⟨√4⟩ Track Loop Amplifier Check

1. Turn the instrument to STBY. Unplug A4 FM Demodulator Assembly. Turn the instrument back to ON.
2. Key in 0.0FF SPCL to inhibit LO sweep. Key in 0.01D SPCL to switch on the track loop.
3. Set the audio source to 100 Hz at 0.5 Vrms. Connect its output to pin 3 of A28XA20.
4. Connect a high-impedance, ac coupled oscilloscope to pin 3 of A28XA20.
5. Fine adjust the audio source level for 2 Vpp as read on the oscilloscope.
6. Connect the oscilloscope to pin 6 of U23A.
7. Key in the Direct Control Functions indicated in Table 8F-66. For each setting, the oscilloscope should read as indicated.

Table 8F-66. *Level at U23A,* ⟨√4⟩ *Step 7*

Direct Control Special Function	Voltage Limits (mVpp)	Resistor Selected
0.004	230 to 270	R22
0.005	120 to 140	R21
0.006	50 to 70	R20
0.007	25 to 35	R19
0.008	12 to 17	R26
0.009	5 to 9	R25
0.00A	2 to 4	R24
0.00B	460 to 520	R23

Hint: U23A should be closed (a TTL high on pin 8). The load on the output of U23A is A23R52 (see Service Sheet 18).

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⟨5⟩ +40V Regulator Check

1. Check the bias voltages shown on the schematic diagram.

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Service Sheet 21 *(2314A to 2622A)*

ASSEMBLY

- **A20 LO Control (Digital Circuits)**

NOTE

For instruments with serial prefixes 2627A and above, see the following Service Sheet 21.

PRINCIPLES OF OPERATION

General

The LO Control Assembly contains the Instrument Bus decoders and latches for the entire RF Section. The enable code for the section is $e = 1$. For a general discussion of the operation and decoding of the Instrument Bus, see *Instrument Bus* in Service Sheet BD5. The Overpower Protect Status is read back on the Instrument Bus via Q16. CR26 prevents Q16 from becoming an active transistor in an inverted mode (that is, the roles of collector and emitter are reversed) when the emitter is high and the collector is low. For a discussion of the readback operation, see *Direct Control Special Functions,* paragraph 8-7. An overpower condition resets register U15 which opens the Overpower Relay (see Service Sheet 4), since the OVERPOWER (H) line goes high, and switches in maximum input attenuation. This is done without intervention of the Controller. Since the Overpower Detector follows the Overpower Relay, the overpower condition is removed immediately after U15 is reset. U15 remains reset until the Instrument Bus sends out the code $esd = 0.04d$, where data bit $d3 = 0$ (that is, d3(H) is low) provided that the overpower condition does not reset U15 again. U23A permits the Instrument Bus to either close the Overpower Relay or leave it in its present state, but not to open the relay. Q28 and CR27 enable the Controller to readback the status the RF Amplifier, that is, whether it is in or not. (The RF Amplifier is chassis part U1. See Service Sheet 4.) Readback operation in similar to Q16 and CR26.

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TROUBLESHOOTING

General

Procedures for checking the LO Control Assembly are given below. The circuits to check are marked on the schematic diagram by a hexagon with a check mark and a number inside, for example, ⟨√3⟩. In addition, any points outside the labeled circuit area that must be checked are also identified. Fixed signals also are shown on the schematic inside a hexagon, for example, ⟨+1.9 TO +2.1 VDC⟩. Extend the board assembly where necessary to make measurements.

CAUTION

CMOS circuits can be damaged by static charges and circuit transients. Do not remove this assembly from the instrument while power is applied. Discharge the board, replacement device, and soldering iron to the same potential. (Use the conductive foam pad provided in the Service Accessory Kit HP 08901-60287.)

Equipment

Oscilloscope ..... HP 1740A
Voltmeter ..... HP 3455A

⟨√1⟩ Decoders and Latches General Check

1. Key in the Direct Control Special Functions indicated in Table 8F-67. For each setting, check the pins indicated with a dc voltmeter or a high-impedance, dc coupled oscilloscope. The Direct Control Special Functions are in the form 0.0sd. "s" is given in the table. Key in 0.0s0 SPCL first; a TTL low should be on the pins. Then key in 0.0sF; a TTL high should be on the pins. Furthermore, the pins should remain at their last state when any other IC is being addressed by the Direct Control Special Function.

   Example: Key in 0.000 SPCL. Pins 16, 15, 10, and 9 of U17 should all read a TTL low. Key in 0.00F SPCL. The pins should all be high. Key in 0.010 SPCL. The same pins should remain high.

Table 8F-67. *ICs, ⟨√1⟩ Step 1*

Direct Control Special Function	IC	Pins to Check
0.00d	U17	16, 15, 10, 9
0.01d	U18	16, 15, 10, 9
0.02d	U16	10, 9
0.03d	U16	16, 15
0.08d	U19	16, 15, 10, 9
0.09d	U20	16, 15, 10, 9
0.0Ad	U21	16, 15, 10, 9
0.0Bd	U22	16, 15, 10, 9
0.0Fd	U7	15, 10, 9

2. Key in 0.010 SPCL. Check pin 7 of U5B. It should be between +12 and +15 Vdc.
3. Key in 0.018 SPCL. Pin 7 of U5B should now be between −15 and −12 Vdc.

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⟨√2⟩ Overpower and Attenuator Control Latch and Amplifier Status Readback Check

1. Check that pin 1 of U15 is not a TTL low.
2. Key in 0.040 SPCL. Check pins 3 and 6 of U15 with a dc voltmeter or a high-impedance, dc coupled oscilloscope. The pins should be TTL high. Pin 14 of U15 should be a TTL low.
3. Key in 0.04F SPCL. Check pins 3, 6, and 14 of U15. The pins should all be TTL low.
4. Momentarily, short pin 1 of U15 to ground. Check pins 3, 6, and 11 of U15. The pins should all go TTL high while pin 1 is grounded but return low when the short on pin 1 has been removed. (U15 does not remain reset because pin 9 is constantly being pulsed.)
5. Key in 0.050 SPCL to enable the Overpower Protect Status read-back transistor Q16. Check the collector of Q16 with a high-impedance, dc coupled oscilloscope. The collector of Q16 should be a steady high. The display should show 000000.0000.
6. Momentarily short pin 1 of U15. The waveform at the collector of Q16 should be a train of short, low-going TTL pulses with a period of approximately 7 ms. The pulses should remain unchanged when pin 1 is ungrounded. Also, the display should go from 000000.0000 to 000001.0000 when pin 1 of U15 is grounded and remain 000001.0000 when pin 1 is ungrounded.
7. Key in 1.8 SPCL to insert the RF Amplifier into the signal path. Key in 0.060 SPCL to enable the Amplifier Status read-back transistor Q28. Check the collector of Q28 with a high-impedance, dc coupled oscilloscope. The collector of Q28 should be a steady high. The display should show 000000.0000.
8. Key in 1.8 SPCL to remove the RF Amplifier. Key in 0.060 SPCL again. The waveform at the collector of Q28 should be a train of short, low-going TTL pulses with a period of approximately 7 ms. The display should show 000001.0000.

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Service Sheet 21 *(2627A and above)*

ASSEMBLY

- **A20 LO Control (Digital Circuits)**

NOTE

For instruments with serial prefixes between 2314A and 2622A, see the previous Service Sheet 21.

PRINCIPLES OF OPERATION

General

The LO Control Assembly contains the Instrument Bus decoders and latches for the entire RF Section. The enable code for the section is $e = 1$. For a general discussion of the operation and decoding of the Instrument Bus, see *Instrument Bus* in Service Sheet BD5. The Overpower Protect Status is read back on the Instrument Bus via Q16. CR10 prevents Q16 from becoming an active transistor in an inverted mode (that is, the roles of collector and emitter are reversed) when the emitter is high and the collector is low. For a discussion of the readback operation, see *Direct Control Special Functions,* paragraph 8-7. An overpower condition resets register U15 which opens the Overpower Relay (see Service Sheet 4), since the OVERPOWER (H) line goes high, and switches in maximum input attenuation. This is done without intervention of the Controller. Since the Overpower Detector follows the Overpower Relay, the overpower condition is removed immediately after U15 is reset. U15 remains reset until the Instrument Bus sends out the code $esd = 0.04d$, where data bit $d3 = 0$ (that is, d3(H) is low) provided that the overpower condition does not reset U15 again. U3A permits the Instrument Bus to either close the Overpower Relay or leave it in its present state, but not to open the relay. Q28 and CR11 enable the Controller to readback the status the RF Amplifier, that is, whether it is in or not. (The RF Amplifier is chassis part U1. See Service Sheet 4.) Readback operation in similar to Q16 and CR10.

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TROUBLESHOOTING

General

Procedures for checking the LO Control Assembly are given below. The circuits to check are marked on the schematic diagram by a hexagon with a check mark and a number inside, for example, ⟨√3⟩. In addition, any points outside the labeled circuit area that must be checked are also identified. Fixed signals also are shown on the schematic inside a hexagon, for example, ⟨+1.9 TO +2.1 VDC⟩. Extend the board assembly where necessary to make measurements.

CAUTION

CMOS circuits can be damaged by static charges and circuit transients. Do not remove this assembly from the instrument while power is applied. Discharge the board, replacement device, and soldering iron to the same potential. (Use the conductive foam pad provided in the Service Accessory Kit HP 08901-60287.)

Equipment

Oscilloscope ..... HP 1740A
Voltmeter ..... HP 3455A

⟨√1⟩ Decoders and Latches General Check

1. Key in the Direct Control Special Functions indicated in Table 8F-68. For each setting, check the pins indicated with a dc voltmeter or a high-impedance, dc coupled oscilloscope. The Direct Control Special Functions are in the form 0.0sd. "s" is given in the table. Key in 0.0s0 SPCL first; a TTL low should be on the pins. Then key in 0.0sF; a TTL high should be on the pins. Furthermore, the pins should remain at their last state when any other IC is being addressed by the Direct Control Special Function.

   Example: Key in 0.000 SPCL. Pins 16, 15, 10, and 9 of U17 should all read a TTL low. Key in 0.00F SPCL. The pins should all be high. Key in 0.010 SPCL. The same pins should remain high.

Table 8F-68. *ICs,* ⟨√1⟩ *Step 1*

Direct Control Special Function	IC	Pins to Check
0.00d	U17	16, 15, 10, 9
0.01d	U18*	16, 15, 10, 9
0.02d	U16	10, 9
0.03d	U16	16, 15
0.07d	U13**	15, 10, 7
0.08d	U19	16, 15, 10, 9
0.09d	U20	16, 15, 10, 9
0.0Ad	U21	16, 15, 10, 9
0.0Bd	U22	16, 15, 10, 9
0.0Fd	U7	15, 10, 7

* Pins 11 and 8 should be the complement of pins 10 and 9 respectively.
** See schematic for Service Sheet 20 ***(2627A and Above)***.

2. Key in 0.010 SPCL. Connect the voltmeter or oscilloscope the pin 31 of A28XA20 (or the junction of R75 and R76). The reading should be between +14 and +15 Vdc.
3. Key in 0.018 SPCL. The reading should now be between −15 and −14 Vdc.

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⟨√2⟩ Overpower and Attenuator Control Latch and Amplifier Status Readback Check

1. Check that pin 1 of U15 is not a TTL low.
2. Key in 0.040 SPCL. Check pins 3 and 6 of U15 with a dc voltmeter or a high-impedance, dc coupled oscilloscope. The pins should be TTL high. Pin 14 of U15 should be a TTL low.
3. Key in 0.04F SPCL. Check pins 3, 6, and 14 of U15. The pins should all be TTL low.
4. Momentarily, short pin 1 of U15 to ground. Check pins 3, 6, and 11 of U15. The pins should all go TTL high while pin 1 is grounded but return low when the short on pin 1 has been removed. (U15 does not remain reset because pin 9 is constantly being pulsed.)
5. Key in 0.050 SPCL to enable the Overpower Protect Status read-back transistor Q16. Check the collector of Q16 with a high-impedance, dc coupled oscilloscope. The collector of Q16 should be a steady high. The display should show 000000.0000.
6. Momentarily short pin 1 of U15. The waveform at the collector of Q16 should be a train of short, low-going TTL pulses with a period of approximately 7 ms. The pulses should remain unchanged when pin 1 is ungrounded. Also, the display should go from 000000.0000 to 000001.0000 when pin 1 of U15 is grounded and remain 000001.0000 when pin 1 is ungrounded.
7. Key in 1.8 SPCL to insert the RF Amplifier into the signal path. Key in 0.060 SPCL to enable the Amplifier Status read-back transistor Q28. Check the collector of Q28 with a high-impedance, dc coupled oscilloscope. The collector of Q28 should be a steady high. The display should show 000000.0000.
8. Key in 1.8 SPCL to remove the RF Amplifier. Key in 0.060 SPCL again. The waveform at the collector of Q28 should be a train of short, low-going TTL pulses with a period of approximately 7 ms. The display should show 000001.0000.

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Service Sheet 22

ASSEMBLY

- **A11 Counter (Time Base Circuits)**

PRINCIPLES OF OPERATION

General

The Counter Assembly contains the 10 MHz Time Base Reference Oscillator (except for Option 002), the Time Base Select Switch, and the Time Base Dividers. The circuits provide a 2 MHz signal for the Controller clock, a 6.25 kHz signal for the Counter time base, and (for Option 002 only) a 10 MHz external time base output.

10 MHz Time Base Reference Oscillator and ECL-to-TTL-Level Translator

Except for instruments with Option 002, the clock and time base signals are derived from the 10 MHz Time Base Reference Oscillator. The ECL complementary OR gate (U2A) is used as the active device for the oscillator. The OR output of U2A is fed back to one input through the 10 MHz crystal (Y1). R12D holds the other input low. The circuit oscillates at the frequency at which the phase shift through the feedback path is zero (namely, the series resonant frequency of Y1) to produce positive feedback. The resonant frequency can be adjusted slightly with C14. C17 and L2 form a parallel resonant circuit in the negative-feedback path which biases the input in the active region and prevents oscillation at harmonics of the crystal. C15 supplies a return path for ac currents; it is chosen to provide a low reactance under all operating conditions.

For instruments with Option 002, Y1 is not present and U2A acts as a buffer for the 10 MHz signal which comes from the high-stability, reference oscillator (see Service Sheet 31).

The time base reference is buffered by U2B and converted to logic levels which are compatible with TTL by Q4 and Q3. For instruments with Option 002, the output from Q3 is available at the rear-panel TIME BASE 10 MHz OUTPUT connector.

External Time Base Buffer and Time Base Select Switch

The Time Base Select Switch senses when a reference signal has been applied to the rear-panel TIME BASE 10 MHz INPUT connector and switches the reference over. The external reference is buffered and converted into sharp-transition, TTL-compatible pulses by the External Time Base Buffer. CR1 and CR2 are input protection diodes. R20 normally pulls the input to U4F high. When an external reference is present, C26 is discharged through CR3 by the lows present at the output of U4A. The result is that output of U4F goes high and the output of U4E goes low; DS1 turns on; and the output of U3B goes high (which shuts off the input from the internal reference). U3C and U3D are now enabled to gate the external reference.

When the output of U4E goes low, U3B is immediately disabled; at the same time, when the output of U4F goes high, CR4 and C28 delay the enabling of U3D. This prevents the possibility of the last internal reference pulse and the first external pulse from triggering U10A in rapid succession, which could cause the Controller to false trigger (the Controller receives its clock from U10A). CR5 and C29 perform a similar task when the reference is switched from external to internal. R10 increases the sensitivity of U21 when the reference switches to external to assure that U21 will continue to trigger even though the input level should drop slightly. This provides hysteresis to the external level-sensing circuits.

Time Base Dividers

U10A divides the selected (that is, internal or external) 10 MHz reference by 5. The 2 MHz signal, buffered by U4B, is used as the clock to the Controller. U9, U8, and U10B divide the 2 MHz signal by 320. The 6.25 kHz output is the time base for the Counter.

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TROUBLESHOOTING

General

Procedures for checking the Counter Assembly are given below. The circuits to check are marked on the schematic diagram by a hexagon with a check mark and a number inside, for example, ⟨√3⟩. In addition, any points outside the labeled circuit area that must be checked are also identified. Fixed signals are also shown on the schematic inside a hexagon, for example, ⟨+1.9 TO +2.1 VDC⟩. Extend the board assembly where necessary to make measurement.

CAUTION

Tighten SMC connectors to 0.6 N·m (5 in·lb). Hand tightening of connectors is insufficient. Hand-tightened connectors can work loose and cause reduced performance or malfunctions.

Equipment

Oscilloscope ..... HP 1740A
Signal Generator ..... HP 8640B

⟨√1⟩ 10 MHz Time Base Reference Oscillator and ECL-to-TTL Translator Check

1. Connect a high-impedance, dc coupled oscilloscope to U2A pin 3. The waveform should be an ECL square wave with a period of 100 ns.

   Hint: If the instrument has Option 002 (the high-stability internal reference oscillator), the input to AllJ4 (10 MHz IN) should be a non-sinusoidal waveform of approximately 1 Vpp and 100 ns period. If the frequency of the time base reference is only slightly off, perform *Adjustment 2—Internal Reference Frequency.*

2. Connect the oscilloscope to the collector of Q4 and then Q3. The waveform in each case should be a TTL "square" wave with a period of 100 ns.

⟨√2⟩ External Time Base Buffer and Time Base Select Switch Check

NOTE

This check assumes that the ⟨√1⟩ 10 MHz Time Base Reference Oscillator and ECL-to-TTL Translator Check *gives positive results.*

1. Set the signal generator to 10 MHz CW at +13 dBm. Connect its RF output to AllJ6 (EXT 10 MHz IN) or to the rear-panel J9 (TIME BASE 10 MHz INPUT).
2. Measure the points indicated in Table 8F-69 with a high-impedance, dc coupled oscilloscope with the signal generator output both on and off.

Table 8F-69. *Time Base Buffer and Select Switch,* ⟨√2⟩ *Step 2*

Signal Generator Output	Signal Condition (TTL)						DS1
	U21-4	U4A-2	U4E-10	U3D-11	U3B-6	U3C-8	
On	(1)	(1)	L	(1)	H	(1)	On
Off	H	H	H	H	(2)	(2)	Off

(1) Square wave at signal generator's frequency.
(2) Square wave at internal time base reference frequency.

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⟨√3⟩ Time Base Dividers Check

NOTE

This check assumes that the ⟨√2⟩ External Time Base Buffer and Time Base Select Switch Check *gives positive results.*

1. Check the points indicated in Table 8F-70 with a high-impedance, dc coupled oscilloscope (all waveforms are TTL pulses).

Table 8F-70. *Time Base Divider ICs,* ⟨√3⟩ *Step 1*

IC	Pin	Nominal Period (μs)
U10A	2	0.5
U10A	12	0.5
U4B	4	0.5
U9A	12	4
U9B	5	8
U8A	12	40
U8B	5	80
U10B	5	160
U20B	6	160

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Service Sheet 23

ASSEMBLY

- **A11 Counter (Counter Circuits)**

PRINCIPLES OF OPERATION

NOTE

The following discussions require understanding of the operation of the Instrument Bus (see Instrument Bus *in Service Sheet BD5) and of Instrument Bus readback (see* Direct Control Special Functions *in paragraph 8-7).*

General

The Counter Assembly contains the first four counter stages, the Input Selector, gating circuits, and Count Transfer Logic. The final counter stages are in the Controller itself. Normally, the Counter counts the frequency of the input, but in the case of the Voltmeter it counts the 10 MHz Selected Time Base Reference as gated under control of the Voltmeter. When an input frequency is being counted, the Controller, as synchronized by the Time Base, enables and disables the counter stages. The duration of the count (that is, the number of Time Base cycles per count cycle) depends on the input and resolution selected.

Stage 1

Stage 1 is the input stage to the Counter when counting the HF VCO ÷8 input; its output drives input 0 of the Input Selector (U7). When any other input is selected, the Input Selector routes it directly to Stage 2. Stage 1 consists of an ECL Divide-by-Two stage (U1A) followed by a TTL Divide-by-Four stage (U6A and U6B). In each case, divide-by-two functions are created by feeding the active-low (reset) output from a D-type flip-flop back to the D input. The ECL-to-TTL Level Translator (Q1 and Q2) shifts the logic level from U1A to make it compatible with the requirements of U6A. The outputs from U1A (via Q2), U6A, and U6B are fed to the D inputs of U5A for readback by the Controller at the end of a count sequence.

The Controller enables and disables the input to U1A by Counter Gate Control No. 1 flip-flop (U1B). To enable U1A, the Controller waits until the TIME BASE(L) line goes low and then issues and holds *esd* = 368 on the Instrument Bus. The D input of U1B (which had been high) now goes low. When the TIME BASE(L) line (which had been high) goes low, the low at the D input of U1B is clocked into the active-high output and enables U1A. This synchronizes the enabling of U1A with the Time Base. If the HF VCO ÷8 input is also high, it too must go low before U1B is clocked. The RC circuit (R23 and C27) at the output of U1B delays the enable input to U1A to insure that U1A will not be clocked until the next negative transition of the HF VCO ÷8 input.

To disable the count, the Controller issues *esd* = 360 or 362 to the Instrument Bus. The D input to U1B now goes high. When the TIME BASE(L) input goes low, U1A is disabled in the manner described above for its enabling. Note that several cycles of the Time Base may have occurred during the count sequence, but that the Controller knows that TIME BASE(L) is high when it issues *esd* = 360 to the Instrument Bus. After disabling the count, the Controller reads the count then issues *esd* = 370 to reset Stage 1 and set U1B.

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Input Selector and Stages 2, 3, and 4

The Input Selector (U7) multiplexes the input into Stage 2 of the Counter under direction of the Controller. It is also the enable and disable gate (via the G8 input) to Stage 2. To enable Stage 2, the Controller issues *esd* = 362 or 363 to the Instrument Bus. This puts a low on the D input of U16B. When the TIME BASE(H) line (which had been low) goes high, it clocks the active-high output of U16B to a low and enables the selected input of U7. The enabling of Stage 2 is thus synchronized with the Time Base.

To disable Stage 2, the Controller issues *esd* = 360 to the Instrument Bus. The D input of U16B now goes high. When the TIME BASE(H) input goes high, U7 is disabled. Note that several cycles of the Time Base may have occurred during the count sequence, but that the Controller knows that TIME BASE(H) is low when it issues *esd* = 360 to the Instrument Bus. After disabling the count, the Controller reads the count then issues *esd* = 370 to reset Stages 2, 3, and 4.

During the actual count, Counter Output Gate U14B is enabled and output 4 (the Counter Carry Output) of Stage 4 (U19A) is read onto the Controller via line d2(L) of the Instrument bus. Similarly, the Time Base is read by the Controller via U14D and line d3(L).

Counter Output Gating

To read back the outputs of the counter stages after completion of a count sequence, the Controller issues *esd* = 350 to the Instrument Bus. The output of U14C (which had been low) goes high and enables Counter Output Gates U15A, U15B, U15C, and U15D. The outputs of Stage 4 are inverted and placed on the readback data lines of the Instrument Bus. Next, the Controller issues *esd* = 340 to the Instrument Bus. U20A goes high and U12C low. This causes Stage 4 to be loaded with the output of Stage 3 and also enables the Counter Output Gates since the output of U14C is high. The output of Stage 3 is thus placed on the Instrument Bus through Stage 4. In a similar manner the Controller issues *esd* = 330 and *esd* = 320 to copy the outputs of Stages 2 and 1 into the subsequent stages and onto the Instrument Bus.

Voltmeter Gate

The Voltmeter Gate routes the (10 MHz) Selected Time Base (TB) Reference into the Input Selector. The signal, however, is gated by the Stop Count output from the Voltmeter's Comparator or the Audio Counter's Counter Gate Control (see Service Sheets 15 and 16). The sequence is as follows: The Controller issues *esd* = 362 to the Instrument Bus. After that, when the TIME BASE(H) line goes high, the active-low output of U16B goes high and initiates a ramp in the Voltmeter's Ramp Generator or a get set command in the Audio Counter. At this time U7 is also enabled, and the 10 MHz Selected Time Base Reference is counted. After a period of time dependent upon the input voltage into the Voltmeter's Comparator or the disabling of the get set command in the Audio Counter, the STOP COUNT (H) line (which was low) goes high. This high causes U20C to block the input into U7 and stop the count. Some time later, the Controller issues *esd* = 360 to the Instrument Bus and begins the process of reading back the count and clearing the counter stages.

Signature Analyzer Initialization

The Signature Analyzer (SA) Initialization circuit forces the Counter (including the Time Base) into a known, initial state when the Counter signature analysis routine is invoked. The Controller then exercises the counter circuitry in a repeatable sequence which produces a repetitive data pattern at each circuit node. The pattern is read by a signature analyzer which produces a signature unique to each data pattern. If the pattern agrees with that documented for the node, the circuits responsible for generating the pattern can be assumed to be working properly.

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Select Decoder, Data Latch, and Oven Warm Readback Circuit

For a general discussion of operation and decoding of the Instrument Bus, see *Instrument Bus* in Service Sheet BD5. The Oven Warm Readback Circuit allows the status of the Option 002 high-stability crystal oscillator to be read back by the Controller. It is called by Special Function 15. Q5 is enabled when a low is put on its emitter. It then acts as an inverter. Schottky diode CR6 prevents Q5 from becoming an active transistor in the inverted mode (that is, the roles of collector and emitter are reversed) when the emitter is high and the collector is low. For a discussion of the readback operation, see *Direct Control Special Functions* in paragraph 8-7.

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TROUBLESHOOTING

General

Procedures for checking the Counter Assembly are given below. The circuits to check are marked on the schematic diagram by a hexagon with a check mark and a number inside, for example, ⟨√3⟩. In addition, any points outside the labeled circuit area that must be checked are also identified. Fixed signals are also shown on the schematic inside a hexagon, for example, ⟨+1.9 TO +2.1 VDC⟩. Extend the board assembly where necessary to make measurements.

CAUTION

Tighten SMC connectors to 0.6 N·m (5 in·lb). Hand tightening of connectors is insufficient. Hand-tightened connectors can work loose and cause reduced performance or malfunctions.

Equipment

Oscilloscope	HP 1740A
Signal Generator	HP 8640B
Signature Analyzer	HP 5005A

⟨√1⟩ Stage 1 Check

1. Disconnect all cables from the A11 Counter Assembly. For Option 002 only, connect W21 (yellow) back to AllJ4 (INT 10 MHz IN) using an extender cable.
2. Set signal generator to 82 MHz CW at 0 dBm. Connect its RF output to AllJ1 (÷8 IN).
3. Jumper pin 10 of U1B to AllTP1 (GND) to enable stage 1.
4. Key in 0.314 SPCL to assure SA Initialization is disabled.
5. Connect a high-impedance, dc coupled oscilloscope to the collector of Q2 then the collector of Q1. The oscilloscope should have a low-capacitance 10:1 divider probe. The waveform should be sinusoidal and TTL compatible with a period of approximately 24 ns.

   Hint: Pins 4, 5, and 6 of U1A should be ECL low. Pin 11 of U1B should be an ECL square wave with a period of 160 μs. See logic level definitions on the service sheet schematic for the ECL levels used in the instrument.
6. Connect the oscilloscope to pin 9 of U6B. The waveform should be a TTL square wave with a period of approximately 100 ns. Ringing of the waveform is normal.

   Hint: Pins 1 and 4 of U6A should be TTL high. The waveform at pin 5 of U6A should be a TTL square wave with a period of approximately 50 ns.
7. Set the signal generator frequency to 40 MHz. The waveform on pin 9 of U6B should now have a period of approximately 200 ns.
8. Remove the jumper from pin 10 of U1B.
9. Key in 0.363 SPCL to enable Stage 1. Connect the oscilloscope to pin 10 of U1B. The waveform should be low-going ECL pulses with a period of approximately 7 ms.
10. Key in 0.360 SPCL to disable Stage 1. Pin 6 of U1A should be an ECL high. The collectors of Q1 and Q2 should be steady TTL complements (either may be high).
11. Key in 0.370 SPCL to initialize Stage 1. The collector of Q2 and pins 5 and 9 of U6 should be TTL low.

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⟨√2⟩ Stages 2, 3, and 4, Count Transfer Logic, and Counter Gate Control Check

NOTE

This check assumes that ⟨√1⟩ Stage 1 Check *gives positive results and that the internal 10 MHz Time Base Reference and Time Base Dividers are operative (see Service Sheet 16).*

1. Remove the three ribbon cables (W14, W46, and W47) that connect to the rear of the A27 Digital Mother Board Assembly. W46 is on the bottom of the mother board.
2. Set LINE to STBY. Remove the A14 Remote Interface Assembly from its socket. Set LINE back to ON.
3. Connect the signature analyzer start and stop to A13TP5 (TEST A), clock to A13TP4 (WRT), and ground to A13TP15 (GND) on the A13 Controller Assembly. Set start to trigger on a rising edge; set stop to trigger on a falling edge; set clock to trigger on a falling edge.
4. Disconnect all cables from the A11 Counter Assembly. Jumper A11J1 (÷8 IN) to A11J5 (INT 10 MHz OUT). For Option 002 only, connect W21 (yellow) back to A11J4 (10 MHz IN) using an extender cable.
5. Jumper A13TP7 (TEST C) to A13TP15 (GND) on the A13 Controller Assembly. Momentarily ground A13TP9 (RESET). This initiates the signature analysis routine.
6. Check the points indicated in Table 8F-71 with the signature analyzer probe.

   Hint: If d0(L) only is faulty, the Oven Warm Readback Circuit (Q5) may be faulty. If a data line itself is suspected (for example, if the signature for d2(L) only is faulty), the line itself may be faulty; see *CPU I/O Port Check* in Service Sheet BD5. Otherwise, continue with step 7. If no signatures are faulty, perform the other checks on this service sheet.

Table 8F-71. *Signatures,* ⟨√2⟩ *Step 6*

Description	Location	Signature
+5V	A13TP10 (+5V)	U637
d0(L)	A11U15 pin 6	139U
d1(L)	A11U15 pin 3	7864
d2(L)	A11U15 pin 11	0009
d3(L)	A11U15 pin 8	UU97

7. Remove A11U14 and U15 from their sockets.

CAUTION

The IC sockets are a high-grip type. Their lifetime is limited to only a few insertions. Use caution when removing or inserting ICs to avoid damage to the socket or IC.

8. Check the points indicated in Table 8F-72 with the signature analyzer probe (the pin numbers for A11U15 are the socket pin numbers).

   Hint: If faulty, the problem is with the data line itself; see *CPU I/O Port Check* on Service Sheet BD5.

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Table 8F–72. *Signatures,* ⟨√2⟩ *Step 8*

Description	Location	Signature
+5V	A13TP10 (+5V)	U637
d0(L)	A11U15 pin 6	F4H6
d1(L)	A11U15 pin 3	F4H6
d2(L)	A11U15 pin 11	4058
d3(L)	A11U15 pin 8	U637

9. Check the points indicated in Table 8F–73 with the signature analyzer probe.

   Hint: If faulty, check the components associated with the first faulty node (relative to the signal flow).

Table 8F–73. *Signatures,* ⟨√2⟩ *Step 9*

Pin	U12	U13	U16	U17	U18	U20	Pin
1	3U50	U637	4144	5A66	8U7U	747P	1
2	F967	32P1	4U22	0C54	32P1	5CC4	2
3	7948	32P1	3U50	6209	8714	2UFA	3
4	8U7U	C773	U637	29PC	–	–	4
5	2UFA	U637	CFP3	0000	–	–	5
6	H9UH	3910	4AH4	U637	–	–	6
7	0000	8U7U	0000	3U50	0000	0000	7
8	747P	U637	74P6 or 7UUH	0000	–	–	8
9	8249	0000	7A82 or 7199	7948	–	–	9
10	–	C915	3U50	U74A	–	–	10
11	–	4U22	AC99 or 5HAP	5CC4	CFP3	8249	11
12	C773	0000	8714	0FA6	4AH4	8PPU	12
13	4144	C773	4U22	8PPU	U637	0FA6	13
14	U637	U637	U637	4144	U637	U637	14
15	–	0000	–	U637	–	–	15
16	–	0000	–	U637	–	–	16

Note: The signature for a high or +5V is U637. The signature for a low or ground is 0000. Dual signatures for U16 result because Time Base cannot now be read through U14D.

10. Plug in A11U14. Check the points indicated in Table 8F–74 with the signature analyzer probe.

    Hint: If a signature is faulty, check the components associated with the first faulty node (relative to the signal flow). Otherwise, the fault is probably with A11U15. Note that some outputs of Stages 1 and 2 cannot be checked because the data occurs at a higher rate than the signature analysis clock.

11. For reference, the signatures with A11U14 and A11U15 plugged in are listed in Table 8F–75.

    Hint: Note that some of the outputs of Stages 1 and 2 cannot be checked because the data occurs at a higher rate than the signature analyzer clock.

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Table 8F-74. *Signatures,* ⟨√2⟩ *Step 10*

Pin	U5	U7	U11	U14	U19	Pin
1	8PPU	–	747P	32P1	H9UH	1
2	H9FP	–	2P6C	8U7U	9053	2
3	–	–	H9FP	8714	2P6C	3
4	CFP3	–	–	8U7U	UC92	4
5	–	–	UC92	U382	HU31	5
6	–	–	UC92	3202	HU31	6
7	0000	7199	0000	0000	0000	7
8	–	0000	0AHU	2PC7	9AP3	8
9	–	0000	1P16	H9UH	8AHH	9
10	–	0000	–	U74A	1P16	10
11	–	0000	0AHU	FH9F	9AP3	11
12	0AHU	–	9AP3	8PH6	U382	12
13	3U50	–	3U50	8U7U	3U50	13
14	U637	–	U637	U637	U637	14
15	–	–	–	–	–	15
16	–	U637	–	–	–	16

Note: The signature for a high or +5V is U637. The signature for a low or ground is 0000.

Table 8F-75. *Signatures,* ⟨√2⟩ *Step 11*

Pin	U5	U7	U11	U12	U13	U14	U15	U16	U17	U18	U19	U20	Pin
1	8PPU	–	747P	3U50	U637	P5A8	8AHH	4144	5A66	8U7U	H9UH	747P	1
2	H9FP	–	2P6C	F967	P5A8	8U7U	2PC7	4U22	0C54	8P53	9053	5CC4	2
3	–	–	H9FP	7948	8P53	8714	7864	3U50	6209	8714	2P6C	2UFA	3
4	CFP3	–	–	8U7U	C773	8U7U	HU31	U637	29PC	–	UC92	–	4
5	–	–	UC92	2UFA	U637	U382	2PC7	CFP3	0000	–	HU31	–	5
6	–	–	UC92	H9UH	A815	0009	139U	4AH4	U637	–	HU31	–	6
7	0000	7199	0000	0000	CH74	0000	0000	0000	3U50	0000	0000	0000	7
8	–	0000	0AHU	747P	U637	2PC7	UU97	7UUH	0000	–	9AP3	–	8
9	–	0000	1P16	8249	0000	H9UH	U382	7199	7948	–	8AHH	–	9
10	–	0000	–	–	C915	U74A	2PC7	3U50	U74A	–	1P16	–	10
11	–	0000	0AHU	–	4U22	UU97	0009	8PH6	5CC4	CFP3	9AP3	8249	11
12	0AHU	–	9AP3	C773	0000	8PH6	9053	8714	0FA6	4AH4	U382	8PPU	12
13	3U50	–	3U50	4144	C773	8U7U	2PC7	4U22	8PPU	U637	3U50	0FA6	13
14	U637	–	U637	U637	U637	U637	U637	U637	4144	U637	U637	U637	14
15	–	–	–	–	0000	–	–	–	U637	–	–	–	15
16	–	U637	–	–	0000	–	–	–	U637	–	–	–	16

Note: The signature for a high or +5V is U637. The signature for a low or ground is 0000.

⟨√3⟩ Input Selector and Voltmeter Gate Check

NOTE

This check assumes that ⟨√1⟩ Stage 1 Check *gives positive results.*

1. Connect a high-impedance, dc coupled oscilloscope to A11TP3 (SEL OUT). The oscilloscope should have a low-capacitance 10:1 divider probe.
2. For Option 002 only, connect W21 (yellow) to A11J4 (10 MHz IN) using an extender cable.
3. Jumper pin 10 of U1B to A11TP1 (GND) to enable Stage 1. Jumper A11TP6 (VM GATE) to A11TP1 (GND) to force Stop Count Low.

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4. Set the signal generator to 10 MHz CW at +16 dBm (TTL compatible level). Connect its RF output to input indicated in Table 8F-80 with a 50Ω termination in parallel. For each input, key in the Direct Control Special Function indicated and note the period of the waveform at A11TP3. The waveform should be TTL compatible.

   Hint: If the only failure is with Direct Control Special Function 0.316 (a check of the voltmeter input), check pin 10 of U20C which should be a TTL high. Pin 8 of U20C should be a TTL square wave with a period of 100 ns.

Table 8F-76. *Period at A11TP3,* ⟨√3⟩ *Step 4*

Input Connector	Direct Control Special Function	Nominal Period (ns) at A11TP3
A11J1 (÷8 IN)	0.314	800
A11J3 (IF IN)	0.315	100
None	0.316	100
A11J2 (10 MHz IN)	0.317	100
None	0.31C	100
A11J6 (EXT 10 MHz IN)	0.31D	100
None	0.31E	100

5. Remove the short from A11TP6. Check pin 2 of U7 which should be a TTL low.

⟨√4⟩ Select Decoder, Data Latch, and Oven Warm Readback Circuit Check

1. For Option 002 only, connect W21 (yellow) to A11J4 (10 MHz IN) using an extender cable.
2. Key in the Direct Control Special Functions indicated in Table 8F-81. For each setting, check the pins on U17 indicated with a high-impedance dc coupled oscilloscope.

Table 8F-77. *Levels at U17,* ⟨√4⟩ *Step 2*

Direct Control Special Function	Level (TTL) at U17 Pin							
	15	14	13	12	11	10	9	7
0.300	*	H	H	H	H	H	H	H
0.310	H	*	H	H	H	H	H	H
0.320	H	H	*	H	H	H	H	H
0.330	H	H	H	*	H	H	H	H
0.340	H	H	H	H	*	H	H	H
0.350	H	H	H	H	H	*	H	H
0.360	H	H	H	H	H	H	*	H
0.370	H	H	H	H	H	H	H	*
* Low-going TTL pulses, approximately 60 ms period.								

3. Key in the Direct Control Special Functions indicated in Table 8F-78. For each setting, check the pins on U13 indicated.

Table 8F-78. *Levels at U13,* ⟨√4⟩ *Step 3*

Direct Control Special Function	Level (TTL) at U13 Pin			
	16	15	11	9
0.310	L	L	H	L
0.31F	H	H	L	H

4. For Option 002 only, temporarily unplug the A11 Counter Assembly; tape over pin 34 of the edge connector with a small piece of tape so it can no longer make contact, then plug the assembly back in.

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5. Key in 0.300 SPCL to enable the Oven Warm Readback Circuit readback. The display should read 000001.0000 (oven cold).
6. Ground the end of R39 that connects to pin 34 of the edge connector. The display should read 000000.0000 (oven warm).
7. Key in 0.000 SPCL to disable oven readback. Check pin 6 of U15B (the d0(L) line) with the oscilloscope. The signal should be a steady TTL high.
8. Remove the tape from pin 34 of the edge connector.

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Service Sheet 24

ASSEMBLY

- **A13 Controller**

PRINCIPLES OF OPERATION

General

The Controller Assembly controls the entire automated portion instrument's operation. The Controller consists of a microprocessor, Read-Only Memory (ROM), Random-Access Memory (RAM), and input/output circuits. For a general discussion of how the Controller and the Instrument Bus control the operations of the instrument, see *Instrument Bus* in Service Sheet BD5.

Microprocessor

The microprocessor is divided into two ICs, the Central Processing Unit (CPU) and the Static Memory Interface (SMI). In addition, a third IC, the Peripheral Input/Output (PIO) located on the Remote Interface Assembly (see Service Sheet 28), is considered a part of the microprocessor. The PIO is used when it is necessary to interface the CPU with the HP-IB. The CPU (U9) is an eight-bit parallel processor. LC network L1, C19, and C20 determines the frequency of the CPU's internal clock. It is normally overridden by the 2 MHz signal on the Clock line from the Counter. If the Counter Assembly (A11) is removed, the internal clock takes over to keep the Controller functioning. The CPU inputs and outputs are described in Table 8F-79.

Table 8F-79. *Inputs and Outputs of the CPU (U9)*

Pin Name	Description	Type
I/O 00 thru I/O 07	I/O Port Zero	Input/Output
I/O 10 thru I/O 17	I/O Port One	Input/Output
DB0 thru DB7	Data Bus Lines	Bi-Directional (3 state)
ROMC0 thru ROMC4	Control Lines	Output
Φ, WRITE	Clock Lines	Output
EXT RES	External Reset	Input
INT REQ	Interrupt Request	Input
ICB	Interrupt Control Bit	Output
RC	RC Network	Input
XTLX	Crystal Clock Line	Output
XTLY	External Clock Line	Input

The SMI (U8) provides most of the interface logic needed to address up to 65 536 bytes of memory in the microprocessor system. In response to control signals from the CPU, the SMI generates the address and control signals needed by the memory devices. The SMI inputs and outputs are described in Table 8F-80.

The PIO provides most of the interface logic needed to interface the CPU with the HP-IB. The PIO is described in Service Sheet 28.

Memory

The instrument's memory consists of three 16 384 byte, 8 bit ROMs (U4, U7, and U10), a 2048 byte, 8 bit CPU External Register or RAM (U1), and a small RAM within the CPU itself. Memory Decoder U5A controls which memory IC is enabled. Memory Decoder U5B and inverter U2E are provided so that ROM 2 and ROM 3 can be replaced by a single 32 768 byte ROM (ROM 2 only). In that event jumpers W1 and W2 are moved to their alternate positions.

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Table 8F–80. *Inputs and Outputs of the SMI (U8)*

Pin Name	Description	Type
DB0 thru DB7	Data Bus Lines	Bi-Directional (3 state)
ADDR0 thru ADDR15	Address Lines	Output
ROMC0 thru ROMC4	Control Lines	Input
Φ, WRITE	Clock Lines	Input
INT REQ	Interrupt Request	Output
PRI IN	Priority In Line	Input
RAM WRITE	Write Line	Output
EXT IN	External Interrupt Line	Input
REGDR	Register Drive Line	Input/Output
CPU READ	CPU Read Line	Output

To illustrate how a ROM address is accessed for data, assume that the CPU wants to read information from address 255 of ROM 1 (U10). First, the CPU places the necessary information on the ROM Control (ROMC) lines and configures the data lines on the Control Bus to accept data. The SMI decodes this information from the CPU and outputs the required address information on lines A0(H) through A15(H). In this case address lines A0(H) through A7(H) are high, lines A8(H) through A15(H) are low. The SMI then sets CPU READ(H) high. CPU READ(H) is inverted by U2F.

Note that this is a read operation. The RAM WRITE(L) line from the SMI is high. Lines A14(H) and A15(H) are low. Decoder U5A decodes a low on its 0G—the other outputs are high. Since both the ROM 1 (L) and CPU READ (L) lines are low, U10 is enabled, U7, U4, and U1 are disabled. Since A0(H) through A7(H) are high and A8(H) through A13(H) are low, the 8 bits of data at address 255 are output from the ROM on lines DB0(H) through DB7(H). This information is then read into the CPU.

The RAM read and write functions are similar to the ROM function. The CPU READ(H) and RAM WRITE(L) lines are used to determine which function of the RAM (U1) is activated. Decoder U5A enables U1 via Q2C. Q2C prevents enabling U1 when line power is off.

TEST LEDs and Test Points

The TEST LEDs DS1 through DS4 are controlled by the CPU as described in paragraph 8-10. The test points (TP5 through TP8) are used to modify the power-up routine as described in paragraph 8-11 and are also used when performing signature analysis.

Select and Data Buffers

The Select and Data Buffers (U12 and U13) invert and buffer the I/O 00 through I/O 07 input/output lines from the CPU to the Instrument Bus. For a general discussion of the Instrument Bus, see *Instrument Bus* in Service Sheet BD5. In addition, data lines d0(L) through d3(L) are input to the CPU from the Instrument Bus.

Enable Decoder

The Enable Decoder (U11) decodes the e0(H) through e3(H) lines from the CPU into the eight individual enable lines e=0(L) through e=7(L). These are distributed throughout the instrument to enable the desired select decoder.

Power-On Reset

The Power-On Reset circuit (U3C) applies a momentary low on the EXT RES line of the CPU when power is applied to the instrument. When EXT RES is pulled low and then released, a program originating at memory address 0 is executed.

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+12V Regulator

The +12V Supply, which supplies some of the Controller ICs, is derived from the +15V Supply by regulator U6.

+12V and +5V Power Supply Drop Detection and RAM Disable

When either the +12V or the +5V Supply drops 10% or more from its nominal value (usually due to switching the power off), the drop is sensed by the +12V and +5V Power Supply Drop Detection circuit. The circuit disables the RAM (U1) and connects the RAM's supply terminal to battery BT1. This permits U1 to retain its data (that is, the data is nonvolatile). BT1 is a long-life, non-rechargeable battery. Normally, little current is required to back up U1.

When both supplies are up, the inverting (−) inputs of comparators (U3A and U3B) are at a nominal +2V. The non-inverting (+) inputs are set to approximately +1V, which is derived from +6.2V reference VR1. The reference can maintain its level until the +12V supply drops to about half its nominal value. U3A and U3B output active lows of approximately 0V. This combination of outputs turns Q2A off and Q2B on. Q2B becomes a current source, which turns on Q3, Q2E, and Q1 and connects the +5V BATT line to the +5V Supply.

If the +5V Supply drops, the output of U3B switches off, Q2B can no longer supply current to Q3, so Q3, Q2E, and Q1 switch off. The +5V BATT line is now supplied by BT1 through CR5. If the +12V Supply drops, the output of U3B switches off. The base of Q2A begins to conduct current from the +6.2V reference through R21 (unless the +12V Supply drops below +5V). Q2A then conducts the emitter current away from Q2B, and Q2B shuts off. With Q2B off, Q3, Q2E, and Q1 switch off, and the +5V BATT line is supplied by BT1.

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TROUBLESHOOTING

General

Procedures for checking the Controller Assembly are given below. The circuits or points to check are marked on the schematic diagram by a hexagon with a check mark and a number inside, for example, ⟨✓3⟩ . In addition, any points outside the labeled circuit area that must be checked are also identified. Fixed signals are also shown on the schematic inside a hexagon, for example, ⟨+1.9 TO +2.1 VDC⟩ . Extend the board assembly where necessary to make measurements.

CAUTION

MOS and CMOS ICs can be damaged by static charges and circuit transients. Do not remove the A13 Controller Assembly or the A14 Remote Interface Assembly from the instrument while power is applied. Discharge the board and replacement IC to the same potential. (Use a conductive foam pad such as provided in the Service Accessory Kit HP 08901-60287.) When unplugging ICs, place the board on a conductive pad. When the IC is unplugged, insert it into the foam also.

The A13 Controller Assembly contains a soldered-in battery. To prevent shorting out the battery, do not lay the board on a metal surface.

Several ICs on these assemblies are held in high-grip sockets. Both the socket and the device can be damaged if an attempt is made to remove the device with an IC extraction tool. The recommended procedure is to first ground the tip of a small blade-type screwdriver, then slide the tip between the IC and the socket and slowly pry up the IC one pair of pins at a time.

If the Measuring Receiver powers up correctly, it is a strong indication that the Controller circuits are operating properly. In most cases, the two most common indications of a Controller fault is that the instrument fails to complete even the first phase of the power-up routine or that it behaves very erratically. However, be very careful about assuming a Controller failure when the instrument behaves erratically. Because of the close interrelationship of the circuit components, the data feedback loops, and the software, a failure that is occurring in one section of the instrument can affect other areas. For example, almost any malfunction will prevent the Measuring Receiver from tuning properly.

The three rear circuit boards in the Digital Section are bused in parallel. The A14 Remote Interface Assembly contains devices that interface directly with the Controller. If a Controller failure is suspected, remove A14 from its socket to verify that it is not the source of failure.

In addition, keep the following points in mind when troubleshooting the Controller:

1. It is important to understand the structure of the Controller's buses. Data on these buses is often unstable or meaningless because of multiplexing, switching transients, and open-collector circuits. These conditions cause no problems for the Controller itself since it is synchronous and knows when the bus lines contain stable signals. (This is also true for the signature analyzer.) However, this is not true of other instruments testing the Controller such as a logic probe or oscilloscope. These test instruments, though, can still be used to examine qualitative factors such as general activity, logic levels, waveform timing, and bus conflicts.

2. Since bus structures also make it possible for many devices to be connected together on a single node, finding the one bad device on such a node can be difficult. A current tracer is useful for this purpose.

3. The Controller is a sequential processor. Program flow depends on a long sequence of instructions and events. If even a single bit of information is incorrect, the entire sequence can be changed. Bad memory bits are the most common source of single-bit errors.

4. The proper operation of the clock circuits is critical.

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5. An improper reset can cause the Controller to appear to be running, but it may be incorrectly initialized or running the wrong sequence of software.

6. Interrupts are edge triggered. A stuck interrupt will interrupt once and then never again. An intermittent interrupt will keep interrupting. When the Controller is interrupted, the measurement is aborted, and the complete measurement cycle restarts at the beginning. Therefore, if the intermittent interrupt occurs frequently, it will completely prevent the instrument from operating.

Equipment

Digital Test/Extender Board ..... HP 08901-60081
Oscilloscope ..... HP 1740A
Signature Analyzer ..... HP 5005A
Voltmeter ..... HP 3455A

⟨√1⟩ Power-Up and Reset Check

1. Switch POWER to STBY. Extend the A13 Controller Assembly with the Digital Test/Extender Board. Switch POWER to ON. Check the sequencing of the TEST LEDs. If the TEST LEDs are able to sequence through the power-up routine, even though errors are indicated, see the *Power-Up Checks* of Service Sheet BD1. If the TEST LEDs come on and remain in the random state as specified in the Power-Up Checks, perform step 2.

2. While monitoring pin 2 of U3C, momentarily connect A13TP9 (RESET) to A13TP10 (+5V). Pin 2 of U3C should go low momentarily to reset the CPU (U9).

   Hint: If pin 2 of U3C does not go low, momentarily ground it. If the power-up/reset function then proceeds normally, check the Power On-Reset circuit.

⟨√2⟩ Decoder and ROM Check

NOTE

This check is a continuation of the Controller Kernel Check *of Service Sheet BD5.*

1. If A13 is not already extended on the Digital Test/Extender Board, switch POWER to STBY, extend the board, and switch POWER to ON.

2. Short A13TP9 (RESET) to A13TP10 (+5V). Switch the ROMC switches on the extender board to ground. On the extender board, connect the signature analyzer clipleads as follows:

   Clock ..... WRT
   Start ..... ADDRESS 15
   Stop ..... ADDRESS 15
   Ground ..... GND

3. Set the signature analyzer's start, stop, and clock to trigger as follows:

   Start ..... Falling Edge
   Stop ..... Falling Edge
   Clock ..... Falling Edge

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4. Check the pins on U5 indicated in Table 8F-81.

Table 8F-81. *Memory Select Signatures,* ⟨√2⟩ *Step 4*

Selected Memory Device	Pin on A13U5	Signature
ROM 1	4	5FU8
ROM 2	5	29A6
ROM 3	6	64HP
RAM	7	1181

5. Set the signature analyzer's start, stop, and clock trigger as follows:

Start ..... Falling Edge
Stop ..... Rising Edge
Clock ..... Falling Edge

6. Connect the signature analyzer start and stop to the pin on U5 listed in Tables 8F-82 through 8F-82e. Then check the CONTROL BUS test points on the extender board with the signature analyzer probe.

NOTE

The signatures below are valid only for the ROMs with the specified part number. Consult Section 7, Instrument Changes *or the* Manual Changes Packet *for signatures corresponding to ROMs with other part numbers.*

Hint: A faulty signature indicates a faulty ROM.

Table 8F-82. *Data Signatures,* ⟨√2⟩ *Step 6* ***(2314A to 2333A)***

ROM	Start/Stop Pin On U5	Signature on CONTROL BUS DATA Test Point*							
		0	1	2	3	4	5	6	7
1	4	Replace the three ROMs with the latest parts.							
2	5								
3	6								

* Valid ROM part numbers:

ROM Number	Part Number
1	08901-80062
2	08901-80063
3	08901-80064

Table 8F-82a. *Data Signatures,* ⟨√2⟩ *Step 6* ***(2334A to 2426A)***

ROM	Start/Stop Pin On U5	Signature on CONTROL BUS DATA Test Point*							
		0	1	2	3	4	5	6	7
1	4	C38P	6HCC	488F	8430	FC83	8UU8	0PHU	UPF8
2	5	336H	U69A	0P10	U7PC	HF4H	4221	529C	FC58
3	6	AA6C	AUU4	23F7	3U96	H246	F8AU	2UA7	4H09

* Valid ROM part numbers:

ROM Number	Part Number
1	08901-80066
2	08901-80067
3	08901-80068

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Table 8F–82b. *Data Signatures,* ⟨√2⟩ *Step 6* ***(2432A to 2530A)***

ROM	Start/Stop Pin On U5	Signature on CONTROL BUS DATA Test Point*							
		0	1	2	3	4	5	6	7
1	4	A0P0	8PP1	28A6	98F3	HP65	H610	6U6U	796U
2	5	7481	230P	6AHA	UH48	39C6	5526	6508	42PP
3	6	7624	63HA	8C49	7233	F8PA	A17F	3C13	62U2

* Valid ROM part numbers:

ROM Number	Part Number
1	08901-80071
2	08901-80072
3	08901-80073

Table 8F–82c. *Data Signatures,* ⟨√2⟩ *Step 6* ***(2551A only)***

ROM	Start/Stop Pin On U5	Signature on CONTROL BUS DATA Test Point*							
		0	1	2	3	4	5	6	7
1	4	4C50	UC21	074F	5210	86F9	UC26	HPPC	023P
2	5	H2AH	FU3F	F37A	51PU	44H6	30P7	89P7	2P5P
3	6	8P0P	26FC	C0C2	0P58	1549	46AC	C57F	71FA

* Valid ROM part numbers:

ROM Number	Part Number
1	08901-80081
2	08901-80082
3	08901-80083

Table 8F–82d. *Data Signatures,* ⟨√2⟩ *Step 6* ***(2608A to 2642A)***

ROM	Start/Stop Pin On U5	Signature on CONTROL BUS DATA Test Point*							
		0	1	2	3	4	5	6	7
1	4	66H1	CH10	H8HC	2C9F	4726	71P8	A687	7H68
2	5	A2CC	PC7C	A7HP	61AA	P38F	7P8H	F2CP	4PCC
3	6	C5AP	0F28	U741	6A33	2474	52UU	A404	3314

* Valid ROM part numbers:

ROM Number	Part Number
1	08901-80087
2	08901-80088
3	08901-80089

Table 8F–82e. *Data Signatures,* ⟨√2⟩ *Step 6* ***(2644A and Above)***

ROM	Start/Stop Pin On U5	Signature on CONTROL BUS DATA Test Point*							
		0	1	2	3	4	5	6	7
1	4	40U9	2P98	F90H	CA3P	AUHP	8882	235U	5U7P
2	5	9H41	7631	CAH2	14P5	F488	6F71	063H	74A1
3	6	1055	2501	H3H4	FPUP	F4P5	4CHA	8APP	202C

* Valid ROM part numbers:

ROM Number	Part Number
1	08902-80090
2	08902-80091
3	08902-80092

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⟨√3⟩ Enable Decoder Check

1. Key in the Direct Control Special Functions indicated in Table 8F-83. For each setting, check the pins on U11 indicated.

   Hint: If "enable=7" is bad, these functions cannot be keyed into the instrument. Perform the *Front-Panel Keys and Scanners Check—Using Signature Analysis* on Service Sheet 25.

Table 8F-83. *Levels on U11, ⟨√3⟩ Step 1*

Direct Control Special Function	Level (TTL) at U11 Pin											
	1	2	3	4	7	9	10	11	12	13	14	15
0.0	L	L	L	*	H	H	H	H	H	H	H	*
0.1	H	L	L	*	H	H	H	H	H	H	*	H
0.2	L	H	L	*	H	H	H	H	H	*	H	H
0.3	H	H	L	*	H	H	H	H	*	H	H	H
0.4	L	L	H	*	H	H	H	*	H	H	H	H
0.5	H	L	H	*	H	H	*	H	H	H	H	H
0.6	L	H	H	*	H	*	H	H	H	H	H	H
0.7	H	L	H	*	*	H	H	H	H	H	H	H
* Low-going TTL pulse, period approximately 60 ms.												

⟨√4⟩ Select and Data Buffers Check

1. Key in the Direct Control Special Functions indicated in Table 8F-84. For each setting, check the pins indicated.

   Hint: If the outputs of U13C and U13D (that is, pins 3 and 6) are faulty, check pin 2, which should be high.

Table 8F-84. *Levels on U12 and U13, ⟨√4⟩ Step 1*

Direct Control Special Function	Level (TTL) at U12 Pin								Level (TTL) at U13 Pin							
	6	14	8	12	11	9	13	7	12	11	9	8	1	3	4	6
0.000	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L
0.0FF	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H

⟨√5⟩ Nonvolatile Memory Backup Check

1. Check A13TP13 (BATT) with a dc voltmeter. The voltage should be between +2.7 and +2.9 Vdc.

   Hint: If faulty, BT1 is probably in need of replacement. Observe the following warning.

WARNING

See paragraph 8-3 for proper disposal of the battery.

2. Ground the pins on U3 as instructed in Table 8F-85. Observe the dc voltage at the points indicated, which should be within the limits given. When the ground from pins 6 and 8 of U3 is removed, the instrument should be heard resetting itself.

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Table 8F–85. *Levels on Memory Backup,* ⟨√5⟩ *Step 2*

Configuration of U3	Limits (Vdc)			
	U3 Pin 1	U3 Pin 14	Q3 Collector	A13TP14
Normal	<0.1	<0.1	>11	<0.4
U3 Pin 6 Grounded	>4	<0.1	<0.1	>4
U3 Pin 8 Grounded	<0.1	>4	<0.1	>4

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Service Sheet 25

ASSEMBLY

- **A1 Keyboard and Display (Keyboard Circuits)**

PRINCIPLES OF OPERATION

NOTE

The following discussion requires understanding of the operation of the Instrument Bus (see Instrument Bus *in Service Sheet BD5) and of Instrument Bus readback (see* Direct Control Special Functions, *in paragraph 8-7).*

General

The Keyboard and Display Assembly interrupts the Controller when a key has been pressed and provides the circuitry that enables the Controller to determine which key was pressed.

Keystroke Detector

The Keystroke Detector pulses the EXT INT(L) (that is, External Interrupt) line low when a key is pressed. When no key is down (that is, key switches S1 through S46 open), the inverting (−) input of U13A is pulled low by R4. The outputs of the Key Row Scanner (U19) are normally in the high or off state. (The outputs are open-collectors.) The non-inverting (+) input of U13A is biased at approximately +1.2V. Thus, for the condition when no key is pressed, the output of U13A is high, the output of U13B is low, and the output of U14D is high (that is, no interrupt, see Service Sheet 24).

Pressing any key (for example, the AUTO OPER key S11) pulls the inverting input of U13A above +1.2V (via R1E and R2F for the AUTO OPER key). This causes U4D to go low and creates a Controller interrupt. U13A has an open-collector output. When U13A goes low, C2 is rapidly discharged to produce a low on the input to U13B. However, when U13A goes high, C2 can charge only via R8. This action holds the input to U13B low for at least 50 ms regardless of key bounce. R11 adds hysteresis to U13B to improve noise immunity and shorten the transition time of the input to U14D.

Key Scanners and Front-Panel Keys

When the Controller receives an interrupt, it immediately initiates a key scan routine. The scan must identify the pressed key before the key has been released even in the presence of key bounce. Consider the example of pressing the AUTO OPER key (S11). The scan begins by the Controller issuing $esd = 7F0$ to the Instrument Bus. This puts an active low on pin 4 of demultiplexer U19. Note that, $e = 7$ and $s = F$. Inputs 1 and 2 of U19 are high since $s0 = 1$ and $s1 = 1$. A 3 is demultiplexed. The e=7(L) line is low, which enables inputs G4 and G5. Input 4 is enabled since $s2 = 1$. Thus only output 3 of the lower half of U19, which is enabled by input 4, is low.

The same Instrument Bus code enables the readback gates of U20 but not U21. Note that $s3 = 1$. Thus, the inputs to U14C are high. The two inputs to U14A are low. The NAND gates of U20 are enabled and function as inverters. U14B is low and the outputs of the NAND gates of U21 are high, that is, off. The Controller reads back the data (d) lines and scans the data giving priority to the highest number decoded. Since all columns are held high by pull-up resistors, the Controller reads $d = F$. The AUTO OPER key has no effect because the output at pin 7 of U19 is off at this time.

The Controller next issues $esd = 7E0$. Pin 5 of U19 is now low. U20 is still enabled and U21 is still disabled. $d = F$ is read back. Next $esd = 7D0$ is issued, and $d = F$ is again read back. Next $esd = 7C0$ is issued; pin 7 of U19 is low. This time $d = B$ is read back; that is, $d2 = 0$ (the d2(L) line is high). The Controller has now learned that the AUTO OPER key is closed.

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If no key closure is found in the first four columns, the sequence continues until the issuance of $esd = 770$. With this code, the s3(H) input to U14B and U14C goes low, and U20 is disabled, and U21 is enabled. The Controller now starts reading the data lines from U21 to determine if one of the keys in the second four columns is closed.

If no key closure is found (that is, $d = F$ always) due to key bounce, the scan repeats until 50 ms have elapsed and then the instrument reverts back to its previous mode of operation. Whether the key was found or not, the measurement cycle that was interrupted is aborted and a new software cycle is initiated.

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TROUBLESHOOTING

General

Procedures for checking the Keyboard and Display Assembly are given below. The circuits or points to check are marked on the schematic diagram by a hexagon with a check mark and a number inside, for example, ⟨√3⟩. In addition, any points outside the labeled circuit area that must be checked are identified. Fixed signals are also shown on the schematic inside a hexagon, for example, ⟨+1.9 TO +2.1 VDC⟩. Remove the front-panel assembly to gain access to the circuit side of the keyboard.

Equipment

Oscilloscope ..... HP 1740A
Signature Analyzer ..... HP 5005A
Voltmeter ..... HP 3455A

⟨√1⟩ Keystroke Detector Check

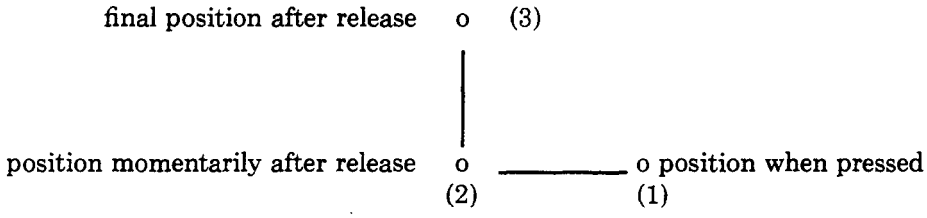
1. Press any key and observe TEST LED (2) on the A13 Controller Assembly. Each time the key is pressed the LED should toggle, that is, change state. If it does, the Controller is being properly interrupted.
2. Remove the ribbon cable W14.
3. Check the voltages indicated in Table 8F-86.

   Hint: Any key should give the same voltage readings. The voltage at pin 2 of U13 will increase as more keys are pressed simultaneously.

Table 8F-86. *Levels at U13 and U21, ⟨√1⟩ Step 3*

Keys Down	Voltage Limits (Vdc) at U13 Pin				Level (TTL) at U21 Pin 1
	2	5	6	7	
None	−0.1 to +0.1	0.6 to 1.1	4.5 to 5.5	0 to 0.5	H
One	2.5 to 4.5	3.0 to 4.3	0 to 0.3	4.0 to 5.5	L

4. Connect a high-impedance, dc coupled oscilloscope to U14D pin 13. Connect the oscilloscope's dc coupled external horizontal input to U13 pin 2. Press then release any key. The dot on the oscilloscope should move as follows:



Hint: The dot should dwell at the intermediate position (2) momentarily after release of the key for 40 to 60 ms.

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⟨√2⟩ Front-Panel Keys and Scanners Check—from Keyboard

NOTE

This check assumes proper operation of the following keys: Shift, SPCL, decimal, and all numeric. Otherwise, use ⟨√3⟩ below which requires a signature analyzer. This check also assumes that the Keystroke Detector works properly (see ⟨√1⟩ above).

1. From Table 8F-87 determine the row of the key to be checked and enter the Direct Control Special Function for that row. (The display should now show 001111.0000.)

Table 8F-87. *Displays, ⟨√2⟩ Step 1*

Direct Control Special Function	Display vs. Key Pressed			
	000111.0000	001011.0000	001101.0000	001110.0000
0.700	>20 kHz	15 kHz	3 kHz	300 Hz
0.710	750 μs	75 μs	50 μs	25 μs
0.720	LOG/LIN	RATIO	AVG	PEAK HOLD
0.730	FREQ	RF POWER	ΦM	FM
0.740	MHz	9	8	7
0.750	kHz ⇑	6	5	4
0.760	kHz ⇓	3	2	1
0.770	SPCL	CLEAR	• (Dec. Point)	0
0.780	50 Hz	LCL	(None)	(None)
0.790	PRE DISPLAY	CALIB	ZERO	(None)
0.7A0	PEAK–	PEAK+	(None)	(None)
0.7B0	AM	S (Yellow)	(None)	(None)
0.7C0	AUTO OPER	AUDIO INPUT	(None)	(None)
0.7D0	TRACK MODE	(None)	(None)	(None)
0.7E0	RANGE HOLD	(None)	(None)	(None)
0.7F0	(Blue)	(None)	(None)	(None)

2. Disable keyboard interrupts by shorting A13TP15 (GND) to A13TP3 (INT) on the A13 Controller Assembly.
3. Pressing any key in the appropriate row of the table should give the display shown. (No key down gives the display 001111.0000. Pressing a key not in the designated row gives this display also.)

NOTE

To repeat step 1 above, it is first necessary to remove the jumper on the Controller.

⟨√3⟩ Front-Panel Keys and Scanners Check—Using Signature Analysis

1. Short A13TP8 (TEST D) to A13TP15 (GND) on the A13 Controller Assembly.
2. Connect the signature analyzer clipleads as follows:

Clock ..... A13TP4 (WRT)
Start ..... A13TP5 (TEST A)
Stop ..... A13TP5 (TEST A)
Ground ..... A13TP15 (GND)

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3. Set the signature analyzer's start, stop, and clock to trigger as follows:

Start	Falling Edge
Stop	Falling Edge
Clock	Rising Edge

4. Set Measuring Receiver's POWER switch to STBY and back to ON. Disregard front panel display readouts.
5. Connect the signature analyzer's probe to A13TP6 (TEST B).
6. Press the front-panel keys and note the signature. The signatures are documented in Figure 8F-33.

   Hint: Pressing keys simultaneously alters the signatures. If no meaningful results can be obtained, continue on with step 7.

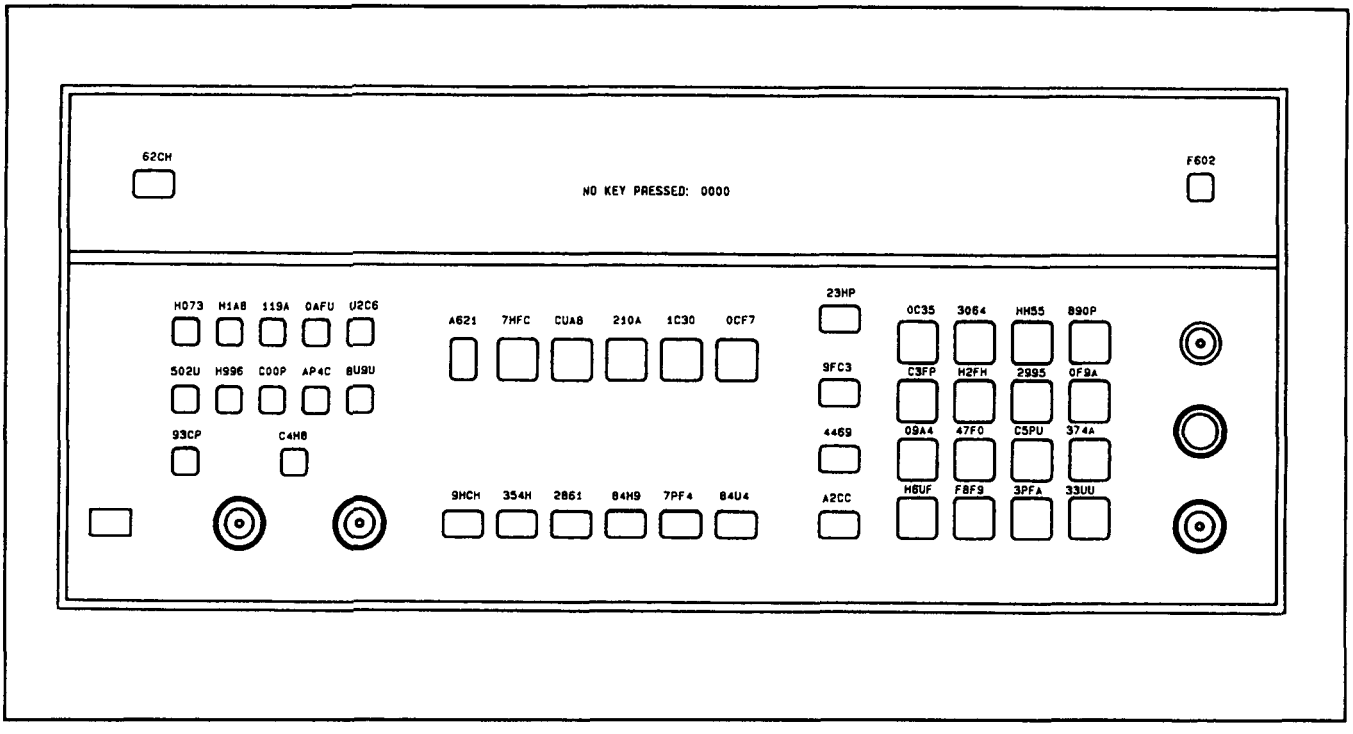


Figure 8F-33. *Signatures,* ⟨√3⟩ *Step 6*

7. Connect the signature analyzer's probe to the points indicated in Table 8F-88 and check the signatures. (No keys should be pressed.)

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Table 8F-88. *Signatures,* ⟨√3⟩ *Step 7*

Pin	U14	U20	U21	U19	Pin
1	U005	24P3	24P3	62AU	1
2	8PAH	U005	1381	F767	2
3	F767	F767	F767	1999	3
4	1381	24P3	24P3	0000	4
5	F767	U005	1381	0000	5
6	AA49	F767	F767	0000	6
7	0000	0000	0000	0000	7
8	AA4P	F767	F767	0000	8
9	AA4P	24P3	24P3	0000	9
10	8PAH	U005	1381	0000	10
11	–	F767	F767	0000	11
12	–	24P3	24P3	0000	12
13	–	U005	1381	FCHA	13
14	24P3	24P3	24P3	F767	14
15	–	–	–	62AU	15
16	–	–	–	24P3	16

Note: The signature for a high or +5V is 24P3. The signature for a low or ground is 0000.

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Service Sheet 26

ASSEMBLY

- **A1 Keyboard and Display (Display Circuits)**

PRINCIPLES OF OPERATION

General

The Keyboard and Display Assembly (A1) contains the front-panel displays and the decoders and latches that control them. Lighting of a display is accomplished by direct decoding of the Instrument Bus with one code sent out for each of the seven segments of the display. For example, to display the digit "3" in display U9 (Digit 7) with no decimal point following, the Controller issues $esd = 66E$, $66D$, $66A$, 669, 666, 665, 663, and 661 in succession. Register U27 decodes the Instrument Bus code and successively outputs and latches the data on the 8D input (that is, d0(L), the least significant bit of the d code) to its internal flip-flops. A low on an output of U27 turns on a segment; a high turns it off. Thus a low appears on the output of flip-flops 1, 3, 5, 6, and 7 (corresponding to $esd = 66D$, 669, 665, 663, and 661) and turns on the LEDs in segments c, d, a, b, and g in U9. A high appears on the output of flip-flops 0, 2, and 4 (corresponding to $esd = 66E$, $66A$, and 666) and turns off segments e and f and the decimal point. This results in a "3" being displayed.

The s code of the Instrument Bus code esd is decoded by U36 and U37. For a general discussion of instrument control, see *Instrument Bus* in Service Sheet BD5.

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TROUBLESHOOTING

General

The procedure for checking the Keyboard and Display Assembly is given below. The circuits are set to a desired (static) state using Direct Control Special Functions. All IC logic levels except the inputs of the displays U3 to U12 are TTL. The inputs of U3 to U12 are about 4.3V when high or 3V when low unless the display diodes are open or shorted. (If the display diodes are open, the input will be 0V in both cases.) Remove the front-panel assembly to gain access to the circuit side of the keyboard.

Equipment

Voltmeter ..... HP 3455A

⟨√1⟩ Display and Decimal Point Check

1. Key in the Direct Control Special Functions listed in Table 8F-89 to turn on the desired display segment or decimal point. (The digit number is the number on the window directly below the digit. See the schematic diagram for identification of segments a through g.)

Table 8F-89. *Displays,* ⟨√1⟩ *Step 1*

Digit Number	Direct Control Special Function
1	0.60d
2	0.61d
3	0.62d
4	0.63d
5	0.64d
6	0.65d
7	0.66d
8	0.67d
9	0.68d
10	0.69d

Segment Displayed	d
a	5
b	3
c	D
d	9
e	F
f	7
g	1
dp	B

Hint: Note that all values of d are odd. If d minus 1 is entered in place of d, the associated segment will turn off. Use of Direct Control Special Function 0.6sd allows only one segment to be lighted at a time; a previously lighted segment will be turned off. However, the previously coded segment will remain off or on until the next special function code is entered and the SPCL key pressed.

Hint: If faulty, check the inputs of the registers (U16 and U22 through U30) driving the displays. Pin 14 of the selected register should be low. Pin 13 should be low to turn on a segment and high to turn it off. The other logic states of the registers are as in Table 8F-90.

Table 8F-90. *Levels,* ⟨√1⟩ *Step 1 Hint*

d	Level (TTL) at Pin		
	1	2	3
1	H	H	H
3	L	H	H
5	H	L	H
7	L	L	H
9	H	H	L
B	L	H	L
D	H	L	L
F	L	L	L

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⟨√2⟩ Select Decoders and Data Line Buffers Check

1. Key in the Direct Control Special Functions indicated in Table 8F-91. For each setting, check the pins on U36 and U37 indicated.

Table 8F-91. *Levels, ⟨√2⟩ Step 1*

Direct Control Special Function	Level (TTL) at U36 or U37 Pin			Level (TTL) at U36-4 or U37-6	Level (TTL) at U36 Pin								Level (TTL) at U37 Pin	
	1	2	3		15	14	13	12	11	10	9	7	15	14
0.600	L	L	L	L	*	H	H	H	H	H	H	H	H	H
0.610	H	L	L	L	H	*	H	H	H	H	H	H	H	H
0.620	L	H	L	L	H	H	*	H	H	H	H	H	H	H
0.630	H	H	L	L	H	H	H	*	H	H	H	H	H	H
0.640	L	L	H	L	H	H	H	H	*	H	H	H	H	H
0.650	H	L	H	L	H	H	H	H	H	*	H	H	H	H
0.660	L	H	H	L	H	H	H	H	H	H	*	H	H	H
0.670	H	H	H	L	H	H	H	H	H	H	H	*	H	H
0.680	L	L	L	H	H	H	H	H	H	H	H	H	*	H
0.690	H	L	L	H	H	H	H	H	H	H	H	H	H	*
* Low-going TTL pulses, approximately 60 ms period.														

2. Check pins 15 through 18 of U15. They should be high.
3. Key in 0.60F SPCL. Recheck pins 15 through 18 of U15. They should be low.

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Service Sheet 27

ASSEMBLY

- **A1 Keyboard and Display (Annunciator Circuits)**

PRINCIPLES OF OPERATION

The Keyboard and Display Assembly (A1) contains the front-panel annunciators and key lamps and the decoders and latches that control them. Lighting of an annunciator or key light is accomplished by direct decoding of the Instrument Bus. For example, to light the FM key light DS24, the Controller issues $esd = 52B$ to the Instrument Bus. $e = 5$ and $s3 = 1$ enable LED Decoder U38. (s3(H), the most significant-bit of s, is high, that is, true.) The three least-significant bits of the s code are decoded by U38 and its 2G output goes uniquely low. This enables register U35. U35 decodes the d code. Inputs d1, d2, and d3 are decoded as a 2 which enables internal flip-flop 2. Input 8D is low (d0(L) is low, that is, true) so the output of flip-flop 2 is low. The low lights DS24.

For a general discussion of instrument control, see *Instrument Bus* in Service Sheet BD5.

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TROUBLESHOOTING

General

The procedure for checking the Keyboard and Display Assembly is given below. The circuits are set to a desired (static) state using Direct Control Special Functions. All IC logic levels are TTL.

Equipment

Voltmeter ..... HP 3455A

⟨√1⟩ Key Light and Annunciator Logic Check

1. Key in the Direct Control Special Functions listed in Table 8F-92 to turn on the desired annunciator or key light.

Table 8F-92. *Annunciators,* ⟨√1⟩ *Step 1*

Direct Control Special Function	Title	Light Type	Direct Control Special Function	Title	Light Type
0.50F	50 Hz	Key Light	0.54F	%	Annunciator
0.50D	300 Hz	Key Light	0.54D	MHz	Annunciator
0.50B	3 kHz	Key Light	0.54B	kHz	Annunciator
0.509	15 kHz	Key Light	0.549	Hz	Annunciator
0.507	>20 kHz	Key Light	0.547	W	Annunciator
0.505	PEAK+	Key Light	0.545	dBm	Annunciator
0.503	PEAK−	Key Light	0.543	dB	Annunciator
0.501	PEAK HOLD	Key Light	0.541	rad	Annunciator
0.51F	PRE DISPLAY	Key Light	0.55F	mV	Annunciator
0.51D	25 μs	Key Light	0.55D	μV	Annunciator
0.51B	50 μs	Key Light	0.55B	REL	Annunciator
0.519	75 μs	Key Light	0.559	V	Annunciator
0.517	750 μs	Key Light	0.557	(None)	
0.515	ZERO	Key Light	0.555	400 Hz	Annunciator
0.513	CALIBRATE	Key Light	0.553	1 kHz	Annunciator
0.511	RMS CAL AVG	Key Light	0.551	LIMIT	Annunciator
0.52F	S (Shift)	Key Light	0.56F	RECAL	Annunciator
0.52D	AM	Key Light	0.56D	AM	Annunciator
0.52B	FM	Key Light	0.56B	FM	Annunciator
0.529	ΦM	Key Light	0.569	ΦM	Annunciator
0.527	RF POWER	Key Light	0.567	LISTEN	Annunciator
0.525	FREQ	Key Light	0.565	TALK	Annunciator
0.523	RATIO	Key Light	0.563	REMOTE	Annunciator
0.521	TRACK MODE	Key Light	0.561	SRQ	Annunciator
0.53F	RANGE HOLD	Key Light	0.57F	UNCAL	Annunciator
0.53D	(Blue)	Key Light	0.57D	(None)	
0.53B	SPCL	Key Light	0.57B	(None)	
0.539	AUDIO INPUT	Key Light	0.579	(None)	
0.537	DISABLE ERROR	Annunciator	0.577	(None)	
0.535	RMS	Annunciator	0.575	(None)	
0.533	dB EXT ATTEN	Annunciator	0.573	f OFS	Annunciator
0.531	AUTO TUNING	Annunciator	0.571	(None)	

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Hint: Note that all values of the d suffix of the Direct Control Special Function codes (0.5sd) are odd. If d minus 1 is entered in place of d, the associated LED will turn off. Use of Direct Control Special Function 0.5sd allows only one LED to be lighted at a time; a previously lighted LED will be turned off.

Hint: If faulty, check the inputs of the registers (U1, U31 through 35, U39,and U40) and buffers (U2, U15, U17, and U18) driving the LEDs. Pin 14 of the selected register should be low. Pin 13 should be low to turn on an LED and high to turn it off. The other logic states of the registers are as in Table 8F-93.

Table 8F-93. *Levels,* ⟨√1⟩ *Step 1 Hint*

d	Level (TTL) at Pin		
	1	2	3
1	H	H	H
3	L	H	H
5	H	L	H
7	L	L	H
9	H	H	L
B	L	H	L
D	H	L	L
F	L	L	L

⟨√2⟩ LED Decoder Check

1. Key in the Direct Control Special Functions indicated in Table 8F-94. For each setting, check the pins on U38 indicated.

   Hint: Pin 4 of U38 should be low; pin 5 should be low-going pulses with a period of approximately 60 ms.

Table 8F-94. *Levels on U38,* ⟨√2⟩ *Step 1*

Direct Control Special Function	Level (TTL) at U38 Pin										
	1	2	3	15	14	13	12	11	10	9	7
0.500	L	L	L	*	H	H	H	H	H	H	H
0.510	H	L	L	H	*	H	H	H	H	H	H
0.520	L	H	L	H	H	*	H	H	H	H	H
0.530	H	H	L	H	H	H	*	H	H	H	H
0.540	L	L	H	H	H	H	H	*	H	H	H
0.550	H	L	H	H	H	H	H	H	*	H	H
0.560	L	H	H	H	H	H	H	H	H	*	H
0.570	H	H	H	H	H	H	H	H	H	H	*
* Low-going TTL pulses, approximately 60 ms period.											

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Service Sheet 28

ASSEMBLY

- **A14 Remote Interface**

PRINCIPLES OF OPERATION

General

The Remote Interface Assembly interfaces the Controller with the HP-IB. It performs the necessary handshake operation, interprets the HP-IB control lines, and is both an input and output peripheral to the Controller. The Remote Interface Assembly consists of three basic elements: the HP-IB I/O, the Handshake Logic, and the Interface Control circuits. In addition, other miscellaneous circuits are used on the assembly. The operation of the three basic elements is explained first. Then, a detailed explanation of how the bus controller (for example, a computing controller) addresses the instrument to talk or to listen is presented. The miscellaneous circuits are then briefly discussed. Table 8F-95 lists and identifies the mnemonics used in the Remote Interface and should be referred to while reading the principles of operation.

Table 8F-95. *Mnemonics for Remote Interface*

Mnemonic	Signal Name
AAD	Acceptor Accepted Data
ACD	Accepted Data
ADS	Addressed
AFC	Address Flip-Flop Clock
ARD	Accepted Received Data
ATL	Addressed to Listen
ATN	Attention
ATT	Addressed to Talk
AVD	Accept Valid Data
CLF	Clear Listen Flip-Flop
CTF	Clear Talk Flip-Flop
DAR	Disable ROM
DAV	Data Valid
DIO1	Data Input/Output 1
DIO8	Data Input/Output 8
DFC	Data Accepted Flip-Flop Clock
EAH	Enable Acceptor Handshake
EIC	Enable Interface Control
ENR	Enable ROM
EOI	End or Identify
ICP	Interrupt CPU

Mnemonic	Signal Name
IFC	Interface Clear
LAD	Listener Accepted Data
LRD	Listener Ready for Data
NDAC	Not Data Accepted
NRFD	Not Ready for Data
RAS	Read Address Selector
RAT	Read Addressing Type
RDR	Reset DAC/RFD
REN	Remote Enable
RFC	REN Flip-Flop Clock
RNL	REN Flip-Flop Latched
RSL	Read Switch Lower
RSU	Read Switch Upper
RTR	Ready to Receive
RVD	Receive Valid Data
SDA	Set Data Accepted
SDV	Set Data Valid
SLF	Set Listen Flip-Flop
SRQ	Service Request
STF	Set Talk Flip-Flop
UUA	Universal Unlisten Address

HP-IB I/O Circuits

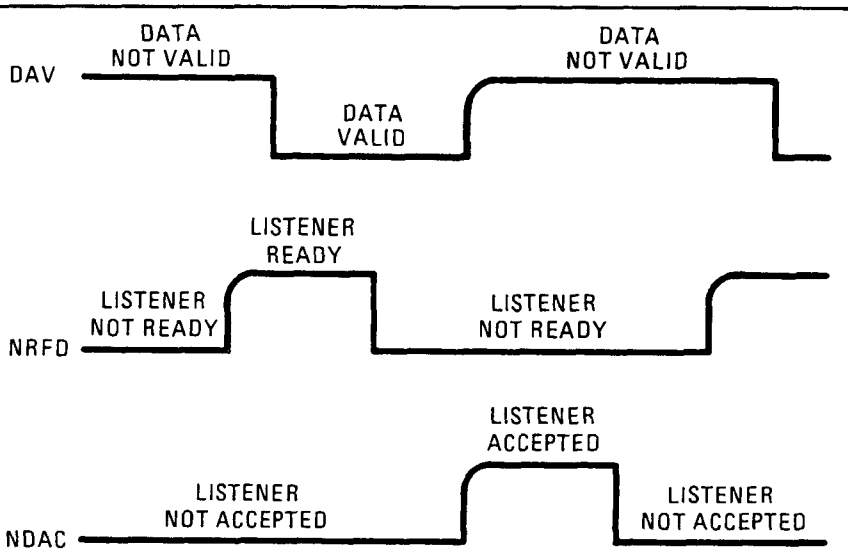
The HP-IB I/O circuits provide bidirectional interface between the Remote Interface assembly and the HP-IB. The circuit consists of U1, U2, U5, and U6. When the TALK(L) line is low, the interface is configured to send data to the HP-IB. In this state, U2 and U6 are disabled, and since they are open collector devices, they are essentially out of the circuit. U1 and U5 provide a direct path from the Peripheral Input/Output (U13) to the HP-IB. When the TALK(L) line is high, the Remote Interface is configured to receive data from the HP-IB. In this mode, U2 and U6 are enabled, and the path through U1 and U5 is reversed. This allows data from the HP-IB to be applied to the Peripheral Input/Output

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configured to receive data from the HP-IB. In this mode, U2 and U6 are enabled, and the path through U1 and U5 is reversed. This allows data from the HP-IB to be applied to the Peripheral Input/Output (U13), the Address Decoder (U8), and the Interface Control ROM (U17). Depending upon the function being performed, this data is either sent to the Controller or used to decode the talk or listen address.

Handshake Logic Circuits

Information is communicated over the HP-IB by means of handshakes between instruments. It is assumed in this discussion that you are familiar with the use of the DAV, NDAC, and NRFD signals as they are used on the HP-IB. (Figure 8F-34 illustrates the handshake.) The instrument can operate as either a talker or a listener when so directed by the bus controller. The primary control circuits in the Handshake Logic are the DAC Flip-Flop (U15B) and gates U12A, U12B, and U19B.



Start with a talker waiting for the listener to release NRFD (not ready for data) indicating it is ready.

When the listener is ready, NRFD goes high (false). The talker then places valid data on DI01 through DI08 and sets DAV (data valid) low (true).

NRFD then goes low (true) and the talker waits for the listener to indicate it has accepted the data (or ingnored it) by releasing the NDAC (not data accpted) to a high (false, that is, data is accepted).

The talker sets DAV high (false) and again waits for the listener to realease NRFD.

NOTE that if ATN is true, all instruments on the bus must handshake regardless of whether they are talkers, listeners, or bystanders. Being in remote or local has nothing to do with handshaking. If ATN is false, they only handshake if addressed.

Figure 8F-34. *Simplified HP-IB Handshake Between a Talker and One Listener*

When the instrument is a listener, the ATL(L) line is low, and the high output from U19B enables U12A and U12B. This condition is also true when ATN(L) goes low and is discussed in detail later. In either case, the DAC Flip-Flop (U15B) controls the handshake. If U15B is set, the RTR(L) line from the reset output is low, and the NRFD(L) line from U12B is high indicating that the instrument is ready to receive data. The ACD(L) line from the active-high output of U15B is high, and (since the other input to U12A is also high), the NDAC(L) line is low. When the bus controller sees all of the required NRFD(L) lines high (more than one instrument can be addressed to listen), it sets DAV(L)

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low. When DAV(L) goes low (indicating the data on the HP-IB is valid), the Interface Control ROM either sets EXT INT low or resets U15B by setting SDA(L) low, depending on whether or not the CPU must be interrupted. See Table 8F-100 for a complete list of the Interface Control ROM input and output signals.) If the CPU is interrupted, it will reset U15B using the DFC(L) line. In either case, ACD(L) goes low and the NDAC(L) line from U12A goes high. When the bus controller sees all of NDAC(L) lines go high, it sets DAV(L) high. The DAV(L) signal is applied through gates U4B, U20B, and U21B to set the DAC Flip-Flop (U15B). Gates U20B and U21B are used to slow down the handshake and prevent a possible race condition. When the DAC Flip-Flop is set, the instrument is returned to a ready-for-data condition.

When the instrument is a talker, the output from U19B is low because both the ATL(L) and the ATN(L) lines are high. The low output from U19B disables U12A and U12B. This prevents the DAC Flip-Flop from driving the NDAC(L) and NRFD(L) HP-IB lines. The Controller (A13) now reads the NDAC(L) line through U4C and U21C and the NRFD(L) line through U4D and U21D. Both of these signals are routed to the Controller through the Peripheral Input/Output (U13). The DAV(L) signal is driven by the Controller through U13 and U12C by the SDV(H) line. U21C is enabled by U20A when the TALK(L) line is low. In the talk mode, the handshaking is entirely controlled by the instrument's firmware and Controller.

Interface Control Circuits

The primary control element in the Interface Control circuits is the Interface Control ROM (U17). U17 is enabled when all the following conditions are satisfied:

1. RTR(L) is low. This indicates the instrument is ready to receive data or commands.

2. EAH(L) is low. This enables an acceptor handshake. It is decoded from the ATL and ATN lines by U20D. Therefore, if the instrument is addressed to listen or if attention is true, the gate is enabled.

3. U19C pin 8 is low. This indicates that the Controller (A23) has enabled the interface to receive data. This state is latched by the flip-flop consisting of U19C and U19D. This flip-flop is also used to disable the Interface Control ROM (U17) when the Remote Interface is preparing to talk. U17 is disabled so that its control circuits do not respond to the data that the instrument itself is sending.

4. AVD(L) is low. This indicates that the bus controller is asserting that the data on the HP-IB is valid by putting DAV(L) low.

When all of these conditions are true, U17 is enabled by setting the EIC(L) line from U20C low. The outputs of U17 are then dependent upon the decoded address line inputs. Depending upon the selected output, the Interface Control ROM will set or clear the appropriate flip-flops, complete a handshake, or interrupt the Controller. The 32 possible states of the output lines are listed and defined in Table 8F-96.

How the Remote Interface Handshakes with the HP-IB

The Remote Interface circuits control the asynchronous transfer of bytes over the HP-IB. The following three conditions require that the instrument complete the handshake requirements:

1. When it is a bystander.

2. When the ATN(L) line is low (true). For example, when the bus controller is addressing the instrument to set it to the talk or listen modes. There are also universal commands that can be sent when ATN(L) is low.

3. When it is already addressed to talk or listen.

The instrument handshakes as a bystander whenever ATN(L) is high and it is not addressed to listen. Actually, this handshake is not an interchange of information because under these conditions the instrument never pulls the NRFD(L) and NDAC(L) output lines low. These lines are held high because ATL(L) and the ATN(L) inputs to U19B remain high. ATL(L) remains high because the instrument is not currently addressed to listen. ATN(L) remains high because it is high at the HP-IB and the signal

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Table 8F–96. *Inputs and Outputs of Interface Control ROM*

Address						Data								Remarks**
Binary Bit Value					Hex	Bit								
16	8	4	2	1		7	6	5	4	3	2	1	0	
Pin Number						Pin Number								
14	13	12	11	10		9	7	6	5	4	3	2	1	
L	L	L	L	L	00	H	*	H	H	H	H	*	L	SCG so AHS only.
L	L	L	L	H	01	H	*	L	H	H	H	*	L	OTA so CTF and AHS.
L	L	L	H	L	02	H	*	H	H	H	H	*	L	OLA so AHS only.
L	L	L	H	H	03	L	*	H	H	H	H	*	H	UBC so INT only.
L	L	H	L	L	04	H	*	H	H	H	H	*	L	SCG so AHS only.
L	L	H	L	H	05	H	*	L	H	H	H	*	L	UNT so CTF and AHS.
L	L	H	H	L	06	H	*	H	H	L	H	*	L	UNL so CLF and AHS.
L	L	H	H	H	07	H	*	H	H	H	H	*	L	NRC so AHS only.
L	H	L	L	L	08	H	*	H	H	H	H	*	L	SCG so AHS only.
L	H	L	L	H	09	H	*	H	L	L	H	*	L	MTA so STF, CLF, and AHS.
L	H	L	H	L	0A	L	*	L	H	H	L	*	H	MLA so SLF, CTF, and AHS.
L	H	L	H	H	0B	L	*	H	H	H	H	*	H	UBC so INT only.
L	H	H	L	L	0C	H	*	H	H	H	H	*	L	SCG so AHS only.
L	H	H	L	H	0D	H	*	L	H	H	H	*	L	UNT so CTF and AHS.
L	H	H	H	L	0E	H	*	H	H	L	H	*	L	UNL so CLF and AHS.
L	H	H	H	H	0F	H	*	H	H	H	H	*	L	NRC so AHS only.
H	L	L	L	L	10	L	*	H	H	H	H	*	H	DATA so INT only.
H	L	L	L	H	11	L	*	H	H	H	H	*	H	DATA so INT only.
H	L	L	H	L	12	L	*	H	H	H	H	*	H	DATA so INT only.
H	L	L	H	H	13	H	*	H	H	H	H	*	L	CDATA so AHS only.
H	L	H	L	L	14	L	*	H	H	H	H	*	H	DATA so INT only.
H	L	H	L	H	15	L	*	H	H	H	H	*	H	DATA so INT only.
H	L	H	H	L	16	L	*	H	H	H	H	*	H	DATA so INT only.
H	L	H	H	H	17	H	*	H	H	H	H	*	L	CDATA so AHS only.
H	H	L	L	L	18	L	*	H	H	H	H	*	H	DATA so INT only.
H	H	L	L	H	19	L	*	H	H	H	H	*	H	DATA so INT only.
H	H	L	H	L	1A	L	*	H	H	H	H	*	H	DATA so INT only.
H	H	L	H	H	1B	H	*	H	H	H	H	*	L	CDATA so AHS only.
H	H	H	L	L	1C	L	*	H	H	H	H	*	H	DATA so INT only.
H	H	H	L	H	1D	L	*	H	H	H	H	*	H	DATA so INT only.
H	H	H	H	L	1E	L	*	H	H	H	H	*	H	DATA so INT only.
H	H	H	H	H	1F	H	*	H	H	H	H	*	L	CDATA so AHS only.

* *Don't care condition.*

** The outputs are active low. The functions of each output are:

Bit 7: INT, interrupts CPU.
Bit 6: Don't care (NC).
Bit 5: CTF, clear Talk Flip-Flop.
Bit 4: STF, set Talk Flip-Flop.
Bit 3: CLF, clear Listen Flip-Flop.
Bit 2: SLF, set Listen Flip-Flop.
Bit 1: Don't care (NC).
Bit 0: AHS, automatic handshake.

Mnemonics used:

CDATA: DATA from Control group
DATA: DATA (interface responds)
MLA: My Listen Address
MTA: My Talk Address
NRC: Non-Recognized Command
OLA: Other Listen Address
OTA: Other Talk Address
SCG: Secondary Command Group
UBC: Universal Bus Command
UNL: Un-Listen
UNT: Un-Talk

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is applied through two inverters (U4E and U21A) to the input of U19B. The resulting low output is applied to U12A and U12B and the NRFD(L) and NDAC(L) lines are always high. In this mode, the Modulation Analyzer is essentially "off the bus". Note that the DAC Flip-Flop (U15B) is also applied to these gates and depending upon its output state would also hold one of the gate outputs high if ATN were true or ATL were true.

When the bus controller wants to address the instrument to talk, ATN(L) is set low. The output of U19B goes high and the status of the NRFD(L) line (U12B) and the status of the NDAC(L) line are controlled by the DAC Flip-Flop (U15B). (The DAC Flip-Flop is already set by DAV(L) being high through U4B, U20B, and U21B). This causes the RTR(L) line from the DAC Flip-Flop to set NRFD(L) high. The bus controller has already placed the instrument's talk address on the bus and it now pulls DAV(L) low indicating that it is valid data.

Since the instrument is not yet addressed to talk, the TALK(L) input to the HP-IB I/O circuits (U1, U5, U2, and U6) is high. The talk address on lines DIO1(L) through DIO5(L) is applied through U1 and U5 to the Address Decoder comparator U8. U8 compares the incoming address with the setting of the first five address switches (S1). If they are the instrument's correct address, the M=N output of U8 goes high. The data on DIO7(L) and DIO6(L) is applied to the Interface Control ROM (U17) to determine whether the instrument is being addressed to talk or to listen. If it is being addressed to talk, DIO7(L) is low and DIO6(L) is high (that is, 10). If it is being addressed to listen, DIO7(L) is high and DIO6(L) is low (that is, 01). These two bits are the only difference between the DIO inputs from the bus controller to the instrument when it is being set to talk or listen.

The EIC(L) from U20C is low to enable U17 and the other inputs to the address lines of U17 select the memory locations that will set output pin 5 to low. The STF(L) line sets the Talk Flip-Flop U16A. At the same time, the SDA(L) output at pin 1 of U17 is low and resets the DAC Flip-Flop (U15B). The low output from pin 9 of U15B is applied to U12A and the NDAC(L) line goes high, indicating that the handshake is complete. Note that the CPU did not need to be interrupted.

Remote Enable Flip-Flop

When the instrument is addressed to listen, the CPU is interrupted and must determine whether or not it has been enabled to the remote mode (or whether it is already in the remote mode). The Controller does this by attempting to set the Remote Enable Flip-Flop (U15A). If the REN(L) line on the HP-IB is low (true), it is inverted by U4F and the reset input to U15A pin 1 is high. In this case U15A can be set by the Controller. Conversely, if REN(L) is high, the reset input is low and U15A is held reset. The Controller checks the set output of U15A RNL(H) through inverter U22A and the Peripheral Input/Output (U13). If the instrument receives its listen address and if the output of U15A is high, it enters remote mode and lights the REMOTE annunciator on the front panel.

Serial Poll Enable Flip-Flop

When the Controller recognizes the SPE (Serial Poll Enable) bus command, the CPU is interrupted and attempts to set the Serial Poll Flip-Flop (U3B). IFC(L) from the HP-IB is applied through U4A and U22D to the reset input of U3B. If IFC(L) is high, the Serial Poll Flip-Flop can be set; if it is low U3B is held reset. If U3B is set, the instrument enters the serial poll mode, and this information is read back via the Instrument Bus to the Controller through U9D. When the instrument is subsequently addressed to talk, it again reads back the output of U3B to determine what information to output to the HP-IB: measurement results or the status byte. If it is still in the serial poll mode, the status byte is output. When the SPD (Serial Poll Disable) bus command is received, the Controller resets U3B.

Other Control Lines

The remaining HP-IB control lines to the instrument are EOI(L), SRQ(L), and IFC(L). EOI(L) is not used by the instrument and is terminated in R7N and R7P. SRQ(L) is output to the HP-IB under Controller direction through U13. IFC(L) is used to clear all talkers and listeners off the HP-IB. IFC(L) is buffered into four lines. At the output of U4A, after CR1, one line is applies to the Address Comparator (U8) to disable it. This keeps the Interface Control ROM (U17) from affecting either the

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Talk or Listen Flip-Flop while IFC is true. Two additional lines (from U21E and U21F) clear the Talk and Listen Flip-Flops (U16A and U16B). The fourth line (from U22D) clears the Serial Poll Flip-Flop.

Address Readback Circuit

When so directed by the operator, the Controller sequentially reads back the status of the Address Switches (S1A through S1E) and the talk-only and listen-only switches (S1G and S1F). This information is processed through gates U9 and U10 under control of the RSU(L) and RSL(L) lines from the Select Decoder (U11). The Controller's internal RAM is also read for service request (SRQ) status. The front-panel display shows not only the HP-IB address and the talk-only or listen-only status, but also whether or not it is issuing a Service request (SRQ). (See *Special Function 21* in Section 3 of the *Operation and Calibration Manual.*)

Peripheral Input/Output

The Peripheral Input/Output (U13) provides the required I/O interface between the Controller and the HP-IB. Refer to Table 8F-97 for a description of inputs and outputs of U13.

Select Decoder

For a general discussion of instrument control, see *Instrument Bus* in Service Sheet BD5.

Table 8F-97. *Inputs and Outputs of the PIO (U13)*

Pin Name	Description	Type
I/OA0 thru I/O A7	I/O Port A	Input/Output
I/O B0 thru I/O B7	I/O Port B	Input/Output
DB0 thru DB7	Data Bus Lines	Bi-Directional (3 state)
ROMC0 thru ROMC4	Control Lines	Input
Φ, WRITE	Clock Lines	Input
EXT INT	External Interrupt	Input
PRI IN	Priority In	Input
PRI OUT	Priority Out	Output
INT REQ	Interrupt Request	Output
DBDR	Data Bus Drive	Output

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TROUBLESHOOTING

General

Procedures for checking the Remote Interface Assembly are given below. The circuits to check are marked on the schematic diagram by a hexagon with a check mark and a number inside, for example, ⟨√3⟩ . In addition, any points outside the labeled circuit area that must be checked are also identified. Extend the board assembly where necessary to make measurements.

CAUTION

MOS and CMOS ICs can be damaged by static charges and circuit transients. Do not remove this assembly from the instrument while power is applied. Discharge the board and replacement IC to the same potential. (Use a conductive foam pad such as HP 4208-0094.) When unplugging ICs, place the board on a conductive pad. When the IC is unplugged, insert it into the pad also.

Several ICs on this assembly are held in high-grip sockets. Both the socket and the device can be damaged if an attempt is made to remove the device with an IC extraction tool. The recommended procedure is to first ground the tip of a small blade-type screwdriver, then slide the tip between the IC and the socket and slowly pry up the IC one pair of pins at a time.

The following checks use the *HP-IB Functional Checks* in the Section 3 (refer to paragraph 3-13) as a basis for troubleshooting the Remote Interface Assembly. It is assumed in the following procedures that the failure was detected during the functional checks. Therefore, it is only necessary to perform the troubleshooting procedures starting with the equivalent functional check in which the failure occurred. During the procedures, the 61.N Service Special Functions are also used to help locate the failure.

When using the troubleshooting flowcharts, it is important that the associated notes be read. These notes help clarify the steps that are flagged. The troubleshooting procedures assume that the bus controller and the bus controller's HP-IB interface are operating properly. Therefore, it is assumed that the required inputs are present at the interface to the Measuring Receiver. Always perform all of the HP-IB Functional Checks after any repair to the Remote Interface Assembly.

When using the flowcharts, refer to the principles of operation to clarify the sequence of troubleshooting. Refer to Figure 8F-34 for an explanation of the HP-IB handshake. If replacement of a probably defective part does not correct the Remote Interface problem, check any related circuits that are connected to the faulty area. For example, some bus controllers simultaneously function as both talker and listener. As a result, they may mask a failure of the Remote Interface handshaking capabilities. This can happen when either the NRFD or NDAC output driver on the bus fails in a high state. This type of failure is a very subtle problem. The quickest way to determine what is happening is to monitor the driver outputs while activating both output levels of the individual drivers.

Equipment

Digital Test/Extender Board ..... HP 08901-60081
Logic Probe ..... HP 5005A
Oscilloscope ..... HP 1740A

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NOTE

The following are the notes for Figures 8F-35 through 8F-38.

1. The Run indicator shows the status of the handshake between the bus controller and the Measuring Receiver. If it is still on, the handshake was not completed.

2. This Special Function reads back and displays the present state of the Talk and Listen Flip-Flops. (See 61.N Display HP-IB Status *in paragraph 8-7.)*

3. This Special Function reads back and displays the present state of the ATN bus control line and the state of the Remote Enable Flip-Flop.

4. X equals "don't care".

5. If TP9 is low, the handshake logic has satisfied the initial requirements to input address data into the Interface Control ROM. If TP9 is high, this requirement is not complete.

6. Displays HP-IB address set on the Address Switches.

7. Remember that the checkout procedure assumes that the Measuring Receiver is set to address 14. If the instrument has been set for a different address, modify the HP-IB Functional Checks *procedure and the troubleshooting information to match the new address.*

8. Indicated IC is the most likely malfunction. However, if replacement does not fix the problem, check the circuits that drive or are driven by the specified IC and all wiring and components that are connected to the same signals.

9. See Figure 8F-34 for a simplified explanation of the HP-IB Handshake.

⟨√1⟩ Address Recognition Check

1. Perform the steps shown in the *Address Recognition Troubleshooting Flowchart,* Figure 8F—35.

⟨√2⟩ Remote and Local Messages and the LCL Key Check

1. Perform the steps shown in the *Remote and Local Messages and the LCL Key Troubleshooting Flowchart,* Figure 8F-36.

⟨√3⟩ Sending the Data Message Check

1. Perform the steps shown in the *Data Message Troubleshooting Flowchart,* Figure 8F-37.

⟨√4⟩ Receiving the Data Message Check

1. Perform the *Receiving the Data Message* portion of the *HP-IB Functional Checks.*

   Hint: Most of the circuits that are used in this check were used in previous checks. Check the inputs and outputs of gates U2 and U6. If they are good, the problem could be U13 (PIO), the Controller (see Service Sheet 24), or the annunciators (see Service Sheet 27).

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⟨√5⟩ Local Lockout and Clear Lockout/Set Local Messages Check

1. Perform the *Local Lockout and Clear Lockout/Set Local Messages* portion of the *HP-IB Functional Checks.*

   Hint: Most of the circuits that are used in this check were used in previous checks. If the instrument fails this check, the problem is probably in the Controller (see Service Sheet 24) or the front-panel keyboard circuits (see Service Sheet 25).

⟨√6⟩ Clear Message Check

1. Perform the *Clear Message* portion of the *HP-IB Functional Checks.*

   Hint: The circuits that are used in this check were used in previous checks. If a problem occurs during the check, repeat the previous checks starting at ⟨√1⟩ *Address Recognition Check.*

⟨√7⟩ Abort Message Check

1. Perform the *Abort Message* portion of the *HP-IB Functional Checks.*

   Hint: Most of the circuits that are used in this check were used in previous checks. The flowchart (Figure 8F-38) is primarily used to check the IFC and serial-poll circuits.

⟨√8⟩ Status Byte Message Check

1. Perform the *Status Byte Message* portion of the *HP-IB Functional Checks.*

   Hint: Most of the circuits that are used in this check were used in previous checks. The most important difference is that the Controller must recognize that the Serial Poll Flip-Flop is set and send the status byte when addressed to talk.

⟨√9⟩ Require Service Message

1. Perform the *Require Service Message* portion of the *HP-IB Functional Checks.*

   Hint: Most of the circuits that are used in this check were used in previous checks. The most important difference is that the Controller must drive the SRQ(L) line low. It does this through gate U12D and the PIO (U13). Repeat the check and monitor the input and output of U12D.

⟨√10⟩ Trigger Message and Clear Key Triggering

1. Perform the *Trigger Message and Clear Key Triggering* portion of the *HP-IB Functional Checks.*

   Hint: Most of the circuits that are used in this check were used in previous checks. The most important difference is that the Controller must recognize that the CLEAR key can be used to trigger the instrument. The problem is probably in the Controller (see Service Sheet 24) or the CLEAR key circuit (see Service Sheet 25).

⟨√11⟩ Select Decoder and Address Switches Check

1. Key in the Direct Control Special Functions indicated in Table 8F-98. For each setting, check the pins on U11 indicated.

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Table 8F–98. *Select Decoder Outputs,* ⟨√11⟩ *Step 1*

Direct Control Special Function	Level (TTL) at U11 Pin							
	15	14	13	12	11	10	9	7
0.400	*	H	H	H	H	H	H	H
0.410	H	*	H	H	H	H	H	H
0.420	H	H	*	H	H	H	H	H
0.430	H	H	H	*	H	H	H	H
0.440	H	H	H	H	*	H	H	H
0.450	H	H	H	H	H	*	H	H
0.460	H	H	H	H	H	H	*	H
0.470	H	H	H	H	H	H	H	*

2. Key in 0.450 SPCL to read back part of S1. The left display should be of the form *abcd* where

   a=1 if S1D is open;
   b=1 if S1C is open;
   c=1 if S1B is open;
   d=1 if S1A is open.

3. Key in 0.460 SPCL to read back the rest of S1 and U3B. The left display should be of the form *abcd* where

   a=1 if U12B is set;
   b=1 if S1G is open;
   c=1 if S1F is open;
   d=1 if S1E is open.

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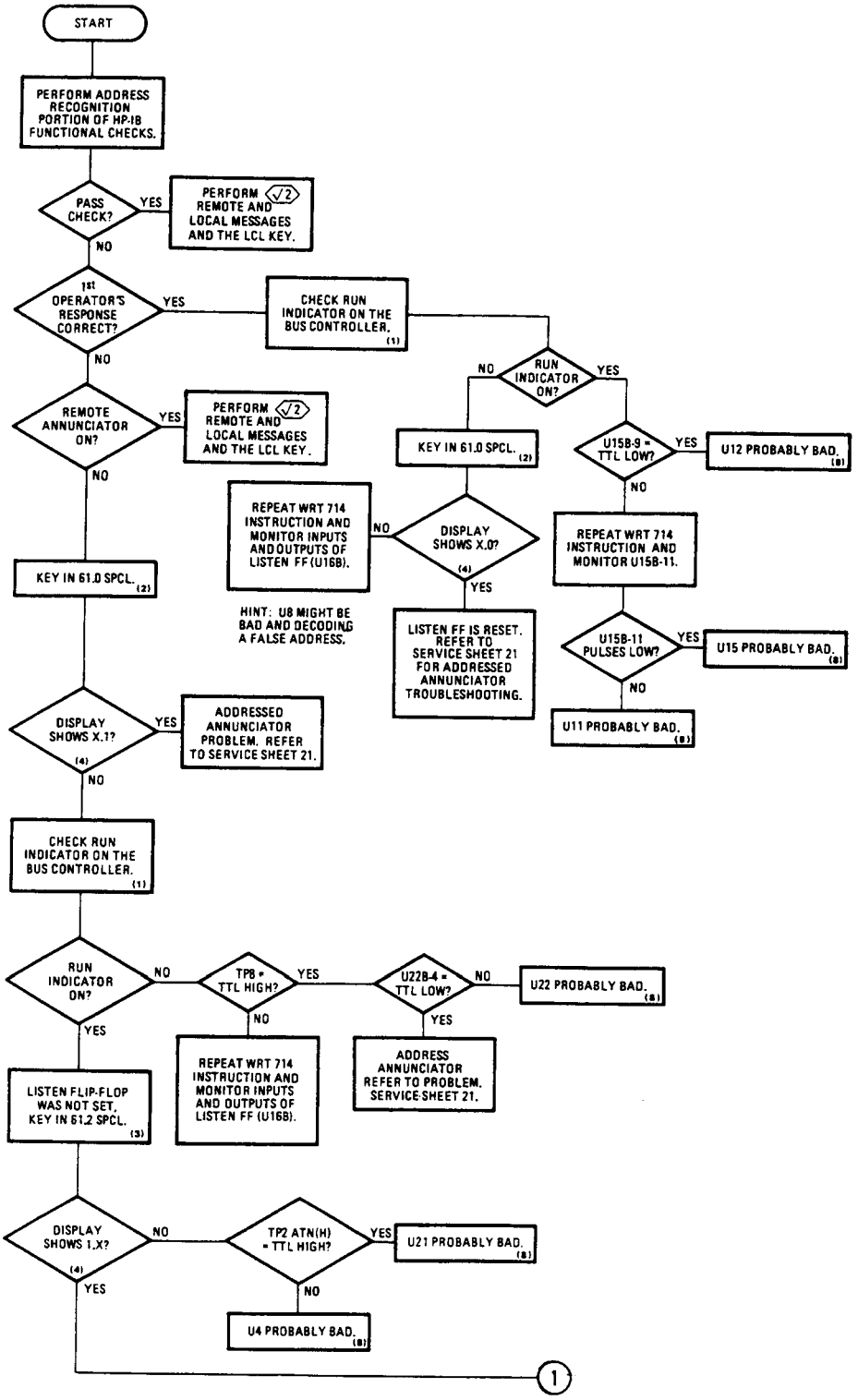


Figure 8F–35. *Address Recognition Check Troubleshooting Flowchart,* √1 *(1 of 2)*

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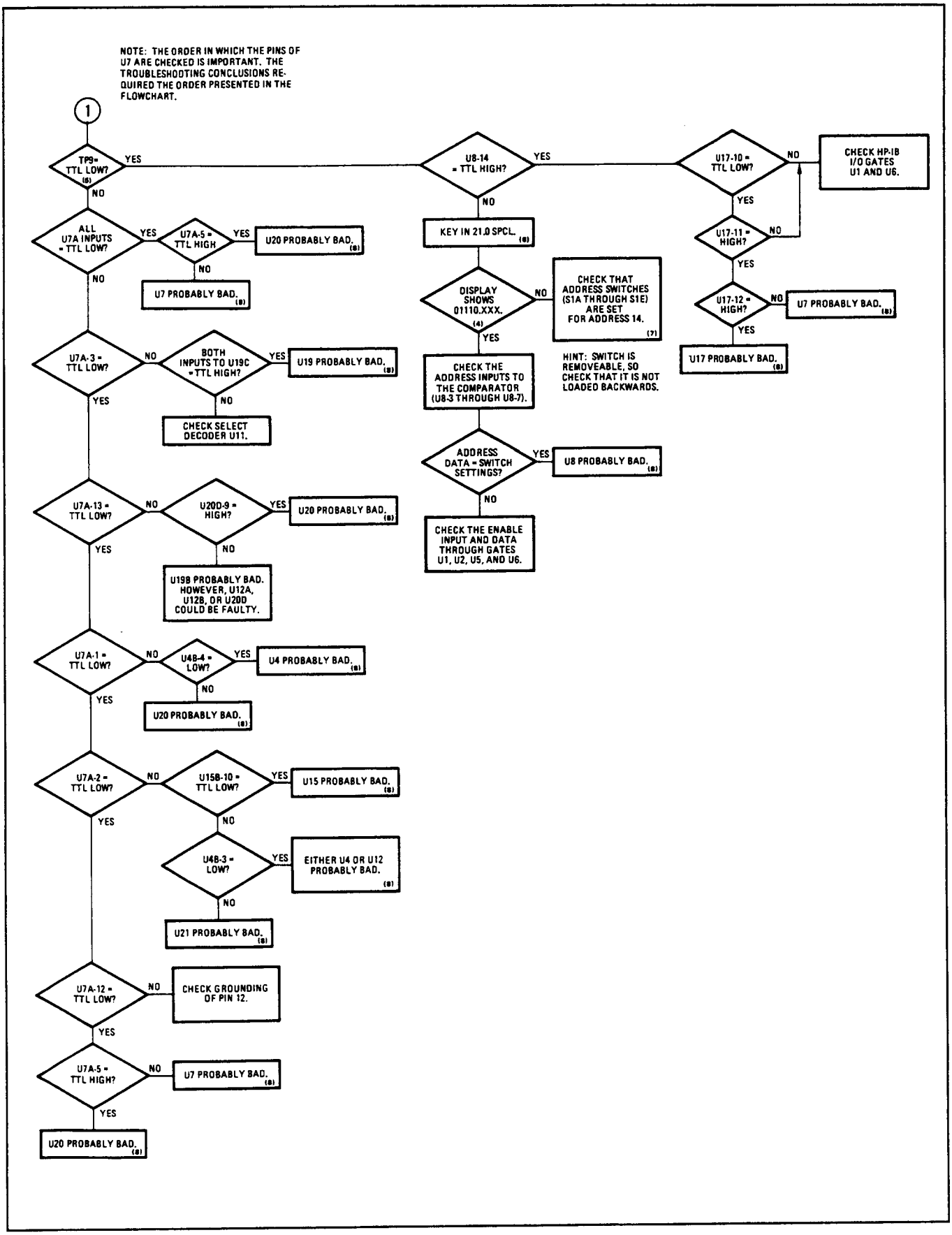


Figure 8F–35. *Address Recognition Check Troubleshooting Flowchart,* ⟨√1⟩ *(2 of 2)*

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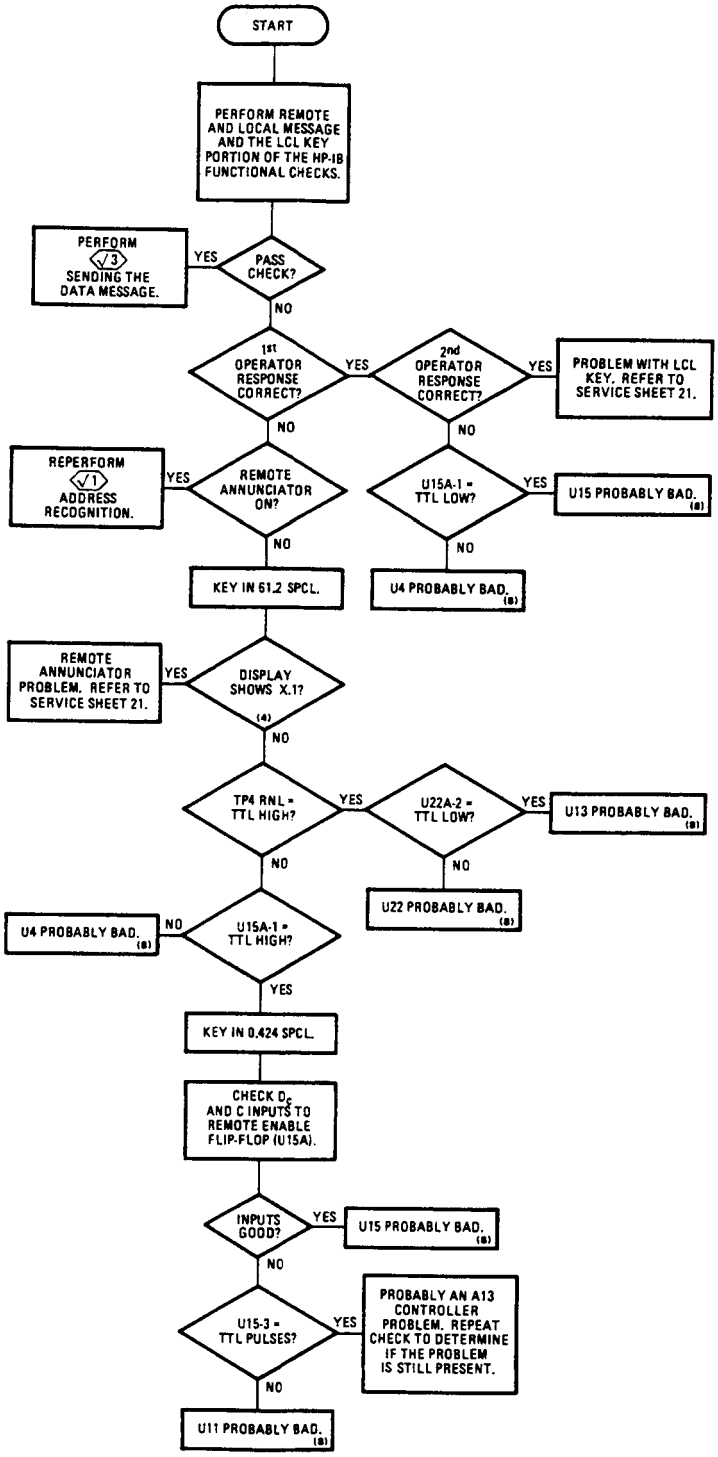


Figure 8F–36. *Remote and Local Message and the LCL Key Check Troubleshooting Flowchart,* √2

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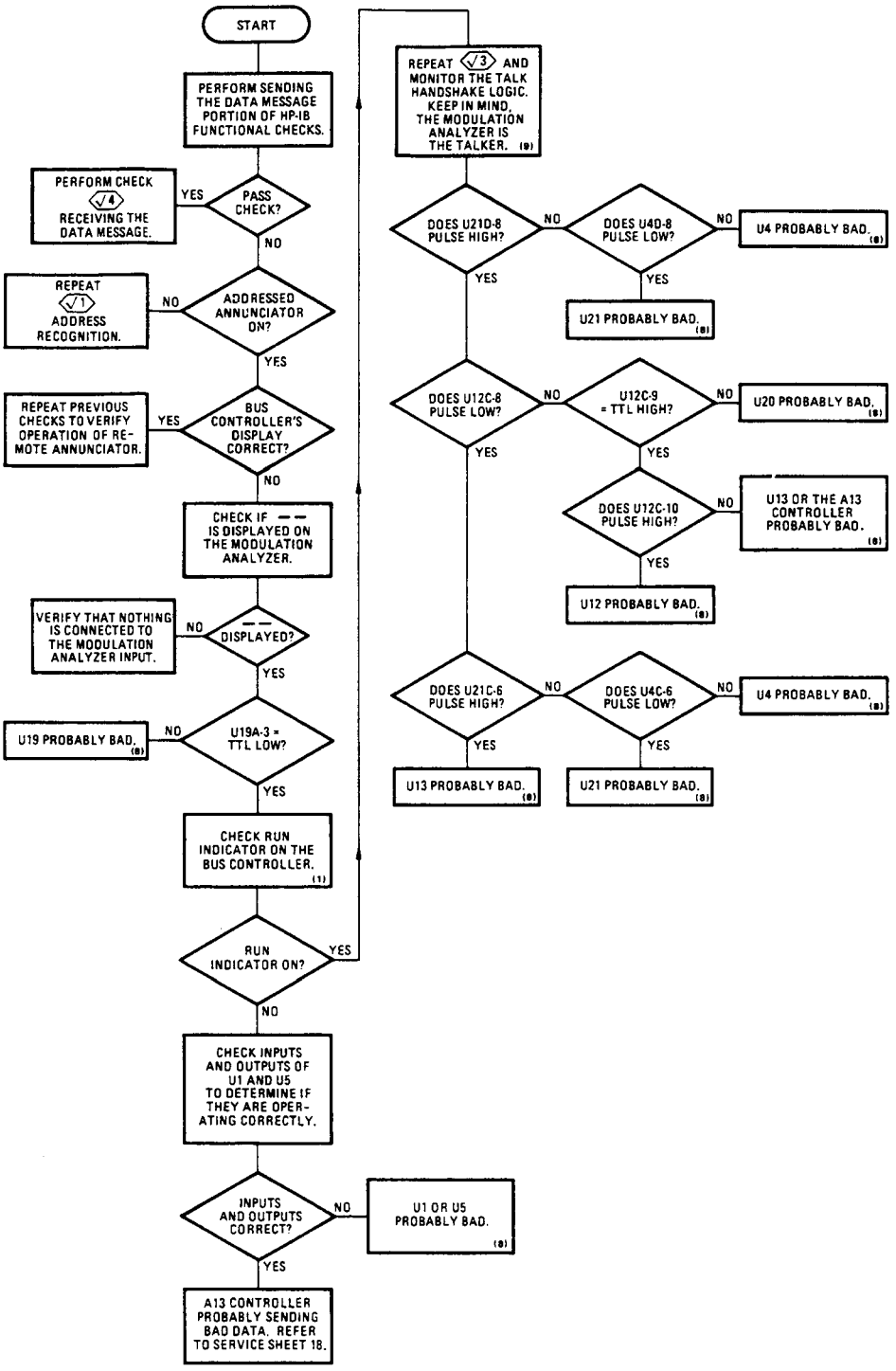


Figure 8F–37. *Sending the Data Message Check Troubleshooting Flowchart,* √3

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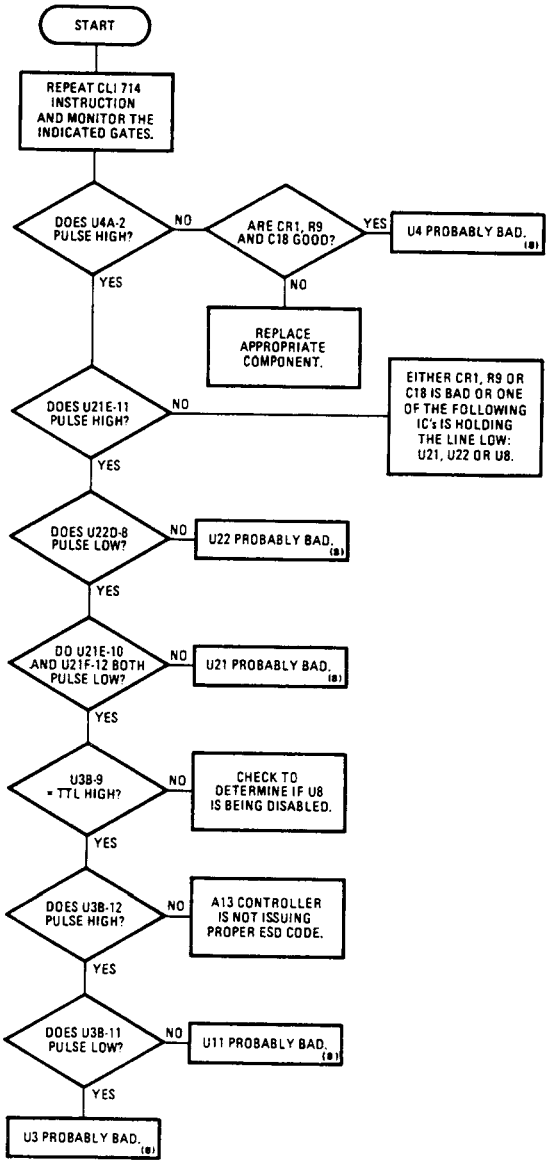


Figure 8F–38. *Abort Message Check Troubleshooting Flowchart,* ⟨√7⟩

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Service Sheet 29

ASSEMBLY

- **A51 FM Calibrator**

PRINCIPLES OF OPERATION

General

The FM Calibrator provides a 10.1 MHz signal with an amount of FM which can be determined by the Controller. It also is the source of RF for the AM Calibrator (see Service Sheet 30).

10.1 MHz VCO and Output Amplifier

The 10.1 MHz Voltage Controlled Oscillator (VCO) is Colpitts type. Q7 provides the gain necessary for oscillation. The tank circuit is composed of the series combination of C16 and C17 in parallel with CR3, CR5, CR6, C20, and L7 in series with L6. Varactor diodes CR3, CR5, and CR6 tune the oscillator approximately 68 kHz peak-to-peak. Q8 is a temperature-compensated current source for the emitter of Q7. Q2 provides a regulated, positive supply for the oscillator and the varactor cathodes; it has a thermal characteristic which compensates for the frequency drift caused by the varactor diodes. C18 and C19 assure that the supply has a low ac impedance. Current source Q4 provides a stable reference voltage across R32 for the base of Q2.

The output from the oscillator, taken from the inductive divider L6 and L7, is buffered by differential pair Q6 and Q1 and drives the AM Calibrator. The base of Q1 is referenced to the output of the Oscillator Collector Supply. Q2 is a constant-current source for the emitters of Q1 and Q6. Q5 is a common-base isolation amplifier which drives the Counter Buffer (U9).

Trapezoid Generation Circuits

The trapezoid generation circuits create a 10 kHz trapezoidal wave form with rounded corners that drives the varactor diodes of the 10.1 MHz VCO. The waveform must rise and fall to full value with a transition time that causes no ringing when the FM signal is demodulated by the FM Demodulator and fed through the audio circuits which have been set for maximum bandwidth. In generating the trapezoidal waveform, a triangle wave is first generated then limited.

Several points in the triangle generation circuits require stable reference voltages. The basic reference is a temperature-stable reference diode VR2. The reference is fed from current source Q13, which itself is temperature stable because its base-emitter junction and its reference (VR1) have similar thermal behavior. The output of the Voltage Reference (taken with respect to the −15V(F) supply) is divided by two by R7 and R8 and converted into a constant current by Current Source U2 and Q11 and by U1 and Q10.

U1 produces a constant voltage across R14 which then generates a constant current. This current also flows through R11, R12, and R13 to produce a constant, but adjustable, voltage at the non-inverting (+) input of U3. U3 is a voltage follower which provides the reference (approximately −5 Vdc) to the non-inverting input of U4.

The Triangle Generator is an integrator configured as a relaxation oscillator. U4 and C11 form the integrator. When the active-high output of U5A is high (that is, 0V), the 5V developed across R19 produces a constant current which, being integrated, produces a negative-slope ramp at the output of U4. Conversely, when the output of U5A goes low (that is, −10V), the 5V of opposite polarity developed across R19 produces a positive-slope ramp at the output of U4.

The output of U4 is compared with two references; namely, ground by U6B and −10V by U6A. When the negative-slope ramp reaches −10V, U6A switches from low to high and resets (the formerly set)

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U5A. The ramp now slopes positively and U6A releases its reset on U5A. When the positive-slope ramp reaches 0V, U6B switches from low to high and sets U5A. The ramp now slopes negatively and U6B releases its set on U5A. Thus, a triangle wave is generated at the output of U4. If the non-inverting input of U6C or U6D is high, the effect of U6B or U6A is overridden and U5A is held either with a set or a reset. U4 falls or rises until CR7 and VR3 or CR8 and VR4 come on and clamp the output of U4 at approximately −10 or 0V.

The triangle wave from U4 is attenuated by a factor of 14 by R21 and R22 and then amplified and limited by the Trapezoid Generator. The Trapezoid Generator is a differential pair, Q9A and Q9B, which has a gain of 1.3 (that is, one-half the ratio of R27 to the sum of R26 and the emitter resistance of Q9A) when both Q9A and Q9B are active. The triangle's positive-going slope turns on Q9B fully, which turns off Q9A. The resulting 0V on the collector of Q9A tunes the VCO to the low end of its range. The negative-going slope turns Q9B off, which allows all of the current from Q11 to flow through Q9A. This produces a negative voltage limit at the collector of Q9A. The resulting −0.33V tunes the VCO to the upper end of its range. The large emitter resistors (R23 and R26) round the waveform as the limits of the output voltage are reached.

−10V Regulator

The −10V Regulator drops the level of the −15V Supply and is the negative supply for U5A.

Select Decoder and Data Latch

For a general discussion of instrument control, see *Instrument Bus* in Service Sheet BD5.

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TROUBLESHOOTING

General

Procedures for checking the FM Calibrator Assembly are given below. The circuits to check are marked on the schematic diagram by a hexagon with a check mark and a number inside, for example, ⟨√3⟩. In addition, any points outside the labeled circuit area that must be checked are also identified. Fixed signals are also shown on the schematic inside a hexagon, for example, ⟨+1.9 TO +2.1 VDC⟩. Extend the board assembly where necessary to make measurements.

CAUTION

Tighten SMC connectors to 0.6 N·m (5 in·lb). Hand tightening of connectors is insufficient. Hand-tightened connectors can work loose and cause reduced performance or malfunctions.

Equipment

Oscilloscope ..... HP 1740A
Voltmeter ..... HP 3455A

⟨√1⟩ Trapezoid Generation Circuits and Mode Control Check

1. Measure pin 3 of U1 with a dc voltmeter. The voltage should be between −12.3 and −11.5 Vdc.
2. Measure the collector of Q10 with a dc voltmeter. The voltage should be between −10.6 and −9.6 Vdc.
3. Measure pin 6 of U3 with a dc voltmeter. The voltage should be between −5.4 and −4.7 Vdc.
4. Key in the Direct Control Special Functions indicated in Table 8F-99. For each setting, check the points indicated with a high-impedance, dc coupled oscilloscope.

Table 8F-99. *Levels, ⟨√1⟩ Step 4*

Direct Control Special Function	Voltage Level (Vdc) at			
	U5A pins 4 and 6	U5A Pin 1	A51TP3	A51TP2
0.191	−10.5 to −9.5	−10.5 to −9.5	+0.6 to +1.0	−0.01 to 0
0.192	−10.5 to −9.5	−0.1 to 0	−10.9 to −10.3	−0.35 to −0.31
0.193	See Fig. 8F-39	See Fig. 8F-40	See Fig. 8F-41	See Fig. 8F-42

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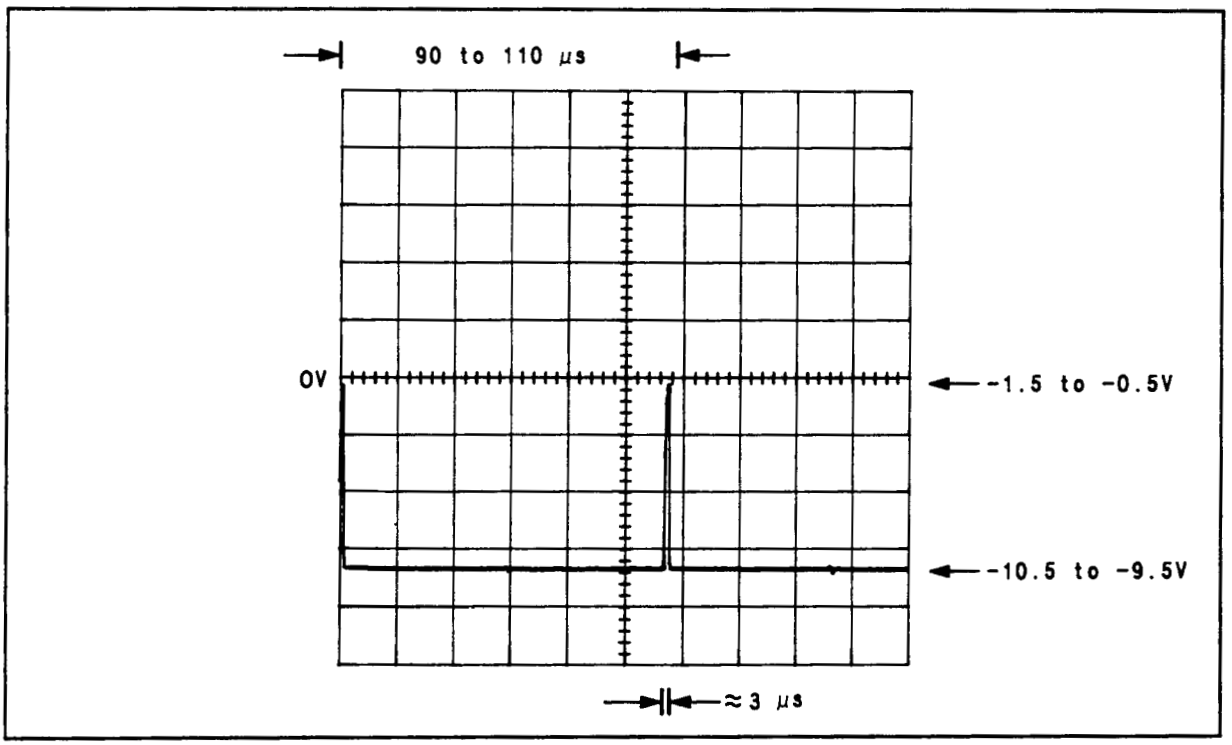


Figure 8F–39. *Waveform for ⟨√1⟩ Step 4 (U5A pins 4 and 6)*

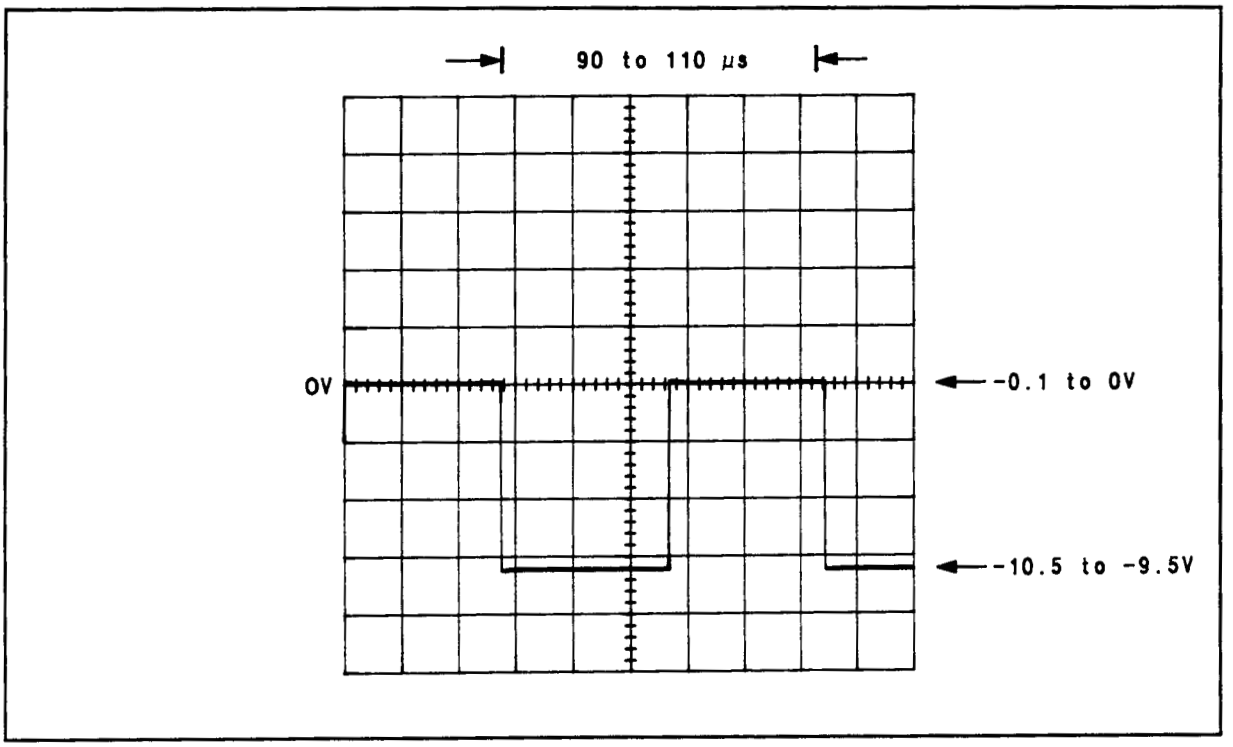


Figure 8F–40. *Waveform for ⟨√1⟩ Step 4 (U5A pin 1)*

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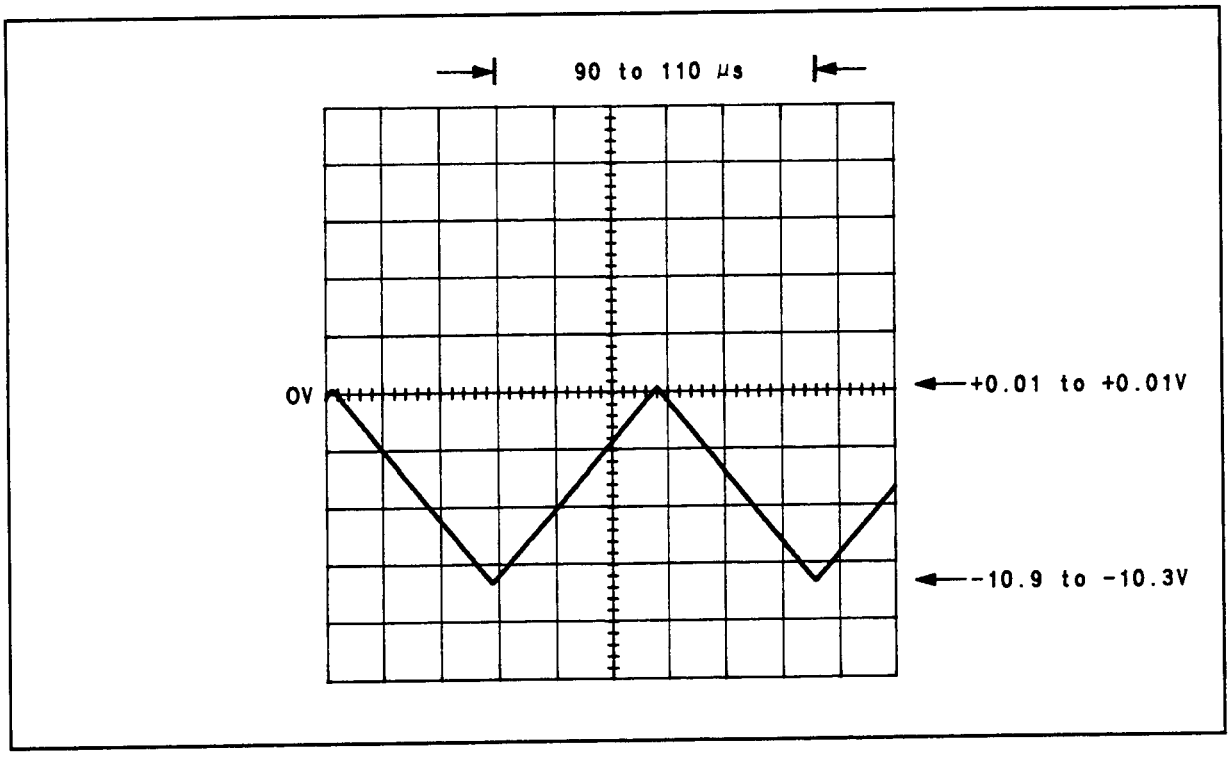


Figure 8F–41. *Waveform for* ⟨√1⟩ *Step 4 (A51TP3)*

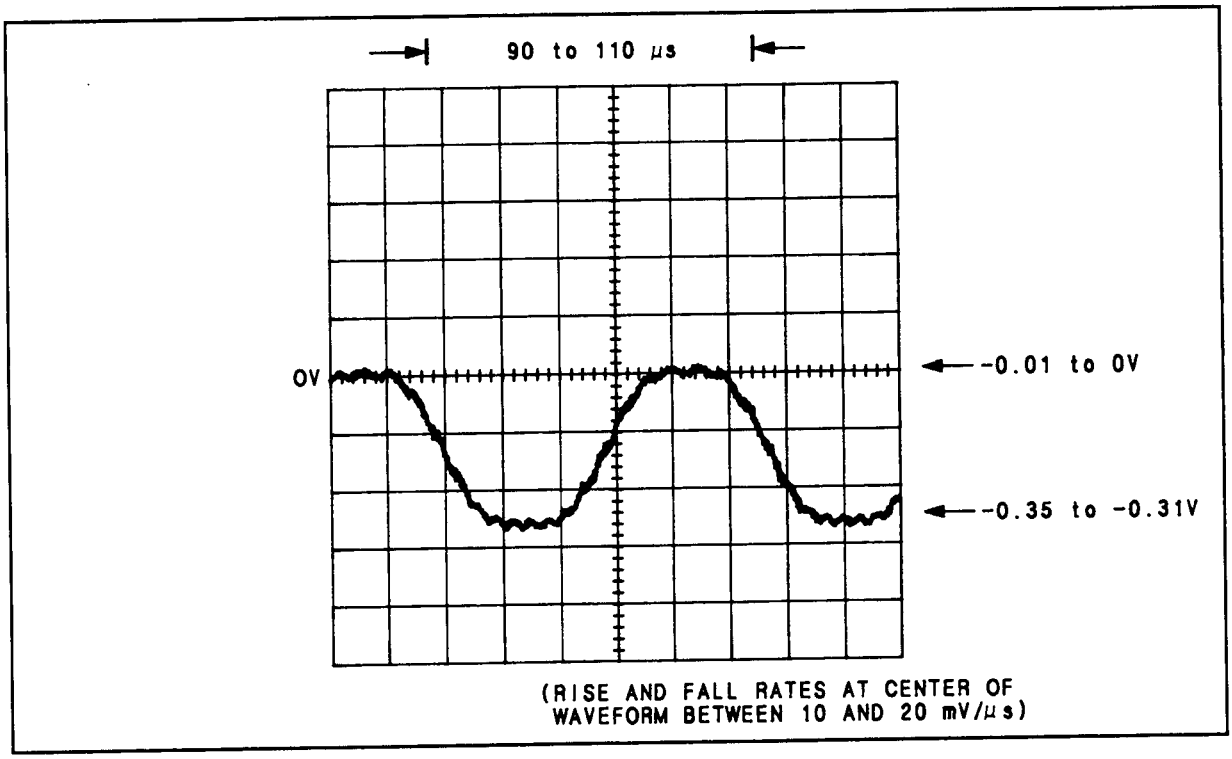


Figure 8F–42. *Waveform for* ⟨√1⟩ *Step 4 (A51TP2)*

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⟨√2⟩ 10.1 MHz VCO, Output Amplifier, and Counter Buffer Check

1. Connect an ac coupled oscilloscope to A51J1 (10 MHz OUT). Switch the input of the oscilloscope to 50Ω or terminate the input in 50Ω using a tee.
2. Key in 0.191 SPCL to set the VCO frequency to low. The oscilloscope waveform should be as in Figure 8F-43.
3. Connect a high-impedance, dc coupled oscilloscope to A51J2 (10 MHz OUT). The oscilloscope input should have a low-capacitance 10:1 divider probe. The waveform should be a TTL-compatible square wave.
4. Connect W19 to A51J2. Use an extender cable if necessary to make the connection.
5. Key in 0.191 SPCL then 46.3 SPCL to set the 10.1 MHz VCO frequency to low and read it with the internal counter. The display should read between 1009000 and 1011000.

   Hint: If the display is grossly in error but the period of step 2 is correct, check the counter. If the display is only slightly in error, perform Adjustment 9—FM Calibrator. The voltage at A51TP2 (TRAPEZOID OUT) should be between −10 and 0 mVdc.
6. Key in 0.192 SPCL then 46.3 SPCL to set the frequency to high and read it. The display should read 6000 to 7600 higher than in step 5.

   Hint: The voltage at A51TP2 should be between −350 to −310 mVdc.
7. Reinstall A51 and secure it with its screws. Reconnect the cables to A51. Reconnect any other assemblies in their normal configuration. Connect CALIBRATION AM/FM OUTPUT to INPUT.

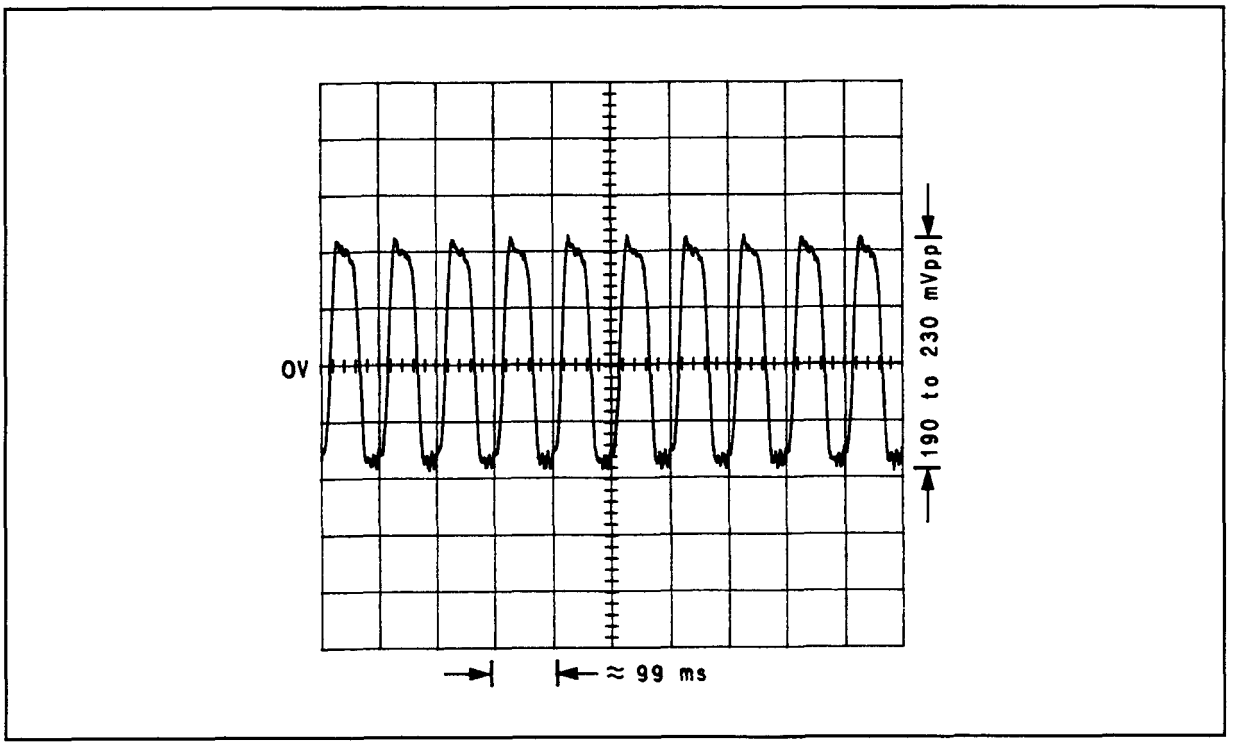


Figure 8F–43. *Waveform for* ⟨√2⟩ *Step 2*

8. Key in 12.1 SPCL to measure the residual FM of the FM Calibrator. The display should read 0.110 kHz or less.

   Hint: If residual FM is excessive, change VR6 then VR5, Q7, and Q2 as first tries.

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⟨√3⟩ Select Decoder and Data Latch Check

1. Key in 0.190 SPCL.
2. Check pin 1 of U7 with a high-impedance, dc coupled oscilloscope. The waveform should be low-going TTL pulses with a period of approximately 60 ms.
3. Check pins 11, 15, and 16 of U8. Pins 15 and 16 should be TTL low; pin 11 should be the complement of the waveform in step 2.
4. Key in 0.193 SPCL. Pins 15 and 16 of U8 should be TTL high.

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Service Sheet 30

ASSEMBLY

- **A50 AM Calibrator**

PRINCIPLES OF OPERATION

General

The AM Calibrator provides a 10.1 MHz signal with an AM depth which can be determined by the Controller. The output of the calibrator appears at the CALIBRATION AM/FM OUTPUT connector.

Input and Modulator Circuits

The source of RF for the AM Calibrator is a 10.1 MHz signal from the FM Calibrator (see Service Sheet 29). This signal is amplified and limited by differential pair Q1B and Q1D and emitter-follower Q2. C8 provides an ac short for the emitters of Q1B and Q1D. The emitter current, which is switched back and forth between Q1B and Q1D, is supplied by current source Q1A.

The limited RF signal is split into two nearly identical paths containing the two modulators. The outputs from the modulators are then summed together to produce the modulated signal. Using the path through Modulator A as an example, the RF signal is amplified by Q3 which switches CR1 and CR3 on and off at the RF rate. The node between the cathodes of CR3 and CR5 is supplied with a current from the A Current Source (Q11). When the output from Q3 switches CR1 and CR3 on, the current from the A Current Source is routed through CR1 and CR3. No current flows through CR5 and CR7, and thus, no voltage is developed at the emitter of Q5A. When the output from Q3 switches CR1 and CR3 off, the current from the A Current Source flows through CR5 and CR7 and develops a voltage at the emitter of Q5A. The voltage level depends on the magnitude of the current and the impedance at the anode of CR7. An RF square wave with a stable amplitude thus appears at the emitter of Q5A.

When the AM Calibrator is producing AM, the A Current Source is held on and the B Current Source is switched on and off at a 10 kHz rate. The RF signal at the emitter of Q5B is thus a 10.1 MHz signal chopped at a 10 kHz rate. The signals from the two modulators are converted to currents by the common-base stages Q5A and Q5B. Since the collectors of Q5A and Q5B share a common load (R66), the two collector currents are summed together, and an AM signal with a nominal modulation index of $^1/_3$ is developed at the calibrator output. Before being applied to the CALIBRATION AM/FM OUTPUT connector, the signal is bandpass-filtered by L7 and C28 and attenuated by the 10 dB Output Attenuator.

Amplifier/Detector

The method for accurately determining the AM depth requires accurate measurement of the relative levels from Modulator A alone and B alone. The Detector converts the RF signal into a dc voltage which can be measured by the instrument's internal Voltmeter.

Q20 and Q19 amplify the summed RF signal by 22 dB. The gain of the stage is 1+(R78/R75). Q17 converts the signal from Q19 to a current which drives the common-base amplifier Q16 into the active region during positive half-cycles and off during negative half-cycles. The current from Q16 develops a voltage across R95 which is a half-wave-rectified RF signal. CR11 is switched on and off out of phase with Q16. The detected signal is filtered by R97 and C45 and buffered by voltage follower U2. The output of U2 is the AM Calibration voltage measured by the Voltmeter. The detected signal is also amplified, inverted, and offset by the X10 DC Amplifier. The $\times 10$ amplification enhances the resolution of the calibrator in discerning the difference in levels between the outputs of Modulator A and B. The gain of U3 is $-[R101/(R96 + R98)] = -10$. Q18 generates a current which, flowing through R101, generates an offset of about +22V. This offset, when added to the amplified and inverted input, produces a dc voltage at the output of U3 ($\times 10$ AM Calibration) which is within the measurement range of the internal Voltmeter. R105, C52, R106, and C54 filter the outputs from the detector amplifiers.

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10 kHz Modulation Oscillator and Modulator Drive Circuits

A 10 kHz square wave is generated by a 20 kHz astable multivibrator whose output is divided by 2. The 20 kHz Modulation Oscillator (U6) is a timer circuit wired for astable operation. The Divide-by-2 circuit (U7A) is a D-type flip-flop with the active-low output driving the D input which creates a divide-by-two function. A resistive divider (R37, R39, and R41) is placed across the two outputs of U7A. The voltage at the adjustable center tap of the divider is a square wave whose amplitude and phase sense vary with the position of the tap and the symmetry (duty cycle) of the output from U7A. The output from the divider is fed back to the timing control input of U6 through voltage follower U5.

The voltage at the timing control of U6 determines the period of the output of U6. The half-frequency square wave, applied to timing control input, lengthens or shortens every other cycle from U6 and thus alters the symmetry of the output from the Divide-by-2.

The output from U7A switches the B Current Source on and off. The basic reference for the B Current Source is a temperature-stable reference diode VR1. The reference is fed from current source Q14, which itself is temperature stable because its base-emitter junction and its reference VR2 have similar thermal behavior. The output of the reference (taken with respect to the −15V(F) supply) is divided by two by R63 and R64 and converted into a constant current source by U4 and Q20. The 10 kHz signal driving the base of Q8 alternately switches the current from Q10 between Q7 and Q6.

The current from Q6 drives Modulator B through Q9. The current waveform, however, is modified (by U1 and its associated components) to give it a slower rise and fall time. When Q6 is off, there is no charge on C34 and no current flows through R81. When Q6 switches on, a constant current begins to charge C34. U1 senses this voltage and turns on Q9 to cause an equal voltage to develop across R81 (since the voltage across the inputs of U1 must always be zero). C34 charges exponentially until all the current from Q6 flows through Q9 and into Modulator B. The converse situation occurs when Q6 switches off.

The A Current Source is switched under command of the Controller. The current for the A Current Source originates in current source Q13. The reference for Q13 is also VR1. Q15, wired as a diode, thermally matches the base-emitter junction of Q13 to stabilize it. R45 adjusts the current supplied to Modulator A so that the detected voltage from Modulator A can be set to the same value as that from Modulator B.

Power Supply Decoupling

Q22 and Q21 drop the level of the −15V Supply to −10 and −5V respectively. They are the supplies for U6, U7A, and some of the bias references. Q23 multiplies the effect of C3 to assist in decoupling audio (for example, line frequencies) on the +15V Supply.

Select Decoder and Data Latch

For a general discussion of instrument control, see *Instrument Bus* in Service Sheet BD5. U8A, U8C, and U8D shift the logic levels from TTL register U9 to levels compatible with the particular devices being driven.

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TROUBLESHOOTING

General

Procedures for checking the AM Calibrator Assembly are given below. The circuits to check are marked on the schematic diagram by a hexagon with a check mark and a number inside, for example, ⟨√3⟩. In addition, any points outside the labeled circuit area that must be checked are also identified. Fixed signals are also shown on the schematic inside a hexagon, for example, ⟨+1.9 TO +2.1 VDC⟩. Extend the board assembly where necessary to make measurements.

CAUTION

Tighten SMC connectors to 0.6 N·m (5 in·lb). Hand tightening of connectors is insufficient. Hand-tightened connectors can work loose and cause reduced performance or malfunctions.

Equipment

Oscilloscope ..... HP 1740A
Signal Generator ..... HP 8640B
Voltmeter ..... HP 3455A

⟨√1⟩ Modulation Source Circuits Check

1. Measure the emitter of Q15 with a dc voltmeter. The voltage should be between −9.1 and −7.9 Vdc.
2. Disconnect W28 from A50J1 (10 MHz IN). Key in the Direct Control Special Functions indicated in Table 8F-100. For each setting, check the points indicated with a high-impedance, dc coupled oscilloscope.

Table 8F-100. *Levels, ⟨√1⟩ Step 2*

Direct Control Special Function	Voltage Level (Vdc) at				
	U7A Pin 4	U7A Pin 6	U7A Pin 1	Q6 Collector	CR6 Cathode
0.181	−5.2 to −4.7	−10.0 to −9.5	−10.0 to −9.5	−6.8 to −6.4	−1.75 to −1.55
0.186	−10.0 to −9.5	−5.2 to −4.7	−5.2 to −4.7	−5.1 to −4.8	−0.1 to 0
0.184	−10.0 to−9.5	−10.0 to −9.5	See Fig. 8F-44	See Fig. 8F-45	See Fig. 8F-46

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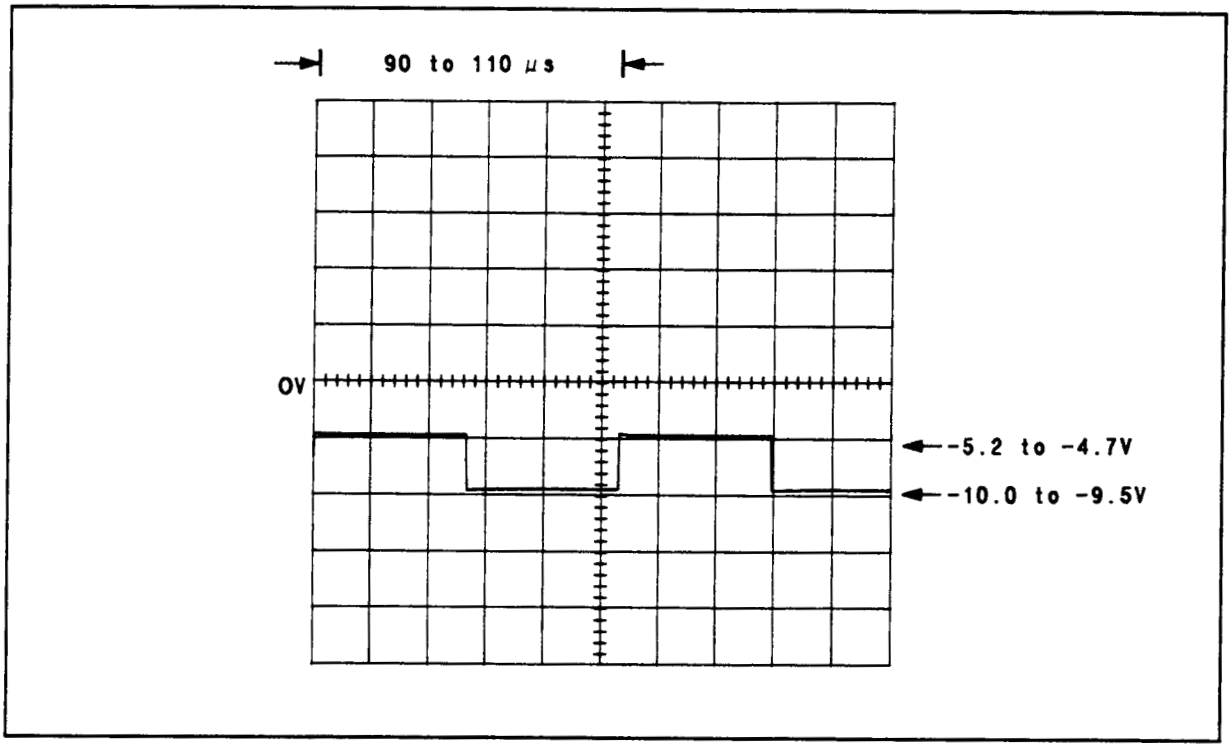


Figure 8F–44. *Waveform for* ⟨√1⟩ *Step 2 (U7A pin 1)*

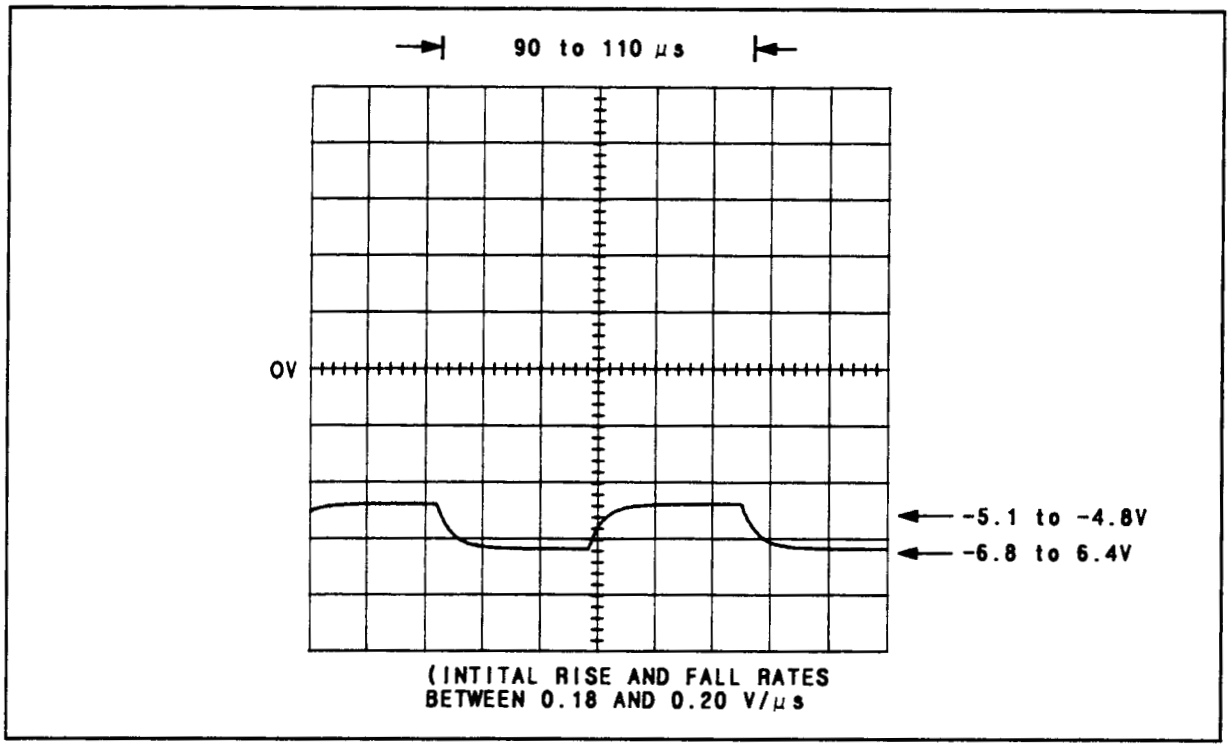


Figure 8F–45. *Waveform for* ⟨√1⟩ *Step 2 (Q6 Collector)*

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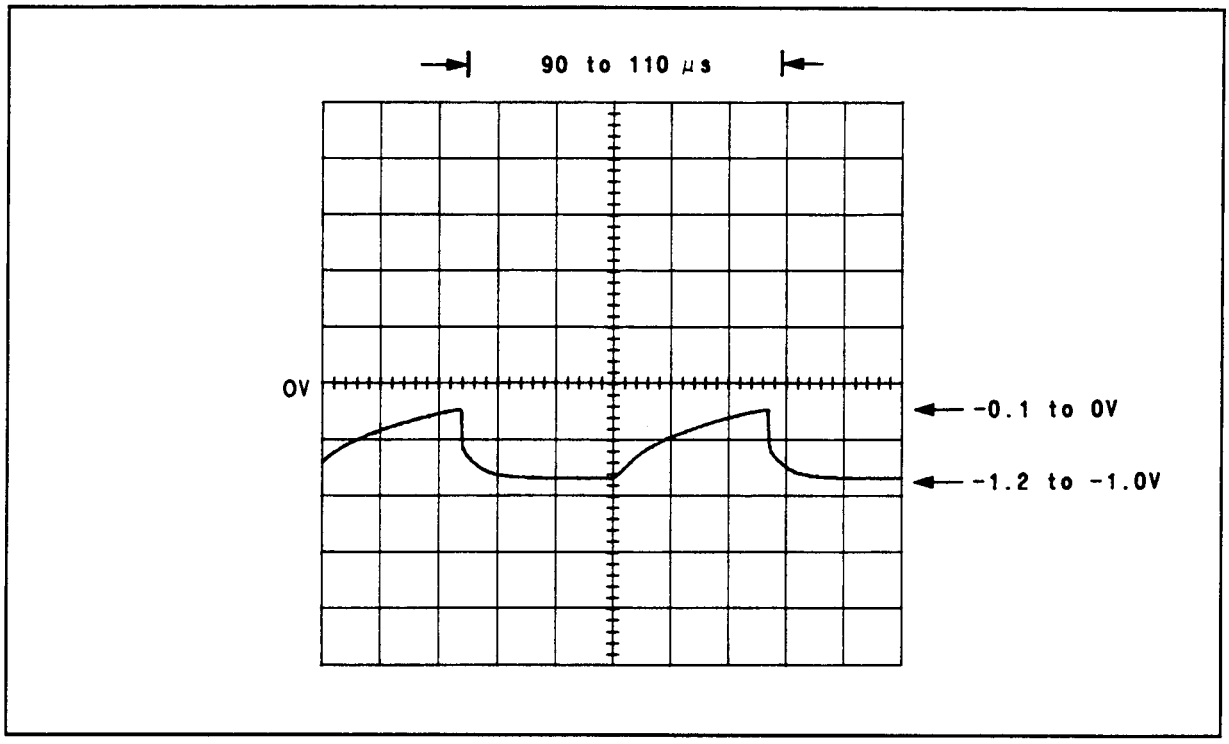


Figure 8F–46. *Waveform for* ⟨√1⟩ *Step 2 (CR6 Cathode)*

Hint: For all settings above, pin 3 of U6 should be as in Figure 8F–47.

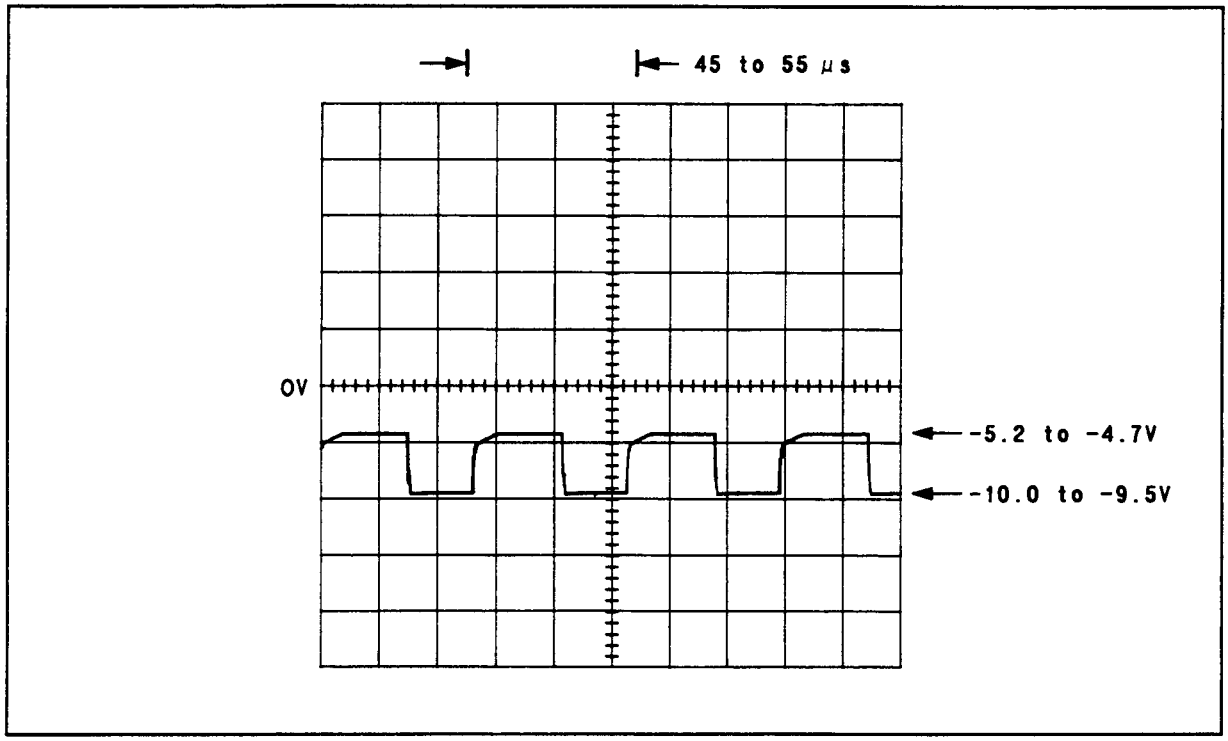


Figure 8F–47. *Waveform for* ⟨√1⟩ *Step 2 Hint*

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3. Key in the Direct Control Special Functions indicated in Table 8F-101. For each setting, check the points indicated.

Table 8F-101. *Levels at U8A and CR5,* ⟨√1⟩ *Step 3*

Direct Control Special Function	Voltage Level (Vdc) at	
	U8A Pin 2	CR5 Cathode
0.186	−9.9 to −9.4	−0.1 to 0
0.183	−6.7 to −6.4	−2.0 to −1.6

⟨√2⟩ RF and Detector Circuits Check

1. Set the signal generator for 10.1 MHz CW at −4.5 dBm. Connect its RF output to A50J1 (10 MHz IN).

2. Connect a high-impedance, ac coupled oscilloscope to the base of Q1B (pin 6). The oscilloscope should have a low-capacitance 10:1 divider probe. Adjust the signal generator level for a waveform of 600 mVpp.

3. Connect the oscilloscope to the collector of Q1D (pin 11). The waveform of the 10.1 MHz signal should be a squarewave with some ringing and an amplitude between 550 and 650 mVpp excluding the ringing.

4. Key in 0.183 SPCL to turn both modulators off. The waveforms at the collectors of Q2 and Q3 should be between 800 and 1200 mVpp excluding the ringing and both waveforms should have the same amplitude within 50 mV.

   Hint: Both modulators should be off; the cathodes of CR5 and CR6 should be between 0 and −100 mVdc.

5. Key in the Direct Control Special Functions indicated in Table 8F-102. For each setting, check the points indicated.

Table 8F-102. *Levels at CR7, CR8 and Q4,* ⟨√2⟩ *Step 5*

Direct Control Special Function	Level Excluding Ringing (mVpp) at		
	CR7 Anode	CR8 Anode	Q4 Collector
0.183	<10	<10	<10
0.186	200 to 300	<10	<10
0.181	<10	200 to 300	200 to 300
0.185	200 to 300	200 to 300	200 to 300

6. Key in 0.186 SPCL to turn Modulator A on and B off.

   Hint: None of the following steps will work properly with both modulators on.

7. Connect the oscilloscope to the collector of Q19. The waveform should be between 1.5 and 2.5 Vpp.

8. Set the oscilloscope to dc coupled and connect it to the collector of Q16. The 10.1 MHz waveform should be as in Figure 8F-48.

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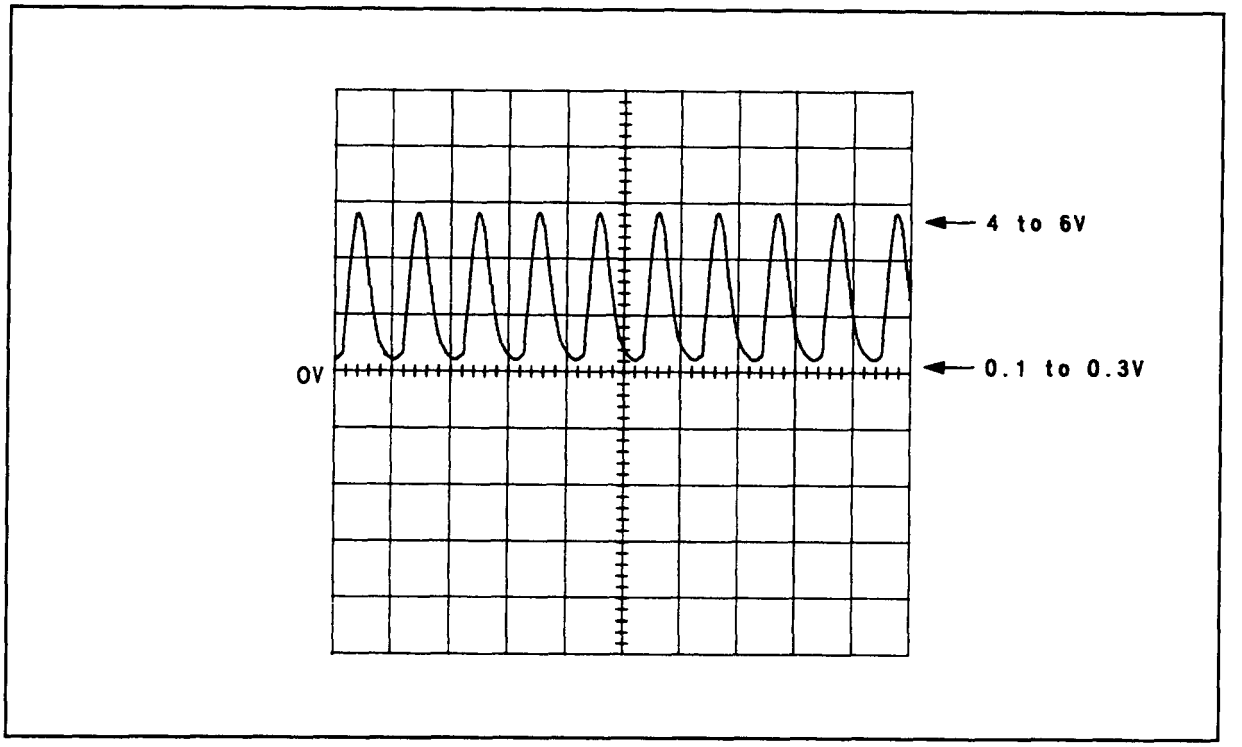


Figure 8F-48. *Waveform for* ⟨√2⟩ *Step 8*

9. Connect a dc voltmeter to pin 3 of U2 and note the reading which should be between +1.8 and +2.2 Vdc.
10. Connect a dc voltmeter to A50TP2 (×1 LVL). The voltmeter should read within ±10 mV of the voltage in step 9.
11. Connect a dc voltmeter to A50TP3 (×10 LVL). The voltmeter should read between −0.1 and +4.0 Vdc.

    Hint: The ×10 DC Amplifier has a gain of −10 and produces an offset of +22 Vdc.

⟨√3⟩ Select Decoder and Data Latch Check

1. Key in 0.180 SPCL. Check pin 1 of U8B with a high-impedance, dc coupled oscilloscope. The waveform should be narrow, high-going pulses with a maximum between +4 and +6V, a minimum between −9 and −10V, and a period of approximately 60 ms.
2. Key in the Direct Control Special Functions indicated in Table 8F-103. For each setting, check the pins on U9 indicated.

Table 8F-103. *Levels at U9,* ⟨√3⟩ *Step 2*

Direct Control Special Function	Level (TTL) at U9 Pin		
	16	15	11
0.180	L	L	H
0.187	H	H	L

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Service Sheet 31

ASSEMBLIES

- **A10 Power Supply Regulators**
- **A26 Power Supply**
- **A29 Series Regulator Heatsink**

PRINCIPLES OF OPERATION

General

The Power Supply Regulators Assembly (A10) and the Power Supply Motherboard Assembly (A26) contain the circuitry for the +15 and −15V Supplies. The two regulators are complements (that is, all polarities reversed, NPN transistors interchanged for PNP, etc.) except (1) the −15V Supply is referenced from the +15V Supply (via R21 and R22); (2) the −15V Supply not adjustable; and (3) the +15V Supply remains on with POWER in STBY to supply the high-stability crystal reference oscillator in Option 002.

Only the +15V Supply will be discussed.

+15V Supply (A10)

The +15V Supply is a series-type regulator. A29Q2 is the series-pass transistor configured as a Darlington pair. A29Q2 is supplied from a full-wave rectifier (chassis part T1, A26CR5, and A26CR6) and filter capacitor A26C6. The Input Overvoltage Protection (or crowbar, consisting of triac A26Q1, reference diodes A26VR1 and A26VR2, and resistor A26R1) protects the instrument against improper line voltage selection. The reference diodes cause the triac to fire (that is, short-circuit) when the secondary voltage exceeds approximately 70V of either polarity. The shorted secondary then causes the line fuse to blow.

The output of the supply is divided down by R23, R24, and R25 and compared to the voltage across reference diode VR1 by differential transistors Q10A and Q10B. Q10C is an intermediate stage which drives the series-pass regulator. CR3 protects the base-emitter junction of Q10A. C1 filters noise generated by the reference diode.

Transistor Q10D senses the voltage drop across R3. If the voltage is too large (because of too much output current), Q10D becomes active and cuts off Q10C, which cuts off the series-pass transistor. The supply voltage drops to zero and the output current drops (or folds back) to a safe level. C2 frequency compensates the supply.

The combination of VR3 and Q6 is an Overvoltage Protection circuit for the +15V Supply. Should the output of the supply exceed approximately +16V, VR3 conducts and fires SCR Q6, which shorts the supply. The supply then folds back. VR5 conducts and lights LED DS1 when the supply is at approximately the right voltage.

Relay A26K1 removes all loads except the heater of chassis part Y1 (Option 002 only) from the +15V Supply when the instrument is in standby. A26K1 is energized by the unregulated +15V Supply via the POWER switch (chassis part S3 on Service Sheet 25). The combination of C9 and R10 suppresses transient load changes as the instrument is switched to on, off, or standby; rapid load changes can activate the Input Overvoltage Protection. A26C5 suppresses capacitively-coupled turn-on spikes between relay contact pairs which can activate the Input Overvoltage Protection. When A26K1 is energized, C9, R10, and A26C5 are shorted by the relay contacts.

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TROUBLESHOOTING

General

Procedures for checking the +15V and −15V Power Supplies are given below. The circuits or points to check are marked on the schematic diagram by a hexagon with a check mark and a number inside, for example, ⟨✓3⟩. In addition, any points outside the labeled circuit area that must be checked are also identified. Fixed signals are also shown on the schematic inside a hexagon, for example, ⟨+1.9 TO +2.1 VDC⟩. Extend the A10 Power Supply Regulators Assembly where necessary to make measurements.

Most often a dead power supply is the result of a short on its output which originates on one of the other assemblies. Follow the Power Supply Check on Service Sheet BD5 to isolate a short to an assembly. Note that the +15V supply remains on in standby.

The supplies are interdependent. Often a short on one supply will shut down another. The interdependency is shown in Table 8F-104.

Table 8F-104. *Power Supply Dependency*

If this supply goes dead:	These supplies will also go dead:
+15V	All Other Supplies
−15V	+5V and −5V Supplies
+5V	No Other Supply
−5V	No Other Supply
+40V	No Other Supply

Equipment

Audio Source ..... HP 8903B
Oscilloscope ..... HP 1740A
Voltmeter ..... HP 3455A

⟨✓1⟩ Input Overvoltage Protection Check

NOTE

This test checks only A26Q1. It does not check the conduction voltage of A26VR1 and A26VR2.

1. Unplug the instrument and set its line voltage selector to 120V.

CAUTION

For the remainder of this check, the instrument must not be connected to a power line.

2. Set the audio source to 50 or 60 Hz. Set its level to deliver 3 Vrms into 600Ω. Connect its 600Ω output to the high and low prongs of a power cord and plug the other end of the power cord into the rear-panel line module socket.
3. Connect a high-impedance, ac coupled oscilloscope to terminal T1 of triac A26Q1. The waveform should be a clipped 50 or 60 Hz sinusoid with an amplitude of 2 Vpp or greater.

   Hint: If the voltage is near zero, check T1 and A26Q1. If the voltage is about 1.5 Vpp, A26C6 or A26C7 may be shorted.

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⟨√2⟩ Fullwave Rectifiers Check

1. If there are any jumpers on the TEST test points on the A13 Controller Assembly, remove them.
2. Connect a high-impedance, dc coupled oscilloscope to A26XA10 as indicated in Table 8F-105. For each connection, key in 40.0 SPCL or switch POWER to STBY then back to ON to reset the instrument. While all front-panel LEDs are lighted, check the average dc voltage and ac ripple (100 or 120 Hz for common mains) which should be within the limits indicated in the table.

Table 8F-105. *Power Supply Levels,* ⟨√2⟩ *Step 2*

Pin to Check on A26XA10	Average Voltage Limits (Vdc)	Maximum AC Ripple (Vpp)
13 or 35	+18 to +28	1
18 or 40	−29 to −19	1.3
10 or 32*	+6 to +12	1
22 or 44*	−13 to −7	1.5
* See Service Sheet 32.		

Hint: An open rectifier diode will result in excessive ripple at the line frequency (50 or 60 Hz for common mains). An average voltage near or above maximum indicates either no loading by the regulator or improper line selection. Lack of ripple indicates no loading by the regulator.

⟨√3⟩ +15V Regulator Check

1. Switch POWER to STBY. A10DS1 (+15V) should be on.

   Hint: If A10DS1 is off with POWER set to ON, but on with POWER set to STBY, the +15V supply is probably working properly but there may be a short on the +15V (SWITCHED) line or the Overcurrent Protection may be defective (or nearly tripping).

2. Measure the voltages indicated in Table 8F-106 with POWER switched to STBY and to ON. Use a dc voltmeter. The voltages given are for normally loaded, unloaded, and short-circuit conditions.

Table 8F-106. *+15V Regulator Levels,* ⟨√3⟩ *Step 2*

Point to Measure on A10	Typical Voltage (Vdc)				
	POWER ON			POWER STBY	
	Normal	Unloaded	Short	Normal	Short
TP2 (+15V UNSW)	+15	+15	0	0	0
TP3 (+15V SW)	+15	+15	0	+15	0
J1 Pin 7	+25	+25	+24	+25	+24
Q10D Pin 12	*	**	*	**	*
* A few hundred millivolts higher than pin 7 of J1.					
** A few millivolts higher than pin 7 of J1.					

Hint: If the above voltages in a column are correct, the supply is working normally under the condition stated. If the supply is oscillating, check A10C2. If the supply voltage is only slightly incorrect, perform *Adjustment 1—Power Supply* in Section 5.

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⟨√4⟩ −15V Regulator Check

1. Measure the voltages indicated in Table 8F-107 with a dc voltmeter. The voltages given are for normally loaded, unloaded, and short-circuit conditions.

Table 8F-107. *−15V Regulator Levels,* ⟨√4⟩ *Step 1*

Point to Measure on A10	Typical Voltage (Vdc)		
	Normal	Unloaded	Short
TP4 (−15V)	−15	−15	0
J1 Pin 4	−24	−26	−23
Q11A Pin 3	*	**	*
* A few hundred millivolts more negative than pin 4 of J1.			
** A few millivolts more negative than pin 4 of J1.			

Hint: When any series of voltage readings in each column are correct, the supply is working normally under the condition stated. If the supply is oscillating, check A10C3.

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Service Sheet 32

ASSEMBLIES

- **A10 Power Supply Regulators**
- **A26 Power Supply**
- **A29 Series Regulator Heatsink**

PRINCIPLES OF OPERATION

General

The Power Supply Regulators Assembly (A10) and Power Supply Motherboard Board Assembly (A26) contain the circuitry for the +40, +5, and −5V Supplies. The +5 and −5V regulators are complements (that is, all polarities reversed, NPN transistors interchanged for PNP, etc.). Both supplies are referenced from the +15V and −15V Supplies and are not adjustable.

Only the +40 and the +5V Supplies will be discussed.

+40V Supply

The +40V supply is a series-type regulator. Q12 is the series-pass transistor. Q12 is supplied from a half-wave rectifier (chassis part T1 on Service Sheet 31 and A26CR8) and filter capacitor A26C8. The output of the supply is divided down by R42 and R43 and compared to the +15V Supply by differential transistors Q9 and Q13. Q14 is an intermediate stage which drives the series-pass regulator. CR7 and CR10 protect the base-emitter junctions of Q9 and Q13. C10 filters the noise from the +15V Supply. R58 and CR14 bring up the supply when the instrument is turned on.

The combination of VR7 and Q8 is an Overvoltage Protection circuit for the +40V Supply. Should the output of the supply exceed approximately +47V, VR7 conducts and fires SCR Q8 which shorts the supply. CR13 protects the supply should the output connect to a negative-polarity supply. VR10 conducts and switches on Q5 to light LED DS5 when the supply is at approximately the right voltage.

+5V Supply

The +5V Supply is a series-type regulator. A29Q1 is the series-pass transistor. A29Q1 is supplied from a full-wave rectifier (chassis parts T1 and CR1) and filter capacitor A26C3 (all shown on Service Sheet 31). The output of the supply is compared to the voltage of the +15V supply (divided down by R50 and R45) by Comparison Amplifier U2A, which drives the series-pass regulator.

Overcurrent Protection amplifier U2B senses the voltage drop across R49. If the voltage is too large (because of too much output current), the output of U2B goes low and cuts off Q2, which cuts off the series-pass transistor. The supply voltage drops to zero and the output current drops (or folds back) to a safe level. CR8 prevents U2B from having an effect on the supply when the supply current is normal. The combination of C13 and C14 frequency compensates the supply.

Overvoltage Protection circuit VR8 and Q1 protects the +5V Supply. Should the output of the supply exceed approximately +5.6V, VR8 conducts and fires SCR Q1 which shorts the supply. The supply then folds back. CR15 protects the supply should the output connect to a negative-polarity supply. VR11 conducts and lights LED DS3 when the supply is at approximately the right voltage.

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TROUBLESHOOTING

General

Procedures for checking the +5V, −5V, and +40V Power Supplies are given below. The circuits or points to check are marked on the schematic diagram by a hexagon with a check mark and a number inside, for example, ⟨✓3⟩ . In addition, any points outside the labeled circuit area that must be checked are also identified. Fixed signals are also shown on the schematic inside a hexagon, for example, ⟨+1.9 TO +2.1 VDC⟩ . Extend the A10 Power Supply Regulators Assembly where necessary to make measurements.

Most often a dead power supply is the result of a short on its output which originates on one of the other assemblies. Follow the Power Supply Check on Service Sheet BD5 to isolate a short to an assembly.

Equipment

Oscilloscope ..... HP 1740A
Voltmeter ..... HP 3455A

⟨✓1⟩ +5V Regulator Check

1. Measure the voltages indicated in Table 8F-108 with a dc voltmeter. The voltages given are for normally loaded, unloaded, and short-circuit conditions.

Table 8F-108. *+5V Regulator Levels,* ⟨✓1⟩ *Step 1*

Point to Measure on A10	Typical Voltage (Vdc)		
	Normal	Unloaded	Short
TP5 (+5V)	+5	+5	0
J1 Pin 10	*	**	+0.2
J1 Pin 12	+9	+11	+10
* A few hundred millivolts higher than TP5.			
** A few millivolts higher than TP5.			

Hint: When any series of voltage readings in a column is correct, the supply is working properly under the condition stated. If the supply is oscillating, check A10C13 and A10C14.

⟨✓2⟩ −5V Regulator Check

1. Measure the voltages indicated in Table 8F-109 with a dc voltmeter. The voltages given are for normally loaded, unloaded, and short-circuit conditions.

Table 8F-109. *−5V Regulator Levels,* ⟨✓2⟩ *Step 1*

Point to Measure on A10	Typical Voltage (Vdc)		
	Normal	Unloaded	Short
TP6 (−5V)	−5	−5	0
J1 Pin 3	*	**	−0.2
J1 Pin 1	−10	−12	−11
* A few hundred millivolts more negative than TP6.			
** A few millivolts more negative than TP6.			

Hint: When any series of voltage readings in a column is correct, the supply is working properly under the condition stated. If the supply is oscillating, check A10C11 and A10C15.

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⟨√3⟩ +40V Regulator Check

1. Measure the voltages indicated in Table 8F-110 with a dc voltmeter. The voltages given are for normally loaded, unloaded, and short-circuit conditions.

Table 8F-110. *-5V Regulator Levels,* ⟨√3⟩ *Step 1*

Point to Measure on A10	Typical Voltage (Vdc)		
	Normal	Unloaded	Short
TP7 (+40V)	+42	+42	0
Q12 Emitter	+68	+72	+70
XA10 Pin 1	*	*	**

* A few volts higher than the emitter of Q12.
** Approximately the same as the emitter of Q12.

Hint: When any series of voltage readings in a column is correct, the supply is working properly under the condition stated. Line ripple at pin 1 of A26XA10 should be approximately 3 Vpp under normal loading.

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Service Sheet 33 *(2642A and Above)*

ASSEMBLY

- **A72 IF Channel Filter Assembly (Option Series 030)**

PRINCIPLES OF OPERATION

General

The channel filters determine the passband characteristics of the IF for the high-selectivity measurement mode. The shape of the IF passband is dependent on the specific option pair (any two of Options 032, 033, 035, and 037) installed.

Channel Filters

The A72 Channel Filter Assembly contains two selectable IF Channel Filters, associated buffer amplifiers, a programmable 20 dB Amplifier, and associated switches. Transformer T1 steps up the IF level 12 dB. FETs Q1 and Q2 select the IF path through the two Channel Filters (FL1 and FL2). The FETs are controlled by the output of U5. For example, if U5 is low (−15V), diode CR1 switches on and CR2 off; FET Q2 is off and Q1 is on. Thus, the secondary winding of T1 is grounded on the low end, and the IF signal appearing at the upper end couples into FL1 via emitter follower Q6. Resistors R5 and R9 present the proper impedance to drive and terminate the crystal filters. (The resistor values vary to match the specific requirements of the Channel Filters.)

The output of the selected Channel Filter is amplified approximately 6 dB depending on filter loss. Diodes CR3 and CR4 steer the signal from the selected channel to the switchable 20 dB pad (R24, R25, and U1) and into the 20 dB output amplifier.

Digital Circuits

Transistors Q3 and Q4 drive coaxial RF switch S2 which switches the LO to either internal or external. (Refer to Service Sheet 5 for serial prefixes 2642A and above.) For a general discussion of instrument control, see *Instrument Bus* in Service Sheet BD5.

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TROUBLESHOOTING

General

Procedures for checking the IF Channel Filter Assembly is given below. The circuits to check are marked on the schematic diagram by a hexagon with a check mark and a number inside, for example, ⟨√3⟩. In addition, any points outside the labeled circuit area that must be checked are also identified. Fixed signals are also shown on the schematic inside a hexagon, for example, ⟨+1.9 TO +2.1 VDC⟩. Extend the board assembly where necessary to make measurements.

CAUTION

Tighten SMC connectors to 0.6 N·m (5 in·lb). Hand tightening of connectors is insufficient. Hand-tightened connectors can work loose and cause reduced performance or malfunctions.

Equipment

Oscilloscope ..... HP 1740A
Signal Generator ..... HP 8640B

⟨√1⟩ First Channel 1 Filter Check

1. Set the signal generator to between 454 and 456 kHz CW at −10 dBm (70.7 mVrms into 50Ω). Connect its RF output to A72J2 (IF IN) on the Measuring Receiver.
2. Press the blue key, then press INSTR PRESET (the AUTOMATIC OPERATION key) to preset the instrument.
3. Connect a high-impedance, ac coupled oscilloscope to the emitter of Q6. The 455 kHz signal should have an amplitude between 1.0 and 1.5 Vpp.

   Hint: The gate of Q2 should be approximately −9 Vdc. Pin 7 of U4 should be a TTL low.
4. Set the oscilloscope gain for a display of 6 divisions peak-to-peak.
5. Connect the oscilloscope to the base of Q11. Fine tune the signal generator for an amplitude peak. The amplitude should be between 1.5 and 2.5 divisions peak-to-peak.
6. Set the oscilloscope gain for a display of 6 divisions peak-to-peak. Tune the signal generator up and down and note the frequencies at which the waveform drops to 3 divisions. The difference between the highest and lowest frequencies should be within the limits listed in Table 8F-111.

   Hint: R5 and R9 are supplied with FL1 when FL1 is replaced.

Table 8F-111. *Bandwidth of First Channel 1 Filter, ⟨√1⟩ Step 6*

Option Combination	Frequency Difference Limits (kHz)	
	Minimum	Maximum
032 and 035 033 and 035 035 and 037	25.0	35.0
032 and 033 033 and 037	12.4	16.9
032 and 037	6.4	10.4

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7. Tune the signal generator back to the amplitude peak. Adjust the oscilloscope gain for a display of 2 divisions peak-to-peak. Connect the oscilloscope to the collector of Q12. The waveform should have an amplitude between 5 and 6 divisions peak-to-peak.
8. Connect the oscilloscope to pin 8 of U1A. The waveform should have the same amplitude as in step 7.

⟨√2⟩ First Channel 2 Filter Check

1. Set the signal generator to between 454 and 456 kHz CW at −10 dBm (70.7 mVrms into 50Ω). Connect its RF output to A72J2 (IF IN) on the Measuring Receiver.
2. Press the blue key, then press INSTR PRESET (the AUTOMATIC OPERATION key) to preset the instrument.
3. Connect a high-impedance, ac coupled oscilloscope to the emitter of Q5. Key in 0.3D3 SPCL to select channel 2. The 455 kHz signal should have an amplitude between 1.0 and 1.5 Vpp.

   Hint: The gate of Q1 should be approximately +9 Vdc. Pin 7 of U4 should be a TTL high.
4. Set the oscilloscope gain for a display of 6 divisions peak-to-peak.
5. Connect the oscilloscope to the base of Q9. Fine tune the signal generator for an amplitude peak. The amplitude should be between 1.0 and 1.6 divisions peak-to-peak.
6. Set the oscilloscope gain for a display of 4 divisions peak-to-peak. Tune the signal generator up and down and note the frequencies at which the waveform drops to 2 divisions. The difference between the highest and lowest frequencies should be within the limits listed in Table 8F-112.

   Hint: R6 and R10 are supplied with FL2 when FL2 is replaced.

Table 8F-112. *Bandwidth of First Channel 2 Filter,* ⟨√1⟩ *Step 6*

Option Combination	Frequency Difference Limits (kHz)	
	Minimum	Maximum
032 and 037 033 and 037 035 and 037	3.0	7.0
032 and 033 032 and 035	6.4	10.4
033 and 035	12.4	16.9

7. Tune the signal generator back to the amplitude peak. Adjust the oscilloscope gain for a display of 2 divisions peak-to-peak. Connect the oscilloscope to the collector of Q10. The waveform should have an amplitude between 6 and 9 divisions peak-to-peak.
8. Connect the oscilloscope to pin 8 of U1A. The waveform should have the same amplitude as in step 7.

⟨√3⟩ Channel Output Circuit Check

1. Set the signal generator to between 454 and 456 kHz CW at −10 dBm (70.7 mVrms into 50Ω). Connect its RF output to A72J2 (IF IN) on the Measuring Receiver.
2. Press the blue key, then press INSTR PRESET (the AUTOMATIC OPERATION key) to preset the instrument.
3. Connect a high-impedance, ac coupled oscilloscope to pin 8 of U1A. Fine tune the signal generator for an amplitude peak. The 455 kHz signal should have an amplitude between 1.0 and 1.2 Vpp.

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Hint: If the signal is faulty, perform ⟨√1⟩ *First Channel 1 Filter Check.*

4. Set the oscilloscope gain for a display of 6 divisions peak-to-peak. Connect the oscilloscope to pin 9 of U1A. Key in 0.3D1 SPCL to switch out the Channel Output Attenuator. The waveform should have the same amplitude as in step 3.

   Hint: Pin 1 of U1A should be a TTL low, pin 2 of U1B a TTL high.

5. Key in 0.3D0 SPCL to switch in the Channel Output Attenuator. The waveform should have an amplitude between 0.5 and 0.7 divisions peak-to-peak.

   Hint: Pin 2 of U1B should be a TTL low, pin 1 of U1A a TTL high.

6. Connect the oscilloscope to the collector of Q7. The waveform should have an amplitude between 6 and 7 divisions peak-to-peak.

⟨√4⟩ LO Input Switch Control Check

1. Check that W55 is connected to A72J3.
2. Key in the Direct Control Special Functions listed in Table 8F-113. For each setting, connect a high-impedance, dc coupled oscilloscope to the points listed in the table. The voltages should be within the limits indicated.

Table 8F-113. *LO Input Switch Control Levels,* ⟨√4⟩ *Step 2*

Direct Control Special Function	Level (TTL) on U2 Pin		Level (Vdc) on Collector of		DS1
	6	2	Q3	Q4	
0.3D0	H	L	L	H	Off
0.3D4	L	H	H	L	On

⟨√5⟩ Select Decoder and Data Latch Check

1. Key in the Direct Control Special Functions listed in Table 8F-114. For each setting, check the pins on U3 indicated.

Table 8F-114. *Levels at U3,* ⟨√5⟩ *Step 1*

Direct Control Special Function	Level (TTL) at U3 Pin			
	14	10	9	7
0.390	•	H	H	H
0.3D0	H	•	H	H
0.3E0	H	H	•	H
0.3F0	H	H	H	•
• Low-going TTL pulses, ≈60 ms period.				

2. Key in the Direct Control Special Functions listed in Table 8F-115. For each setting, check the pins on U4 indicated.

Table 8F-115. *Levels at U4,* ⟨√5⟩ *Step 2*

Direct Control Special Function	Level (TTL) at U4 Pin				
	2	3	7	15	14
0.3D0	L	H	L	L	H
0.3DF	H	L	H	H	L

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Service Sheet 34 *(2642A and Above)*

ASSEMBLY

- **A71 IF Amplifier/Detector (Option Series 030)**

PRINCIPLES OF OPERATION

General

The IF Amplifier/Detector Assembly (A71) contains three stages of IF amplification, four stages of attenuation, two selectable bandpass filters, and an IF rms detector. The IF gain is selectable in 5 dB steps over a range of 0 to 60 dB.

IF Amplifiers and Attenuators

IF Amplifiers 1, 2, and 3 are nearly identical and have between 21 and 24 dB gain each. IF Amplifier 4 has 33 dB gain. Gain stability is more critical than the accuracy. Using IF Amplifier 1 as an example, the gain is 1+(R7/R6). Schottky diodes CR1 through CR4 prevent saturation of Q3, Q1, Q6, and Q8 respectively during overloads to speed up recovery time.

Switches U2, U1, and U3 select three, 20 dB voltage dividers. Switch U4 select one of four, 5 dB taps of a 20 dB voltage divider. The divider resistors are high-precision, low-drift types. Voltage follower Q7 prevents the bandpass filters from loading IF Attenuator 3.

IF Filters and RMS Detector

FL1 and FL2 are crystal-type, bandpass filters. They are switched in by Q11 and Q12 which are driven by switch U5. The filters have a passband loss of approximately 14 dB.

The amplified and filtered IF signal at the output of is detected by the IF RMS Detector (U6). U6 is a true-rms detector which produces a dc output equal to the rms level of the IF signal. The output of U6 goes to the Voltmeter.

The output of IF Amplifier 4 is also made available at J1 for testing and troubleshooting purposes.

Digital Circuits

Transistor Q14 provides a means of identifying the installation of Option Series 030. For a general discussion of instrument control, see *Instrument Bus* in Service Sheet BD5.

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TROUBLESHOOTING

General

Procedures for checking the IF Amplifier/Detector Assembly is given below. The circuits to check are marked on the schematic diagram by a hexagon with a check mark and a number inside, for example, ⟨√3⟩. In addition, any points outside the labeled circuit area that must be checked are also identified. Fixed signals are also shown on the schematic inside a hexagon, for example, ⟨+1.9 TO +2.1 VDC⟩. Extend the board assembly where necessary to make measurements.

CAUTION

Tighten SMC connectors to 0.6 N·m (5 in·lb). Hand tightening of connectors is insufficient. Hand-tightened connectors can work loose and cause reduced performance or malfunctions.

Equipment

Oscilloscope	HP 1740A
Signal Generator	HP 8640B

⟨√1⟩ Programmable IF Amplifier Check

1. Set the signal generator to between 454 and 456 kHz CW at −7 dBm (100 mVrms into 50Ω). Connect its RF output to A71J2 (IF IN) on the Measuring Receiver.
2. Press the blue key, then press INSTR PRESET (the AUTOMATIC OPERATION key) to preset the instrument. Connect a high-impedance, ac coupled oscilloscope to pin 5 of U2B. Set the oscilloscope gain for a display of 6 divisions peak-to-peak.
3. Key in 0.391 SPCL to set Attenuator 1 to 0 dB and Attenuators 2 and 3 to 20 dB. Key in 0.3EE SPCL to set Attenuator 4 to 15 dB. Connect the oscilloscope to pin 4 of U2B. The waveform should have the same amplitude as in step 2.

   Hint: Pin 2 of U2B should be a TTL low, pin 1 of U2A a TTL high.
4. Key in 0.390 SPCL to set Attenuators 1, 2, and 3 to 20 dB. The waveform should have an amplitude between 0.5 and 0.7 divisions peak-to-peak.

   Hint: Pin 2 of U2B should be a TTL high, pin 1 of U2A a TTL low.
5. Connect the oscilloscope to pin 5 of U1B. The waveform should have an amplitude between 6.0 and 7.2 divisions peak-to-peak.
6. Adjust the signal generator level for a display of 6 divisions peak-to-peak. Key in 0.392 SPCL to set Attenuator 2 to 0 dB and Attenuators 1 and 3 to 20 dB. Connect the oscilloscope to pin 4 of U1B. The waveform should have the same amplitude as in step 5.

   Hint: Pin 2 of U1B should be a TTL low, pin 1 of U1A a TTL high.
7. Key in 0.390 SPCL. The waveform should have an amplitude between 0.5 and 0.7 divisions peak-to-peak.

   Hint: Pin 2 of U1B should be a TTL high, pin 1 of U1A a TTL low.
8. Connect the oscilloscope to pin 9 of U3A. The waveform should have an amplitude between 6.0 and 7.2 divisions peak-to-peak.
9. Adjust the signal generator level for a display of 6 divisions peak-to-peak. Key in 0.394 SPCL to set Attenuator 3 to 0 dB and Attenuators 1 and 2 to 20 dB. Connect the oscilloscope to pin 8 of U3B. The waveform should have the same amplitude as in step 8.

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Hint: Pin 1 of U3A should be a TTL low, pin 2 of U3B a TTL high.

10. Key in 0.390 SPCL. The waveform should have an amplitude between 0.5 and 0.7 divisions peak-to-peak.

    Hint: Pin 1 of U3A should be a TTL high, pin 2 of U3B a TTL low.

11. Connect the oscilloscope to pin 2 of U4. Decrease the oscilloscope gain by a factor of 2. The waveform should have an amplitude between 4.4 and 5.0 divisions peak-to-peak.

12. Adjust the signal generator level for a display of 6 divisions peak-to-peak. Key in the Direct Control Special Functions listed in Table 8F-116. For each setting, the waveform amplitude should be within the limits indicated. If faulty, also check the logic level of the pins on U4 indicated.

Table 8F-116. *Levels on U4,* ⟨√1⟩ *Step 12*

Direct Control Special Function	Waveform Amplitude (div pk-pk)	Level (TTL) at U4 Pin			
		1	8	9	16
0.3E7	5.9 to 6.0	L	H	H	H
0.3EB	3.3 to 3.5	H	L	H	H
0.3ED	1.8 to 2.0	H	H	L	H
0.3EE	1.0 to 1.2	H	H	H	L

13. Key in 0.3E7 SPCL. Connect the oscilloscope to A71TP1. The waveform amplitude should be 5.4 to 6.0 divisions peak-to-peak.

⟨√2⟩ Channel Filters, Output Amplifier, and IF RMS Detector Check

1. Set the signal generator to between 454 and 456 kHz CW at −7 dBm (100 mVrms into 50Ω). Connect its RF output to A71J2 (IF IN) on the Measuring Receiver.

2. Press the blue key, then press INSTR PRESET (the AUTOMATIC OPERATION key) to preset the instrument. Connect a high-impedance, ac coupled oscilloscope to A71TP1.

3. Key in 0.390 SPCL to set Attenuators 1, 2, and 3 to 20 dB and switch in FL1. Key in 0.3EE SPCL to set Attenuator 4 to 15 dB. The waveform should have an amplitude between 300 and 400 mVpp.

   Hint: If the signal is faulty, perform ⟨√1⟩ *Programmable IF Amplifier Check.*

4. Set the oscilloscope gain for a display of 6 divisions peak-to-peak. Connect the oscilloscope to the base of Q10. Fine tune the signal generator to peak the display on the oscilloscope. The waveform should be between 1 and 2 divisions peak-to-peak.

   Hint: The amplitude at this point is quite sensitive to the capacitive loading of the oscilloscope. This step is mainly a check of continuity. Pin 2 of U5B should be a TTL low, pin 1 of U5A a TTL high. Q11 should be on, Q12 off.

5. Key in 0.398 SPCL to switch in FL2. Fine tune the signal generator to peak the display on the oscilloscope. The waveform should be between 1 and 2 divisions peak-to-peak.

   Hint: Pin 2 of U5B should be a TTL high, pin 1 of U5A a TTL low. Q11 should be off, Q12 on.

6. Set the oscilloscope gain for a display of 1 division peak-to-peak. Connect the oscilloscope to the A71TP2. Decrease the oscilloscope gain by a factor of 10. The waveform should have an amplitude between 3 and 8 divisions peak-to-peak.

   Hint: The change in loading on the base of Q10 makes this an inexact measurement.

6. Set the oscilloscope for a calibrated level measurement. Adjust the signal generator level for a display of 2 Vpp. Connect the oscilloscope to pin 9 of U6. Set the oscilloscope to read dc. The oscilloscope should read between 0.69 and 0.73 Vdc.

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7. Key in 49.C SPCL to measure the IF level with the IF RMS Detector. The Measuring Receiver should display between 0.69 and 0.73.

   Hint: If the reading is faulty, see Service Sheet 15.

8. Adjust the signal generator level for a Measuring Receiver display of 0.60, then tune the signal generator up and down and note the frequencies at which the level drops to 0.30. The difference between the highest and lowest frequencies should be between 3 and 7 kHz.

9. Key in 0.390 SPCL to switch in FL1. Key in 49.C SPCL. Fine tune the signal generator to peak the Measuring Receiver's display. Adjust the signal generator level for a Measuring Receiver display of 0.60, then tune the signal generator up and down and note the frequencies at which the level drops to 0.30. The difference between the highest and lowest frequencies should be between 33 and 55 kHz.

⟨√3⟩ Data Latches and Option Series 030 Indicator Check

1. Key in the Direct Control Special Functions listed in Table 8F-117. For each setting, check the pins on U8 indicated.

Table 8F-117. *Levels at U8, ⟨√3⟩ Step 1*

Direct Control Special Function	Level (TTL) at U8 Pin							
	2	3	7	6	10	11	15	14
0.390	L	H	L	H	L	H	L	H
0.39F	H	L	H	L	H	L	H	L

2. Key in the Direct Control Special Functions listed in Table 8F-118. For each setting, check the pins on U7 indicated.

Table 8F-118. *Levels at U7, ⟨√3⟩ Step 2*

Direct Control Special Function	Level (TTL) at U7 Pin			
	2	7	10	15
0.3E0	L	L	L	L
0.3EF	H	H	H	H

3. Key in 0.3F0 SPCL to read back the Option Series 030 Installed Indicator. The Measuring Receiver should display 000001.0000.

   Hint: The waveform at the collector and the emitter of Q14 should be low-going TTL pulses with a period of approximately 60 ms.

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