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Find the *Acqiris SC240 / U1080A-002* at our website: ***Click HERE***

Streamer Analyzer Platforms

■ SC240
8-bit
1 GHz
2 GS/s

■ SC210
8-bit
1 GHz
1 GS/s



XL*Fidelity*
Jet*Speed*
Technology

ODL
Optical Data Link

DPU Ctrl²

ASBus
Auto Synchro Bus

Ctrl I/O

Data Processing Unit

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Main Features

- **On-board reconfigurable Data Processing Unit (DPU) for real-time operations**
- **Front-Panel Optical Data Links (ODL), providing aggregate 5 Gbps (30 Gbps optional)**
- **Streamer Firmware for sFPDP data transfer at up to 25 Gbps, with no dead time and no loss of data**
- **Front-panel digital I/O connectors for real-time data processing control (DPU Ctrl²)**
- **1 GHz analog bandwidth in all FS ranges**
- **1 GS/s synchronous dual-channel (SC240) and single-channel (SC210) data acquisition with independent gain and offset on each channel**
- **Interleaved single-channel mode (SC240) on either input, software selectable, providing up to 2 GS/s sampling rate**
- **Multipurpose I/O connectors for trigger, clock, reference and status control signals (Ctrl I/O)**
- **Optional external processing memory providing 512 MB of SDRAM and 1 MB dual-port SRAM**
- **Modular, 6U CompactPCI standard (PXI compliant)**
- **Fully-featured 50 Ω mezzanine front-end design, with internal calibration and input protection**
- **High-speed PCI bus for data transfer to host PC at sustained rates up to 100 MB/s**
- **Device drivers for Windows, Wind River VxWorks and Linux**
- **Auto-install software with application code examples for C/C++, Visual Basic, Lab VIEW and LabWindows/CVI**

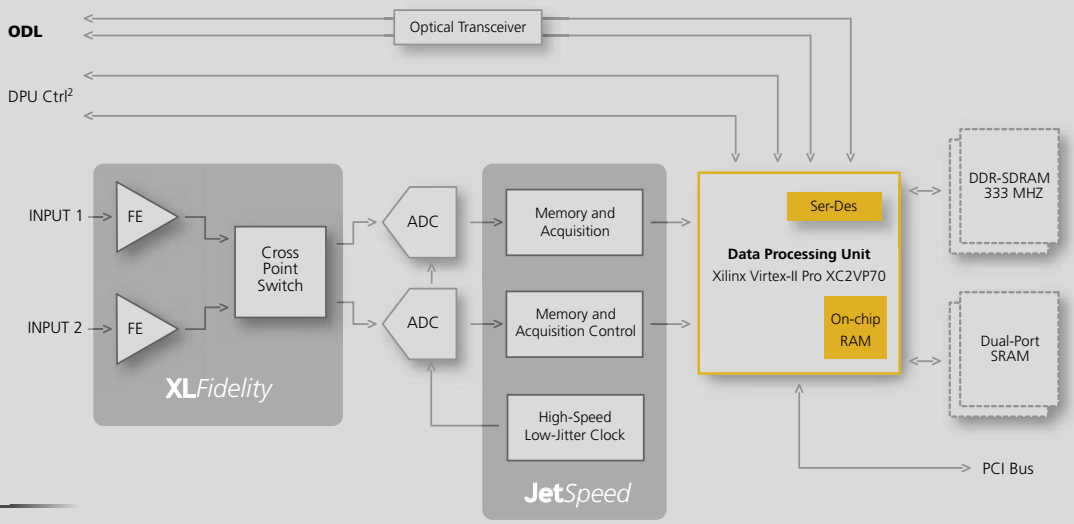
High-Speed Digitizers with Maximum Data Throughput



Data Processing Unit

On-Board FPGA Processing

The SC240 and SC210 are dual- and single-channel 8-bit CompactPCI®/PXI™ digitizers with on-board real-time data processing and fast front-panel data output. Incorporating Acqiris' proprietary **XL***Fidelity* and **Jet***Speed* ADC chipsets, the platforms are designed to cover requirements encountered in radar or similar mass storage-related applications. The SC240 and SC210 Streamer Analyzers are particularly suited when direct sampling techniques are used and when signals must be sampled with high rates of up to 2 GS/s and an analog bandwidth of up to 1 GHz. Both models offer on-board high-performance data processing by means of a very large FPGA. Raw or processed data can be transferred through front-panel optical transceivers at rates of up to 30 Gbps. The on-board FPGA based Data Processing Unit (DPU) allows the platforms to be easily reconfigured to perform **user defined** on-board real-time signal processing on the digitized signal. The on-board FPGA is capable of executing multiplications in less than 5 ns and offers more than 74,000 logic cells, up to 7 Mbits of on-chip RAM, and 328 dedicated 18-bit x 18-bit multipliers with 36-bit results.



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DPU Ctrl²

Extended Real-Time Data Processing Unit Control

DPU Ctrl² provides several front-panel connectors for real-time control of the DPU. The function of these connectors and LEDs is user defined through the implemented firmware.

- I/O P1 and P2 are dedicated to the direct control of the data processing unit.
- ANL Out is the output of a 16-bit on-board DAC. This analog signal can be used in simple control systems.
- LEDs L1 and L2 provide a visual reference.
- I/O EXT provides fourteen bi-directional direct lines to the DPU, used as seven differential pairs, through a µDB-15 connector.

Dual-Channel Performance with Interleave

- SC240 offers dual-channel synchronicity for I/Q acquisitions with up to 1 GS/s sample rate. Interleaved single-channel mode up to 2 GS/s sample rate on either input is software selectable.
- SC210 provides a single input channel with 1 GS/s sample rate.



Ctrl I/O

Trigger Mezzanine with I/O Ports

The trigger mezzanine includes the **XL***Fidelity* FEA102 front-end amplifier chip. The trigger processing circuit embedded in the package includes dual comparators for window triggering mode, on chip DACs for threshold adjustment, additional filters for LF and HF reject trigger coupling and a prescaler to allow a HF divide by 4 mode.

The trigger mezzanine provides access to the circuit via a standard 50 Ω terminated BNC connector and Ctrl I/O. These four front-panel MMCX connectors provide access for an external clock or 10 MHz reference signal, a trigger output and two additional I/O digital control lines (I/O A & B) for monitoring or modifying the digitizer's status and configuration or to extract a 10 MHz clock signal.



ASBus

Auto-Synchronous Bus System

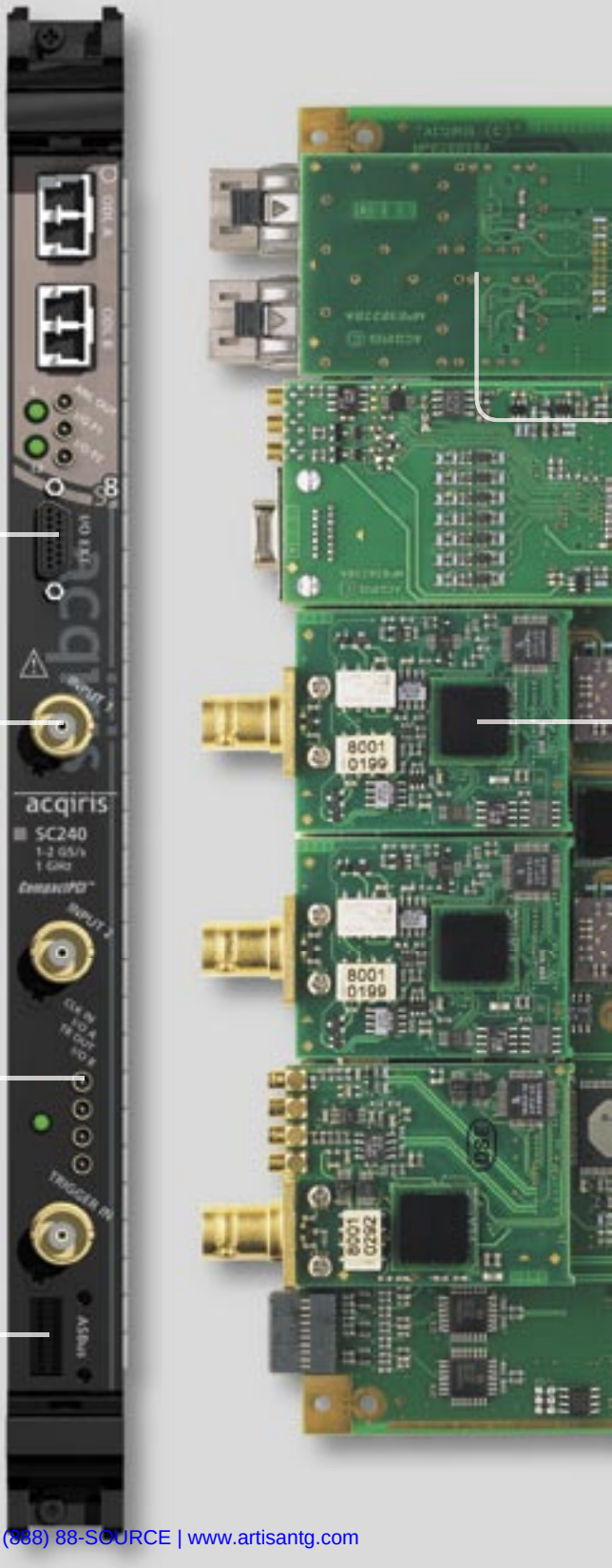
If more than two data acquisition channels are required several streamer analyzer platforms can be combined using Acqiris' ASBus, a proprietary high-bandwidth auto-synchronous bus system. This vital tool takes care of the distribution of all necessary trigger and clock signals to the **Jet***Speed* COS101 clock circuit.



Data Processing Unit

Reconfigurable, On-the-Fly Processing

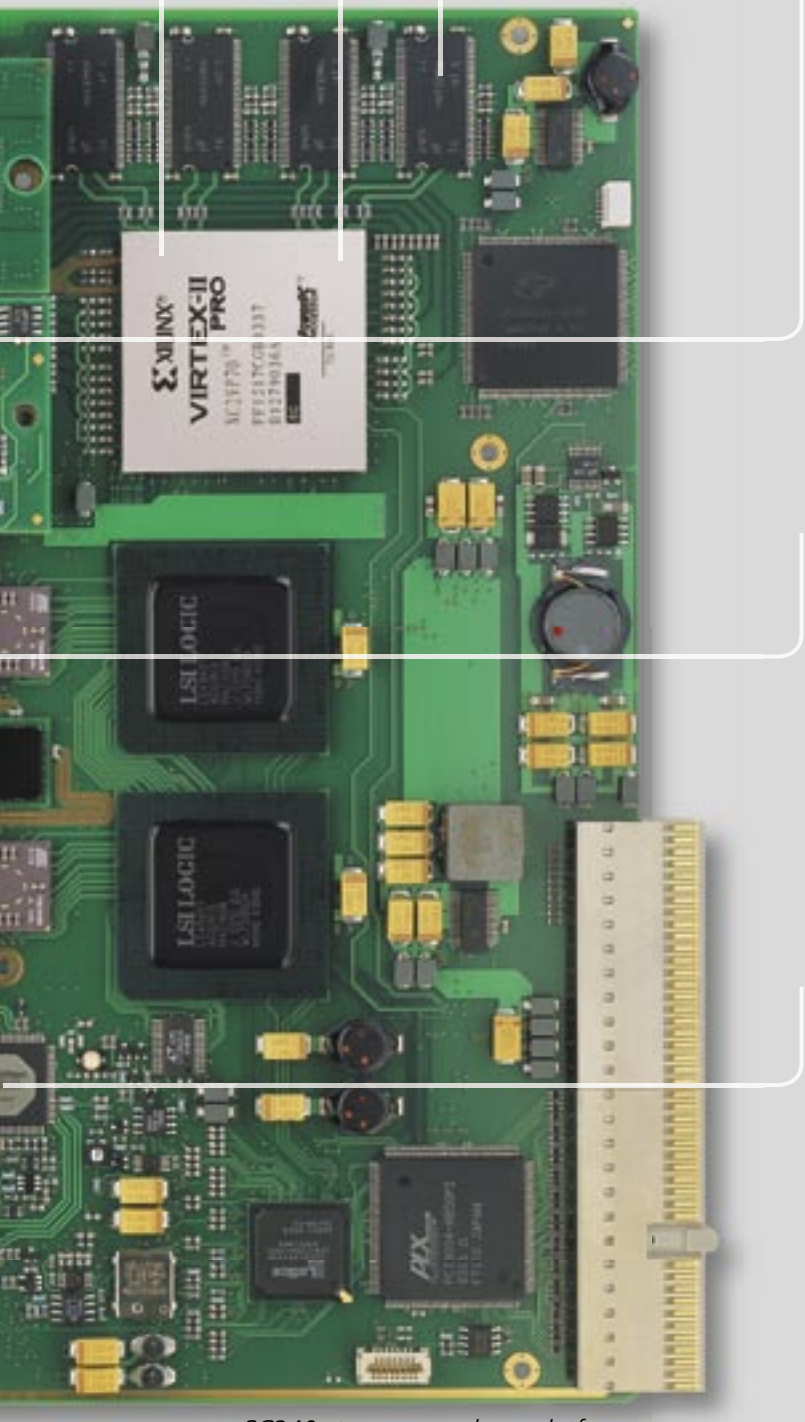
- On-board reconfigurable Data Processing Unit (DPU Xilinx Virtex II Pro) for real-time operations.
- The DPU is easily and quickly reconfigurable using Acqiris-supplied drivers to reload firmware under program control.



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Built-In Processing Memory

> 7 Mbits of on-chip RAM are available to the user for custom real-time algorithms.



SC240 streamer analyzer platform.

External Processing Memory

> Optional external processing memory providing 512 MB of DDR-SDRAM 333 MHz and 1 MB of dual-port SRAM with a read/write throughput of up to 2 GB/s to and from the DPU.



ODL

Maximum Data Throughput

The on-board optical transceivers of the Optical Data Link (ODL) provide for data transfer through 2 or 12 (optional) optical fibers, offering up to 5 or 30 Gbps of data throughput.

Firmware included with the platform allows data streaming of acquired data using the Serial FPDP protocol. This firmware allows acquisition and transfer of all acquired data with no dead-time and no loss of data at rates of up to 2 GS/s.

Each link is connected to a Rocket I/O™ serializer-deserializer circuit present on the on-board FPGA. The ser-des circuits provide direct links between the FPGA and the optical transceiver, and allow generation of parallel data (8, 16 or 32 bits) into a serial data stream for transmission through the optical data links.

GHz BW Front End with 50 mV – 5 V FS

The analyzer's channel inputs feature the **XL***Fidelity* front-end amplifier chip, FEA102. This circuit includes a programmable gain amplifier (PGA) with on-chip filtering and trigger circuitry. It provides pre-ADC signal conditioning and amplification, essential for high performance high-speed data conversion systems.

The PGA provides four global gain settings: 1.0, 2.0, 5 and 10. The filter section, which is useful for signal noise reduction, allows 2-pole Bessel bandwidth limiting at 700 MHz and 200 MHz and a single-pole filter at 20 MHz.

Precision Time Base

The **Jet***Speed* COS101 crystal-controlled precision time base drives the data conversion on both channels and sample rates can be selected in a 1, 2, 2.5, 4 and 5 sequence, from 100 MS/s to 2 GS/s (1 GS/s with the SC210).

In digitizer mode an internal Time-to-Digital Converter (TDC) allows accurate positioning (5 ps resolution) of the trigger signal with respect to the internal clock (sampling time).

The sample rate can also be generated externally, using the dedicated CLK IN connector, for applications where the sample rate must be synchronized with the device generating the signal.

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Streamer Analyzer Platforms

Model SC240

Dual-channel, 8-bit, 1 GHz, 1-2 GS/s, CompactPCI/PXI Streamer Analyzer Platform

Model SC210

Single-channel, 8-bit, 1 GHz, 1 GS/s, CompactPCI/PXI Streamer Analyzer Platform

Signal Input

Bandwidth (-3 dB)
DC to 1 GHz, guaranteed

Bandwidth Limit Filters
700 MHz, 200 MHz and 20 MHz

Full Scale (FS)
50 mV, 100 mV, 200 mV, 500 mV,
1 V, 2 V and 5 V

VSWR (typical)
< 1.25 from DC to 1 GHz

Channels
SC240: two @ 1 GS/s or
one @ 2 GS/s
SC210: one @ 1 GS/s

Offset Range
±2 V from 50 to 500 mV FS
±5 V from 1 to 5 V FS

Connectors
BNC, gold-plated

Coupling
DC, AC, or ground coupling

Maximum Input Voltage
±5 V DC

Impedance
50 Ω ± 1% @ DC

Digital Conversion

Sample Rate
SC240: 100 S/s to 2 GS/s
SC210: 100 S/s to 1 GS/s
In 1, 2, 2.5, 4 and 5 sequence

Resolution
8 bits (1:256)

Differential Nonlinearity
±0.8 LSB

Integral Nonlinearity
< ±1% of FS

DC Accuracy
< ±2.0% of FS at 0 V offset
±1% of FS typical

Effective Bits (typical)
7.0 @ 10 MHz, 1 GS/s
6.7 @ 100 MHz, 1 GS/s

SFDR (typical)
> 55 dB @ 10 MHz
> 40 dB @ 400 MHz

Clock or Reference Input

Input Amplitude
> 500 mV pk-pk into 50 Ω

Connector
MMCX, gold-plated

Ext. Clock/Ref. Threshold
Variable between -2 V and +2 V

Maximum Input Voltage
±2 V DC

Ext. Reference Frequency
[9.0, 10.2] MHz

Ext. Clock Frequency
From 10 MHz to 2 GHz

A high-speed front-panel bus (ASBus) distributes clock and trigger to synchronize multiple modules.

Time Base

Clock Accuracy
Better than ±2 ppm

Trigger Time Interpolator
5 ps resolution (digitizer mode)

Sampling Jitter
< 1 ps RMS
(for 10 µs record length)

Acquisition Modes
Digitizer
Single shot, Sequence

Analyzer
Streaming to DPU

Trigger (Internal and External, Digitizer Mode)

Internal Trigger Input
Threshold adjust range:
same as vertical FSR

Sensitivity: up to full BW
for > 15% FSR pk-pk signals

External Trigger Input
BNC, gold-plated
Impedance: 50 Ω ±1 %
Threshold adjust range:
[-FS/2,+FS/2] for FS = 0.5, 1, 2, 5 V

Maximum input voltage: ±5 V DC

Sensitivity: up to full BW for > 10% FSR
pk-pk signals

Coupling
DC
AC (50 Hz LFReject)
HFReject (50 kHz)

Modes
Edge, positive and negative, Window,
HF: divide by 4

Trigger Output [1)]

Output Level
Adjustable in range ±2.5 V (no load)
Amplitude ±0.8 V (no load)
15 mA max.

Rise/Fall Time
2.5 ns

Connector
MMCX, gold-plated

Coupling
DC

Output Impedance
50 Ω

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Optical Data Links

Standard ODL
Transceiver: 2 x Small Form Pluggable
Multimode 850 nm
Connector: LC™ Duplex
Throughput: up to 2.5 Gbps/link
Aggregate: up to 5 Gbps

High Rate ODL
Transceiver: PAROLI® 2, 1x Tx and 1x Rx,
Multimode 850 nm
Connector: MPOF-12
Throughput: up to 2.5 Gbps/link
Aggregate: up to 30 Gbps

Control I/O (A & B) [1)]

Connectors
2x MMCX, gold-plated

Input
Trigger enable

Signals
TTL & CMOS compatible (3.3 V)

Output
10 MHz reference clock
Acquisition skipping to next segment
Acquisition active
Trigger ready

Data Processing Unit and Control Signals

DPU
Xilinx Virtex-II Pro XC2VP70-6

DPU Ctrl2 Signals
TTL & CMOS compatible (3.3 V)
through I/O P1 & P2 (MMCX)

LVDS & LVPECL (2.5 V)
through I/O EXT (µDB-15)

Analog Output Signal
-5 to +5 V (settling time, 1 µs typical)
through ANL Out (MMCX)

DPU Ctrl Connectors
2x MMCX, gold-plated
1x µDB-15 (additional processing I/Os)

DPU Processing Memory [2)]
Up to 7 Mbits on-chip RAM

Optional 512 MB DDR-SDRAM
333 MHz & 1 MB dual-port SRAM

PC System Requirements

Processor
150 MHz Pentium (or higher)

Operating System
Windows 95/98/NT4/2000/XP
Wind River VxWorks or Linux

CD Drive

Memory
64 MB RAM (more is recommended when working with several cards with large memories)

Hard Drive Space
20 MB minimum

Environmental and Physical

Operating Temperature
0° to 40°C

Required Airflow
> 2 m/s in situ

Relative Humidity [3)]
5 to 95% (non-condensing)

EMC Immunity
Complies with EN61326-1
Industrial Environment

Dimensions
6U CompactPCI/PXI standard
233 mm x 160 mm x 20 mm

Shock [3)]
30 G, half-sine pulse

Vibration [3)]
5 – 500 Hz, random

Safety
Complies with EN61010-1

EMC Emissions
Complies with EN61326-1 Class A for radiated emissions

[1)] Contact Acqiris for details on the implementation of these signals using DPU firmware.

[2)] Available data point capacity of processing memory varies depending on data handling by the applied firmware.

[3)] As defined by MIL-PRF-28800F Class 3.

Front panel complies with IEEE1101.10

CE Certification and Compliance

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