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Edition 2
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Documentation History

All Editions and Updates of this manual and their creation date are listed below. The first Edition of the manual is Edition 1. The Edition number increments by 1 whenever the manual is revised. Updates, which are issued between Editions, contain replacement pages to correct or add additional information to the current Edition of the manual. Whenever a new Edition is created, it will contain all of the Update information for the previous Edition. Each new Edition or Update also includes a revised copy of this documentation history page.

Edition 1 . . . . . Novemberr, 1989
Update 1 . . . . . November, 1989
Edition 2 . . . . . April, 1995

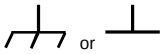
Safety Symbols



Instruction manual symbol affixed to product. Indicates that the user must refer to the manual for specific WARNING or CAUTION information to avoid personal injury or damage to the product.



Indicates the field wiring terminal that must be connected to earth ground before operating the equipment—protects against electrical shock in case of fault.



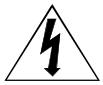
Frame or chassis ground terminal—typically connects to the equipment's metal frame.



Alternating current (AC).



Direct current (DC).



Indicates hazardous voltages.

WARNING Calls attention to a procedure, practice, or condition that could cause bodily injury or death.

CAUTION Calls attention to a procedure, practice, or condition that could possibly cause damage to equipment or permanent loss of data.

WARNINGS

The following general safety precautions must be observed during all phases of operation, service, and repair of this product. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the product. Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements.

Ground the equipment: For Safety Class 1 equipment (equipment having a protective earth terminal), an uninterruptible safety earth ground must be provided from the mains power source to the product input wiring terminals or supplied power cable.

DO NOT operate the product in an explosive atmosphere or in the presence of flammable gases or fumes.

For continued protection against fire, replace the line fuse(s) only with fuse(s) of the same voltage and current rating and type. DO NOT use repaired fuses or short-circuited fuse holders.

Keep away from live circuits: Operating personnel must not remove equipment covers or shields. Procedures involving the removal of covers or shields are for use by service-trained personnel only. Under certain conditions, dangerous voltages may exist even with the equipment switched off. To avoid dangerous electrical shock, DO NOT perform procedures involving cover or shield removal unless you are qualified to do so.

DO NOT operate damaged equipment: Whenever it is possible that the safety protection features built into this product have been impaired, either through physical damage, excessive moisture, or any other reason, REMOVE POWER and do not use the product until safe operation can be verified by service-trained personnel. If necessary, return the product to a Hewlett-Packard Sales and Service Office for service and repair to ensure that safety features are maintained.

DO NOT service or adjust alone: Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT substitute parts or modify equipment: Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to a Hewlett-Packard Sales and Service Office for service and repair to ensure that safety features are maintained.

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Manufacturer's Name: Hewlett-Packard Company
Loveland Manufacturing Center

Manufacturer's Address: 815 14th Street S.W.
Loveland, Colorado 80537

declares, that the product:

Product Name: Register Based Breadboard Module

Model Number: E1399A

Product Options: All

conforms to the following Product Specifications:

Safety: IEC 1010-1 (1990) Incl. Amend 1 (1992)/EN61010-1 (1993)
CSA C22.2 #1010.1 (1992)
UL 1244

EMC: CISPR 11:1990/EN55011 (1991): Group1 Class A
IEC 801-2:1991/EN50082-1 (1992): 4kVCD, 8kVAD
IEC 801-3:1984/EN50082-1 (1992): 3 V/m
IEC 801-4:1988/EN50082-1 (1992): 1kV Power Line
.5kV Signal Lines

Supplementary Information: The product herewith complies with the requirements of the Low Voltage Directive 73/23/EEC and the EMC Directive 89/336/EEC and carries the CE-marking accordingly.

Tested in a typical configuration in an HP B-Size VXI mainframe.



April, 1995 **Jim White, QA Manager**

European contact: Your local Hewlett-Packard Sales and Service Office or Hewlett-Packard GmbH, Department HQ-TRE, Herrenberger Straße 130, D-71034 Böblingen, Germany (FAX +49-7031-14-3143).

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• Examples are clear and useful.	O	O	O	O	O
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Chapter 1
HP E1399A Introduction

Manual Contents

This manual has three chapters and two appendixes:

- **Chapter 1 - Introduction** summarizes manual contents, warranty status, and specification compliance. It also includes an overall description of the module.
- **Chapter 2 - Configuring the HP E1399A** describes module hardware and dimensions, and discusses operation of the backplane interface circuits on the module. It also provides a typical application example showing user circuits connected to the backplane interface circuits.
- **Chapter 3 - Using the HP E1399A** shows how to use the module in a VXIbus system.
- **Appendix A - HP E1399A Breadboard Specifications** lists the hardware specifications for the HP E1399A module.
- **Appendix B - HP E1399A Parts List/Schematic** provides HP part numbers and descriptions of all parts required by the HP E1399A. It also includes a complete schematic of the E1399A digital backplane interface.

Specification Compliance/Warranty

The HP E1399A Breadboard Module is designed in full compliance with the VMEbus Specification (Revision C.1) and the VXIbus specification (Revision 1.3).

The HP E1399A warranty statement, located at the front of this manual, is different from the standard Hewlett-Packard warranty for the HP E1300A/E1301A mainframe and other plug-in modules. Hewlett-Packard is only responsible for defects in materials and workmanship of the blank circuit board and supplied hardware.

Warning **Hewlett-Packard is not responsible for the performance of your custom-designed circuitry. Hewlett-Packard is not responsible for damage to or improper operation of your VXI mainframe or other plug-in modules caused by the HP E1399A Breadboard Module.**

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HP E1399A Description

The HP E1399A Breadboard Module is a B-size register-based device that provides a convenient interface to a VXI mainframe backplane. It allows you to construct your own custom hardware for use with the mainframe.

General Module Features

The module is supplied with all interface components loaded and soldered.

Your VXI mainframe can communicate with this module configured as an A16/D16 device. The breadboard module interface circuitry is implemented and accessible according to the requirements outlined in the VXIbus Specification.

Users can still provide custom extensions to expand module addressing capability to A24 or A32 by adding appropriate circuitry according to the VMEbus and VXIbus specifications.

Backplane Interface Features

An overview of the HP E1399A interface features follows. Figure 1-1 shows a block diagram of this interface.

Note

For hardware operation, a mnemonic suffixed with an asterisk (such as WRITE*) indicates inverse logic (0 or low = true; 1 or high = false). A high state (1) is defined as a positive voltage (usually +5 V) and a low state (0) is defined as zero V (ground) at the specified signal point.

The HP E1399A interface features are:

- **Address Lines and Register Decoding.** The module implements 15 address lines (A1-A15) to allow for: 1. decoding one of 255 switch-selectable logical device addresses in the upper fourth of the A16 VME address space, and 2. selecting one of the breadboard configuration registers for read/write operations. The module decodes the Address Modifier lines AM0-AM5 and acts on codes 29_{16} and $2D_{16}$ only.
- **Data Lines.** Data lines D0-D15 are available for use on the Breadboard module. These 16 lines are buffered by data bus drivers and used for writing to, and reading from, the configuration registers (Status, ID, Device Type, and Control) via an internal data bus (DB0-DB15).

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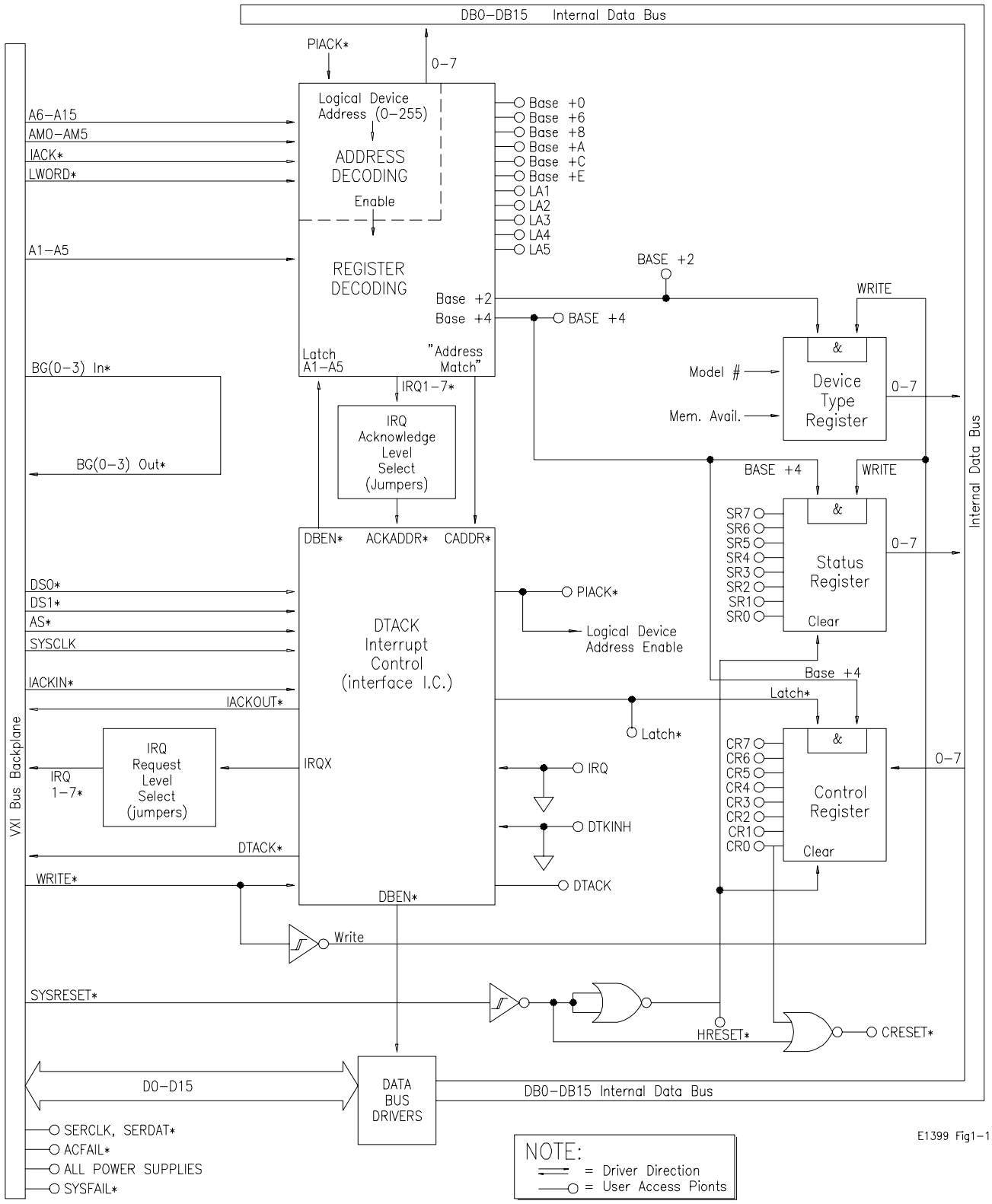


Figure 1-1. Digital Backplane Interface Block Diagram

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- **Status Register.** A read of this 8-bit register provides information about the status of the breadboard module. Implemented signals are "Extended*" and "Passed". There are also provisions for implementing device-dependent status bits.

- **ID Register.** A read of this 16-bit register identifies the Manufacturer ID number, the Device Class, and the addressing mode of the Breadboard. This register is implemented as a Hewlett-Packard A16 register bassed device.

- **Device Type Register.** A read of this 8-bit register identifies the unique card model as defined by the device manufacturer. The card model number is switch selectable.

- **Control Register.** A write to this 8-bit register causes specific actions to be executed by the device. "Reset" and "System Fail Inhibit" are implemented. Other device-dependent control bits may be implemented by the user.

- **Read/Write Operations.** Using the backplane interface circuitry provided, it is possible to read the contents of the Status, ID, or Device Type Registers onto the data bus (D0- D15), or to write information into the Control Register from the data bus.

- **DTACK.** The interface contains the circuitry required for generating a delayed DTACK* (data transfer acknowledge) signal.

- **Interrupt Interface.** The breadboard module has D16 interrupter capability. It does not contain an interrupt handler. Interrupt priority is jumper-selectable for pulling the appropriate interrupt request line IRQ1* - IRQ7*. Interrupts are generated by the IRQ state machine on the Interface IC (U6). The daisy-chained IACKIN*/IACKOUT* signal pair is implemented.

- **Module Reset.** Both hardware and software reset signals are provided to initialize the backplane interface circuitry and your own custom-designed circuitry to a known state.

- **Backplane Buffering.** Buffering is provided for all signals that interface with the VXIbus backplane.

- **Power Supply.** The following power supply voltages (all unfiltered) are available:
  - +5 VDC, fused at 4 Amps
  - + 12VAC, fused at 4 Amps
  - -12VAC, unfused
  - +5VDC standby, unfused

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HP E1 399A Hardware Features

An overview of the HP E1399A hardware features follows.

- **Connectors.** Two 96-pin DIN connectors are provided with the module. P1 connects to the VXI backplane, while J1 allows connection of devices from the front of the board, or connection of an E1399A terminal card.
- **Component Area.** An area of approximately 220 cm^2 (34 in^2) is available on the module to install your own custom circuitry. This area does not include the portion of the circuit board required by the backplane interface components.
- **Component Height/Lead Length.** The maximum component height allowed above the circuit board is 12.7 mm (0.5 in). The maximum component lead length allowed below the circuit board is 1.3mm (0.05 in).

Warning **Since the inputs to the HP1399A Breadboard Module are through a 96-pin connector and a terminal card assembly, limit voltage to 250Vdc/250Vrms.**

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Chapter 2
Configuring the HP E1399A

This Chapter contains a detailed hardware description of the breadboard module and discusses the backplane interface circuitry. It also shows a sample application to control 16 relays on the module.

Handling Precautions

WARNINGS, CAUTIONS, and guidelines to reduce the risk of static discharge damage to the HP E1399A follow.

Warning **SHOCK HAZARD. Only qualified, service-trained personnel who are aware of the hazards involved should install, remove, or configure any module. Before removing any installed module, turn off all power to the mainframe and to all external devices connected to the mainframe or to any of the modules.**

For electrical shock protection, ensure that the module face plate is securely tightened against the mainframe.

Warning **Since the inputs to the HP 1399A Breadboard Module are through a 96 pin connector and a terminal card assembly, limit voltage to 250Vdc/250Vrms.**

Caution **STATIC SENSITIVITY. The backplane interface circuitry described in this Chapter uses static-sensitive CMOS integrated circuit devices. If you implement the circuitry described herein, you must use clean-handling and anti-static techniques when handling the module to protect the sensitive components from damage due to electro-static discharge (ESD).**

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Reducing Risk of Static Discharge Damage

The smallest static voltage most people can feel is about 3500 V. It takes less than one-tenth of that (about 300 V) to destroy or severely damage static-sensitive circuits. Often, static damage does not immediately cause a malfunction, but significantly reduces the component's life. Adhering to the following precautions will reduce the risk of static discharge damage.

- Keep the module in its conductive plastic bag when not installed in a VXIbus mainframe. Save the bag for future module storage.
- Before handling the module, select a work area where potential static sources are minimized. Avoid working in carpeted areas and non-conductive chairs. Keep body movement to a minimum. If possible, use a static-controlled workstation.
- Avoid touching any components or edge connectors. When you are ready to configure the module, remove it from its protective bag and lay it on top of the bag while keeping your free hand in contact with the bag. This technique maintains your body and the module at the same static potential.
- When you install the module, keep one hand in contact with the protective bag as you pick up the module with your other hand. Then, before installing the module, move your free hand to a metal surface on the mainframe, thus bringing you, the module, and the mainframe to the same static potential.

Hardware Description

Figure 2-1 shows the module with interface circuit components installed. As shown, the module consists of a circuit board with one backplane connector (P1) and a front panel connector (J1). Approximately one-third of the circuit board contains traces for installing the backplane interface circuitry. See "Backplane Interface Circuitry" for interface circuitry installation.

Backplane Connections

The breadboard module interfaces your custom circuits to a standard B-size VXIbus backplane (connector P1). This enables you to access the backplane control signals, data lines, address lines, and power supplies. Figure 2-1 shows backplane connector (P1) which connects to the VXIbus backplane.

Module Dimensions

Figure 2-2 shows the dimensions of the module and the component height and lead length restrictions. The maximum component height allowed above the circuit board is 12.7mm (0.5in). The maximum component lead length allowed below the circuit board is 1.3mm (0.05in). Do not mount components closer than 4mm (0.16in) to the extreme upper or lower edges of the circuit board. This space is used to guide the module into the mainframe module slot. An area of 220 cm^2 (34 in^2) is available on the module to install your own circuitry.

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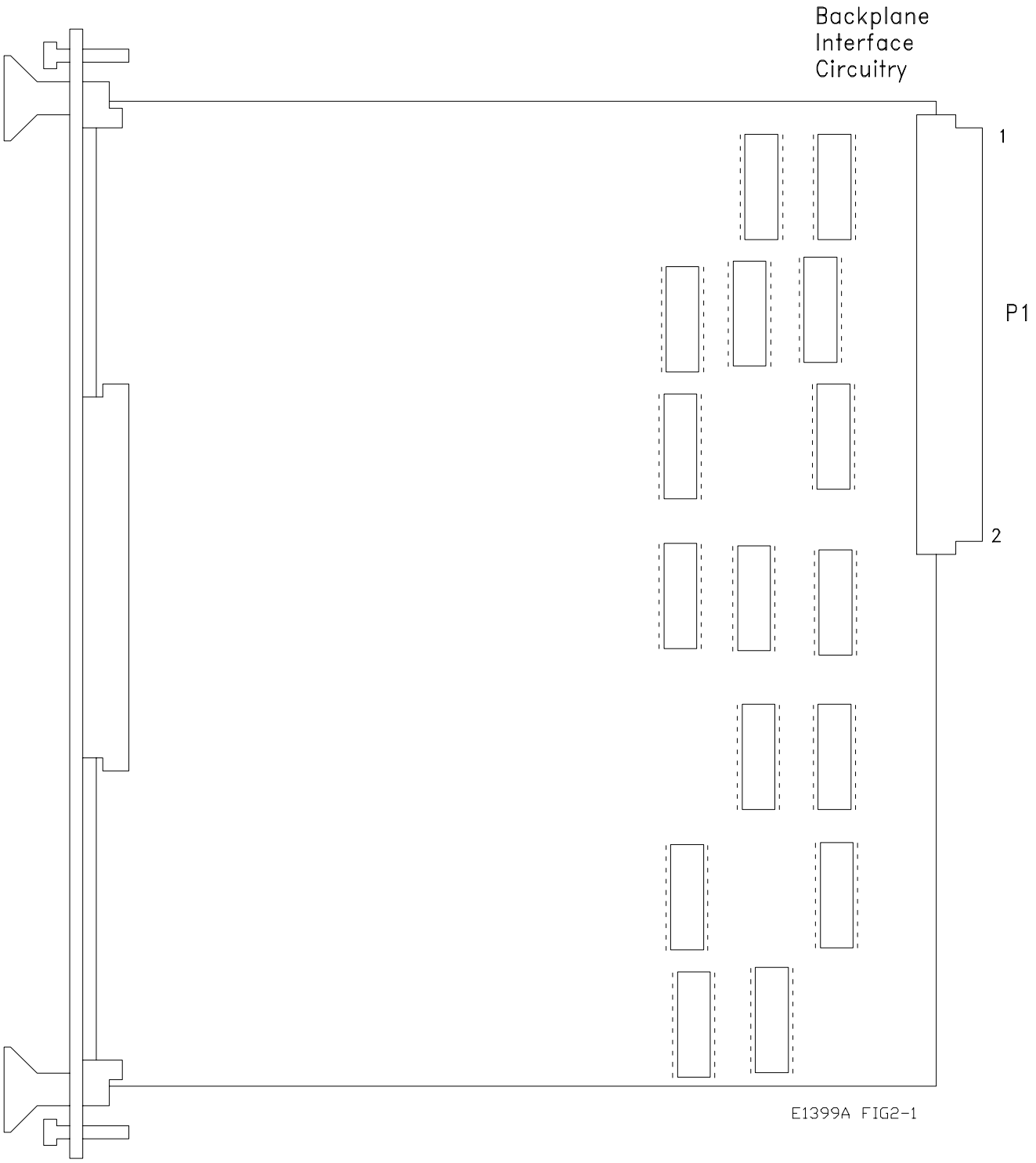


Figure 2-1. HP E1399A Breadboard Module & Connector Pinout

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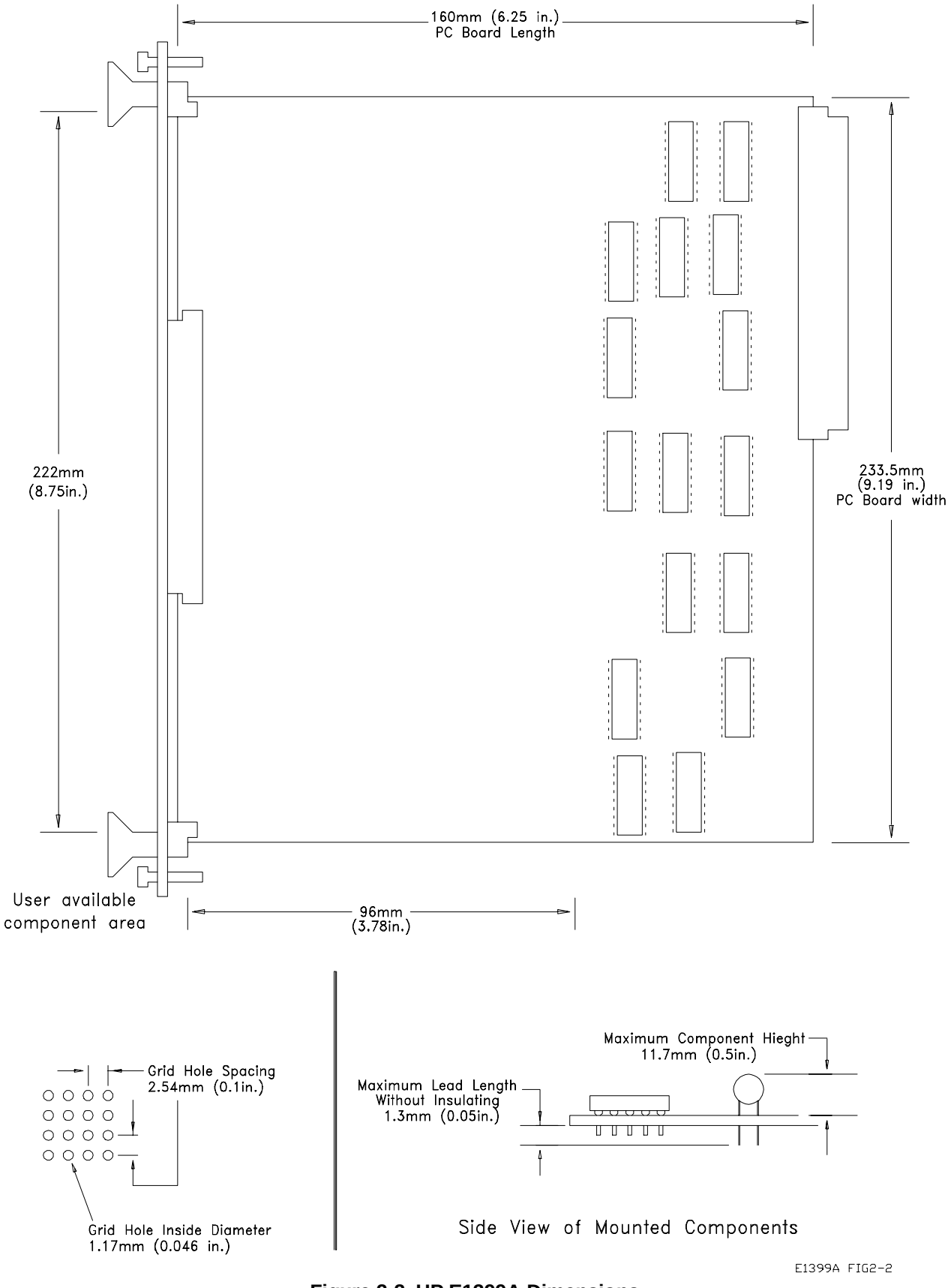


Figure 2-2. HP E1399A Dimensions

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Cooling Requirements

The VXIbus Specification requires module manufacturers to establish a cooling specification for each of their modules. The specification is to consist of: (1) the airflow required (in liters/second) for adequate cooling, and (2) the pressure drop that occurs across the module when the specified airflow is applied.

Note

It is the user's responsibility to furnish adequate cooling for any module to be used in a VXIbus system. Module cooling requirements are described in the VXIbus Specification (Rev 1.3) in Section B.7.2.4. Mainframe cooling requirements are discussed in Section B.7.3.5.

For ease of integration, you should label the airflow requirements for your finished application circuitry on the module. For example, the label might read: 0.3 liters/sec @ 0.2 mm/H_2O.

Due to the nature of a breadboard module, it is not possible to specify cooling requirements without knowing the application and the amount of power to be dissipated. Given the application, however, cooling requirements may be estimated as follows:

1. Determine the airflow required as a function of power dissipation. To maintain a 10ºC rise, approximately 0.08 liters/second are required for every watt dissipated. For example, if a module dissipates 20 watts, 1.6 liter/second of airflow is required for cooling.
2. Establish the relationship between airflow and pressure drop. For a breadboard loaded with typical components (such as ICs, relays, and a few heat sinks), the curve in Figure 2-3 may be used to determine the pressure drop across the module. Determine the pressure drop as the intersection of the curve and the required airflow. For example, if the airflow required is 1.6 liter/second, the pressure drop across a typically populated breadboard will be approximately 0.05 mm H_2O.

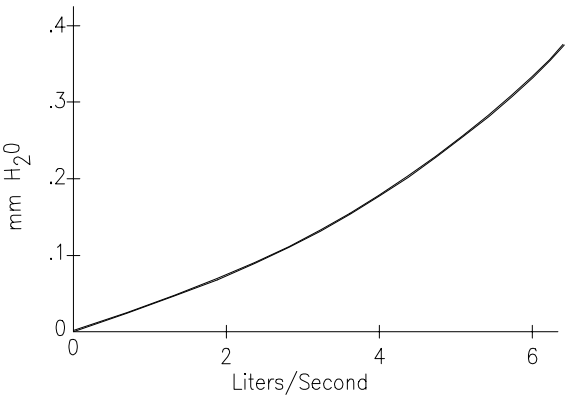


Figure 2-3. Pressure vs. Airflow

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Terminal Module

An optional terminal module is available for making external connections to the HP 1399A Breadboard Module. This module consists of a connector mounted on a breadboard so that you can access the connector pins by soldering wires to the breadboard. Figure 2-4 shows the layout of this terminal module. Figure 2-5 shows how to make the connections and install the module.

Warning

Since the inputs to the HP 1399A Breadboard Module are through a 96-pin connector and a terminal card assembly, limit voltage to 250Vdc/250Vrms.

For electrical shock protection, ensure that the module face plate is securely tightened against the mainframe before installing the terminal card.

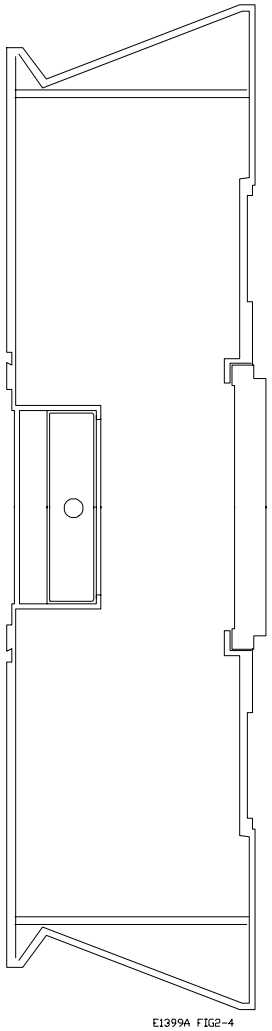


Figure 2-4. Terminal Module Assembly

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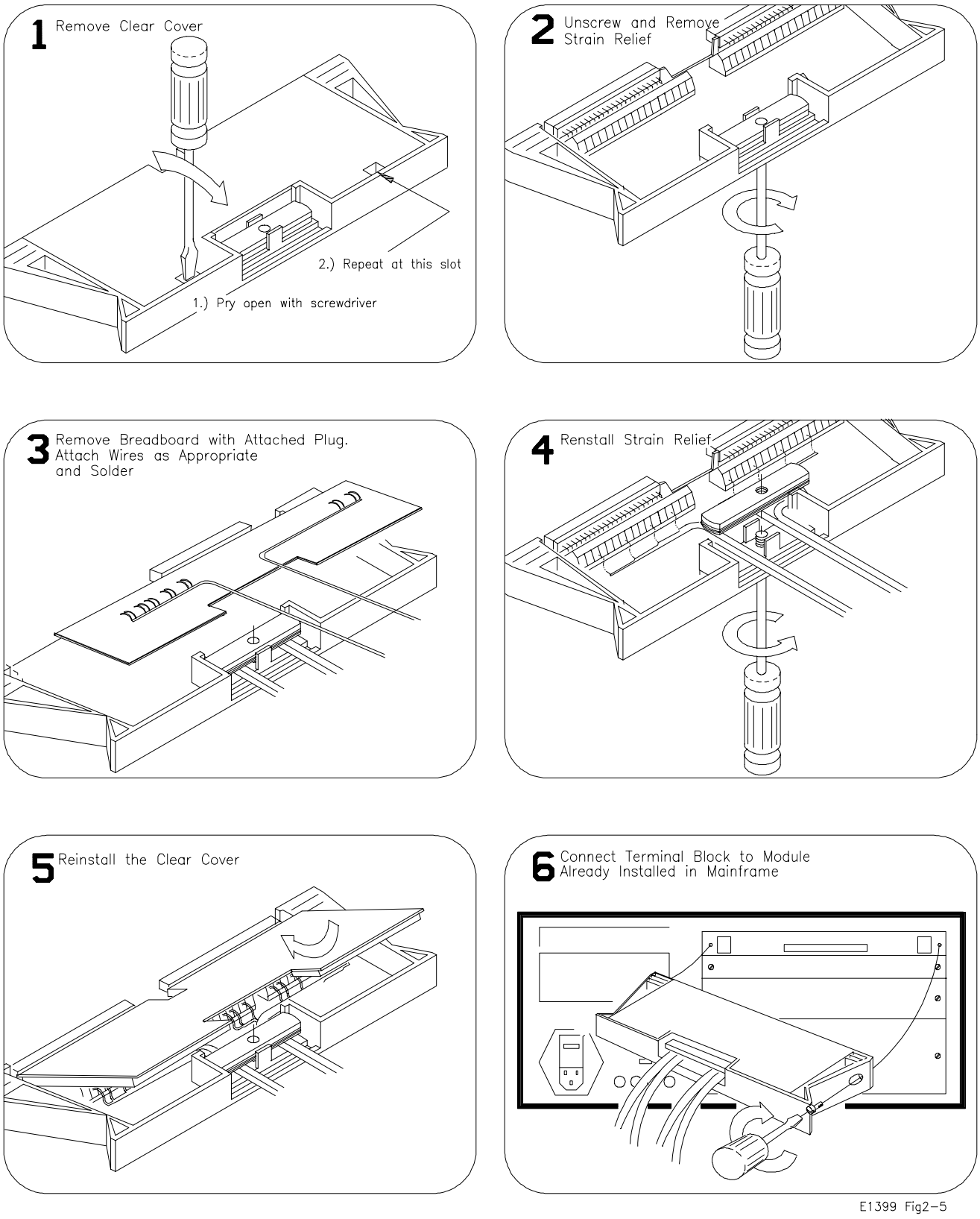


Figure 2-5. Terminal Module Installation

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Backplane Interface Circuitry

The backplane interface circuitry allows you to access the backplane control signals, data lines, address lines, and power supplies. Approximately one-fourth of the circuit board is reserved for installing the backplane interface components. All of the components required for the interface are provided with the module and are already loaded and tested. Your VXIbus mainframe can communicate with the HP E1399A in a manner similar to other VXIbus plug-in modules. The backplane interface circuitry consists of the following functional groups:

- Address Lines and Register Decoding
- Data Bus Drivers
- Status Register
- ID Register
- Device Type Register
- Control Register
- DTACK, Interrupt and Control
- Backplane Signals and Voltages Available on the Module

The following sections discuss the backplane interface functional groups. Each section includes a description, partial schematics, timing diagrams (where applicable), and a parts list showing the components required by that group. See Appendix B, "HP E1399A Parts List/Schematic" for a complete parts list, and for a schematic of the entire backplane interface.

Note

In the discussions of hardware operation that follow, a high state (1) is indicated by a positive voltage (usually +5 V) and a low state (0) is indicated by zero V (ground) at the specified signal point. A mnemonic suffixed with an asterisk (such as WRITE*) indicates inverse logic (0 or low = true; 1 or high = false).

Address Lines and Register Decoding

Figure 2-6 shows the address line and register decoding circuitry, while Table 2-1 shows the applicable parts list. The HP E1399A Breadboard Module is designed to be used as an A16/D16 device. As such, only backplane address lines A1-A15 and data lines D0-D15 have been implemented on the module.

To address the module, the information present on backplane lines A6-A13 must be identical to the logical address as set by address switch SP1(0-7). These eight bits allow up to 255 different VXIbus logical devices to be selected on a VXIbus system.

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Table 2-1. Address Lines and Register Decoding Parts

Reference Designator	HP Part Number	Description
RP25	1810-0279	Resistor, Network, 9-by- 4.7kOhms
SP1	3101-3066	Switch, DIP, 8 rocker 0.05A, 30VDC
U11	1820-3975	IC, 74HC541 Octal Line Driver
U20A, 9C	1820-4242	IC, 74HCT14, Schmitt Trigger Inverter
U17, 18	1820-3631	IC, 74HCT688N 8-bit Magnitude Comparator
U7, 8	1820-3079	IC, 74HC138N 3-to-8 Line Decoder
U15	1820-4147	IC, 74HCT573 Octal D-Type Latch

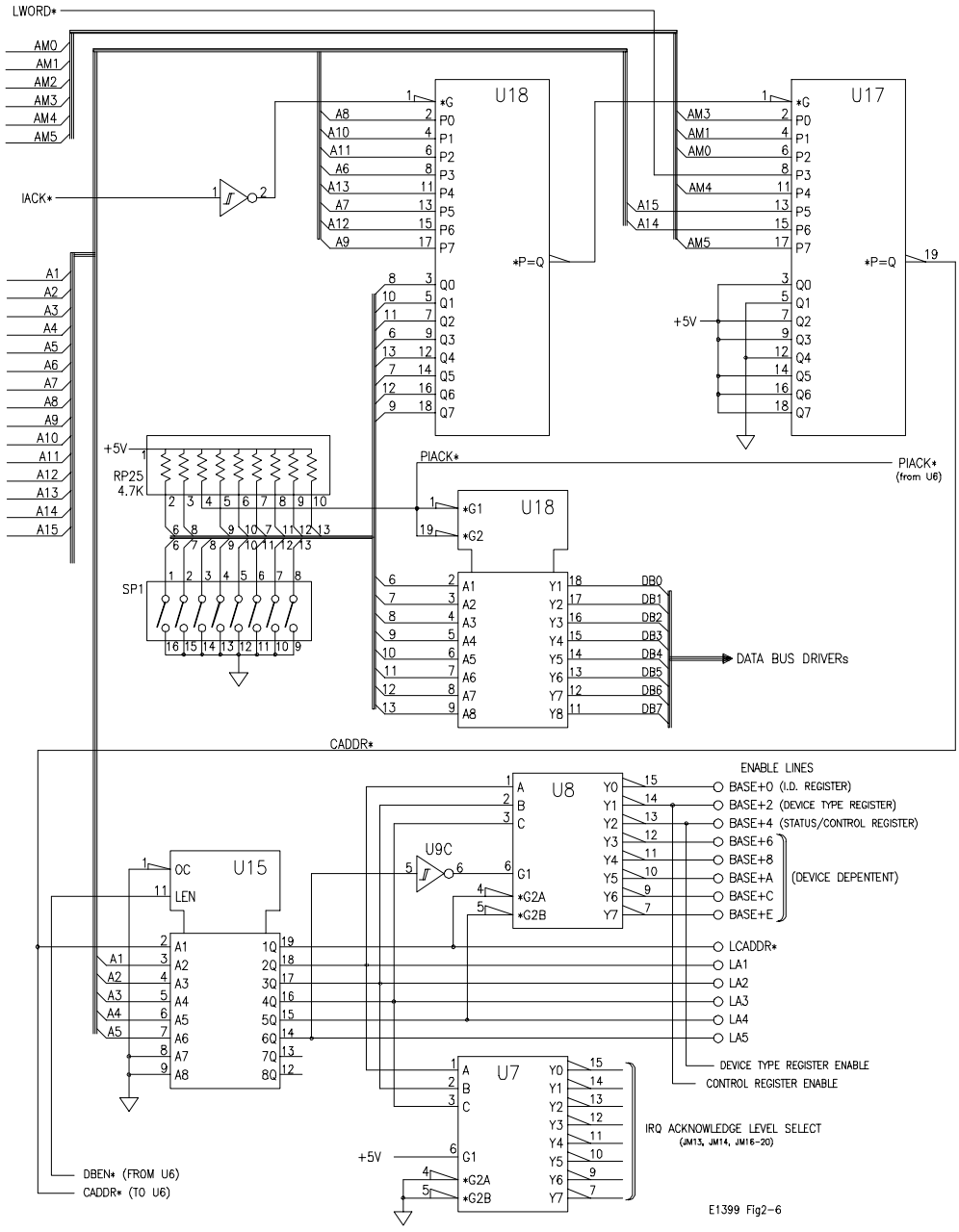


Figure 2-6. Address Lines and Register Decoding

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If a logical address match occurs and IACK* is high (false), equality detector U18 produces a low at its output which enables U17. Next, equality detector U17 compares the information on backplane lines A14, A15, AM0, AM1, and AM3-AM5 to a hardwired code of $11101X01_2$. Since AM2 is not examined, this hard-wired code will be a match if all three of the following conditions are true:

- a hexadecimal code of either 29_{16} or $2D_{16}$ is present on lines AM0-AM5.
- A14 and A15 are both high (1).
- LWORD* is high (false).

Either of the two address modifier hexadecimal codes indicated above will establish A16 addressing per the VXIbus Specification (Section C.2.1.1.4). In the VXIbus addressing scheme for an A16 device, A14 and A15 are always set to 1 to select the upper 16K of the 64K A16 address space (per the VXIbus Specification, Sections A.2.3.3 and C.2.1.1.1). LWORD* is high (false) when decoding short word transfers.

If a second match occurs at U17, its output goes low. This triggers a data transfer cycle using the DTACK state machine in the Interface IC (U6) by the low at U6 input CADDR* (See "DTACK, Interrupt, and Control" for more information on the DTACK state machine). As part of the data transfer cycle, U6 sets DBEN* low (true), latching the remaining backplane address lines (A1-A5) at the U15 outputs to the two 3-to-8-line decoders (U7 and U8).

Latch U15 ensures that the data is held valid until the data strobes go high (false) even though the address lines may no longer be valid.

U8 is enabled if G1 is high and both G2A and G2B are low. Therefore, A4 and A5 must both be low to select a register for connection to the data bus (D0-D15). G1 will be high (via U9C) if there was a match at U17. If U8 is enabled, backplane lines A1-A3 are decoded to specify which register (Status, ID, Device Type, or Control) is to be connected to the data bus.

Other user-supplied registers can be selected also. If additional decoding is necessary, A4 and A5 are accessible on the module. See Table 2-2 and Figure 2-6, for information on implementing your own register selections.

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Table 2-2. 1 Register Selection

A3 A2 A1	Enable Line	Register
0 0 0	Base + 0	ID
0 0 1	Base + 2	Device Type
0 1 0	Base + 4	Status/Control
0 1 1	Base + 6	User Assignable
1 0 0	Base + 8	User Assignable
1 0 1	Base + A	User Assignable
1 1 0	Base + C	User Assignable
1 1 1	Base + E	User Assignable

Data Bus Drivers

The HP E1399A Breadboard Module is designed to be used as an A16 and a D16 device only. As such, only backplane address lines A1-A15 and data lines D0-D15 have been implemented on the module.

VXIbus backplane connector P1 contains 16 bi-directional data lines labeled D0 through D15. The breadboard module connects to these data lines using the circuitry shown in Figure 2-7 (Table 2-3 shows the Data Bus Drivers parts list). Data buffering is provided for the data lines by two tri-state octal bus transceivers. U16 buffers D0 through D7 and U35 buffers D8 through D15. Note that the data lines are labeled DB0 through DB15 on the module side of the buffers.

U16 and U35 are enabled during a data bus transfer cycle when DBEN* (Data Bus Enable) goes low (true). This occurs whenever the breadboard is correctly addressed by a match of the module's logical address as set by SP1(0-7).

The direction of data transfer is determined by WRITE*. When WRITE* is low (a "write" operation), information present on backplane lines D0-D15 is transferred to the breadboard Control Register via DB0-DB15. When WRITE* is high (a "read" operation), information present on DB0-DB15 is transferred to backplane lines D0-D15.

Note WRITE* is the signal available on the VXI bus backplane. This signal is converted immediately to WRITE via U20F (schmidt trigger inverter). The signal accessible to the user on the breadboard is WRITE, not WRITE*.

During a normal read operation, the information present on DB0-DB15 is selected by the Address Decode circuitry from one of two sources:

- Status Register (U14)
- Device Type Register (U10)

You can also write to or read from up to five more device-dependent registers using the extra enable lines provided. Refer to Table 2-2 and to Figure 2-6 to see the user-assignable enable lines.

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Table 2-3. Data Bus Drivers Parts

Reference Designator	HP Part Number	Description
RP26,32 U16,35	1810-0279 1820-3714	Resistor Network, 9- by 4.7kOhm IC, 74ALS245A-1 Octal Bus Trnscvr, TTL

Status Register

The Status Register is an 8-bit register which provides some specific status information (as defined by the VXIbus Specification), and which has other bits available for custom (device dependent) status information as implemented by the user.

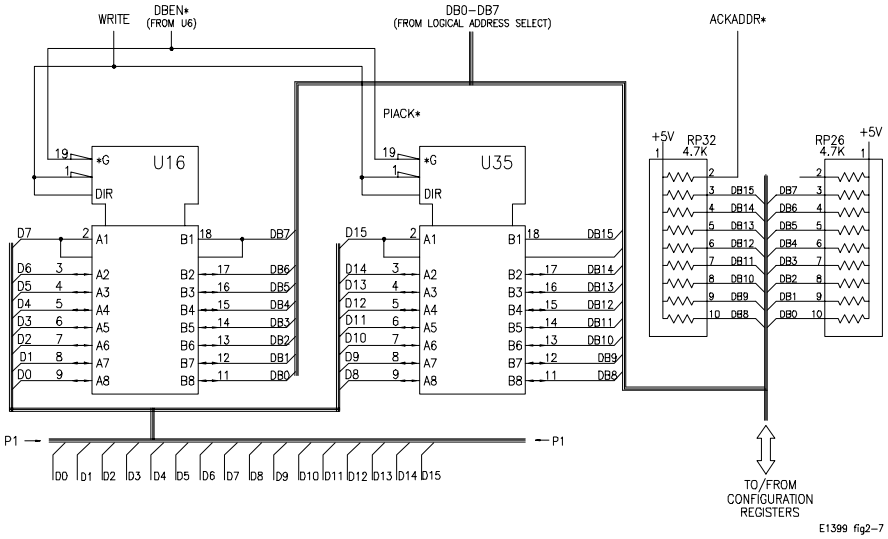


Figure 2-7. Data Bus Drivers

Table 2-4 shows the status register bit definitions. See Chapter 3, "Using the HP E1399A" for additional information on using the status register. Refer to the VXIbus Specification, Section C.2.1.1.2, for detailed information concerning status register implementation restrictions.

Table 2-4. Status Register Bit Definitions

Data Bit(s)	Definitions
SR0 - SR1 SR2 SR3 SR4 - SR7	Device Dependent (User assignable) (0=Failed/Executing Self-test, 1=Passed Self-test) (If 0, and Passed bit = 1, Extended Self-test active) Device Dependent (User assignable)

As shown in Figure 2-8, the status register circuitry consists primarily of the data bus line Driver U14, and a resistor network. Table 2-5 shows the parts list for the status register.

The status register is enabled during a "read status register" operation by the BASE+4 enable line set low (decoded from address lines A1-A3), and by

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WRITE* set high (false). The information presented to U14 by status lines SR0-SR7 is placed on the internal data bus (DB0-DB7). The user must provide any latches required to latch and hold this information.

Table 2-5. Status Register Parts

Reference Designator	HP Part Number	Description
RP2 U14	1810-0279 1820-3975	Resistor Network, 9- by 4.7kOhm IC, 74HC541 Octal Line Driver

Device Type Register

The Device Type Register is an 8-bit register which contains a device-dependent "module type" identifier. This field is set on the module by the use of an 8-position DIP switch on the inputs to the data bus line driver U10, as shown in Figure 2-9. Table 2-7 shows the resistor and IC part numbers for a Device Type Register.

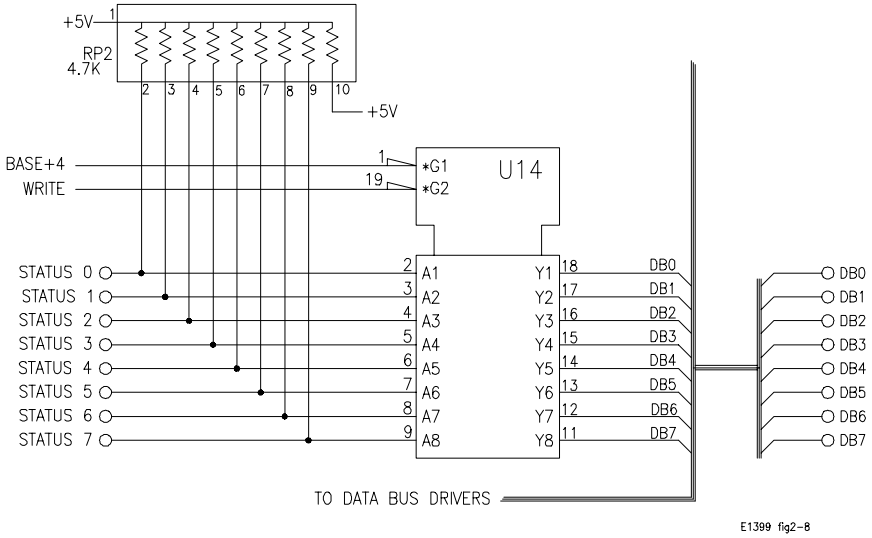


Figure 2-8. Status Register

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Table 2-6. Device Type Register Bit Definitions

Data Bit(s)	Definitions
DB0-DB7 DB8-DB15	Device Type or Model Code (Range = 0-4095) Set to "1"

Table 2-7. Device Type Register Parts

Reference Designator	HP Part Number	Description
RP1 U10 SP2	1810-0279 1820-3975 3101-3066	Resistor Network, 9- by 4.7kOhm IC, 74HC541 Octal Line Driver Switch,DIP,8-Rocker .OSA 30VDC

Each bit in the Device Type Register is normally pulled high (1) by RP1.

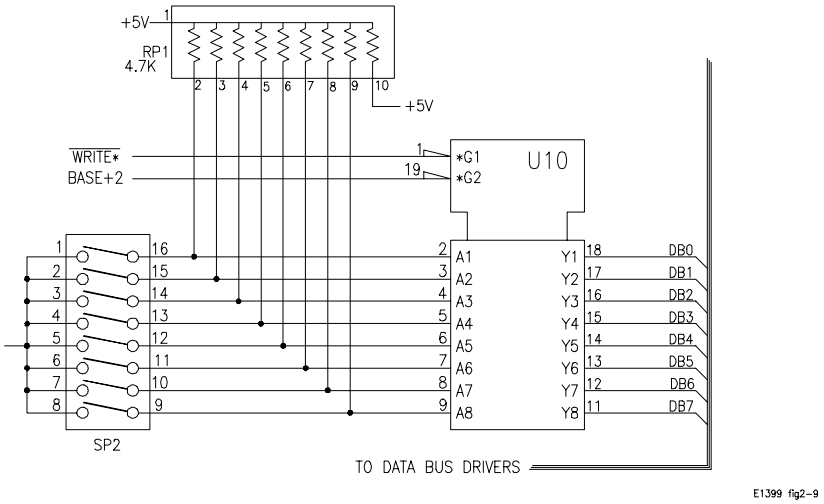


Figure 2-9. Device Type Register

The bits can be reconfigured using the DIP switch. The range of device types for an A24 or A32 device is 0 - 4095. For an A16 device, all 16 bits are available for specifying the device type for a range of 0- 65535. The user will need to add the required buffer and resistor network to implement the full A16 device type range. The default factory setting is FFxxh.

Note Per the VXIbus Specification (OBSERVATION C.2.6), device types 0-255 are reserved for register-based Slot 0 devices.

Refer to the VXIbus Specification, Section C.2.1.1.2 for detailed information concerning Device Type Register implementation restrictions. Table 2-6 shows the Device Type Register bit definitions.

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Control Register

The Control Register is an 8-bit register which causes specific actions to be executed by the breadboard module when written to from the backplane data bus. The primary component of the Control Register is U13, as shown in Figure 2-10. Table 2-9 shows the part number for U13.

Table 2- 8. Control Register Bit Definitions

Data Bit(s)	Definitions
CR0 CR1 CR2-CR7	CRESET (software reset) SYSFAIL INHIBIT Device Dependent (User assignable)

Table 2-9. Control Register Parts

Reference Designator	HP Part Number	Description
U13	1820-4086	IC, 74H(T~73 Octal D-Type Flip Flop

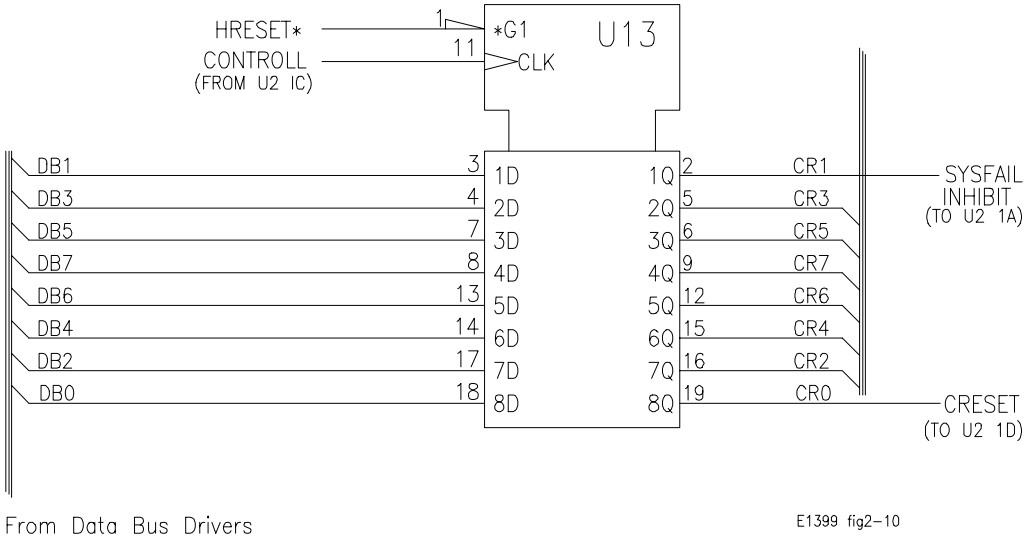


Figure 2-10. Control Register

Table 2-8 shows the Control Register bit definitions. The Control Register is selected for writing to by the BASE+4 enable line (see Table 2-2). BASE+4 going low at the input of U21C, combined with a negative pulse (for one clock cycle of SYSCLK) from the LATCH* output of U6 (also applied to U21C), provides a positive-going edge clocking pulse (CONTROL) to U13. This pulse clocks whatever is present on DB0-DB7 through U15 to the Control Register access points (CR0-CR7).

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Users may connect any or all of these points to custom circuitry, keeping in mind the pre-defined bit assignments shown in Table 2-2. Data present on DB0-DB7 would have been written there by the same DTACK state machine data transfer cycle that provided the LATCH pulse. See "DTACK" for a discussion of the DTACK state machine operation.

See Chapter 3, "Using the HP E1399A" for additional information on using the Control Register. Refer to the VXIbus Specification, Section C.2.1.1.2 for detailed information concerning Control Register implementation restrictions.

DTACK, Interrupt, and Control

An Interface IC (U6) provides the timing and control signals for standard data transfer cycles and interrupt requests/acknowledgments. Hardware and software reset signals, together with a card fail signal, have also been implemented.

DTACK

The Data Transfer ACKnowledge (DTACK) circuitry is centered around the Interface IC (U6). A state machine in this IC controls all read and write data transfer cycles. Operation begins with the state machine in the idle state. See Figure 2-11 for the following discussion. Table 2-10 lists the parts for the DTACK circuitry.

Table 2-10. DTACK Circuitry Parts

Reference Designator	HP Part Number	Description
U21C	1820 4643	IC, 74HCT02N Quad 2-input NOR
U6	1820-6731	IC, Interface (PAL)
U5C	1820-4057	IC, 74F38N Quad 2-input NAND Buffer
U20C,D,F	1820-4242	IC, 74HCT14 Hex Schmitt-Trig Invrtr

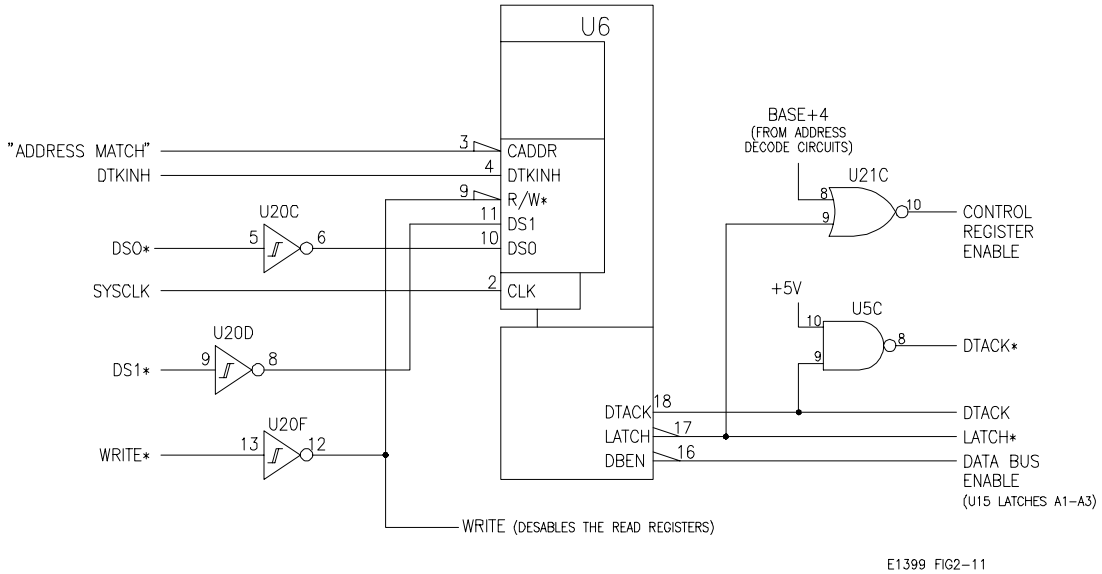


Figure 2-11. DTACK Circuitry

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In the first part of the transfer cycle, the system controller places the address of the breadboard module on the backplane address (A1-A15), address modifier (AM0-AM5), and address strobe (AS*) lines, and then sets the appropriate data strobe lines low (DS0* and DS1* for a D16 device). When the address equality detectors (U17, U18) detect the address match, the output of U17 goes low.

This low is sensed at the Card ADDRess (CADDR*) input to U6 which, together with the active data strobes, tells the DTACK state machine in the Interface IC (U6) that the module has been addressed for a data transfer cycle. This starts the state machine, with all signals being clocked by SYSCLK (16 MHz).

In the first active state, the data bus drivers (U16,U35) are enabled and the register-specifier part of the address (A1-A5) is latched onto the outputs of U15 using the Data Bus ENable (DBEN*) output of U1. If the data transfer cycle is a read operation (as indicated by WRITE* high), the decoded output of U8 determines which one of the registers (Status, ID, or Device Type) is enabled to put its contents onto the module's internal data bus (DB0-DB15).

The next state then generates a high at the DTACK output of U6. This forces DTACK* low (true) on the backplane through U5C, acknowledging to the system controller that the module has received the request for data and has placed the contents of the specified register onto the data lines. With U16 and U35 enabled, internal data lines DB0-DB15 are connected directly to the backplane data lines D0-D15.

If the data transfer cycle is a write operation (as indicated by WRITE* low), an additional state sets the U1 LATCH output low (enabling the Control Register to receive data from the data bus drivers) before DTACK* is set low (true). The resulting Control Register outputs (CR0-CR15) can then control the user's circuits, as desired. Again, DTACK* going low (true) tells the system controller that the data transfer cycle is complete. In a write operation, WRITE* going low (true) disables the Status Register, the ID Register, and the Device Type Register.

For both read and write operations, the DTACK state machine holds DTACK* low and the address latched until the data strobes are invalid. After the data strobes go invalid, the data bus drivers are disabled and the address latch is released. In the next state, DTACK* is released and the state machine returns to the idle state. If the DTACK INHibit signal (DTKINH) is set high (it is wire jumpered low on the HP E1399A implementation), it allows the user to hold the state machine in the first state of latched address and enabled data bus drivers.

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Interrupt

A priority interrupt scheme has been implemented using the Interface IC (U6). Another state machine controls interrupt request and acknowledge operations. See Figure 2-12 for the following discussion. Table 2-11 lists the parts for the Interrupt Circuitry.

Table 2-11 Interrupt Circuitry Parts

Reference Designator	HP Part Number	Description
U21C	1820-4643	IC, 74HCT02N Quad 2-input NOR Gate
U6	1820-6731	IC, Interface (PAL)
U5A,B,C	1820-4057	74F38N Quad 2-input NAND Buffer
U20B,C,D,F	1820-4242	IC, 74HCT14 Hex Schmitt-Trig Invrtr

The VMEbus interrupt request levels IRQ1*-IRQ7* are jumper-selectable

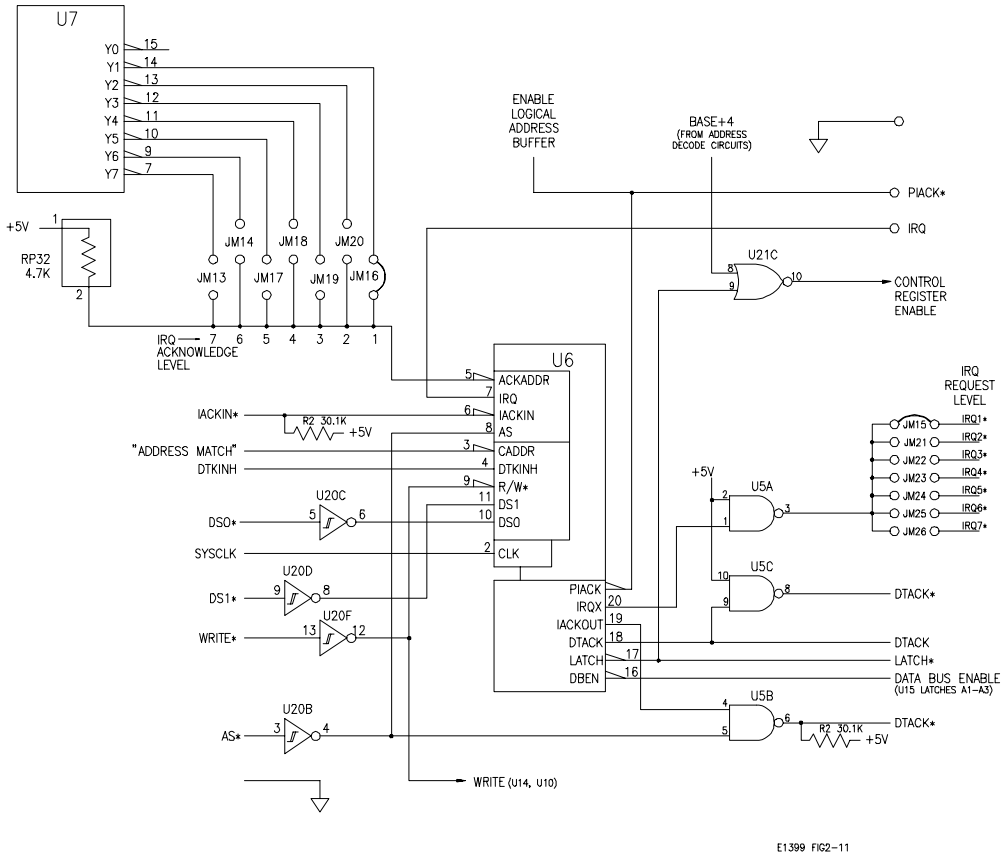


Figure 2-12. Interrupt Circuitry

(only one at a time allowed) for both the IRQ request output line (IRQ1*-IRQ7$) and the IRQ acknowledge input line (ACKADDR*). IRQ request and acknowledge levels must always be the same (IRQ1* is shown selected in Figure 2-12). To generate an interrupt request to the interrupt handler and start the IRQ state machine in U6, the user's custom circuits must provide a high signal at the IRQ access point input to U6 (ACKADDR).

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The IRQ state machine monitors the following interrupt-related lines to determine its actions: IACK*, valid DS0*, IACKIN*, AS*, ACKADDR*. If the module is asserting IRQ and the interrupt-related lines are in the proper state, the IRQ state machine asserts IRQX high (true) on U6.

IRQX high (true), inverted by USA, pulls the jumper-selected IRQ1* line low (true) on the backplane. The state machine then waits for the interrupt handler to recognize the interrupt request. When the interrupt handler responds, it places the code for the interrupt request priority level that it is acknowledging onto lines A1-A3. It then sets IACK* low (true) which sets IACKIN* low (true).

IACK* low (true) starts the interrupt acknowledge cycle, disabling normal address decoding on the breadboard module. When IACKIN* goes low (true), the IRQ state machine checks to see if its own IRQ level has been acknowledged (input line ACKADDR at U1 will be set low by a correct match of U7's decoded output and the jumper selection for IRQ ACKNOWLEDGE).

If its own level is not being acknowledged, or if the module is not asserting IRQ, the state machine passes the daisy-chained IACKIN* signal through IACKOUT on U6. The IACKOUT signal is gated with an inverted AS* to meet release time requirements for IACKOUT* as outlined in the VMEbus Specification.

If the acknowledge level matches the request level, the IRQ state machine sets PIACK* low (true), releases IRQX (and IRQ1*) and starts the DTACK state machine for a read cycle. The interrupt handler initiates the read cycle to get the logical device address from the interrupter when it sees IRQ1 * go low (true). PIACK* low (true) enables U11 to place the module's logical address (from SP1) onto the lower eight bits of the internal data bus (DB0-DB7).

The logical address is then transferred to backplane lines D0-D7 during the read data transfer cycle. In this way, the interrupt handler knows which device is asserting IRQ if more than one device has the same interrupt priority assigned to it.

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Control Table 2-12 shows the control signals which are implemented (see the "Backplane Interface Schematic" in Appendix B):

Table 2-12. Control Signals

Signal	Definition
AS*	Address strobe, used in data transfer cycles.
DSO*, DS1*	Data strobes, used in the data transfer cycles.
SYSCLK	Provides 16-MHz clock signals to Interface IC (U6) for clocking the state machines.
SYSFAIL*	SYSFAIL input. If the SYSFAIL INHBT line output of the Control Register (CR1) is also low (not inhibited), then SYSFAIL* is asserted.
SYSRESET*	System reset signal, normally used to initialize the backplane interface circuitry (and your own custom circuits) to a known state. Provides a hardware reset capability. As implemented (HRESET*), it clears the Status Register and the Control Register. It also asserts the software reset line (access point CRESET* on the module). CRESET* can also be asserted via software by writing a high signal to the Control Register (access point CR0), providing an input to U21D.

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User Access Points

The breadboard module contains traces (stubs) for accessing many of the signal lines on backplane connector P1. Table 2-13 shows the signal lines that are brought onto the module but not implemented. They are available as signal access points for your custom circuits.

Table 2-14 shows all of the implemented signal lines available as access points, either as inputs from the backplane to your own custom circuitry, or as outputs to the backplane from your custom circuits.

Table 2-13. User Access Points (Stubs)

Signal Lines	Description
ACFAIL*	AC Input Power failure
BERR*	Bus ERRor signal
SERCLK	Synchronizes data transmission on the VMSbus
SERDAT*	Used for VMSbus data transmission

Table 2-14. User Access Points (Implemented Signals)

A1-A5	Backplane address lines A1-A5 (latched)
BASE+0	ID Register Enable line
BASE+2	Device Type Register Enable line
BASE+4	Status and Control Registers Enable line
BASE+6	User-assignable Enable line
BASE+8	User-assignable Enable line
BASE+A	User-assignable Enable line
BASE+C	User-assignable Enable line
BASE+E	User-assignable Enable line
CR2-CR7	Control Register output lines
DB0-DB15	Breadboard Module internal Data Bus lines
DS0 & DS1	Buffered data strobes
SR0, SR1	Status Register (pulled up)
SR2	Status Register (pulled up)
SR3	Status Register (pulled up)
SR4-SR7	Status Register (pulled up)
DBEN*	Data bus buffer enable
CRESET*	Card RESET, software (CRO) or hardware (SYSRESET*)
DTACK	Data Transfer ACKnowledge (DTACK high = DTACK* low)
DTACK INH	DTACK INHibit
AS	Buffered address strobe
SYSFAIL	Card failure signal (jumpered to GND)
SYSFAIL INH	SYSFAIL INHibit (jumpered to GND)
HRESET*	Hardware RESET (from SYSRESET*)
IRQ	Interrupt ReQuest line, User-implemented jumper to ground
LATCH*	Latches data into write registers
PIACK*	Peripheral Interrupt ACKnowledge line
CADDR	Card ADDRess match

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Power Supplies

All of the power pins on P1 (as shown in Table 2-15) are available on short stubs from the connectors. The +5 VDC and +12 VDC power supplies are fused. Users should fuse and filter any other power supplies they access to protect their mainframe.

All ground pins are connected together and are accessible in several places. No ground loops are present in the module. The front panel of the module is not grounded.

Table 2-15. Power Supply Voltages and Pin Numbers

Voltage	Connector and Pin Numbers
+5 V dc +5V stdby + 12 V dc -12 V dc	(P1) A32, B32, C32 (P1) B31 (P1) C31 (P1) A31

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Chapter 3
Using the HP E1399A

This chapter shows how to use the backplane interface circuitry on the HP E1399A Breadboard Module. This chapter includes:

- Reading Data From Registers
- Writing Data to Registers
- Using Interrupts
- Resetting the Module
- Detecting Errors
- Using Other Power Supplies

Reading Data From Registers

The breadboard module contains circuitry for two readable registers, as determined by the VXIbus Specification:

- Status Register
- Device Type Register

Status Register Bit Definitions

Table 3-1 shows the status register bit definitions. It will be used as an example of how to read from a register on the breadboard module. As shown in Table 3-1, only four of the eight bits in the register are predefined by the VXIbus Specification. The other four bits are "device dependent". That is, they can represent any condition that you define.

The inputs to the status register are provided by the user from the custom circuitry on the module. Access points (SR0-SR7) are provided on the module to tie into the status register, as shown in Figure 3-1.

You must add latches to the circuitry if you need to latch your status bits to catch a transient condition. Otherwise, you can tie into the status register line drivers directly at the access points provided.

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Table 3-1. Status Register Bit Descriptions

Data Bit(s)	Defintions
SR0 - SR1 SR2 SR3 SR4 - SR7	Device Dependent (User assignable) (0=Failed/Executing Self Test, 1=Passed Self Test) (If 0, ands Passed bit = 1, Extended Self Test Active) Device Dependent (User Assignable)

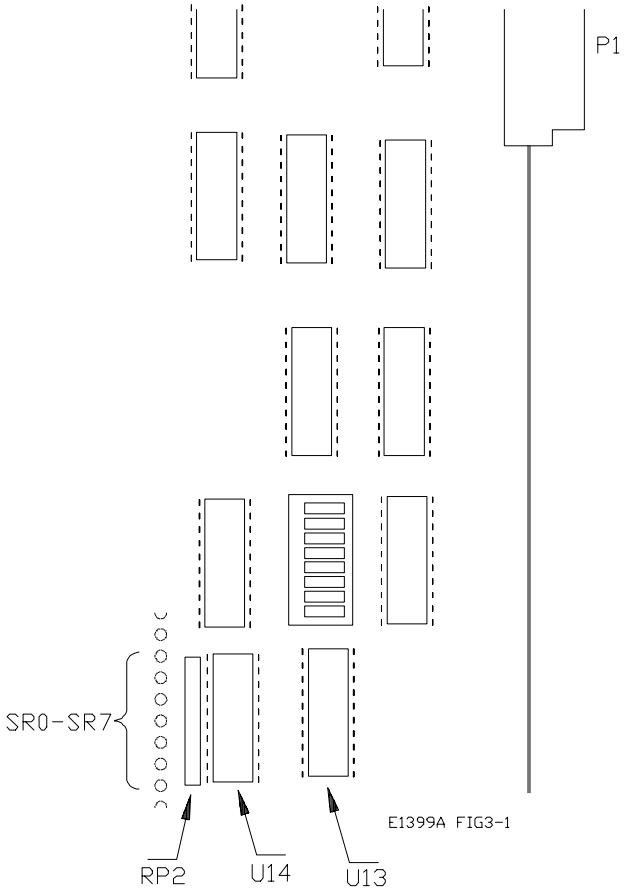


Figure 3-1. Status Register Access Points

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Reading the Status Register

For example, assume you need to use up to 8 bits of the status register. To latch your status data and then read the 8-bit contents of the status register onto the backplane, you must implement the following signal and control lines:

1. Address the module correctly by placing the data shown in Table 3-2 on the backplane address lines:

Table 3-2. Backplane Address Lines - Status Register

Line(s)	Data Required
Lines A1-A3	Must be set low/high/low (010) to select the BASE+4 enable line. BASE+4 provides one half of the enable function for line driver U7 (See Table 2-2 in Chapter 2).
Lines A4, A5	Must both be low (0) to enable 3-to-8 line decoder U8.
Lines A6-A13	Must equal the logical address of the module as set on DIP switch SP1.
Lines A14, A15	Must always be set high (1) to access the upper 16K of address space.
Lines AM0-AM5	Must be set to either hexadecimal 29 (101001) or hexadecimal 2D (10 1101). Refer to the VMEbus Specification and the VXIbus Specification (Rule C.2.10)
Line LWORD*	Must always be set high (false) since this is a D16 device. (short word transfer = 16 bits or less).

2. This is a read operation, so WRITE* must remain high (false) to provide the second half of the U14 enable function.
3. Set IACK* high (false) to enable address equality detector U18.
4. Set both data strobes DS0* and DS1* low (true) to indicate a 16-bit data transfer.

Figure 3-2 shows timing required for the Interface IC (U6) control and signal lines.

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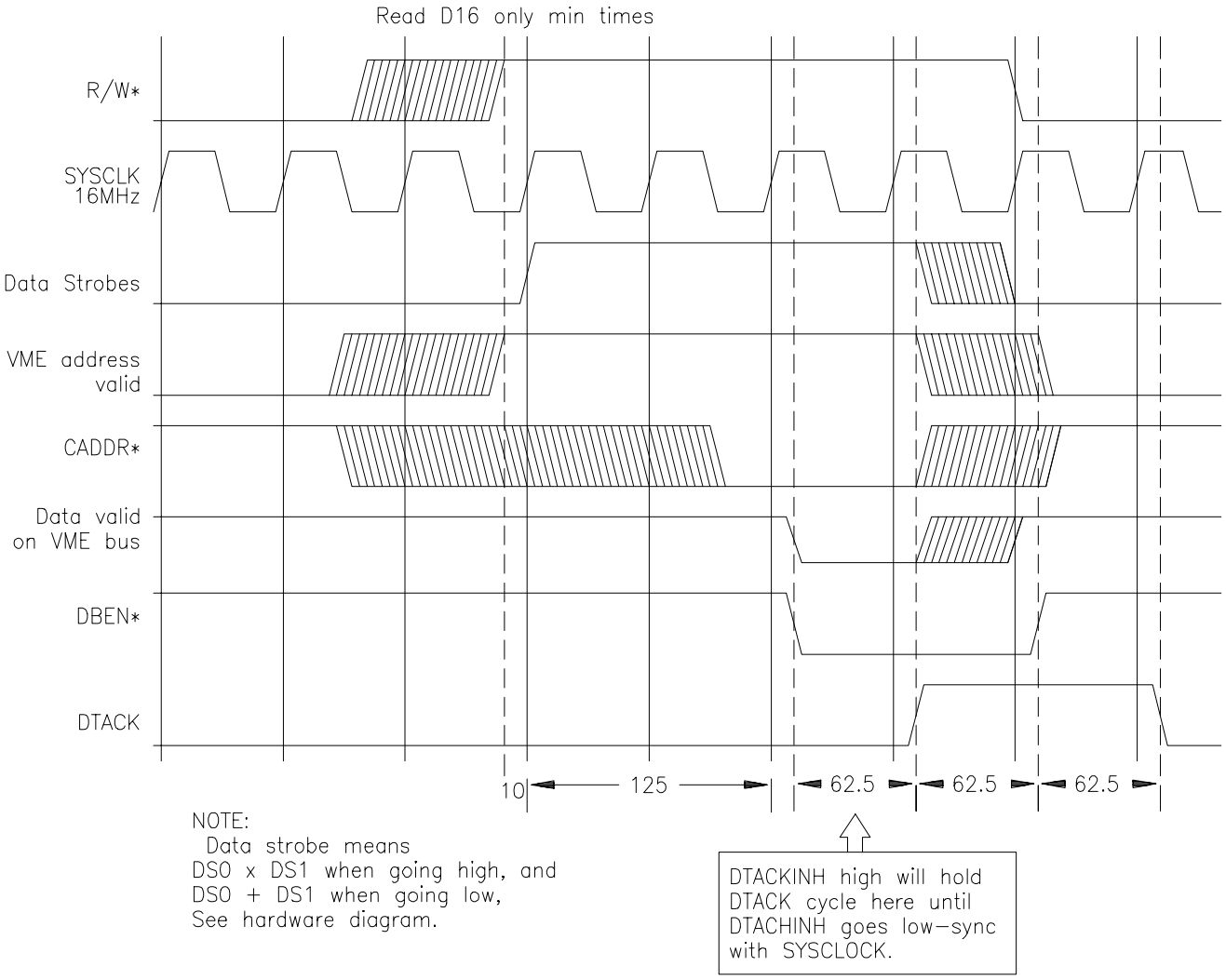


Figure 3-2. Timing for Reading the Status Register

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Writing Data to Control Register

The breadboard module contains circuitry for a control register. You can write to this register from the backplane over data lines D0-D15. The data is passed to the internal data bus DB0-DB15 and then clocked into the control register for use by the custom circuitry on the breadboard at access points CR2-CR7.

Control Register Bit Definitions

Table 3-3 shows the definitions preassigned to control register data bits per the VXIbus Specification (Section C.2.1.1.2).

Table 3-3. Control Register Bit Definitions

Data Bit(s)	Definitions
CR0	CRESET (1=Reset the module; User defines reset actions)
CR1	SYSFAIL inhibit (1=Inhibit setting of SYSFAIL* Reset, 0=Safe)
CR2 - CR14	Device Dependent (User assignable)
CR15	(1=Enable access to A24/A32 Registers; 0=Disable)

You may connect any of the control register outputs to your custom circuitry using the control register access points (CR0-CR15) shown in Figure 3-3.

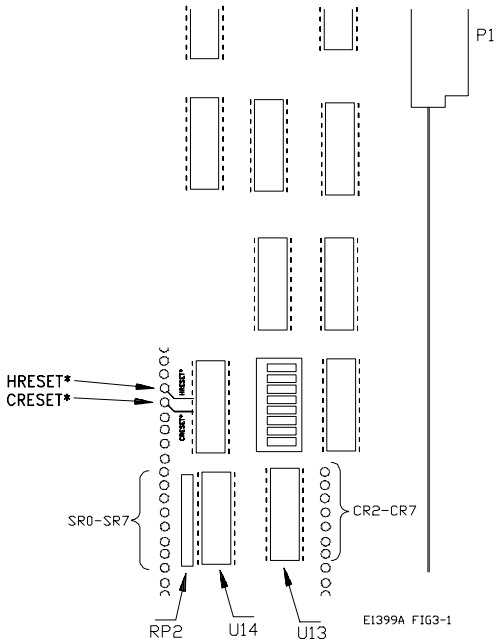


Figure 3-3. Control Register Access Points

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Writing to Control Register

To write to the control register from the backplane data lines, you must implement the following signal and control lines:

1. Address the module correctly by placing the data shown in Table 3-4 on the backplane address lines:

Table 3-4 . Backplane Address Lines - Control Register

Line(s)	Data Required
Lines A1-A3	Must be set low/high/low (010) to select the BASE+4 enable line. BASE+4 set low provides an enable function at U21C for control register drivers U13 to be clocked by the LATCH pulse (See Table 2-2).
Lines A4, A5	Must both be low (0) to enable 3-to-8 line decoder U8.
Lines A6-A13	Must equal the logical address of the module as set on DIP switch SW1.
Lines A14, A15	Must always be set high (1) to access the upper 16K of address space.
Lines AM0-AM5	Must be set to either hexadecimal 29 (10 1001) or hexadecimal 2D (10 1101). Refer to the VMEbus Specification and the VXIbus Specification (Rule C.2.10).
Line LWORD*	Must always be set high (false) since this is a 16D device (short word transfer = 16 bits or less).

2. This is a write operation, so WRITE* must go low (true) to provide the LATCH signal from the DTACK state machine in U6. LATCH is a one clock cycle negative-going pulse that is applied to the other input to U21C. With both inputs to U21C set low, the output is a positive-going pulse that clocks the control data from DB0-DB7 through U13 to access points CR0-CR15.
3. Set LACK* high (false) to enable address equality detector U18.
4. Set data strobes DS0* and DS1* low (true) to indicate a 16-bit data transfer.

Figure 3-4 shows timing required for the Interface IC (U6) control and signal lines.

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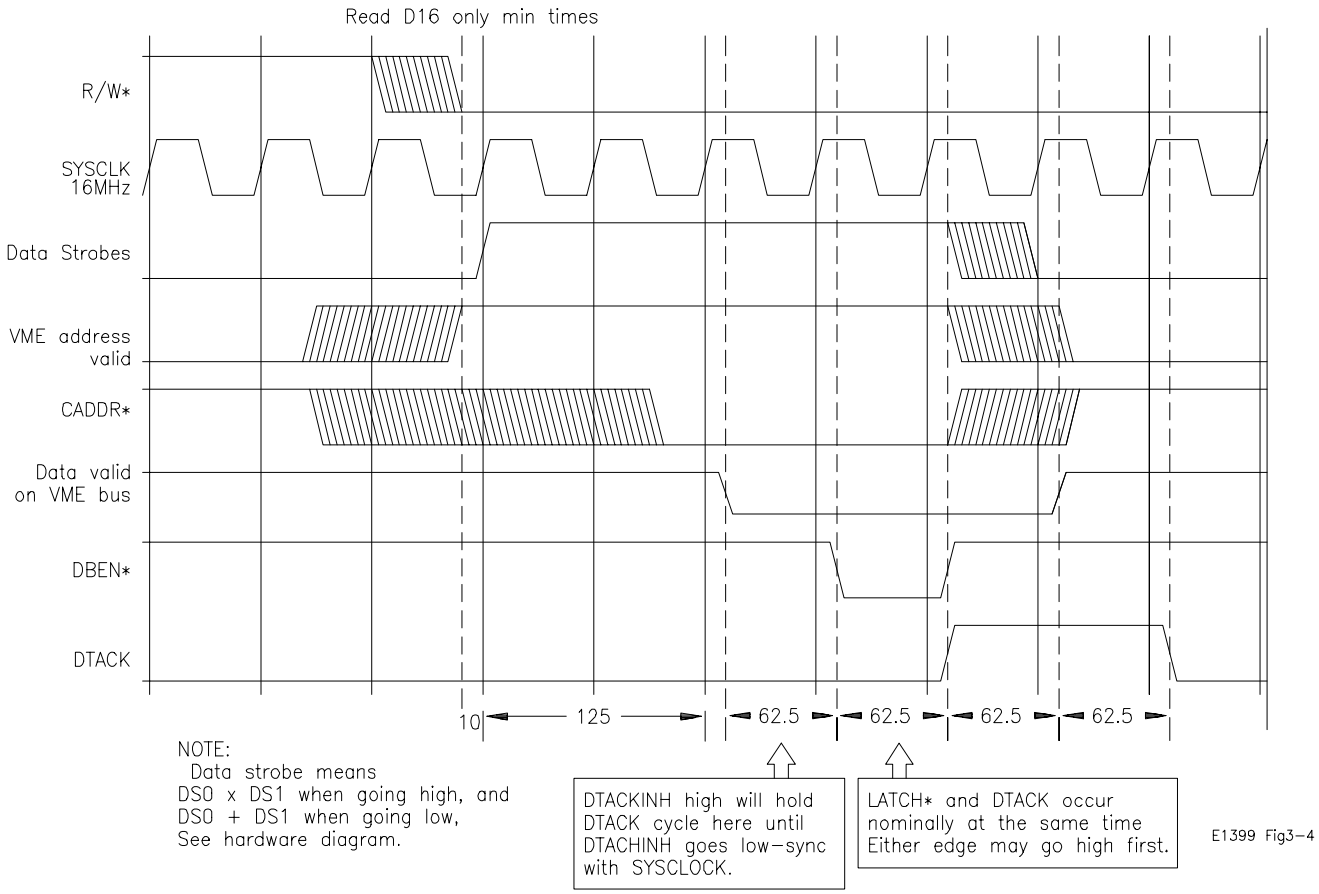


Figure 3-4. Timing for Writing to the Control Register

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Using Interrupts

The breadboard module can be configured to generate an interrupt to the interrupt handler when service is required. (If you are not going to implement the interrupt capability on your breadboard module, you must tie the IRQ user access point to ground to prevent undesired interrupts.)

Configuring for Interrupts

To configure the module to generate interrupts, you must first assign an interrupt level to the module. Levels 1-7 are available, with level 7 being the highest level. Connect a jumper in two places for the selected level, one for the IRQ REQuest line and one for the IRQ ACKnowledge line. As shown in Figure 2-12 (Chapter 2), jumpers have been installed to select interrupt level 1 (IRQ1*). Remember, both level selects must be the same.

Generating Interrupt Requests

To generate the interrupt request and accept the interrupt acknowledgment from the interrupt handler, you must implement the following actions:

1. You must provide the interrupt request from your custom circuits by setting the IRQ access point high (1) when the interrupt is to occur.
2. Monitor PIACK* after setting IRQ. After PIACK* goes low (true) and before it goes high (false), release IRQ or another interrupt will be generated.
3. If you do not implement the interrupter capability, leave the jumper between IRQ and GND intact.
4. Your system controller and/or interrupt handler must react to the signal timing in the Interface IC (U6) for the IRQ and DTACK state machines as shown in Figure 3-5.
5. The circuitry provided implements a read operation for only the lower 8 bits of status/ID during the interrupt acknowledge cycle, using PIACK* to enable buffer U11. If you want to use the upper 8 bits also, you must provide an additional buffer to the internal data bus that is enabled by PIACK* low (true) and DS1* low (true).

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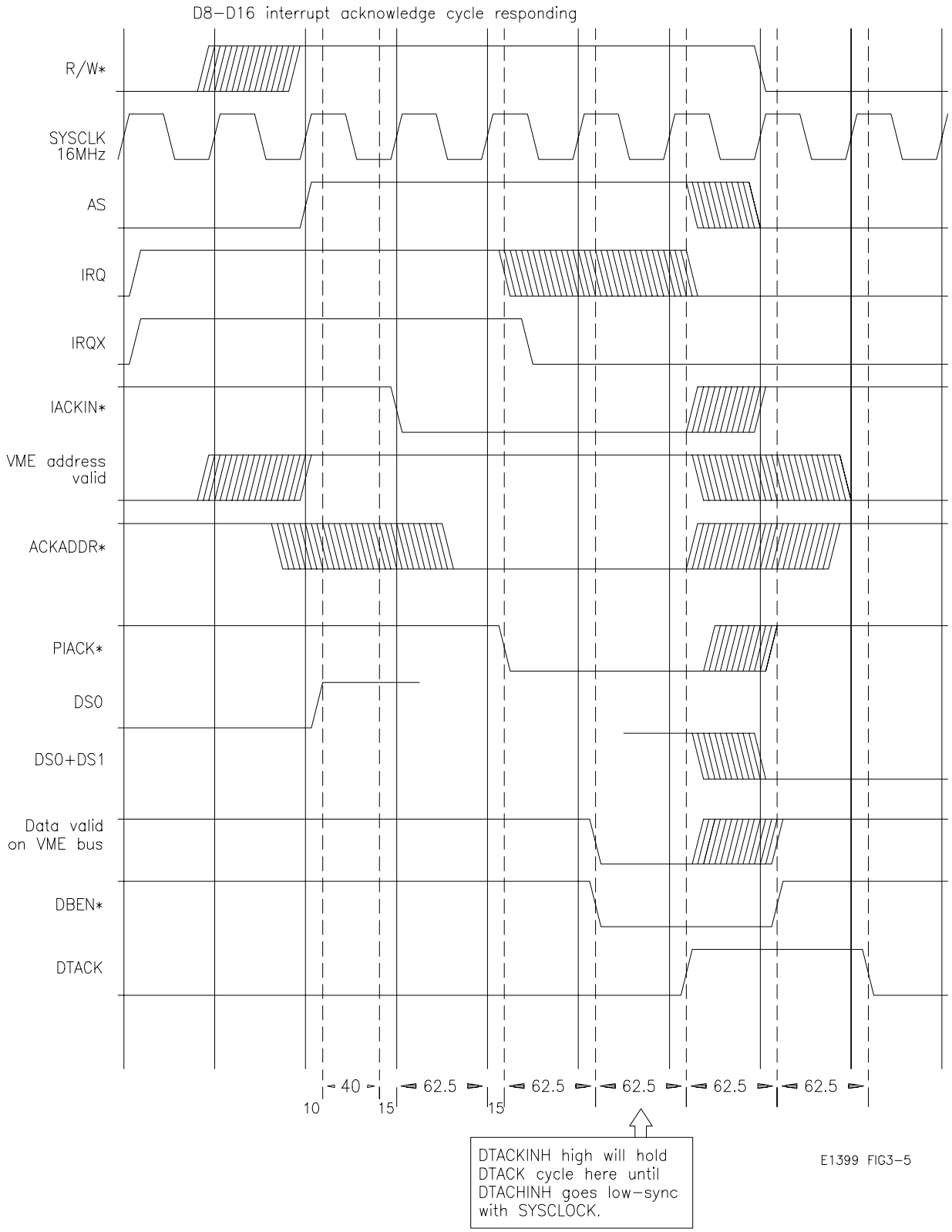


Figure 3-5. Interrupt Timing

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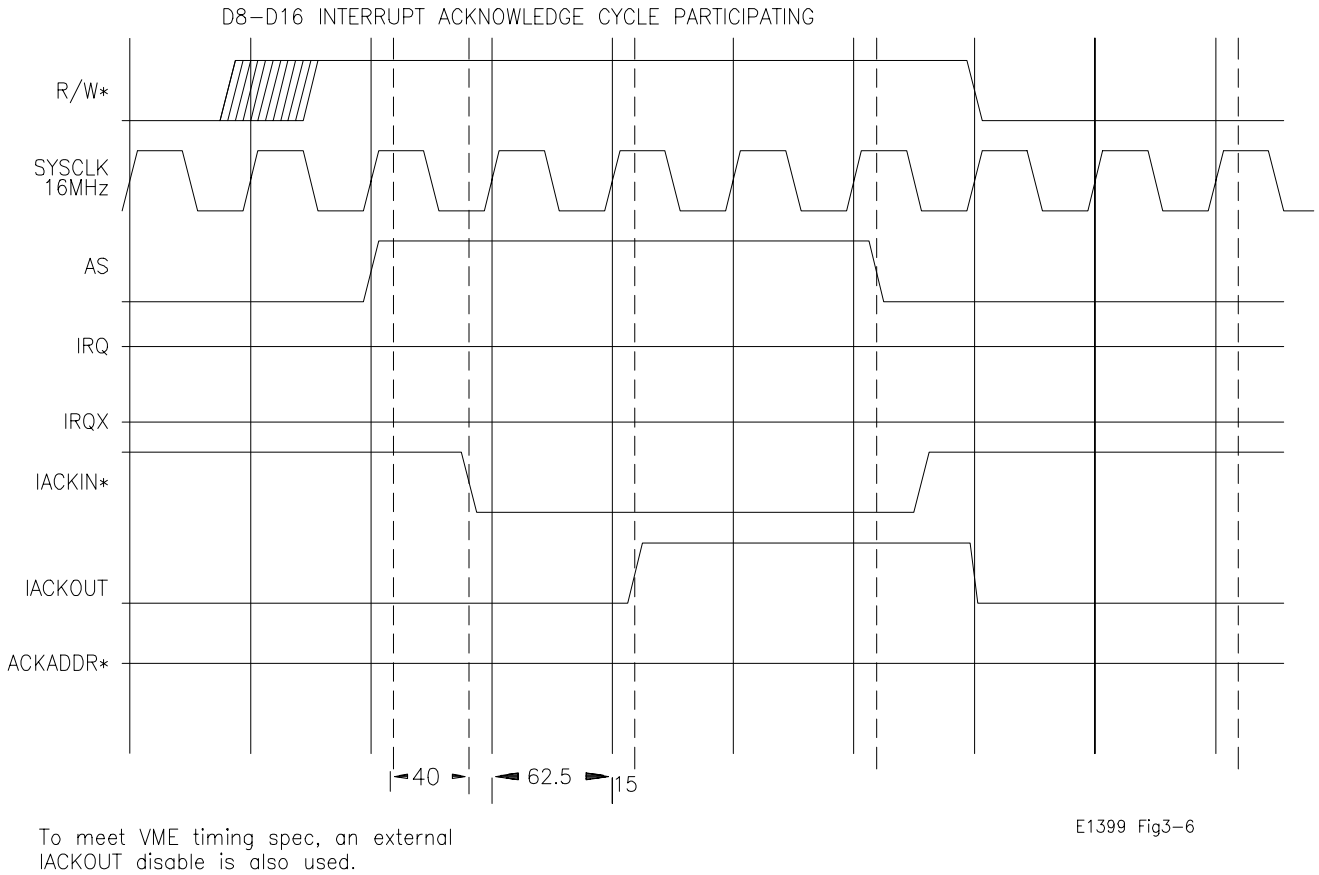


Figure 3-6. Interrupt Timing
Wrong IRQ Level or No Interrupts Pending

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Resetting the Module

A reset signal is provided to initialize the backplane interface circuit and your own custom-designed circuitry to a known state. Both hardware and software resets are implemented for your convenience.

Hardware Reset

The backplane SYSRESET* line drives both the hardware reset (HRESET*) and the software reset (CRESET*) user access points low (0) on the breadboard module. HRESET* also goes to the clear input of U13, which drives all of the control register outputs (access points CR0-CR7) low (0).

Software Reset

Control register output bit CR0 is used for the software reset. If you write a "1" to bit CR0, the CRESET* access point on the module is driven low (0) by U21D. You can use CRESET* any way you choose in your custom circuitry.

Detecting Errors

The breadboard module implements the following error/fail circuitry:

- The status register implements bit SR2 as a self-test "Passed/Failed" bit (see Table 2-4). If SR2 (PASSED access point) is set low (0), indicating your custom circuit self-test either failed or is currently still executing and the SYSFAIL INHBT bit (CR1 output of the control register) has been set low (O), then the module sets the backplane SYSFAIL* line low (true) through U21A and U5D (this is the default). If either SYSFAIL INHBT or the "PASSED" bit are set high, SYSFAIL* remains high (false).
- The ACFAIL* line has been stubbed onto the module from backplane connector P1 (pin B3) and is available as a user access point for your convenience.
- BERR* (Buss ERRor). If an invalid bus cycle is discovered, this can be asserted instead of DTACK*.

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Using Other Power Supplies

You can use any of the other power supply voltages from a standard VXIbus backplane as described in the VXIbus Specification. All of the available voltages have been stubbed onto the breadboard module as user access points. Just remember that you must provide your own fusing and filtering on board the module for each power supply you access from the backplane.

You must also provide adequate cooling for dissipation of the heat generated by the power requirements of your customs circuitry. See "Cooling Requirements" in Chapter 2 for more information on establishing cooling specifications for your module. Recommended power supply voltage applications are listed in Table 3-5.

Table 3 5. Power Supply Voltage Applications

Supply	Application
+5 VDC	Main power source for all systems. Used for supplying power to logic devices.
+ 12 VDC	General purpose power for switching power converters, analog devices, and disc drives.
-12 VDC	General purpose power for analog devices.
+5 VDC Stdby	Power to sustain memory, clocks, etc. when +5 V dc is lost. User may supply this power if necessary.

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Appendix A
HP E1399A Breadboard Specifications

Mechanical

Module Size:	B
Weight:	0.7 Kg
Connectors Used:	P1
Number of Slots Used:	1
User Component Area:	222 mm X 96 cm (8.75 in X 3.78 in)
Grid Hole Spacing:	2.54 mm X 2.54 mm (0.1 in X 0.1 in)
Grid Hole Inside Diameter:	1.17 mm (0.046 in)
Max Component Height:	12.7 mm (0.5 in) above board
Maximum Lead Length:	1.3 mm (0.05 in) below board

VXIbus Interface

Device Type:	Register Based
VXIbus Interface Capability:	Slave, Interrupter, A16, D16
Interrupt Level:	1-7, selectable

Power and Cooling

Maximum Power Dissipation:	Determined by mainframe cooling. Cannot exceed the number of watts (per module) per slot total cooling (backplane interface circuitry consumes 0.5 watts).
Power Requirements:	Voltage = +5 Vdc Peak Module Current, IPM (A) = 0.10 Dynamic Module Current, IDM (A) = 0.01
Watts per Slot:	0.5 (backplane interface circuitry only. User circuitry not included).

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Cooling per Slot:	To maintain less then 10C rise on the breadboard, about 0.08 liter/sec of airflow is required for each watt dissipated. At a power dissipation of 20W, the pressure drop across a typically populated breadboard will be 0.05 mm H_{2O}.

Environment

Humidity:	65%, 0 - 40 ºC
Operating Temperature:	0 - 55 ºC
Storage Temperature:	-40 ºC to 70 ºC
Safety EMI/RFI Safety:	ets FTZ 1046/1984, CSA 556B, IEC 348, UL 1244

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Appendix B
HP E1399A Parts List/Schematic

The parts list below shows parts which are supplied by Hewlett-Packard when you order the HP E1399A. See Chapter 2, "Configuring the E1399A" for components required by each interface functional group. See Figure B-1 for the schematic of the digital backplane interface circuitry.

To order a part listed in the tables, quote the Hewlett-Packard part number, the desired quantity, the check digit (abbreviated CD), and the description. Address the order to the nearest Hewlett-Packard Sales and Support Office (addresses are provided at the back of this manual).

Terminal Block Parts List

HP Part Number	Total Qty.	Description
E1300-84401	1	Terminal Board Case Assembly
E1300-01202	1	Strain Relief Clamp
E1300-44101	1	Clear Molded Cover
1515-2109	1	Screw, PH 10-24 by 5/8
1390-0846	2	Screw, PH M25 by 15 SL
E1399-66510	1	Terminal Breadboard Assembly
E1399-26510	1	Blank Terminal Breadboard
0361-1294	2	Rivet 0099 by 0328LG
1252-1593	1	Connector, Right Angle, 96 Pin

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Breadboard Parts List

Reference Designator	HP Part Number	Total Qty.	Description
	E1399-66201	1	Breadboard Assembly
ron	E1399-00202	1	F t Panel (blank) (formerly E1399-00201*)
	E1300-84308	1	Handle, Front Panel, HP logo (formerly E1300-04115*)
	E1300-84309	1	Handle, Front Panel, VXI logo (formerly E1300-04116*)
	0515-0444	2	Screw, PH M25 by 08 Torx
	0515-1968	2	Screw, PH M25 by 11
	3050-0082	2	Washer, Flat, Non-Metalic
	E1399-26501	1	PC Board, Blank
	0050-2183	1	Bracket, Panel Mount
	0361-1295	2	Rivet, 0099 by 0406LG
	0361-1294	2	Rivet, 0099 by 0328LG
P1	1252-1596	2	Connector, Right Angle, 96-Pin
U6	1820-6731	1	IC, Interface (PAL)
C44	0180-1746	1	Fixed Capacitor, 15 μF,10%, 20 V
C38-42	0160-4835	5	Fixed Capacitor, 0.1 μF, 10%, 50 V
C45, 46	0160-4835	2	Fixed Capacitor, 0.1 μF, 10%, 50V
F1, F2	2110-0665	2	Fuse, Subminiature, 1A, 125V
R9	0757-0417	1	Fixed Resistor, 562 Ohm, +/-1%, 1/8 W
RP1,2,25	1810-0279	3	Resistor Network, 9 by 4.7 kOhm 10-pin
RP26, 32	1810-0279	2	Resistor Network, 9 by 4.7 kOhm 10-pin
SP1,2	3101-3066	1	Switch, DIP, 8-rocker, 0.05 A, 30 V dc
U21	1820-4643	1	IC, 74HCT02N Quad 2-input NOR Gate, CMOS
U10, 14	1820-3975	7	IC, 74HC541N, Octal Line Driver, CMOS
U5	1820-4057	1	IC, 74F38N Quad 2-input NAND Buffer, TTL
U9, 20	1820-4242	2	IC, 74HCT14 Hex Schmitt-Trig Invrtr, CMOS
U13	1820-4086	4	IC, PC74HCT273N, Octal D-Type Flip Flop, CMOS
U17-U18	1820-3631	2	IC, 74HCI688N, 8-bit Magnitude Comp, CMOS
U16, 35	1820-3714	2	IC, 74ALS245A-1N, Octal Bus Xcvr, 3-state, TTL
U7, 8	1820-3079	2	IC, 74HC138N, 3-to-8-line Decoder, CMOS
U15	1820-4147	1	IC, 74HCI573, Octal D-Type Trnspnt Latch, CMOS

* indicates part used on modules with serial numbers 2934A00824 and earlier.

Backplane Interface Schematic

Figure B-1 shows the complete schematic of the digital backplane interface circuitry. See Chapter 2, "Configuring the HP E1399A" for information on individual interface groups.

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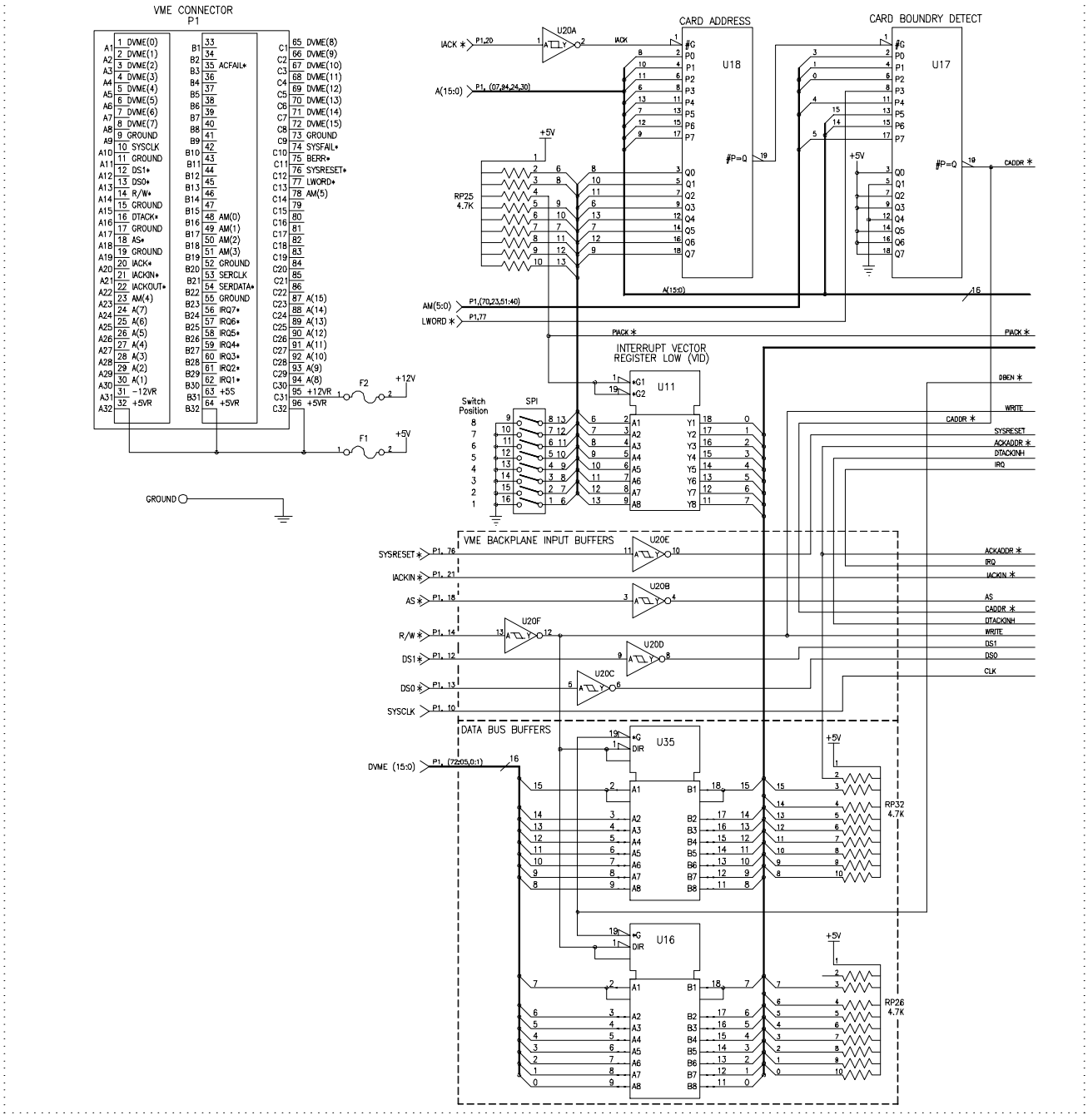


Figure B-1. HP E1399A Breadboard Schematic (1 of 2)

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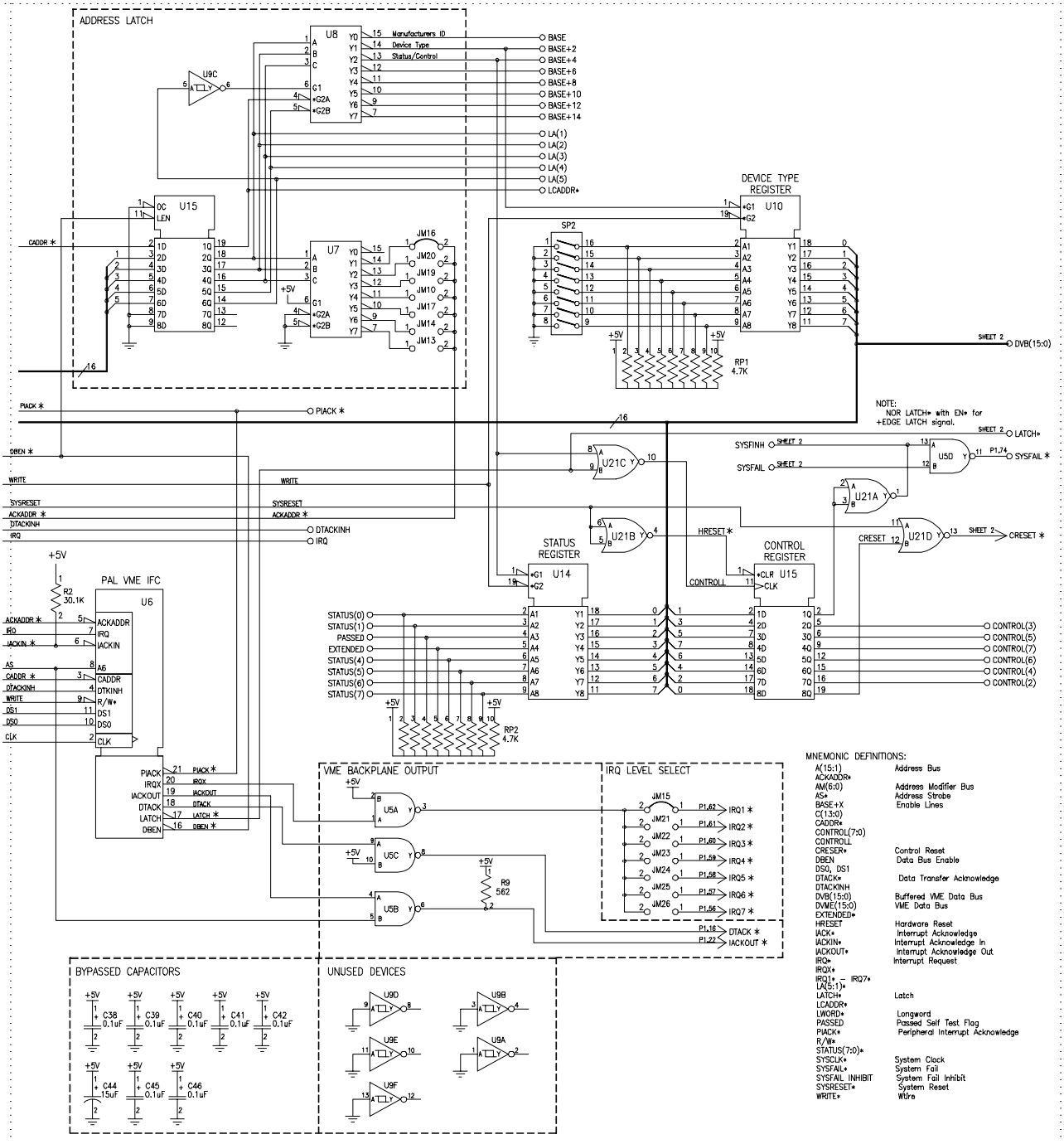


Figure B-1. HP E1399A Breadboard Schematic (2 of 3)

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