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Find the *Keysight / Agilent E1429A* at our website: ***Click HERE***

E1429A

Product Specifications

General
Number of channels: 2
Built-in DSP: No
Alias protection: Oversample
Basic accuracy: 0.5%
Low-Frequency CMRR: 68 dB
Variable bandwidth: External Filters
2 dB Input Range
headroom: No
Dual-Ported memory: No
Dual-Rate sampling: Yes

Sampling
Number of digitized bits: 12, including sign
Effective bits: 10 bits at 100 kHz; 9.5 bits at 10 MHz
(typical on 1 V range, 50 ohm input, full scale input)
Sample rates: 0.05 to 20 MSa/s in 1-2-5 sequence
Dual sample rate: switches between programmed rates upon receipt of arm

Memory
Memory length: 512 k readings per channel, battery-backed
Segmented memory: yes

Input
Input impedance: 50 or 75 ohm single-ended and 1 Mohm||20 pF differential
(both inputs on each channel, DC coupled, nominal)
Signal ranges: 50/75 ohm is 0.1 V to 1 V; 1 M ohm is 0.1 V to 100 V in 1-2-5 steps
Analog bandwidth: 50 MHz @ 1 V single-ended, 5 MHz @ 10 V differential, typical
Filtering: 10 MHz nominal, 2-pole Bessel, switchable
Signal to noise ratio: -62 dB typical

Timebase
Internal reference: 20 MHz,
50 ppm, <25 ps rms jitter typical
Reference sources: internal crystal, faceplate BNC, CLK 10, and ECLTRG
Timebase resolution: 50 ns

Arm and Trigger
(Each trigger event causes one A/D conversion in both channels ;
each Arm event allows acquisition of a burst of one or more dual-channel A/D conversions)
Programmable arm delay: 50 ns to 32 ms using internal 20 MHz reference
(derived from reference)

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Readings per arm: 1, 7 to 16,777,215, or continuous post-arm; 0 or 3 to 65,535 pre-arm
Re-arm rate: up to 2 MHz (non-segmented memory)
Arm sources: internal, faceplate BNC, input voltage level, TTLTRG, ECLTRG, and logical OR of any two signals
Trigger (sample clock) sources: internal, VME read, faceplate BNC, TTLTRG, and ECLTRG
ECLTRG functions: arm, trigger, and reference (input and output)
TTLTRG functions: trigger and arm (input) arm and ready for trigger (output)

Connectors
EXT1 faceplate BNC: arm and trigger (input) arm, trigger and reference (output)
EXT2 faceplate BNC: trigger and reference (input)

VXIbus Compliance
Data paths: VXI word serial protocol on VXI data transfer bus or VME register access (16- or 32-bit; up to 4 or 8 MB/s)
Device type: message-based servant and register-based (A24) slave; A16/A24, D8/D16, D32 (data read only)

VXI Characteristics
VXI device type:Message-based
Datatransfer bus: A24 slave; A16/A24, D8/D16, D32 data read only
Size: C
Slots: 1
Connectors: P1/P2
Shared memory: n/a
VXI busses: TTL Trigger Bus, ECL Trigger Bus
C-size compatibility: Yes

Command module
firmware: n/a
Command module
firmware rev: n/a
I-SCPI Win 3.1: n/a
I-SCPI Series 700: n/a
C-SCPI LynxOS: n/a
C-SCPI Series 700: n/a
HP VEE Drivers: Yes
VXI*plug&play* Win
Framework: Yes
VXI*plug&play* Win95/NT
Framework: Yes
VXI*plug&play* HP-UX
Framework: No (not available attimeofpublication)

Module Current
I_{PM} I_{DM}
+5 V: 2.9 0.5
+12 V: 0.2 0.04
-12 V: 0.2 0.04
+24 V: 0.1 0.05
-24 V: 0.1 0.05
-5.2 V: 3.6 0.05
-2 V: 1.2 0.12

Cooling/Slot
Watt/slot: 41.50

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deltaP mm H_2O: 0.80
Air flow liter/s: 3.80

Backplane Connector Shielding
To ensure compliance with RFI levels specified in standards EN55001 and CISPR11, this product requires the Backplane Connector Shields installed in a VXI C-size mainframe. Option 918 is available with the purchase of a new mainframe; accessories, E1400-80920 and E1421-80920, are available for retrofitting existing mainframes E1401A/B and E1421B, respectively (one accessory per mainframe required).



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