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## Agilent E1430A

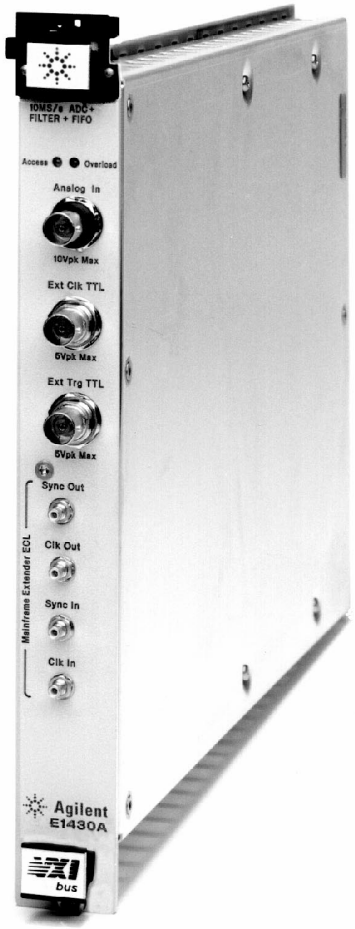
# 10-Megasample-per-Second Analog-to-Digital Converter with Filter and Memory

Product Note

In addition to analog-to-digital conversion, the Agilent E1430A addresses the problems of gain ranging, anti-aliasing protection, frequency band selection, triggering, data buffering, and multichannel synchronization.

**Agilent E1430A analog-to-digital converter module.**

The E1430A is implemented as a single-slot, C-size VXIbus module. The primary analog connections are the three BNC connectors on the front panel, which are for the analog input signal, an external clock, and an external trigger. The four SMB connectors on the front panel provide the capability of sending synchronizing signals from one VXIbus mainframe to another mainframe containing additional E1430A modules.



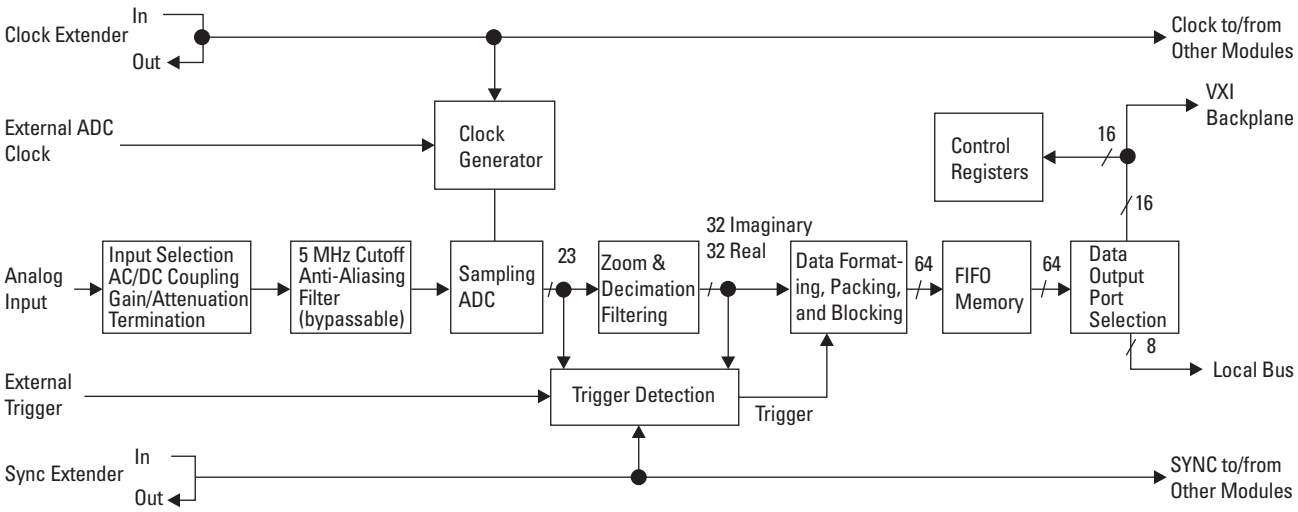

The Agilent E1430A is a VXIbus-based analog-to-digital converter (ADC) module containing a high-dynamic-range, 23-bit-resolution, 10 MSa/s (megasample-per-second) ADC, a family of octave-spaced anti-aliasing filters, a complex frequency shifter, and a 8 Mbyte FIFO buffer memory. It is designed to provide maximum performance and flexibility for capturing a bandlimited continuous analog signal in a format compatible with digital computers.

According to Nyquist's sampling theorem, any signal confined to a finite frequency bandwidth can be completely represented by a sequence of discrete samples taken at a rate of at least twice the signal bandwidth. If we are interested only in a finite time segment of the analog signal, all the necessary information is contained in a finite number of these samples taken from the appropriate segment of the sequence. In the absence of additive measurement

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**Figure 1:**
**Block diagram of the Agilent E1430A ADC Module.**




noise we could theoretically represent the signal with infinite precision, although this would require infinite precision for each discrete sample. However, all analog measurements have some level of additive noise, which limits the amount of signal information available. Therefore, it is only necessary to store each sample with sufficient finite precision to retain the available signal information in the presence of the additive noise.

In other words, it is theoretically possible to completely determine a finite time segment of a bandlimited analog signal, to the extent allowed by additive measurement noise, by collecting a finite number of finite-precision samples of the signal. To maintain complete generality in capturing such a signal, the signal bandwidth, center frequency, start time, and time duration should all be independently specifiable. The E1430A offers a wide range of independent choices of all of these parameters while guaranteeing that the sample rate and data precision are sufficient to characterize the signal. The E1430A also minimizes the amount of additive measurement noise to preserve as much signal information as possible.

The E1430A is much more than an analog-to-digital converter. It also addresses the problems of gain ranging, anti-aliasing protection, frequency band selection, triggering, data buffering, and multichannel synchronization.

The rear panel contains the standard VXIbus connectors, which are used for programming and reading data from the module. The E1430A complies with the VXIbus register-based protocol. Status lights are provided to indicate when the module is being accessed via the VXIbus backplane or when the input range is exceeded, producing an overload in the ADC.

## Analog Signal Conditioning

It is common practice at audio frequencies to provide high-impedance balanced differential inputs for ADC modules. However, maintaining good frequency response to a band-width of 4 MHz requires the use of a terminated transmission line to drive the input. The E1430A implements a 50 ohm pseudofloating input as shown in Figure 2. The cable ground is isolated from chassis ground by 50 ohms in parallel with a 0.04 µF capacitor. This is sufficient impedance to break up low-frequency ground loops, maintaining the key benefit of a differential input. At high frequencies where ground loops are no longer a problem, the 0.04 µF capacitor shorts out the common-mode signal, reducing the impact



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of common-mode feedthrough at high frequencies. The resistor damps out resonances of the input cable inductance with the cable-to-chassis capacitance.

Diodes are placed between the grounds to protect against damage and to satisfy safety concerns arising from high common-mode voltages. The result is an input termination that maintains good flatness to 4 MHz, suppresses low-frequency ground loop pickup, reduces high-frequency common-mode feedthrough, and eliminates unsafe high common-mode voltages.

Opening S1 under program control causes the input signal to be ac coupled through a 0.2 µF capacitor. This makes possible the measurement of low-level ac signals in the presence of a large dc offset. Programming S2 to the grounded position provides a 0 volt reference so that the offset DAC can be programmed to eliminate any dc offset in the input amplifier.

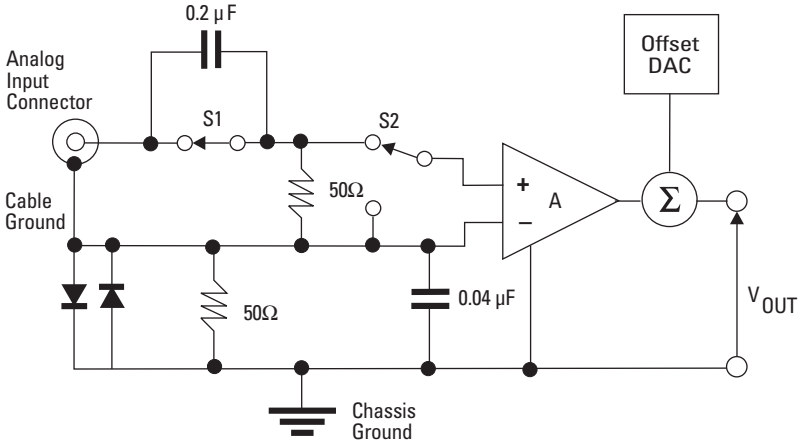
The gain or attenuation of the input amplifier is programmable in 6 dB steps so that sinusoidal input signals ranging from -32 dBm to +28 dBm can be scaled to produce a full-scale sine wave at the ADC. The noise added to the signal by the E1430A is -136 dB/Hz relative to full scale (dBfs/Hz) for the -14 dBm and higher ranges. It is -128 dBfs/Hz for the -20 dBm and lower ranges. This represents a 14 dB noise figure in the -32 dBm range. Most ADC modules have fixed, high-level input ranges requiring the user to provide low-noise external amplification.

## Anti-Aliasing Filter

Since the normal ADC sample rate is 10 MHz, a complete representation of the input signal can be achieved only for bandwidths up to 5 MHz. To eliminate the possibility of higher-frequency components causing ambiguous results as a result of aliasing, all signal components above 5 MHz need to be removed before sampling occurs.

The analog anti-aliasing filter in the E1430A is flat to 4 MHz and rejects signals above 6 MHz by at least 110 dB. Thus the 0 to 4 MHz frequency range of the sampled signal will be alias-free. The analog filter transition band from 4 MHz to 6 MHz affects the flatness and allows some aliasing in the sampled signal frequency range of 4 MHz to 5 MHz. In some applications a complete, unambiguous representation of a continuous signal may not be necessary, or the user may have additional information about the signal to allow a valid interpretation of the aliased components. In those cases anti-aliasing filtering may not be necessary, and the analog filter may be bypassed. This programmable mode allows the user to take advantage of the full 20-MHz sampler bandwidth. The anti-aliasing filter bypass mode should be used with caution and is not recommended for normal operation.

**Figure 2: Analog signal conditioning equivalent circuit.**





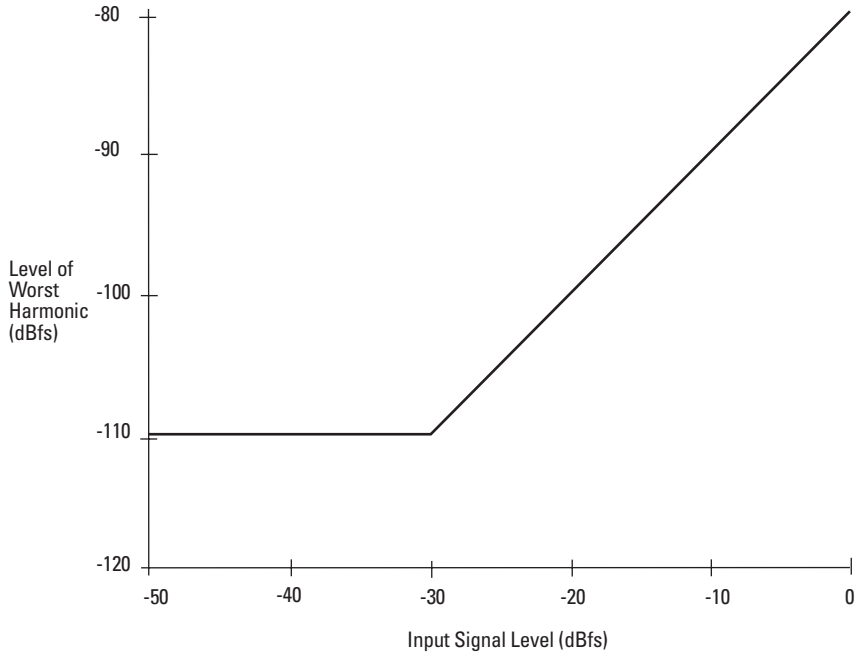

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## Sampling ADC

The heart of the E1430A is a precision ADC that generates 23-bit outputs at sample rates up to 10.24 MHz. The amplitude resolution is far in excess of the converter's analog noise. Thus, the effects of finite quantization levels can be completely ignored, leaving the main error mechanisms, which are random white noise and linearity errors. For each sample the random error has a Gaussian amplitude distribution with an rms level of -70 dB relative to a full-scale sine wave. The random error for each sample is essentially uncorrelated with previous samples, meaning that the spectral energy of the noise is uniformly distributed across the 5 MHz Nyquist band. Therefore, the noise can be expressed as -137 dBfs/Hz. With the input amplifier noise included, the overall E1430A noise level is -136 dBfs/Hz (-128 dBfs/Hz for input ranges < -20 dBm). This low noise density is comparable to the best available ADCs at any sample rate.

In many applications, random errors can be filtered, averaged, or otherwise processed to reduce their impact on the final result. In these applications the deterministic signal-related errors — that is, distortion components — may limit the resulting accuracy unless they are significantly lower than the -70 dB broadband noise level. The E1430A achieves distortion errors of -80 dBfs to -110 dBfs depending on the level and dynamics of the applied signal. The graph shown in Figure 4 shows the worst-case harmonic level for sinusoidal inputs of various levels. This distortion performance is considerably better than traditional ADCs in the 10 MSa/s class.

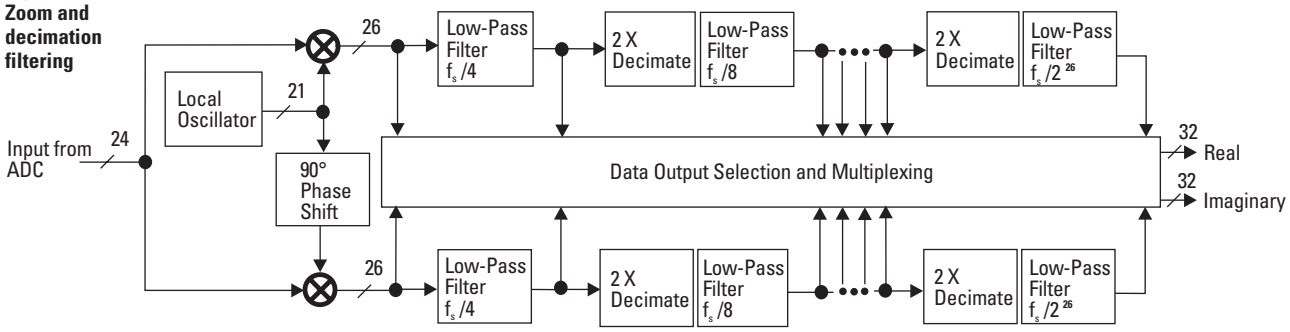
**Figure 3: Harmonic distortion as a fucntion of input level.**






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**Figure 4: Zoom and decimation filtering**




## Zoom and Decimation Filtering

For changing the signal bandwidth and center frequency, the E1430A provides a complex frequency shifter (zoom) and a complex low-pass filter. Both functions are implemented digitally with proprietary Agilent high-speed ICs to achieve real-time operation. A block diagram of the digital signal processing is shown in Figure 4.

The local oscillator generates cosine and sine waves with spurious components smaller than -110 dBc and frequency resolution better than 10 µHz. These are then multiplied by the incoming signal to produce the real and imaginary components of the down-converted complex baseband signal. The complex baseband signal is then filtered to the desired bandwidth by separately filtering the real and imaginary components.

Bandwidth choices are provided with a cascaded chain of digital low-pass filters, each of which reduces the bandwidth by a factor of two. With the ADC sample rate, $F_S$ , set to the standard internal 10 MHz rate, the available bandwidth choices are ±5 MHz, ±2.5 MHz, ..., ±0.149 Hz around the programmed LO frequency. Each of the filters has ±0.35 dB amplitude flatness to 75% of its indicated corner frequency and has >105 dB rejection for signals above 125% of its indicated corner frequency. Because of the sharp cutoff, the time-domain step response of the filters has approximately 20% overshoot. Also, since the filters are not linear-phase, the time-domain impulse response is not symmetric. In time-domain applications where overshoot and/or impulse response symmetry are important the user can apply additional signal processing to achieve the desired filter response. Although the E1430A does not include this compensation filtering, all the necessary signal information is preserved to accomplish it within a host computer or signal processing module.

Once the signal bandwidth is reduced below $\pm f_S/4$ the sample rate is also reduced by a factor of two in each filter stage. Thus, each filter output is generated with a sample rate of four times the nominal cutoff frequency. This is sufficient to avoid any aliasing within the filter passband and transition band. The user can program an additional factor-of-two sample rate reduction to get an output sample rate of only two times the nominal filter cutoff. This is still sufficient to avoid aliasing within the passband, but the transition band will not be fully alias-free. This additional decimation is useful in applications such as FFT-based spectrum analysis, where the lower sample rate is beneficial but transition band aliasing is not of concern.

The data multiplexing block can be programmed to output only samples from a particular filter or to multiplex the outputs of all of the filters beyond a selected one. In the multiplexed filter mode each output sample is tagged with a number to indicate from which filter it came. This mode is useful in the implementation of 1/N-octave analysis algorithms.

The real and imaginary components are each computed to 32-bit precision to preserve the processing gain provided in the narrowband filters. Thus, each complex output sample contains 64 bits. Whether or not all these bits are stored in memory can be programmed in the data formatting block.

## Data Formatting and FIFO Memory

The E1430A can be programmed to save only the real component of the signal or to save the complete complex signal. The data precision can be set to 16 bits or 32 bits. Thus, each



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sample occupies from two to eight bytes of memory. The data formatting block packs the selected data into 64-bit words, which are stored in the FIFO memory. Since the standard FIFO depth is 1 Mwords (8 Mbytes), it is possible to hold up to 4 Msamples in memory at one time.

The memory can be configured either in block mode or in continuous mode. In block mode, data collection initiated by a trigger proceeds until a specified block length is captured. The measurement is then paused so that the data can be read out. Before a new block can be collected, the module must be rearmed and triggered again. This mode is useful in capturing single transient events or whenever the output data rate is too high to be read and processed in real time.

In the continuous mode, data collection is initiated by a trigger and continues as long as the FIFO memory does not overflow. Data can be read out of the memory while the measurement is in progress. If the reading of data is sufficiently fast then the memory will never overflow and the measurement will continue indefinitely. If the memory should ever overflow then the measurement will stop and wait until data is read out, the measurement is rearmed, and a new trigger occurs. This mode of operation is useful for real-time applications that employ a high-speed signal processor to read and operate on each sample of data. The deep FIFO memory allows the consumer to read the data in bursts to accommodate pauses for such things as disk access times or block mode computations.

The effective trigger time can be offset from the actual trigger event by programming a trigger timing offset. The pretrigger offset is limited to the physical depth of the FIFO memory. The post-trigger offset is limited to 226 samples.

## Data Output

The output data from the FIFO memory can be directed to a VXIbus register or a high-speed local bus. The VXIbus register can be read by any controller compatible with the VMEbus standard. The memory is unpacked from the 64-bit memory and sent to the 16-bit register as four separate words. Although this mode provides compatibility with a broad range of controllers, it limits the data flow to approximately 4 Mbytes/s. The local bus mode supports data transfers over a high-speed 8-bit ECL bus to an adjacent module (to the right) in the VXIbus mainframe. The E1430A can output data over the local bus at rates up to 80 Mbytes/s. This mode requires the use of a consumer module that supports Agilent's ECL local bus protocol. The protocol accommodates multiple adjacent E1430A modules sending data to a single signal processor module such as the E1485A. In addition to the increased data rates, the local bus mode allows output data to flow concurrently with control traffic over the standard VMEbus backplane. This can simplify the design of real-time signal processing systems that require interactive control. In both of the data output modes the samples must be read out sequentially, beginning with the sample following the effective trigger. The E1430A does not support random access or memory-mapped access to the data.

## Clock and Trigger Generation

Normally the ADC clock is produced by a 10 MHz crystal oscillator inside the clock generation block. However, for applications requiring a customer-supplied sample clock, E1430A can accept an external TTL clock signal at a front-panel connector. The ADCs of multiple E1430A modules can be synchronized by programming them to use a common ECL clock line on the backplane. One of the modules can then be programmed as the clock master that drives this line. For systems involving more than one VXIbus mainframe, the backplane clock line can be extended to another mainframe by using the SMB connector on the front panel.

The trigger event used to start a measurement can be generated in four different ways: software trigger, external TTL, ADC threshold, and log magnitude. Any E1430A module can synchronously trigger multiple E1430A modules via a shared sync line on the VXIbus backplane. This line can be extended between mainframes in the same manner as the ADC clock described above. All modules in a synchronous system are triggered on exactly the same ADC sample. All triggering modes support slope selection. The ADC and log magnitude modes also allow user selection of a trigger threshold, with hysteresis to prevent noise-generated false triggers on the wrong slope. The log magnitude triggering is based on the magnitude of the complex signal after zooming and filtering. The frequency selectivity of this mode is ideally suited to capturing low-level burst communication signals in the presence of larger interfering signals.



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## Control

All control of the E1430A module is accomplished by means of twenty-four writable and eighteen readable 16-bit registers mapped into the 16-bit VXIbus address space. The operating and service manual documents the function of each of these registers in detail. The module can be programmed from any VXIbus or VMEbus controller. The registers allow direct, high-speed access to all of the functions of the module.

To assist a programmer in using the E1430A effectively, the operating and service manual also includes documentation and a distribution disk or tape for a library of functions to facilitate programming the registers. These functions provide a C-language interface for setting up single modules and synchronous groups of modules spanning multiple VXIbus mainframes. Along with the low-level control functions, the library provides setup save and recall, autorange, auto-zero, and diagnostics. Also included are filter correction coefficients and a resampling algorithm to facilitate high-resolution, time-domain sampling. Because source code is included, the functions can be modified or translated to other languages. An executable program that invokes the diagnostic functions is included so that users with a supported controller can test the E1430A without writing any code.

For users who are accustomed to a high-level ASCII control interface, the distribution disk or tape includes software that will configure an E1405B command module to respond to ASCII commands from a supported external controller. The commands conform to the SCPI (Standard Commands for Programmable Instruments) protocol. The E1405B interprets each SCPI command and performs the appropriate register read/write operations on the E1430A. A driver is provided to support the Agilent ITG (Interactive Test Generator) and Agilent VEE-Test interactive environments. Either of these environments can use this driver and SCPI commands to provide a virtual front panel on the computer screen for control of the E1430A. The ITG and VEE software environments are sold separately.

## Summary

The primary features that set the E1430A module apart from a typical ADC module are its high accuracy, high sample rate, selectable anti-aliasing filters, selectable center frequency, deep FIFO memory, analog signal conditioning, triggering, and fast data transfers. These are important considerations in modern communications receivers, radar and sonar processors, and transient capture equipment. Before digital signal processing algorithms can be applied effectively to signals, those signals must first be captured accurately in digital form. The E1430A provides all the necessary capabilities to perform this function with a high degree of flexibility.

## References

1. *VMEbus Extensions for Instrumentation System Specification*, Revision 1.3, July 14, 1989.

2. L.A. DesJardin, "VXIbus: A Standard for Test and Measurement System Architecture," *Hewlett-Packard Journal*, Vol. 43, no. 2, April 1992, pp. 6-14.



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