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6.3 Mb/s (J2) Electrical Line Interface

Agilent Technologies Broadband Series Test System

E1613A



A line interface for the E4200/E4210 Broadband Series Test System, the E1613A generates and analyzes ATM cell streams contained within a J2 framing format. The E1614A provides the same testing functionality with an optical interface.

Product Features

- Cell based implementation
- Supports J2 framing format (NTT specification)
- Operates in Terminal, Repeater and Local Loopback modes
- Provides physical layer measurements as well as error generation
- Internal traffic generator has 1 foreground channel and up to 100 background channels
- Works with Cell Protocol Processor

The Agilent Technologies E1613A 6.3 Mb/s (J2) Electrical Line Interface generates and analyses ATM cell streams contained within a J2 framing format as used by the user-network interface (UNI) of NTT's ATM Cell Relay service. It is a single-slot module that provides test capability at the physical and ATM cell layers for the Agilent E4200/E4210 Broadband Series Test System.

Note that the 6.3 Mb/s frame specified in ITU-T G.704 is not the same as the DS2 frame structure specified by ANSI T1.107 and used in North America. Line interface modules not only connect the device or system under test to your BSTS but also provide physical, convergence, and ATM cell testing capabilities. Your Broadband Series Test System, equipped with an E1613A, becomes an extremely comprehensive transmission and protocol test tool for those developing new products and services supporting NTT's ATM Cell Relay service.

Transmission test functionality includes:

- Traffic generation
- Cell error, loss & delay measurements
- Traffic capture & playback

A companion product, the E1614A 6.3 Mb/s (J2) Optical Line Interface provides similiar test capabilities over an optical fiber physical interface.

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Typical Applications

The Broadband Series Test System (BSTS) is a modular test platform for high-speed ATM transmission and protocol testing. The BSTS can perform comprehensive testing of all layers, from physical through higher services. Due to its modular nature, you can create a customized configuration that suits your specific test needs. The fully-programmable BSTS is ideal for R&D engineering, product development, quality assurance, performance, type approval, and conformance testing.

The E1613A 6.3 Mb/s J2 Electrical Line Interface can be used in conjunction with other BSTS line interfaces, dedicated test modules, and test software to perform these tests.

Key Features

Generate Normal or Abnormal Test Traffic

Create and detect erroneous test traffic on demand to test the robustness of a protocol implementation. Sophisticated protocol data unit builder, sequencing, and library functions let you easily create complex and realistic traffic. You can generate test traffic in the foreground channel, and use up to 100 background channels to simulate loading effects.

Cell Error, Loss & Delay Measurements

Bit error rate testing is done by placing PRBS patterns in cells, and looping these cells back through a system under test. The received cells are analyzed to detect PRBS errors. These errors can then be used as a trigger to capture data.

Cell delay, interarrival time, and loss measurements are easily accomplished with the BSTS. Timestamps are inserted in cells transmitted by the line interface. These cells can then be captured, and graphs for both cell delay and cell interarrival time displayed.

Sequence numbers are transmitted in AAL-1 PDUs and looped back through a system under test. The lost cells can then be detected and counted with statistics or used as a trigger to capture data.

You can generate physical and convergence layer errors and alarms. You can also capture and playback convergence layer frames.

Real-time statistics can be gathered for the physical, convergence and cell layers. Statistics can be reported as errored seconds, event counts, or as error ratios.

Traffic Capture & Playback

Traffic can be captured with a large capture memory. Complete control is available; continuously capture with memory buffer lapping, or trigger on user-defined events. Captured traffic can be played back with automatic decoding into an English-language display. Terminology from standards documents is used wherever possible.

Since high-speed networks carry considerable volumes of traffic, you can increase your test productivity by using filters and triggers to display or capture only traffic of interest. Filters let you select virtual channels or paths of interest.

Triggers can be used to capture data matching a specific pattern. For example, triggers can be used to capture cells with header errors or sequence number errors, or upon changes in convergence layer frame bytes.

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Configuration, Ordering Information & Warranty

Configuration & Use With Other BSTS Line Interfaces, Test Modules & Test Software

Line interface modules can perform physical layer testing with a minimal BSTS configuration consisting of a line interface module and chassis. A complete range of test software applications and dedicated test modules is available to perform upper layer testing.

The E4209 Cell Protocol Processor provides monitoring and simulation test functions at the ATM and adaptation layers by executing optional protocol testing software applications. The CPP performs many functions in hardware that are usually done in software -- such as an automatic segmentation and reassembly engine for sophisticated real-time ATM, AAL and other higher layer protocol testing.

The E4219 ATM Network Impairment Emulator module lets you find the limits of performance by inserting impairments into an ATM cell stream. Route in your test cells, set cell delay and loss values to emulate a real-world network, connect the impaired cell stream output to your system under test, and see what happens.

Your local Agilent Technologies field engineer will help you select the best test system configuration to meet your needs. Since the Broadband Series Test System is a flexible and modular ATM/B-ISDN test platform, you can maximize the return on your test equipment investment by selecting a chassis, line interfaces, dedicated hardware modules, and test software that suits your specific needs. Remember that you can always add extra software or modules at any time.

Warranty & Support Options

All BSTS hardware components are warranted for a period of 3 years. Products must be returned to an authorized Agilent service center for service. At the time of purchase you may select warranty option W01, a no-charge option which converts the standard 3-year return to Agilent warranty to a 1-year on-site warranty.

Support option UK6, available at time of purchase, is a standards-compliant calibration which ensures that your BSTS test system operates within specified tolerances. A certificate of calibration is issued for compliance with ISO 9000 standards which require that records documenting the calibration of measuring and test equipment are maintained. Certificates of calibration are not available for products which do not contain components requiring calibration (such as software).

Two other types of calibration, commercial and standards-complaint, are available at any time from your local Agilent service center. Both provide test data and a certificate for your records. With a commercial calibration, any problems are resolved as they are detected, and test data reflecting performance of your calibrated test system is provided. The standards-compliant calibration provides comprehensive before and after test data to document problem resolution.

If you should have an out-of-warranty test system, you can arrange for service simply by contacting your local Agilent sales office.

Product Numbers

- **E1613A** 6.3 Mb/s (J2) Electrical Line Interface
- **E1614A** 6.3 Mb/s (J2) Optical Line Interface
- **E4200B** BSTS Form-7 Transportable Chassis
- **E4210B** BSTS Form-13 Mainframe Chassis
- **E4209B** Cell Protocol Processor
- **E4219B** ATM Network Impairment Emulator

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Technical Specifications

Traffic Generation

Modes

Three Tx/Rx modes are available. In Terminal mode, full signal generation and analysis functions are available. In Repeater mode, the received signal is re-transmitted (physical layer loopback). In Local Loopback mode, the transmit signal is electrically looped to the receiver.

ATM Cell Generation

The transmitted cell stream can contain ATM cells generated internally by the E1613A, and ATM cells generated by an optional E4209 Cell Protocol Processor module. ATM cells generated on-board can consist of one foreground channel to stimulate the channel under test, and up to one hundred background channels for loading purposes. Fill cells are used to occupy unused bandwidth.

Total Bandwidth	6.144 Mb/s
Modes	User-Network Interface (UNI) or Network-Node Interface (NNI)
HEC	Automatic generation
Fill Cells	Idle or unassigned
Channel Priority Order	OAM Fault-Management cells, Foreground, Background, CPP (highest to lowest priority)
Channel Control	VCI VPI GFC Payload Type Cell Loss Priority
SAR-PDU Support	AAL-0 AAL-1

Foreground Channel

Bandwidth	100 b/s to 6.144 Mb/s
Accuracy	+/- 0.02 ppm
Distribution	Off Single burst Periodic (according to the specified bandwidth)
Channel Depth	1500 cells (variable)
Cell Payload	Timestamp Single cell PRBS Cross cell PRBS Data pattern User Value

Background Channels

Number of Channels	Up to 100
Bandwidth	3 kb/s to 6.144 Mb/s
Accuracy	+/- 10 ppm
Distribution	Off or Periodic
Channel Density	Bandwidth and cell distribution for each background channel is individually assignable up to maximum bandwidth
Channel Depth	16 cells
Cell Payload	Single cell PRBS Data pattern User Value

Cell Payloads

Payloads	Timestamp (32-bit departure timestamp value with 100 nanosecond resolution) Cross cell PRBS-9 PRBS-15 (inverted and not inverted) PRBS-23 Single cell PRBS-9 Data pattern or User Value
Data Patterns	User Edit AA55h or FF00h Incrementing (value of each successive byte is incremented by 1)
Byte Access	Payload of all cells in the selected channel can be edited by the user in an active channel environment, or off-line as a sequence of PDUs AAL-1 automatically inserts first payload byte containing SN/SNP values and CSI bit

ATM Erroring Control

Error conditions can be introduced to simulate alarm signals and signal stressing. Error stressing is used to generate incorrect bytes in a test signal.

Error Stressing Control	Off On Pulse On (error condition is normally off; pulses on) Pulse off (normally on; pulses off) Sequence On (normally off; alternates on/off/on) Sequence Off (normally on; alternates off/on/off)
ATM Error Injection	Cell header or payload bytes with bit error masking
Cell Loss	Sequence Number in the SAR-PDU is is skipped and a fill cell is inserted
PRBS Error Add	Single bit error add to the PRBS pattern in the cell payload
OAM Fault Management	VP/VC-AIS and FERF cells transmitted at a rate of one per 0.2 to 10 seconds continuously or in bursts of 1 to 63 F4 or F5 level Segment and end-to-end OAM flows are supported Payload octets 2 to 46 can be edited Bit error masking on payload octets 2 to 48

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G.704 Frame Stressing

Alarm Generation	AIS RAI
Error Injection	FAS CRC-5
Overhead Stressing	a-bit (0 or 1) x-bits (individually 0 or 1)

ATM & G.704 Frame Measurements

Measurements are sampled every 100 milliseconds and accumulated over the user-specified measurement period. Results from the most recent complete measurement period are retained.

Measurement Period	Range 1 second to 3 days in resolutions of 1 second
Result Types	Cumulative or latched (based on most recent measurement period)
Result Formats	Count Ratio Seconds
ATM Cell Measurements	HEC errors Corrected headers Cell count Cell bandwidth Select Cell Not Received (SCNR) alarm seconds
Cell Delay Measurements	Cell delay Inter-arrival time Cell delay variation
Virtual Channel Errors	AAL-1 SN/SNP errors Cells Lost PRBS errors PRBS sync loss errored seconds
OAM Cell Measurements	OAM cell count VP-AIS errored seconds VP-FERF errored seconds VP-AIS errored seconds VC-FERF errored seconds CRC-10 errors
G.704 Measurements	Coding violation errors CRC-5 errors FAS errors Loss of signal errored seconds Loss of frame errored seconds AIS errored seconds RAI errored seconds Frame count

Traffic Capture & Playback

ATM Capture

Provides capture of 1500 cells from the selected ATM cell stream. Capture is manual or event triggered. Manual triggering captures 1500 cells after the trigger. Event triggering captures 749 cells pre-trigger, 1 trigger cell, and 750 cells post-trigger.

Manual	Triggered on user request
ATM Cell Triggers	Cell loss Header error PRBS Pattern Error Sequence Number Error

Frame Capture

Provides capture of 2048 G.704 frame payloads (octets 1-98).

Trigger	Manually-triggered

Front Panel Connectors & Indicators

J2 Input	BNC connector 75 ohm inpedance 6.312 Mb/s B8ZS code
J2 Output	BNC connector 2.3 V into 75 ohm load 75 ohm impedance 6.312 Mb/s B8ZS code
External Clock Input	BNC connector TTL input Nominal 50 ohm impedance 6.312 Mhz +/- 40 ppm frequency
Trigger Output	BNC connector TTL output Nominal 50 ohm impedance
LED Indicators	Failed Error Access Gating Signal LOF AIS RAI LOCS SCNR Reference Clock

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Size, Weight & Power Dissipation

Size	1 slot C-size VXI card
Weight	1.3 kg (2.9 lb) nominal
Power Dissipation	20 Watts (max)

Applicable Standards

ATM Cells	ITU-T Recommendation I.361 1995 B-ISDN ATM layer specification Telcordia TA-NWT-001113 1993 Asynchronous Transfer Mode and ATM Adaptation Layer (AAL) Protocols Generic Requirements
SONET/SDH	SDH as per ITU-T G.708 and I.361 for BSTS software releases prior to version A.10; SDH as per ITU-T G.707 (draft) COM 15-163-E, July 1995 Draft revised ITU-T recommendation G.707 network node interface for the synchronous digital hierarchy (SDH) for software releases A.10 and later SONET as per Telcordia TA-NWT- 000253 for BSTS software releases prior to version A.10; SONET as specified by Telcordia GR-253-CORE Synchronous Optical Network (SONET) Transport Systems: Common Generic Criteria for software releases A.10 and later
PRBS Patterns	PRBS-9 as per ITU-T O.153 1992 PRBS-23 as per ITU-T O.151 1992
EMC	CISPR11, Class A

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Agilent Technologies Broadband Series Test System

The Agilent Technologies BSTS is the industry-standard ATM/BISDN test system for R&D engineering, product development, field trials and QA testing. The latest leading edge, innovative solutions help you lead the fast-packet revolution and reshape tomorrow's networks. It offers a wide range of applications:

- ATM traffic management and signalling
- Packet over SONET/SDH (POS)
- switch/router interworking and performance
- third generation wireless tesing
- complete, automated conformance testing

The BSTS is modular to grow with your testing needs. Because we build all BSTS products without shortcuts according to full specifications, you'll catch problems other test equipment may not detect.

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Specifications subject to change.

Rev B, February 27, 2001.
5965-6753E

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