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According to ISO/IEC Guide 22 and EN 45014

The Hewlett-Packard Company declares that the HP E2074/5A conforms to the following Product Specifications.

Safety: IEC 1010-1 (1990) Incl. Amend 1 (1992)/EN61010 (1993)
CSA C22.2 #1010.1 (1992)
UL 1244

EMC: CISPR 11:1990/EN 55011 (1991): Group1 Class A
IEC 801-2:1991/EN 50082-1 (1992): 4kVCD, 8kVAD
IEC 801-3:1984/EN 50082-1 (1992): 3 V/m
IEC 801-4:1988/EN 50082-1 (1992): 1kV Power Line

Supplementary Information: The product herewith complies with the requirements of the low voltage Directive 73/23/EEC and the EMC Directive 89/336/EEX.



Q.A. Manager,
Hewlett-Packard Company

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Printing History

This is the third edition of the *HP E2074/5 GPIO Interface Installation Guide.*

September 1994 — First Edition

September 1995 — Second Edition

May 1996 — Third Edition

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General Information

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General Information

This guide explains how to install the HP E2074/5 GPIO (General Purpose Input Output) interface in either an HP Series 700 HP-UX workstation, or a Microsoft® Windows 95™ or Windows NT® PC.

In contrast to the HP 98622 GPIO interface, the HP E2074/5 is configured mainly within the software, rather than by setting switches on the GPIO hardware interface itself. To set the configuration values for the HP E2074/5 within the software, you will either run a software configuration utility, or edit a software configuration file. Therefore, this guide provides a detailed description of the HP E2074/5's functionality for software configuration purposes. You will need this information to set the values you want for the HP E2074/5 via the configuration method required for your particular software.

NOTE

This guide does *not* explain how to configure the HP E2074/5 via the software configuration methods. Please refer to "Related Software Documentation" at the end of this chapter. It explains what software manuals you should follow to configure the HP E2074/5 with the particular software (HP Standard Instrument Control Library or HP BASIC/UX 700) that you will use for I/O applications.

This guide contains three chapters. This first chapter provides an overview of the HP E2074/5 GPIO interface. In addition:

- Chapter 2 - Installation explains how to install the HP E2074/5 in either a Series 700 HP-UX workstation, or a Windows 95 or Windows NT PC.
- Chapter 3 - Configuration Information provides detailed functional information about the HP E2074/5 so you can set the proper configuration values for it via the software configuration method required for your software.

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Overview of the HP E2074/5 GPIO Interface

GPIO is a parallel interface that is flexible and allows a variety of custom connections. The HP E2074/5 GPIO interface works either in Series 700 workstations that run the HP-UX version 9.x or 10.x operating system, or in PCs that run Microsoft Windows 95 or Windows NT. A workstation or PC must also have an EISA/ISA expansion slot to accommodate the GPIO interface card.

The HP E2074/5 provides for 16-bit data exchange with peripheral devices that do not support more common interface protocols like HP-IB or RS-232. Connection flexibility is augmented in the HP E2074/5 GPIO interface by extra status and control lines, a choice of handshake methods, several data-latching options, and selectable data width and polarity.

There are two basic modes for the data ports in the HP E2074/5 GPIO interface. The HP E2074/5 can be configured like an HP 98622 GPIO interface, which is called *Compatibility Mode*. Alternately, the HP E2074/5 can be configured with a bi-directional data port and auxiliary control lines, which is called *Enhanced Mode*. Each of these modes is described in Chapter 3 of this guide.

Environmental Specifications for the HP E2074/5 GPIO Interface

Specification	Minimum	Maximum
Power Supply Voltage	+4.75 volts	+5.25 volts
Power Supply Current	2.0 amperes typical	
Operating Temperature	0° C	+55° C
Non-Operating Temperature	-40° C	+70° C
Operating Humidity		80% RH
Non-Operating Humidity		95% RH/24 hours

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Radio and Television Interference

This device has been verified to comply with FCC Rules Part 15. Operation is subject to these two conditions: (1) this device may not cause radio interference, and (2) this device must accept any interference received (including interference that may cause undesired operation).

This equipment generates and uses radio frequency energy. If not installed and used in accordance with this manual, it can cause interference to radio and television communications. The rules with which it must comply afford reasonable protection against such interference when it is used in most locations. However, there can be no guarantee that such interference will not occur in a particular installation. If you think your workstation is causing interference, turn off the system. If the radio or television reception does not improve, your workstation is probably not causing the interference. If your workstation does cause interference to radio and television reception, you are encouraged to try to correct the interference by one or more of the following measures:

- Relocate the radio or TV antenna.
- Move the workstation away from the radio or television.
- Plug the workstation into a different electrical outlet, so that the workstation and the radio or television are on separate electrical circuits.
- Make sure you use only shielded cables to connect peripherals to your workstation.
- Consult your dealer, Hewlett-Packard, or an experienced radio/television technician for other suggestions.
- Order the FCC booklet *How to Identify and Resolve Radio-TV Interference Problems* from the U.S. Government Printing Office, Washington, D.C. 20402. The stock number of this booklet is 004-000-00345-4.

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Related Software Documentation

HP Standard Instrument Control Library for HP-UX

To configure the HP E2074 GPIO interface for the HP Standard Instrument Control Library (HP SICL) for HP-UX, see the "Installing and Configuring the HP I/O Libraries" chapter of the *HP I/O Libraries Installation and Configuration Guide for HP-UX*.

To develop HP SICL I/O applications for the HP E2074 on HP-UX, see the "Using GPIO with HP SICL" chapter of the *HP SICL User's Guide for HP-UX*. HP SICL functions, including those that are GPIO-specific, are fully defined in the *HP SICL Reference Manual*.

HP Standard Instrument Control Library for Windows

To configure the HP E2075 GPIO interface for the HP Standard Instrument Control Library (HP SICL) for Windows, see the "Installing and Configuring the HP I/O Libraries" chapter of the *HP I/O Libraries Installation and Configuration Guide for Windows*.

To develop HP SICL I/O applications for the HP E2075 on Windows, see the "Using GPIO with HP SICL" chapter of the *HP SICL User's Guide for Windows*. HP SICL functions, including those that are GPIO-specific, are fully defined in the *HP SICL Reference Manual*.

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HP BASIC/UX 700 Version 8.x

HP BASIC/UX 700 version 8.x runs on the HP-UX version 10.x operating system. To configure the HP E2074 GPIO interface for HP BASIC/UX version 8.x, see the "Installing and Configuring SICL for BASIC/UX 8.x" chapter of the *Installing and Using HP BASIC/UX 8.x* manual.

To develop HP BASIC/UX 8.x I/O applications for the HP E2074, see "The GPIO Interface" chapter of the *HP BASIC Interface Reference* manual.

HP BASIC/UX 700 Version 7.x

HP BASIC/UX 700 version 7.x runs on the HP-UX version 9.x operating system. To configure the HP E2074 GPIO interface for HP BASIC/UX version 7.x, see the "Configuring HP SICL for Series 700" chapter of the *Installing and Maintaining HP BASIC/UX* manual.

To develop HP BASIC/UX 7.x I/O applications for the HP E2074, see "The GPIO Interface" chapter of the *HP BASIC Interface Reference* manual.

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2

Installation

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Installation

This chapter explains how to install the HP E2074/5 GPIO interface either in an HP Series 700 HP-UX workstation, or in a Microsoft Windows 95 or Windows NT PC. To complete the installation, you will:

1. Unpack the GPIO interface.
2. Set the DIP switch on the interface for the I/O base address.
3. Install the GPIO interface in the workstation or PC.
4. Prepare and install the GPIO interface cable.

The following sections explain how to complete these installation steps.

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Unpacking the Interface

CAUTION

Observe the following precautions to reduce the risk of damaging the interface.

- Protect the interface from static electricity. The interface can be damaged by static electricity.

  For protection, the interface is packed in an antistatic bag. Leave the interface in its antistatic bag until you are ready to install it. Save the antistatic bag so you can protect the interface if you have to remove it from the workstation or PC.

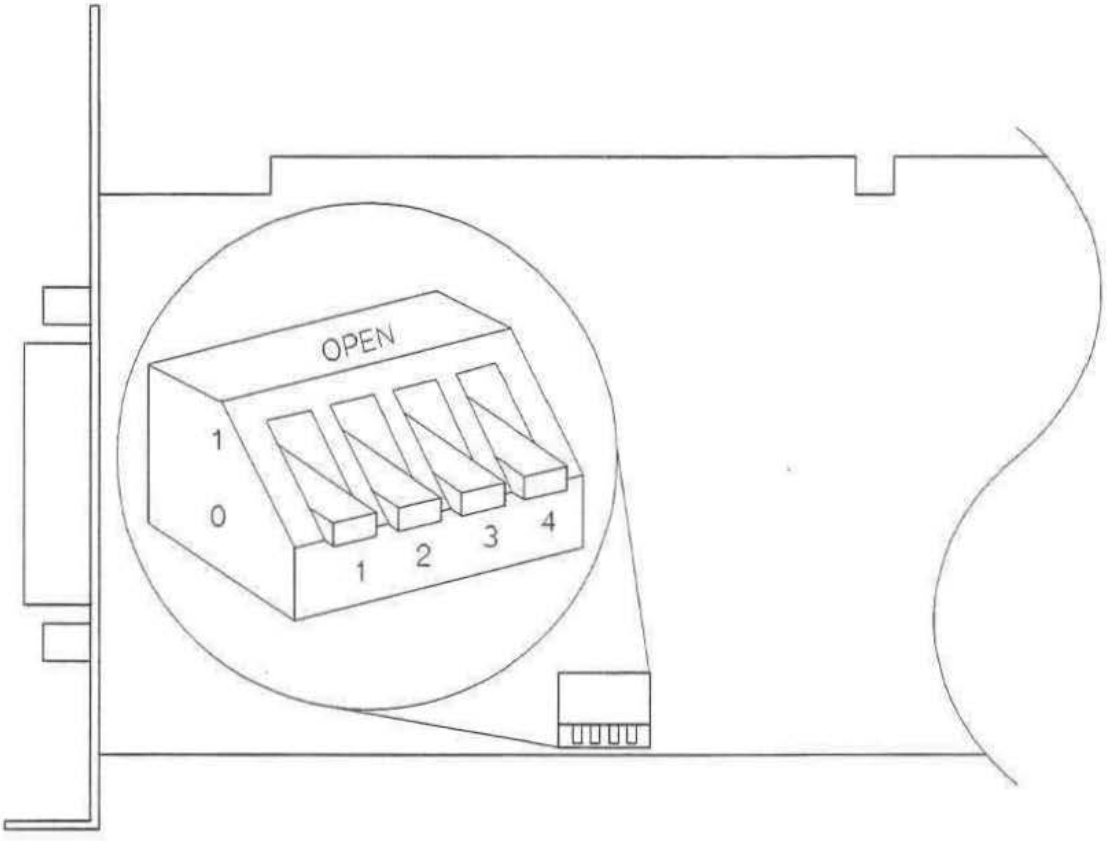
- Handle the interface gently. Do not drop the interface or handle it roughly. Be careful while unpacking and installing the interface.

- Hold the interface only by its edges. Never touch any other part of the interface. In particular, do not put fingerprints on the connector. Fingerprints can cause a bad connection when the interface is plugged into the workstation or PC.

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Setting the DIP Switch for the I/O Base Address

The DIP switch on the HP E2074/5 GPIO interface sets the I/O base address of the interface. As shown in the following figure, the DIP switch is set at the factory with the default, hexadecimal I/O base address of 228. Switches 1, 2, and 3 determine the I/O base address of the GPIO interface. Switch 4 is not used.



If you are installing additional GPIO interfaces, you need to change the switch settings. Use the following table for switch positions to set unique address ranges for each interface.

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NOTE

The chosen I/O address ranges must not conflict with other I/O interfaces installed in your workstation or PC, including other manufacturers' products. Refer to the documentation for the other interfaces and the table below to select unique addresses for all interfaces in your workstation or PC.

HP E2074/5 DIP Switch Settings

Switches 1 2 3 4*	I/O Base Address (Hexadecimal)	I/O Address Range Used (Hexadecimal)
0 0 0 0	228	228-22F, 628-62F
1 0 0 0	238	238-23F, 638-63F
0 1 0 0	258	258-25F, 658-65F
1 1 0 0	288	288-28F, 688-68F
0 0 1 0	328	328-32F, 728-72F
1 0 1 0	348	348-34F, 748-74F
0 1 1 0	388	388-38F, 788-78F
1 1 1 0	398	398-39F, 798-79F

* A 0 (zero) indicates a closed switch.

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Installing the Interface

Follow these steps to install the GPIO interface in your workstation or PC:

1. *Before turning the power off,* shut down your workstation or PC as described in the documentation provided with your workstation or PC.
2. Power down the workstation or PC, as well as all connected peripheral devices. Disconnect the power cord from the workstation or PC.
3. Expose the EISA/ISA expansion slots in your workstation or PC by removing the cover plate as described in your workstation or PC documentation.
4. Insert the GPIO interface edge connector into the expansion slot connector of the workstation or PC. Make sure the interface is fully seated by pushing down firmly with the palm of your hand. The GPIO connector should extend through the backpanel opening to allow cable installation.
5. Replace the cover plate on the workstation or PC.

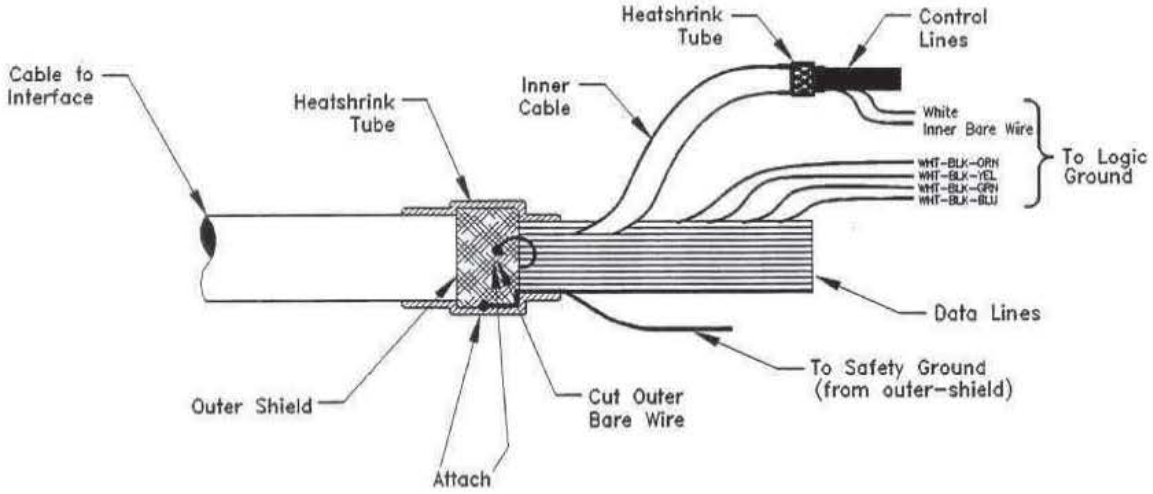
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Preparing and Installing the GPIO Cable

The HP E2074/5 GPIO interface is shipped with a 4.6 M (15 ft) unterminated GPIO cable (HP part #5061-4209). The connector at the one end of this cable fits the HP E2074/5 interface connector on the backplane of your workstation or PC. This section explains how to prepare the other, unterminated end of the GPIO cable so you may connect it to your peripheral device. This section then explains how to attach the cable to both the HP E2074/5 interface connector and your peripheral's connector to complete the installation.

To complete the cable, you will need to add the proper connector that will attach to your peripheral device. You may also want to read the next chapter (Chapter 3, "Configuration Information"), as well as your peripheral's hardware documentation, before actually completing the cable. By doing so, you will understand how to connect and use the various lines of the HP E2074/5 GPIO interface with your peripheral device.

The following figure shows how to prepare the unterminated end of the GPIO cable. The procedure on the next page explains how to prepare and install the cable.



Preparing the GPIO Cable

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To prepare and install the GPIO cable:

1. Cut the cable to the required length, allowing sufficient length for slack.
2. Strip off approximately 10 cm (4 inches) of the outer plastic jacket.
3. Cut off all but approximately 1 cm (1/2 inch) of the outer shield.
4. Fold the outer shield back over the outer jacket.
5. Fold back and cut the outer bare wire.
6. Attach the bare wire to the outer shield.
7. Attach a wire to the outer shield which will connect to the safety ground.
8. Completely cover the end of the outer jacket and outer shield with heatshrink tubing or electrical tape.
9. Cut back the inner shield and its nylon jacket to within 2.5 cm (1 inch) of the outer jacket. (Do *not* cut off the bare inner wire.)
10. Attach the bare inner wire (inner shield) to the logic ground.
11. Completely cover the end of the inner shield and nylon jacket with heatshrink tubing or electrical tape.

NOTE

Do *not* allow the inner and outer shields to short together.

12. Strip and connect the cable wires to the connector for your peripheral device, as required. (Refer to your peripheral's hardware documentation.)
13. Connect the logic ground wires as shown in the previous figure to your peripheral's logic ground.

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14. Connect the safety grounds to the peripheral connector.
15. Insulate unused wire with heatshrink tubing or electrical tape.
16. Connect the original connector to the HP E2074/5 GPIO interface connector on the backplane of the workstation or PC. Tighten the GPIO connector screws.
17. Connect the other connector to your peripheral device, as required. (Refer to your peripheral's hardware documentation.)

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Where to Go Now

You have now finished installing the HP E2074/5 GPIO interface. Please continue on to Chapter 3, "Configuration Information," to learn about the functionality of the HP E2074/5. The information provided in Chapter 3 is essential to your setting the proper configuration values for the HP E2074/5 via the configuration method required for your software.

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3

Configuration Information

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Configuration Information

This chapter provides a detailed, functional description of the HP E2074/5 GPIO interface. You will need to understand this information in order to set the appropriate configuration values for the HP E2074/5 via the configuration method required for your software. This information should also be helpful when you are preparing and installing the GPIO cable.

After you have read this chapter and decided how you want to configure the HP E2074/5, refer to your software documentation to configure your I/O application software for the HP E2074/5. (See the "Related Software Documentation" section in Chapter 1 of this guide.)

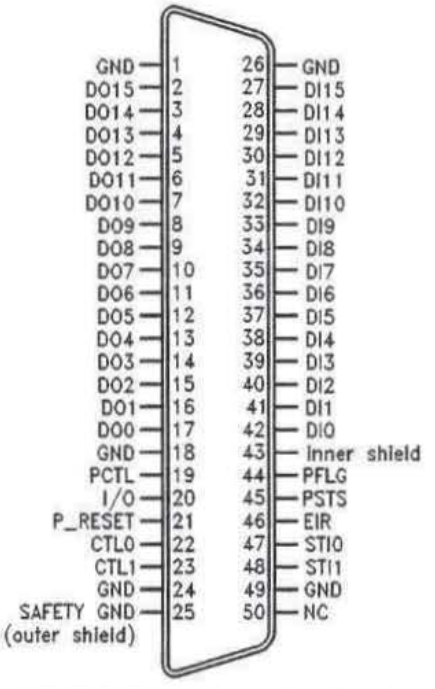
This chapter contains the following sections:

- Connector Pinouts
- Data Lines
- Peripheral Information Lines:
  - Peripheral Control and Peripheral Flag Handshake Lines (PCTL and PFLG)
  - Input/Output Direction Control Line (I/O)
  - Peripheral Status Line (PSTS)
  - Peripheral Reset Line (P_RESET)
  - External Interrupt Request Line (EIR)
  - Control Output Lines (CTL0 and CTL1)
  - Status Input Lines (STI0 and STI1)
- Direct Memory Access (DMA)

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Connector Pinouts

First, to help you become oriented, the following figure shows you the pinouts on the HP E2074/5 GPIO interface connector.



HP E2074/5 GPIO Connector Pinouts

Label	Line(s)
DI0 through DI15	Data Input
DO0 through DO15	Data Output
PCTL and PFLG	Peripheral Control and Peripheral Flag handshake
I/O	Input/Output direction control
PSTS	Peripheral Status
P_RESET	Peripheral Reset
EIR	External Interrupt Request
CTL0 and CTL1	Control Output
STI0 and STI1	Status Input

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Data Lines

There are 32 data lines on the HP E2074/5: 16 designated as data input, and 16 designated as data output.

The 16 data input lines are labeled DI0 through DI15. The following table lists the connector pin numbers and wire color codes for the data input lines.

Data Input Lines

Label	Pin No.	Wire Color Code
DI0	42	Black
DI1	41	Brown
DI2	40	Red
DI3	39	Orange
DI4	38	Yellow
DI5	37	Green
DI6	36	Blue
DI7	35	Violet
DI8	34	White/Brown/Red
DI9	33	White Brown/Orange
DI10	32	White/Brown/Yellow
DI11	31	White/Brown/Green
DI12	30	White/Red/Orange
DI13	29	White/Red/Yellow
DI14	28	White/Red/Green
DI15	27	White/Red/Blue

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The 16 data output lines are labeled DO0 through DO15. The following table lists the connector pin numbers and wire color codes for the data output lines.

Data Output Lines

Label	Pin No.	Wire Color Code
DO0	17	White/Black
DO1	16	White/Brown
DO2	15	White/Red
DO3	14	White/Orange
DO4	13	White/Yellow
DO5	12	White/Green
DO6	11	White/Blue
DO7	10	White/Violet
DO8	9	White/Orange/Yellow
DO9	8	White/Orange/Green
DO10	7	White/Orange/Blue
DO11	6	White/Orange/Violet
DO12	5	White/Yellow/Green
DO13	4	White/Yellow/Blue
DO14	3	White/Yellow/Violet
DO15	2	White/Yellow/Gray

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Peripheral Information Lines

In addition, there are 10 peripheral information lines. The following table lists the connector pin numbers and wire color codes for the peripheral information lines.

Peripheral Information Lines

Label	Pin No.	Wire Color Code
PCTL	19	White/Gray
PFLG	44	Gray
I/O	20	White/Black/Brown
PSTS	45	White/Black/Gray
P_RESET	21	White/Black/Red
EIR	46	White/Brown/Gray
CTL0	22	White/Red/Violet
CTL1	23	White/Red/Gray
STI0	47	White/Brown/Blue
STI1	48	White/Brown/Violet

All of the HP E2074/5 data lines and peripheral information lines are described fully in the following sections.

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Data Lines

The data lines of the HP E2074/5 GPIO interface consist of the lines designated for data input, DI0 through DI15, and those for data output, DO0 through DO15. Like all the HP E2074/5 lines, the default logic sense (polarity) of the data lines is low-true. However, you can change the polarity of either set of data lines to high-true with the HP E2074/5 *polarity* configuration value in your software.

In addition, the data lines of the HP E2074/5 can be configured in two primary ways. You set the configuration mode you want via the *mode* or *Data Port* configuration value in your software. You can configure the HP E2074/5 data lines in either of the following two ways:

- With the standard data input and data output path. In this configuration, lines DI0 through DI15 are the data input lines, and lines DO0 through DO15 are the data output lines, as usual.

  This configuration is the same as (compatible with) that used with the HP 98622 GPIO interface. Hence, this configuration of the data lines for the HP E2074/5 is called *Compatibility Mode*.

- With a bi-directional data port and auxiliary control path. In this configuration, lines DI0 through DI15 (that is, the lines normally designated for data input) serve as a bi-directional data path. Lines DO0 through DO15 (the lines normally designated for data output) serve as independent, auxiliary control lines.

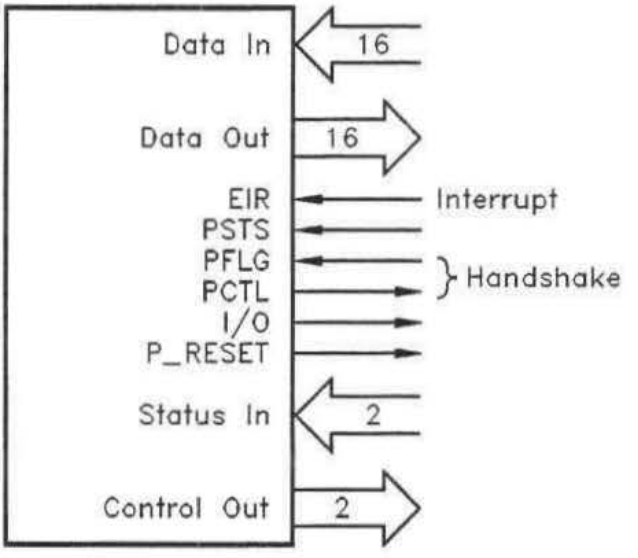
  This configuration of the data lines for the HP E2074/5 is called *Enhanced Mode*.

Given the two different configurations that are possible, this section discusses the data lines for the HP E2074/5 with regard to each particular configuration you can use. The first subsection explains how the data lines function in Compatibility Mode, and the second explains how they function in Enhanced Mode. The final subsection then describes the choices available for data-in clocking.

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Compatibility Mode

When configured in Compatibility Mode, all the lines of the HP E2074/5 appear the same as the HP 98622 GPIO interface. This is summarized in the following figure.



Overview of Compatibility Mode

Thus, in Compatibility Mode, data input and data output are handled on separate, independent ports. Each port (the data input port and the data output port) has 16 lines (labeled 0 through 15) for a maximum of 16 bits each. You can configure the logic level of either port as either high-true or low-true.

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If you are using an HP E2074/5 with the same peripheral device and same cable as an existing HP 98622 application, you should use Compatibility Mode. The HP E2074/5 software configuration values set all the same characteristics that were set by DIP switches on the HP 98622, except interrupt level. The interrupt level is always 5 for EISA cards, such as the HP E2074/5. If your existing HP 98622 application uses an 8-bit data width, note that the upper data byte is *undefined* in 8-bit mode on these cards. Although every effort was made to provide complete compatibility, there is no guarantee that the undefined lines on the HP E2074/5 and the undefined lines on the HP 98622 will assume matching states at all times.

The next subsections describe the data input and the data output lines in Compatibility Mode.

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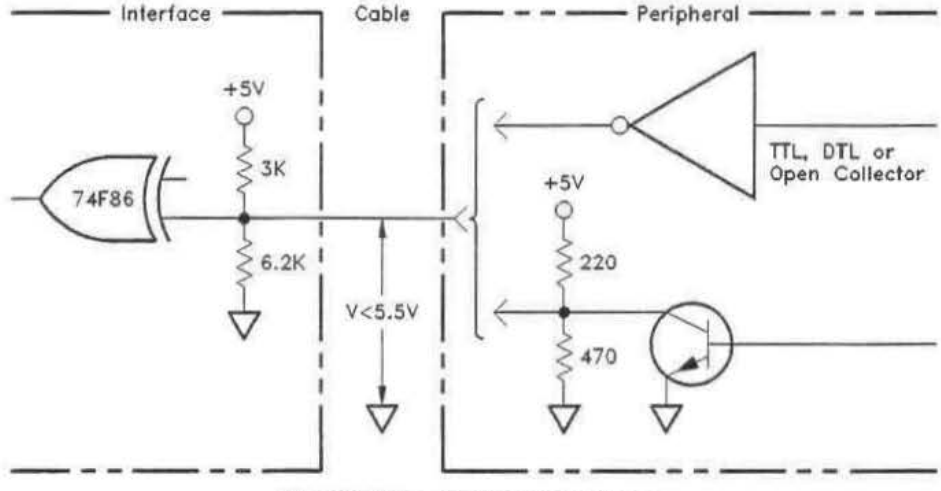
Data Input Lines

In Compatibility Mode, there are 16 data input lines labeled DI0 through DI15. Input lines DI0 through DI7 are the low (least-significant) byte, and DI8 through DI15 are the high (most-significant) byte. Three choices of data-in clocking are available for each byte or for the 16-bit word. Refer to the "Data-In Clocking" subsection later in this section for more information.

The data input lines are TTL lines. A resistive divider biases open lines to approximately +3.4 volts. The following figure shows one data input line and some possible ways a peripheral device might connect to it.

CAUTION

The voltage applied to a data input line must never exceed +5.5 volts.



Electrical Detail of Data Input Lines

The following is a list of requirements for the data input lines. Any peripheral driver circuit must be compatible with these input requirements:

I_{in}low max = −2.3 ma (V_{in}low = 0.4 V)

V_{in}max = 5.5 V

V_{in}high > 2 V

V_{in}low < 0.7 V

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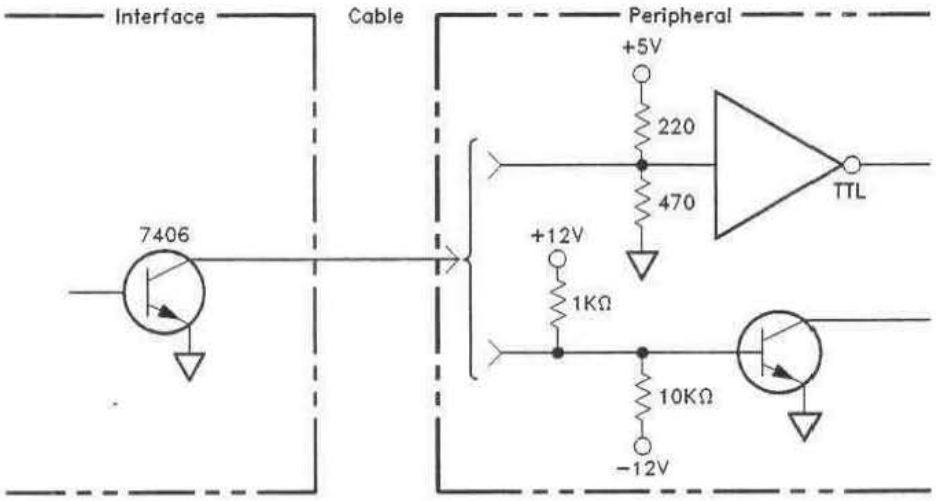
Data Output Lines

In Compatibility Mode, there are 16 data output lines labeled DO0 through DO15. Output lines DO0 through DO7 are the low (least-significant) byte, and DO8 through DO15 are the high (most-significant) byte.

The data output lines are open-collector drivers which can sink a maximum current of 40 ma. For best flexibility, no internal pull-ups are used. Thus, the peripheral device must provide a pull-up to a positive voltage, not to exceed 30 volts. The following figure shows one data output line and some possible ways a peripheral device might connect to it.

CAUTION

Do *not* apply a negative voltage to the data output lines.



Electrical Detail of Data Output Lines

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The following is a list of requirements for the data output lines. Any peripheral receiver circuit must be compatible with these output requirements:

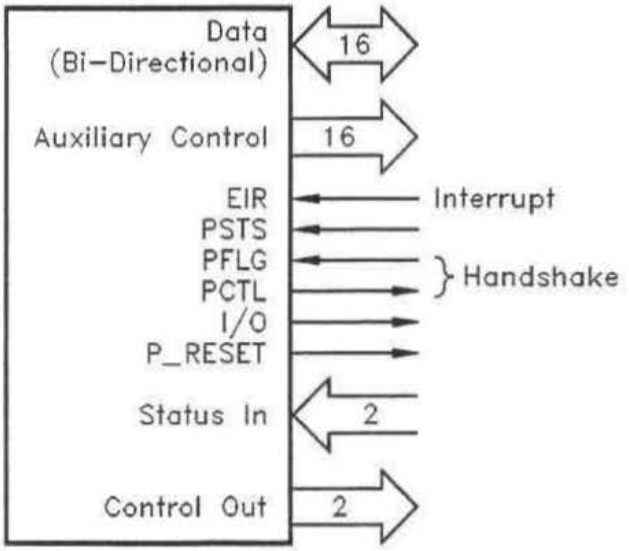
V_{out}low

(I_{out}low = 16 ma)	= 0.4 V max
(I_{out}low = 40 ma)	= 0.7 V max
V_{out}high (open collector)	= 30 V max
I_{out}low	= 40 ma max
I_{out}high(Vout = 30 V)	= 250 ua

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Enhanced Mode

When configured in Enhanced Mode, the HP E2074/5 uses a bi-directional data port on the lines normally designated for data input (DI0 through DI15). The data output lines (DO0 through DO15) are thus free to be used as independent auxiliary control lines. This is summarized in the following figure.



Overview of Enhanced Mode

Enhanced Mode allows more interfacing flexibility than Compatibility Mode. However, Enhanced Mode is only appropriate for use with peripheral devices that have bi-directional data ports.

The next subsections describe the bi-directional data lines and the auxiliary control lines in Enhanced Mode.

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Bi-Directional Data Lines

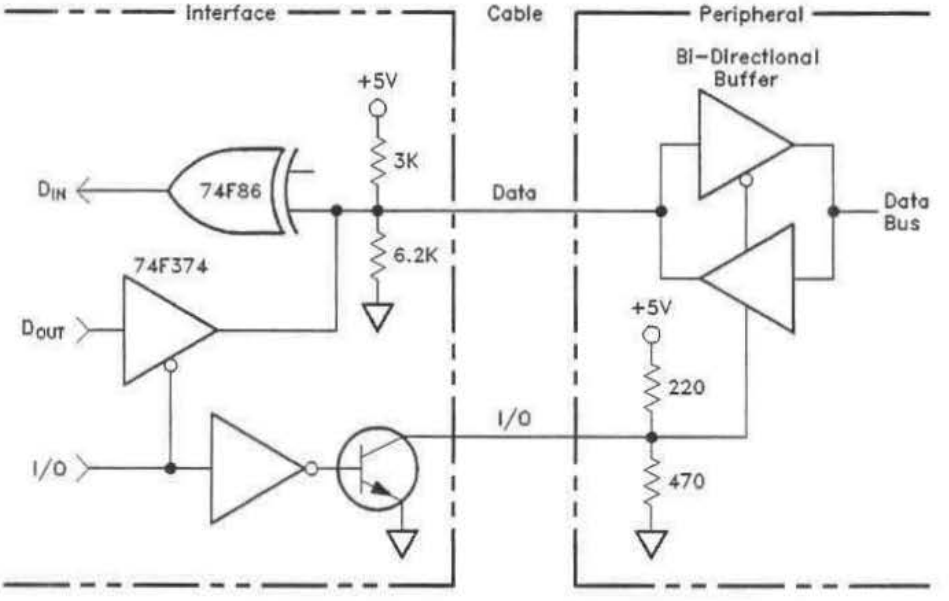
In Enhanced Mode, the bi-directional data port is TTL level. It has resistive pull-ups to +5 volts. The peripheral device must use a data port compatible with bi-directional protocol.

The HP E2074/5 port direction is controlled by the I/O (Input/Output) direction control line. Likewise, the peripheral device must use the I/O line to set the proper direction of its data port. The I/O line is low when the HP E2074/5 drivers are enabled (output) and is high when the HP E2074/5 drivers are disabled (input). The following figure shows one bi-directional data line and one way a peripheral device might connect to it.

CAUTION

The voltage applied to the bi-directional data lines (DI0 through DI15) must never exceed +5.5 volts.

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Electrical Detail of Bi-Directional Data Lines

CAUTION

When connected to an HP E2074/5 in Enhanced Mode, the peripheral device must never attempt to drive the data lines at the same time that the HP E2074/5 drivers are enabled. Also, the peripheral device must not exceed TTL voltage or current levels on the data lines.

Failure to follow these specifications can result in damage to the HP E2074/5 hardware interface. If your peripheral device cannot conform to these specifications, do *not* use Enhanced Mode. See the previous subsection on "Compatibility Mode" instead.

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Auxiliary Control Lines

The auxiliary control lines created by Enhanced Mode are connected to the 7406 open-collector drivers described in the previous "Compatibility Mode" subsection. They have the same 30 volt, 40 ma limits. Like the control output lines (CTL0 and CTL1), the auxiliary control lines are write-only and use no handshake with the peripheral device.

NOTE

Because of internal connections, the auxiliary control lines created by Enhanced Mode inherit the same logical polarity configured for the data output port.

Programming Notes. In C programs, the auxiliary control lines are set by the `I_GPIO_AUX` parameter of the `igpioctrl` function in HP SICL. For example:

```
igpioctrl(id, I_GPIO_AUX, value);
```

For more information, please refer to the HP SICL documentation.

In HP BASIC/UX 700 programs, the auxiliary control lines are set by CONTROL register 4. For more information, please refer to the HP BASIC/UX 700 documentation.

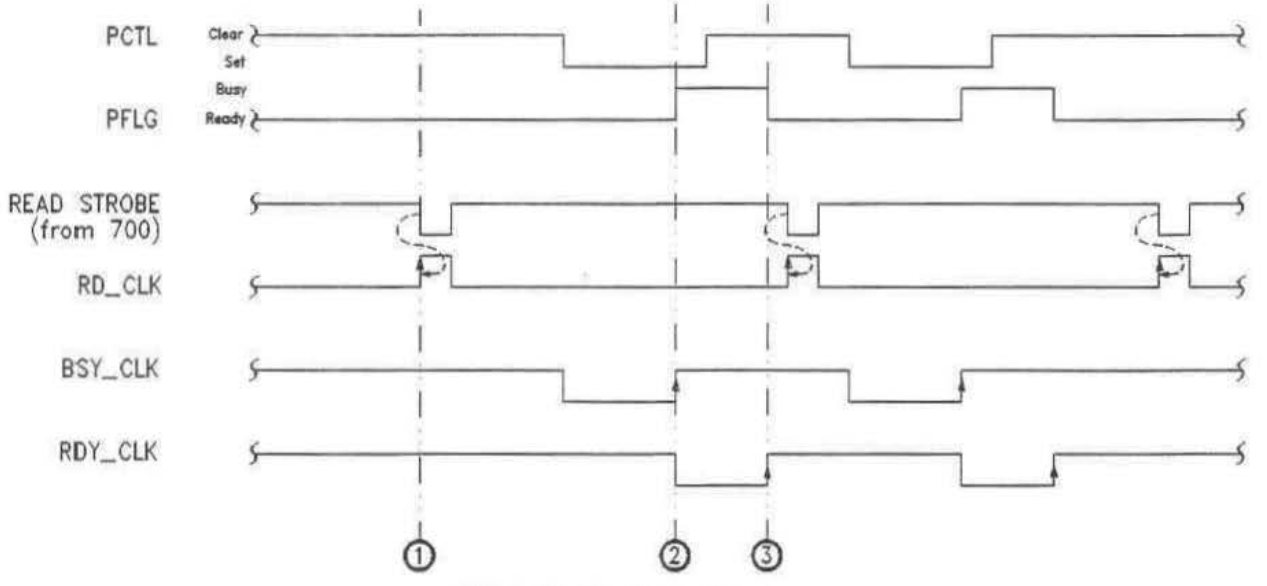
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Data-In Clocking

Three choices of data-in clocking are available for each byte or for the 16-bit word. You set this in the HP E2074/5 *read_clk* or *Read Clock* configuration value in your software.

As explained earlier, the 16 data input lines are divided into two data bytes. The lower, least-significant byte consists of data input lines DI0 through DI7. The upper, most-significant byte consists of data input lines DI8 through DI15. Data-in clocking can be selected from any of three clock sources for both upper and lower bytes.

The following figure shows the timing diagram for data-in clocks on a full standard read. The clocking for the other operating modes, including pulse mode, follows these same guidelines.



Data-In Clocking Timing Diagram

The next subsections describe the three clocks which can be selected to latch data. The descriptions are applicable to either the upper or lower byte.

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Read Clock

The Read clock causes the data to be latched into the data input register when the register is read. (See the previous figure, phase 1.) The Read clock accomplishes this by clocking the register on the leading edge of the read strobe of the register. During a DMA transfer, the Read clock causes the data to be latched with DMA acknowledge which is generated by the DMA controller.

Bsy Clock

The Busy clock latches the data into the data input register by the leading edge of the PFLG line. (Refer to the previous figure, phase 2.) This transition also clears the PCTL line. This is the ready-to-busy transition of the PFLG line.

Rdy Clock

The Ready clock latches the data into the data input register by the trailing edge of the PFLG line. (Refer to the previous figure, phase 3.) This is the busy-to-ready transition of the PFLG line.

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Peripheral Information Lines

Ten lines control the exchange of information between the HP E2074/5 GPIO interface and the peripheral device. Five of these lines are outbound to control the peripheral:

- PCTL
- I/O
- P_RESET
- CTL0 and CTL1

The other five peripheral information lines are inbound to communicate the state of the peripheral:

- PFLG
- PSTS
- EIR
- STI0 and STI1

All 5 incoming lines have Schmitt trigger receiver circuits. These circuits accept signals with slow rise and fall times. They also provide good noise immunity. Although the voltage on these lines must not exceed 5.5 volts, there are no restrictions on the input rise and fall times.

All of the peripheral information lines are described in the following subsections.

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Peripheral Control and Peripheral Flag Handshake Lines (PCTL and PFLG)

The peripheral control line (PCTL) and the peripheral flag line (PFLG) are used as a 2-wire handshake between the HP E2074/5 interface and the peripheral device. The HP E2074/5 interface controls the PCTL line, and the peripheral device controls the PFLG line.

The HP E2074/5 provides both handshake modes of the HP 98622, plus an additional async output mode. Also, the logic sense of the PCTL and PFLG lines on the HP E2074/5 can be configured differently. Like all the HP E2074/5 lines, PCTL and PFLG have the default logic sense (polarity) of low-true. The polarity of either or both the PCTL and PFLG lines can be changed with the HP E2074/5 *polarity* configuration value in your software.

If you are porting an HP 98622 application, notice that the bits in the *polarity* field correspond to DIP switches on the HP 98622 interface card. However, many old cards had "1" and "0" markings that were backwards from the electrical state of the switch. When transferring your old settings to the *polarity* value, keep in mind that all the bits might be upside-down (0→1).

The following subsections describe each handshake line (PCTL and PFLG), as well as the handshake modes for the HP E2074/5.

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PCTL Line

The PCTL line is an outgoing line to the peripheral. PCTL has two states: set and clear. The HP E2074/5 sets the PCTL line to start a handshake.

The peripheral device clears the PCTL line when a ready-to-busy transition occurs on the PFLG line. (A ready-to-busy transition is when PFLG goes from the ready state to a busy state.) During an output transfer, PCTL is delayed to allow new output data to settle. This delay is explained in the next subsection, "PCTL Delay."

PCTL Delay. You can select the delay (settling time) from when data is placed on the GPIO bus to when PCTL is Set during an output data transfer. The delay selection is set with the HP E2074/5 *delay* configuration value in your software. The delay selections are: 200 ns, 400 ns, 700 ns, 1.2 μs, 2 μs, 5 μs, 10 μs, and 50 μs.

The delay selections are for DMA and auto-handshake mode. If you use standard-handshake mode, the actual delay is approximately 500 ns longer than the delay configuration value you select in your software. (Refer to the "Handshake Modes" subsection for more information.)

PFLG Line

The PFLG line is an incoming line from the peripheral device. PFLG must be driven to complete a data transfer. PFLG has two states: ready and busy.

When the peripheral device is ready to transfer data, it responds by setting PFLG to ready. When the computer sets PCTL, the computer has initiated a data transfer either in or out, depending on the state of the I/O line. (See the "Input/Output Direction Control Line (I/O)" later in this section.)

After the data transfer occurs, the peripheral device responds by setting PFLG to busy. This causes the HP E2074/5 to clear the PCTL line on the ready-to-busy transition. In the full handshake mode, the computer waits until the peripheral device makes PFLG ready before initiating another data transfer. In the pulse handshake mode, the computer initiates the transfer without waiting. Refer to the next subsection on "Handshake Modes" for more information.

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Handshake Modes

Like the HP 98622, the PCTL and PFLG lines on the HP E2074/5 can be used for **full-mode** or **pulse-mode** handshakes. Additionally, the HP E2074/5 provides an **async-mode** for output.

You set the handshake modes with the HP E2074/5 *mode* or *Handshake* configuration value in your software. All of the handshake modes for the HP E2074/5 are explained in the following subsections.

Full-Mode Handshakes. With full-mode handshakes, the computer first checks to see that the peripheral device is Ready before initiating the transfer of each byte or word. With this handshake mode, the interface detects Ready *when both PCTL is Clear and PFLG is Ready*. If the peripheral device does not indicate Ready, the computer waits until a Ready is indicated.

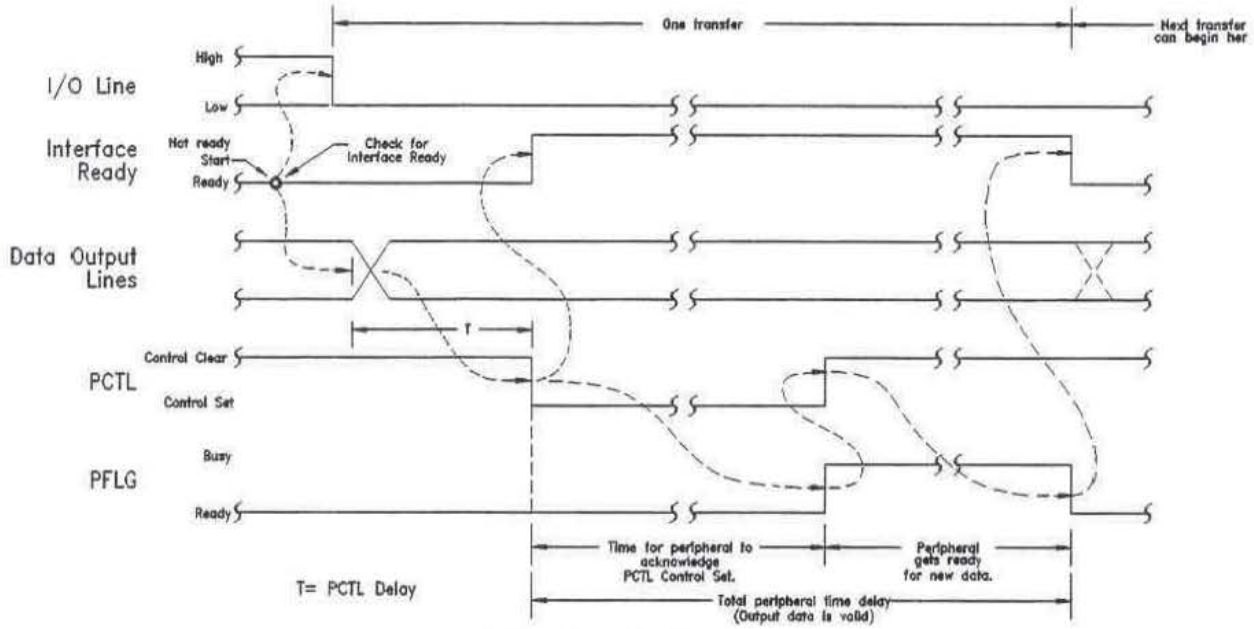
During a write cycle, when a Ready is sensed, the computer drives the I/O line Low, then places data on the appropriate data lines. The interface then waits the PCTL delay time before initiating the transfer by placing PCTL in the Set state.

The peripheral acknowledges the computer's request by placing the PFLG line Busy; this PFLG transition automatically Clears the PCTL line. However, the computer cannot initiate further transfers until the peripheral is Ready with full-mode handshake. Ready is not sensed until both PCTL is Clear and PFLG is Ready.

The data on the data lines is held valid from the time PCTL is Set until after the peripheral device indicates Ready. The peripheral may read the data any time within this time period.

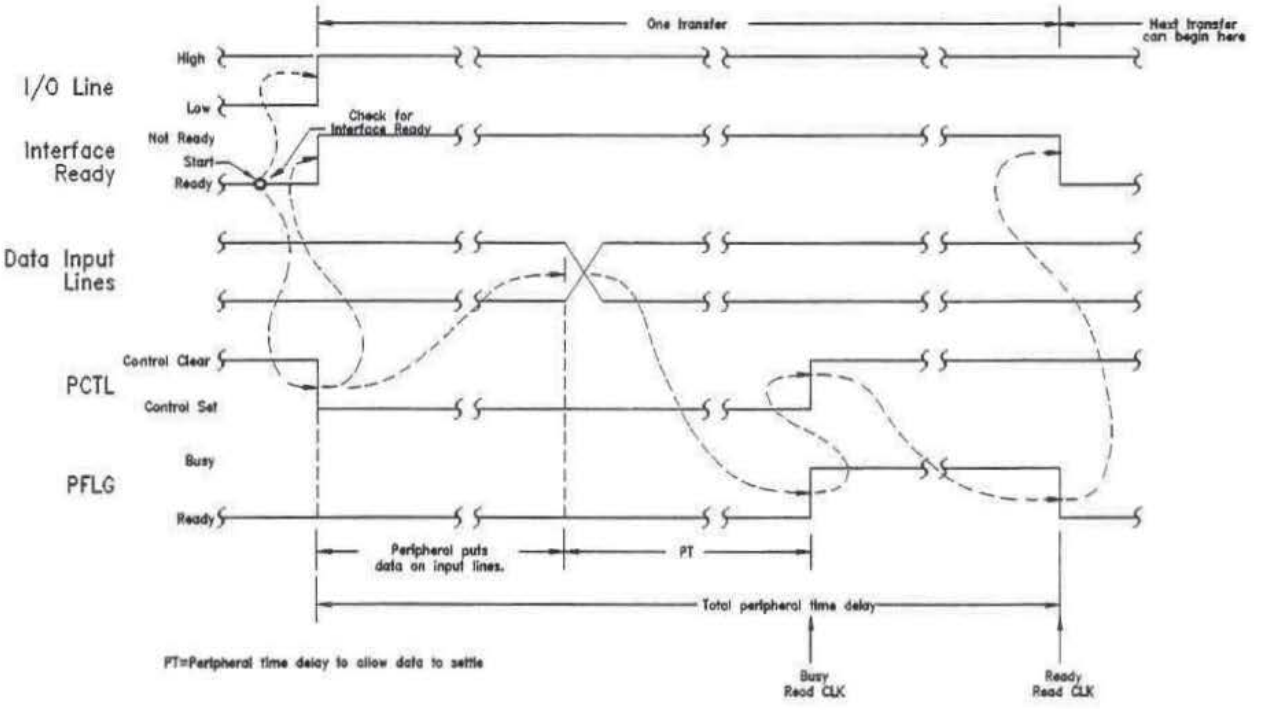
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The following two figures show the order of events during full-mode output and input operations.



Full-Mode Timing Diagram: Output Operation

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Full-Mode Timing Diagram: Input Operation

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Pulse-Mode Handshakes. The main difference between full-mode and pulse-mode handshake is that the PFLG line is not checked for Ready before the computer initiates pulse-mode handshakes. With pulse-mode handshakes, the computer may initiate a subsequent data transfer as soon as the PCTL line is Cleared by the Ready-to-Busy transition of PFLG.

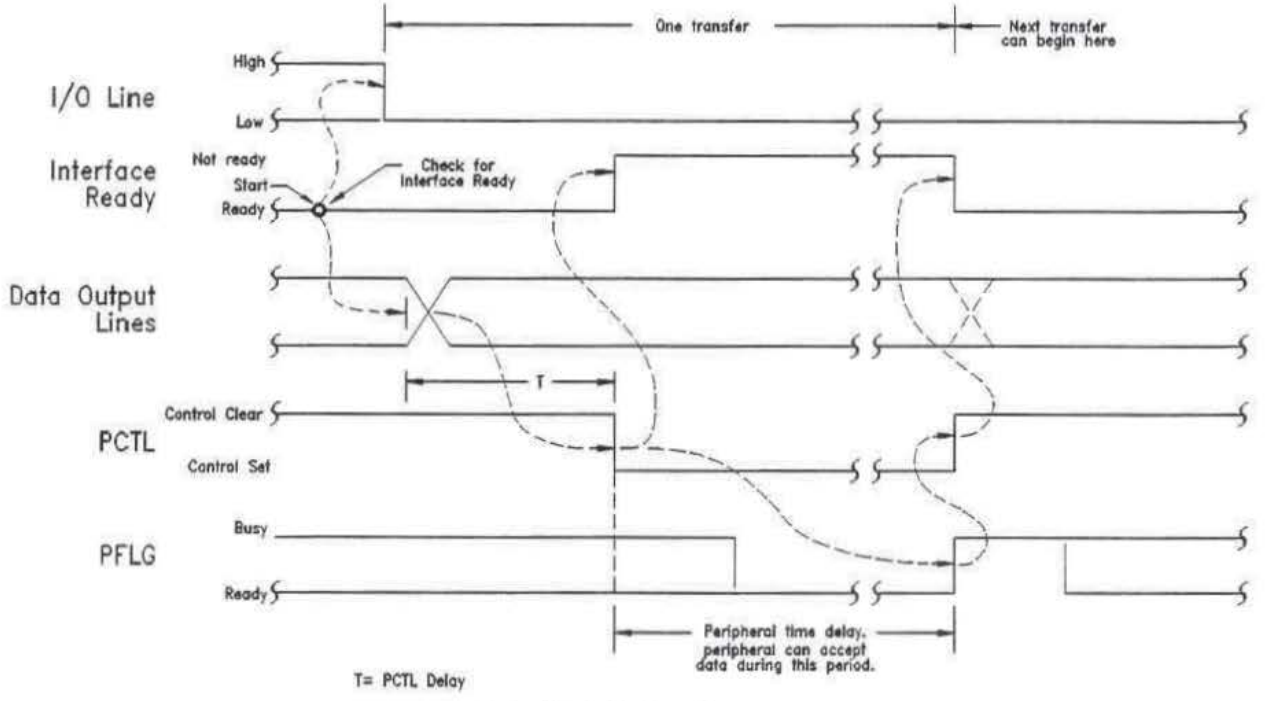
This absence of the PFLG check can give a slightly higher data-transfer rate than possible with full-mode handshakes. However, in some cases, it places additional timing restrictions on the peripheral device's response time.

During a write cycle, the PFLG line is not checked for Ready before the computer drives the I/O line Low and places data on the appropriate data lines. A PCTL delay time later, the interface initiates the transfer by placing PCTL in the Set state.

The peripheral device acknowledges by placing PFLG Busy; this transition automatically Clears PCTL. Then the computer may initiate another transfer any time after PCTL is Clear, possibly before the peripheral places PFLG in the Ready state.

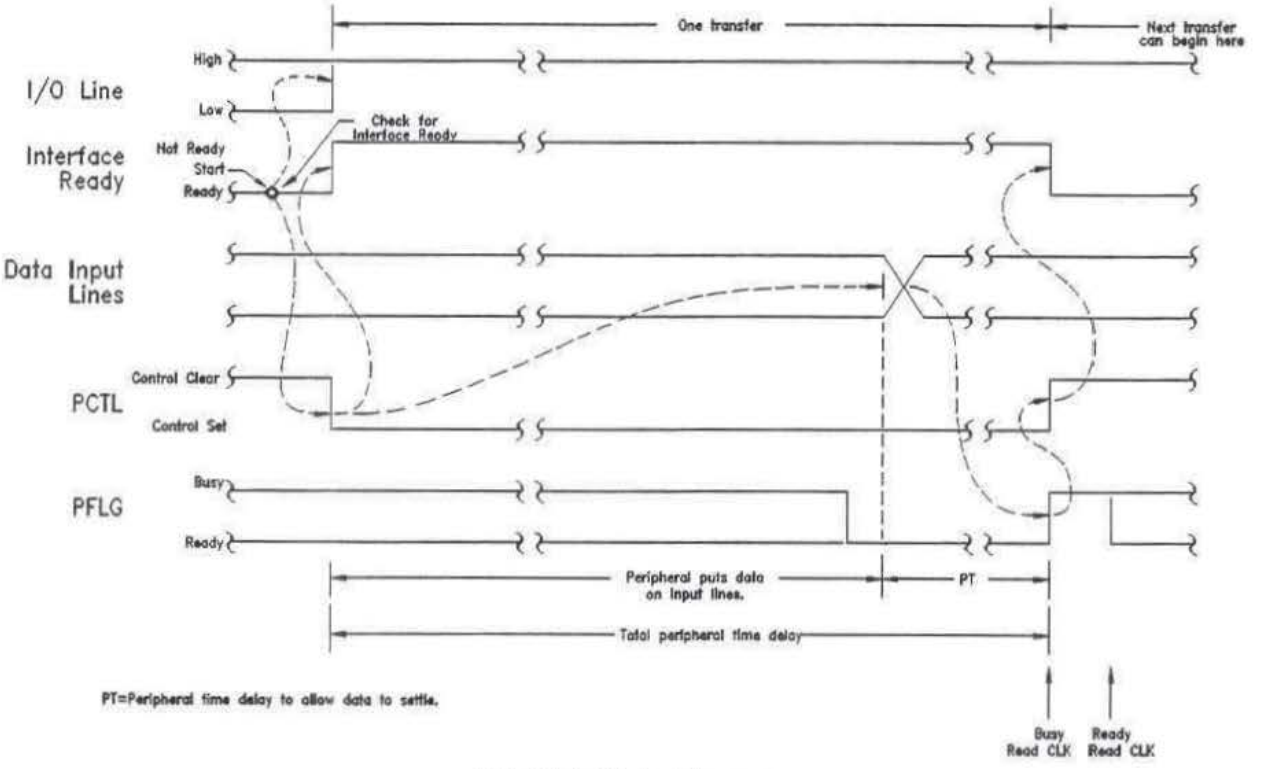
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The following two figures show the order of events during pulse-mode output and input operations.



Pulse-Mode Timing Diagram: Output Operation

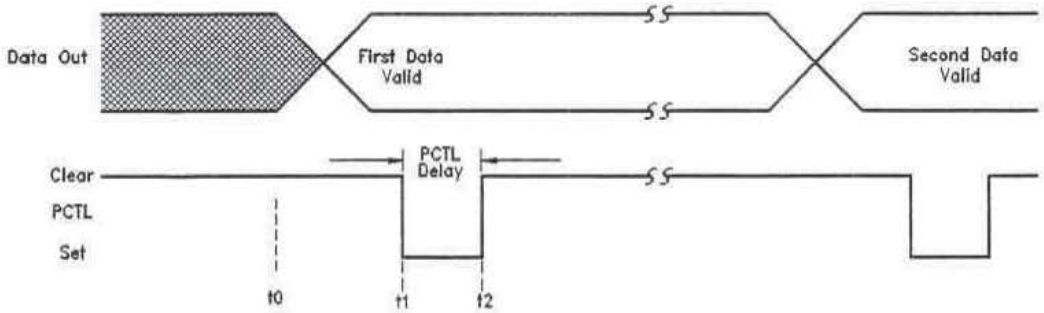
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Pulse-Mode Timing Diagram: Input Operation

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Async Output Mode. The HP E2074/5 async output mode is not really a handshake, because it completely ignores the PFLG line, and it has no concept of peripheral Ready. It is intended for peripheral devices which cannot implement a handshake, but need only a fleeting strobe to catch their data. The following figure shows the order of events in async output mode.



Async Output Mode Timing Diagram

The computer drives the I/O line low (not shown) and places data on the data out lines (t0). Soon after, the interface puts the PCTL line in the Set state (t1). The interface then waits the specified PCTL delay time, and clears the PCTL line (t2). In other words, there is a PCTL pulse immediately after each data output.

The width of the PCTL pulse is configurable by the PCTL *delay* configuration value in your software. The time from t0 → t1 depends upon other handshake parameters. In auto-handshake mode, it is very short (around 50 ns). In standard-handshake mode, this time is roughly 500 ns. Because t0 → t1 is short and not controllable, it is recommended that the peripheral device latch its data at the trailing edge (t2) of PCTL, rather than the leading edge.

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Standard-Handshake and Auto-Handshake Modes. Please note that this discussion does not refer to the *type* of handshake configured; it refers only to the method for *starting* that handshake. The handshake types (full and pulse) are discussed earlier in this section.

The term "standard" handshake is not especially descriptive; it refers to the polling method used by the old HP 98622 drivers. In standard-handshake mode, the computer starts a handshake by writing to a PCTL register on the interface. The driver may perform this operation for you, as with an `OUTPUT` statement in HP BASIC/UX 700, or an `iread` function in HP SICL. Or you may perform this operation explicitly, as with `CONTROL` or `igpioctrl`.

Auto-handshake mode is the default method for the HP E2074/5, and is the only method used for DMA transfers. In this mode, the computer starts a handshake simply by accessing the data register on the interface. The separate step of writing to a PCTL register is avoided, so performance is increased.

The operation that benefits the most from auto-handshake mode is an inbound transfer of known size. Examples are `ENTER 12 USING "1024A"`, or `iread` with no `itermchr`. With a sufficiently fast peripheral device, auto-handshake mode can be 10% to 20% faster than standard-handshake mode.

Auto-Handshake can always be used for outbound operations like `OUTPUT` or `iwrite`. Keep in mind that the most significant factor in outbound performance is the amount of PCTL delay time. The extra register access in standard-handshake mode adds about 500 ns to the configured PCTL delay, so auto-handshake mode can be faster. However, you should not reduce the PCTL delay to the point where data integrity is lost. The PCTL delay time should be set according to the characteristics of your GPIO cable and peripheral device.

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Because any data register access automatically starts the next handshake, auto-handshake mode cannot be used for inbound operations of unknown size (such as an HP BASIC/UX 700 free-field **ENTER**, or expecting an **itermchr** with **iread** in HP SICL). In these cases, the *next* handshake would have already started before the computer saw that a termination condition had been reached. Therefore, the HP E2074/5 driver automatically disables auto-handshake mode in these cases.

Programming Notes. Auto-handshake mode is obviously incompatible with programs that implement a custom, explicit handshake. Attempts to manually set PCTL (with **I_GPIO_SET_PCTL** in HP SICL, or with HP BASIC/UX 700 register 1) during auto-handshake mode will cause a program error. Therefore, programs that implement an explicit handshake *must* disable auto-handshake mode.

Auto-handshake mode is the default for the HP E2074/5. In C programs, it can be disabled by the **I_GPIO_AUTO_HDSK** parameter in HP SICL. For example:

```
igpioctrl(id, I_GPIO_AUTO_HDSK, 0);
```

The current auto-handshake state is reported in the **I_GPIO_INFO** value. For example:

```
int value;
igpiostat(id, I_GPIO_INFO, &value);
if (value & I_GPIO_AUTO_HDSK)
  printf("Auto-Handshake enabled\n");
:
```

For more information, please refer to the HP SICL documentation.

In HP BASIC/UX 700 programs, auto-handshake mode is controlled and reported in register 6. For more information, please refer to the HP BASIC/UX 700 documentation.

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Input/Output Direction Control Line (I/O)

The input/output direction control line (I/O) is an outbound line to the peripheral device. I/O indicates to the peripheral which direction the data transfer is to go. I/O goes high when the HP E2074/5 GPIO interface is reading data and low when the interface is writing data.

Peripheral Status Line (PSTS)

The peripheral status line (PSTS) is an incoming line from the peripheral device. It signals to the computer that all is "OK" with the peripheral. PSTS has two states: not OK and OK.

The logic sense (polarity) for PSTS can be changed from low-true (the default) to high-true through the HP E2074/5 *polarity* configuration value in your software.

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Peripheral Reset Line (P_RESET)

NOTE

This is the same as the PRESET line on the HP 98622 GPIO interface.

The peripheral reset line (P_RESET) is an outbound line to the peripheral device. P_RESET is used to reset and/or initialize the peripheral device. P_RESET is pulsed low when the computer is first turned on. It is also pulsed low when the interface is reset by `iclear` in HP SICL, or by Control register 0 in HP BASIC/UX 700. This pulse lasts for at least 12 μs.

External Interrupt Request Line (EIR)

The external interrupt request line (EIR) is an inbound line from the peripheral device. You can use EIR to trigger an interrupt on an external event. EIR should be held low until the interrupt service routine has been invoked and has acknowledged the interrupt. The method for acknowledging an EIR interrupt is device-dependent. Please consult your peripheral's hardware documentation.

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Control Output Lines (CTL0 and CTL1)

The control output lines (CTL0 and CTL1) provide two additional, outgoing control lines to the peripheral device. You can use these low-true logic signals for any purpose to control the peripheral.

CTL0 and CTL1 have two states: control set (low) and control clear (high). These lines are latched and can be set or cleared (low = 1, high = 0) by a control operation. The states of these lines are cleared at power up and are unchanged after a reset.

Status Input Lines (STI0 and STI1)

The status input lines (STI0 and STI1) provide two additional, incoming status lines from the peripheral device. You can use these low-true logic signals for any purpose that reflects the status of the peripheral.

STI0 and STI1 have two states: low (logic 1) and high (logic 0), and they cannot be inverted. You can examine the state of these lines with a status operation.

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Direct Memory Access (DMA)

NOTE

DMA is *not* supported on Windows 95 or Windows NT.

Direct Memory Access (DMA) provides more efficient system performance by freeing the computer's CPU during data transfers. DMA transfers can be done using either byte (8-bit) or word (16-bit) accesses. This data width is set by the **igpiosetwidth** function in HP SICL for HP-UX, or the **ASSIGN** statement in HP BASIC/UX 700.

The computer has several DMA channels available. Some are 8-bit channels, and some are 16-bit channels. The *dma* configuration value in your software is used to specify which channel the HP E2074/5 interface will use for DMA transfers. Channels 1 and 2 are supported for 8-bit transfers, and channels 5, 6, and 7 are supported for 16-bit transfers. If you do not specify a channel in the software configuration (*dma* = 0), then DMA will not be used.

Ideally, an HP E2074/5 interface should be assigned to a DMA channel that is not used by any other interface. If multiple HP E2074/5 interfaces are assigned to the same DMA channel, they can cooperate (see the following subsection, "Programming Notes"). If some other type of interface is already assigned to a specific DMA channel, the HP E2074/5 may be prevented from using that channel.

Although the software configuration specifies two DMA channels, the HP E2074/5 does not allocate both those channels. Assuming that the interface's data width remains constant within a given application, only the one channel corresponding to that data width will be used.

Programming Notes. Specifying a DMA channel in the software configuration does not guarantee that all your transfers will be done with DMA. There are several factors that influence the allocation of DMA channels. Some of those factors come from choices in your program, and some come from the sharing of resources in a multi-tasking environment.

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Your program might make requests that are inconsistent with DMA. One example is character matching on inbound data. The DMA controller works strictly by counting; it cannot detect other termination reasons such as line-feed characters. If you specify `itermchr` or `I_GPIO_READ_EOI` in HP SICL for HP-UX, or use free-field `ENTER` in HP BASIC/UX 700, the computer will not use DMA. DMA is also prevented if you enable "Ready" interrupts. The DMA controller cannot do interrupt-driven transfers. Of course, DMA is not used if you explicitly disable it, as with the HP SICL function: `ihint(id, I_HINT_USEPOLL)`.

If there is contention for a DMA channel, the results are influenced by the current `ihint` value in HP SICL for HP-UX. In the default case, your program will first try to get the specified DMA channel. If that channel is already in use, your program will abandon its attempt to use DMA and will continue with a non-DMA transfer. This is also the behavior for some other hints, like `I_HINT_SYSTEM`, and for HP BASIC/UX 700.

If a program specifies `I_HINT_USEDMA`, it will not resort to non-DMA transfers. In this case, the second process to request a specific DMA channel will sleep until the first process is done using that channel. When the first process releases the channel, the second process will resume with its DMA transfer. If the first process never releases the channel, the second process will sleep forever waiting for it. If the second process has a timeout value, it can timeout waiting for a DMA channel.

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Where to Go Now

Please refer to your software documentation to configure the HP E2074/5 GPIO interface for your software, as well as to use the HP E2074/5 with your I/O application software. (See "Related Software Documentation" in Chapter 1 of this guide.)

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