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User's Guide

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June 2001

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Agilent Technologies E2487C Analysis Probe for Intel IA-32 Processors

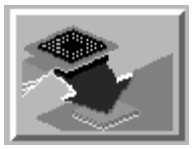
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The Agilent Technologies E2487C Analysis Probe — At a Glance

The Agilent Technologies E2487C Analysis Probe provides a complete interface for state analysis between various Intel IA-32 processors and Agilent Technologies logic analyzers. The Agilent Technologies E2487C requires a processor-specific probe adapter to connect to the supported processors. The supported logic analyzers are listed in chapter 1.

Supported Microprocessors

Microprocessor	Package	Probe Adapter Ordering Information
Intel Pentium II-III®	Slot 1	Agilent Technologies E2492B
Intel Pentium II-III® Xeon ™	Slot 2	Agilent Technologies E2492C
Intel Celeron®	Slot 1	Agilent Technologies E2492B
Intel Celeron®	PPGA	Agilent Technologies E2492E
Intel Pentium III®	FC-PGA	Agilent Technologies E2492E

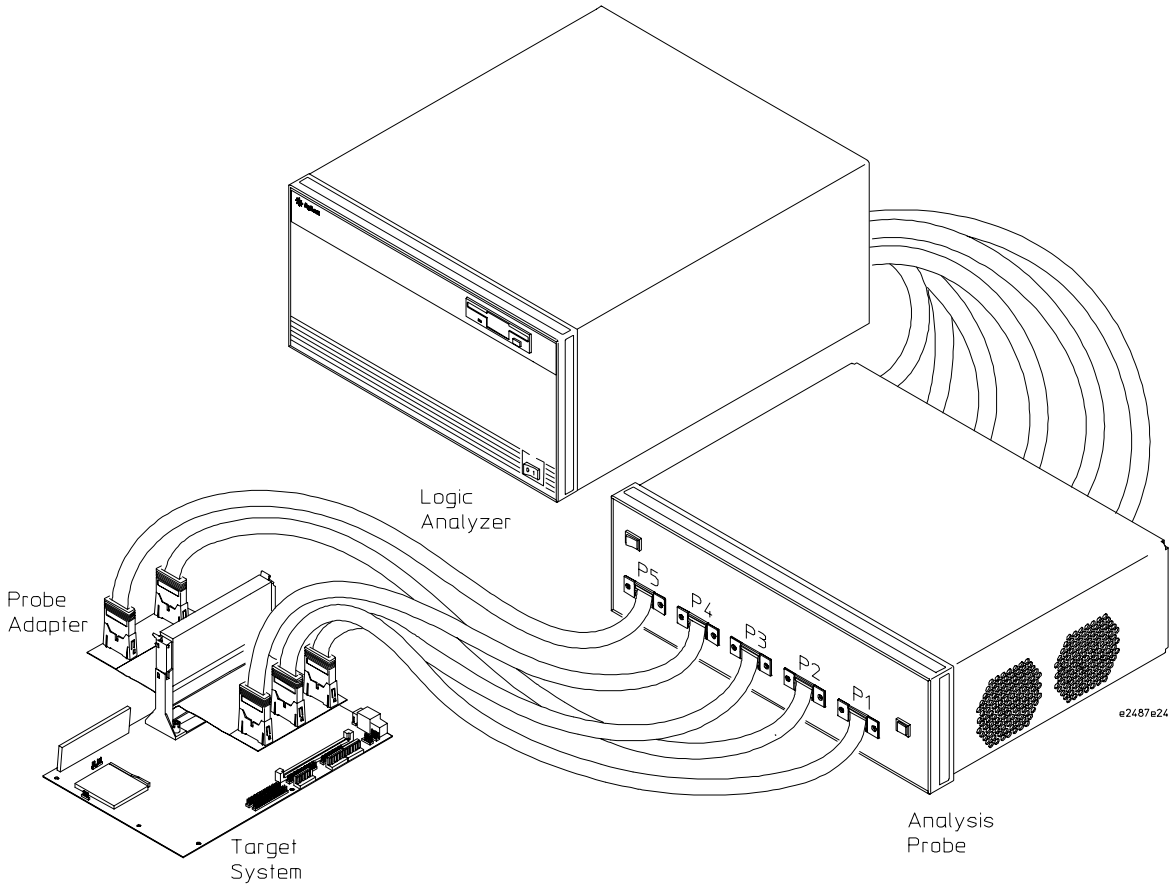


The analysis probe and probe adapter provides the physical connection between the target microprocessor and the logic analyzer. The configuration software sets up the logic analyzer for compatibility with the analysis probe. The inverse assembler lets you obtain displays of the data bus in IA-32 assembly language mnemonics.

The Agilent Technologies 16700 series logic analysis systems contain a Setup Assistant, which guides you through the connection and configuration process using on-screen dialog windows. For an overview of of Setup Assistant, refer to Chapter 1, "Setup Assistant."

For more information on the logic analyzers or microprocessor, refer to the appropriate reference manuals for those products.

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Analyzing a Target System with the Agilent Technologies E2487C Analysis Probe

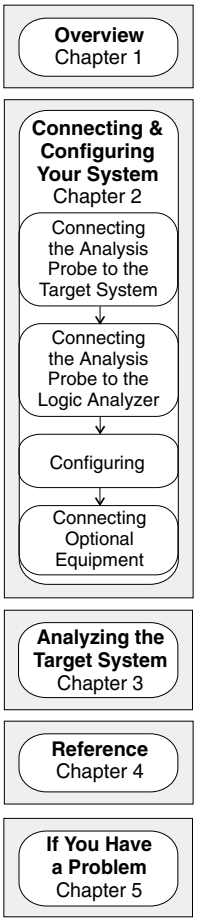
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In This Book

This book is the User's Guide for the Agilent Technologies E2487C Analysis Probe. It assumes that you have a working knowledge of the logic analyzer used and the microprocessor being analyzed.

This user's guide is organized into the following chapters:



Chapter 1 contains overview information, including a list of required equipment.

Chapter 2 explains how to connect the logic analyzer to your target system through the analysis probe, and how to configure the analysis probe and logic analyzer to interpret target system activity. The last section in this chapter shows you how to hook up optional equipment to obtain additional functionality.

Agilent Technologies 16700 Series Logic Analysis Systems

The Agilent Technologies 16700 contains a Setup Assistant, which guides you through the connection and configuration process using on-screen dialog windows. For an overview of Setup Assistant, refer to chapter 1, "Setup Assistant."

Chapter 3 provides information on analyzing the supported microprocessors.

Chapter 4 contains reference information on the analysis probe.

Chapter 5 contains troubleshooting information.

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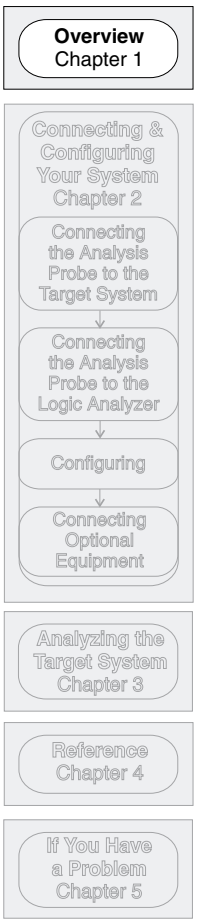
Overview

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Overview

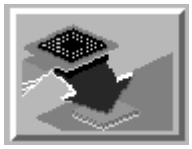
This chapter describes:

- Setup Assistant
- Logic analyzers supported
- Logic analyzer software version requirements
- Equipment used with the analysis probe
- Equipment supplied
- Minimum equipment required
- Additional equipment supported



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Setup Assistant



Setup Assistant is an online tool for connecting and configuring your logic analysis system for microprocessor and bus analysis. Setup Assistant is available on the Agilent Technologies 16700-series logic analysis systems. You can use Setup Assistant in place of the connection and configuration procedures provided in chapter 2.

This menu-driven tool will guide you through the connection procedures for connecting the logic analyzer to an analysis probe, an emulation module, or other supported equipment. It will also guide you through connecting an analysis probe to the target system.

Access Setup Assistant by clicking its icon in the Logic Analysis System window. The on-screen dialog prompts you to choose the type of measurements you want to make, the type of target system, and the associated products that you want to set up.

If you ordered this product with your Agilent Technologies 16700 logic analysis system, the logic analysis system has the latest software installed, including support for this product. If you received this product after you received your logic analysis system, this product might not be listed under supported products. In that case, you need to install the IA-32 Processor Support Package. Use the procedure on the CD-ROM jacket to install the IA-32 Processor Support Package.

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Logic Analyzers Supported

The table below lists the logic analyzers supported by the Agilent Technologies E2487C analysis probe. Logic analyzer software version requirements are shown on the following page.

The Agilent Technologies E2487C requires 11 logic analyzer pods (180 channels) for inverse assembly. The analysis probe contains one additional pod to which the Agilent Technologies E2467A APIC analysis probe can be connected.

Logic Analyzers Supported

Logic Analyzer	Channel Count	State Speed	Timing Speed	Memory Depth
16752A (3 or 5 cards)	68/card	400 MHz	400 MHz	32/64 M states
16751A (3 or 5 cards)	68/card	400 MHz	400 MHz	16/32 M states
16750A (3 or 5 cards)	68/card	400 MHz	400 MHz	4/8 M states
16717A (3 or 5 cards)	68/card	333 MHz	333 MHz	2 M states
16716A (3 or 5 cards)	68/card	167 MHz	333 MHz	512 k states
16715A (3 or 5 cards)	68/card	167 MHz	333 MHz	2 M states
16557D (3 or 5 cards)	68/card	135 MHz	250/500 MHz	2M/4M states
16556D (3 or 5 cards)	68/card	100 MHz	200 MHz	2 M states
16556A (3 or 5 cards)	68/card	100 MHz	200 MHz	1 M states
16555D (3 or 5 cards)	68/card	110 MHz	250 MHz	2 M states
16555A (3 or 5 cards)	68/card	110 MHz	250 MHz	1 M states

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Logic analyzer software version requirements

The logic analyzers must have the latest software to make a measurement with the Agilent Technologies E2487C.

Logic Analyzer Software Version Requirements

Mainframes*	Minimum Logic Analyzer Software Version for use with Agilent Technologies E2487C
Agilent Technologies 16700 Series	Agilent Technologies 16700 logic analyzer software version A.01.20.00 or later.

* The mainframes are used with the Agilent Technologies 1655/56/57, 16715/16/17, and 16750/51/52 logic analyzer modules.

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Equipment Used with the Analysis Probe

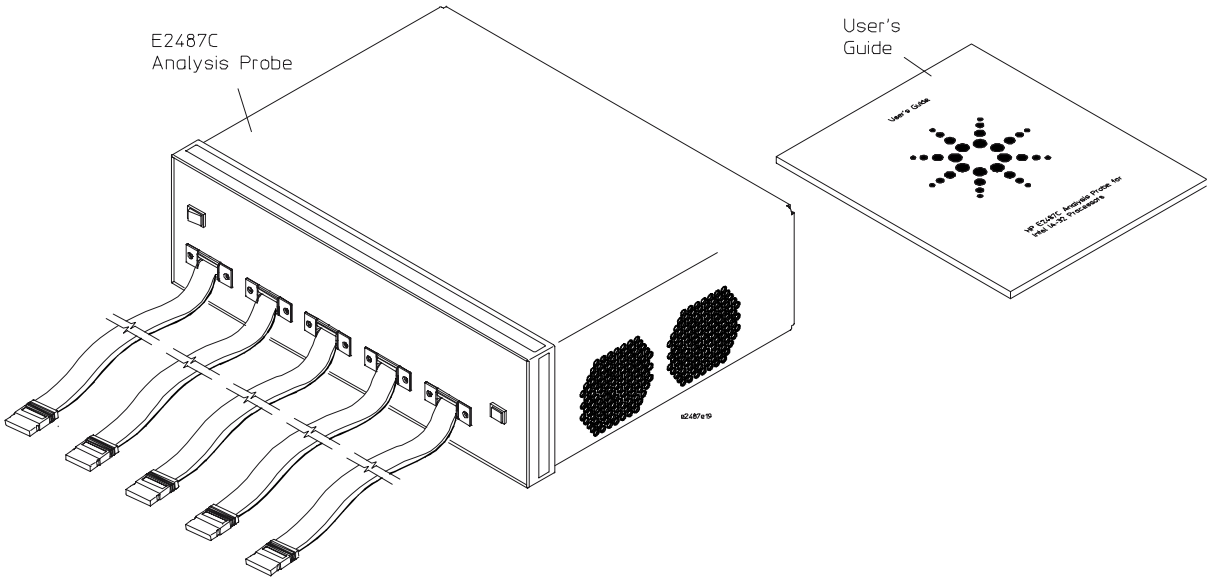
This section lists equipment used with the analysis probe. This information is organized under the following titles: equipment supplied, minimum equipment required, and additional equipment supported

Equipment supplied

The equipment supplied with the analysis probe is shown in the illustration on the next page. It is listed below:

- The analysis probe hardware, which processes the signals. The analysis probe hardware has front-panel cables for connecting the analysis probe to the probe adapter, and rear-panel connectors for the logic analyzer cables.
- Configuration software and inverse assembly software on CD-ROM or already loaded in the Agilent Technologies 16700-series logic analysis system.
- This user's guide

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Equipment Supplied with the Agilent Technologies E2487C

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Minimum equipment required

For state analysis of an IA-32 target system, you need all of the following items.

- The Agilent Technologies E2487C Analysis Probe, configuration files, and inverse assembly software on CD-ROM or already loaded in Agilent Technologies 16700 series logic analysis system.
- One of the processor-specific probe adapters listed on page ii..
- One of the logic analyzers listed on page 1-4, in an Agilent Technologies 16700-Series Logic Analysis Mainframe.The logic analyzer software version requirements are listed on page 1-5.

Additional equipment supported

Instruction disassembly

For instruction disassembly, Branch Trace Messages must be enabled and instruction caches must be disabled. An easy way to do this is with an emulator or run-control tool (such as the Agilent Technologies E5900A #510 or E5901A #510) and a 30-pin debug port on the target system. The Agilent Technologies E5900A #510 and E5901A #510 run-control tools require firmware version v2.22 or higher and processors with ITP voltage greater than 1.5V.

CAUTION Using run control on processors with ITP voltage lower than 1.5V could damage the processor.

Capturing APIC bus signals

For capturing data on the APIC bus you need the Agilent Technologies E2467A APIC Bus Analysis Probe. The flying leads of the E2467A connect to the APIC signals on Pod 10 of the Agilent Technologies E2487C Analysis Probe.

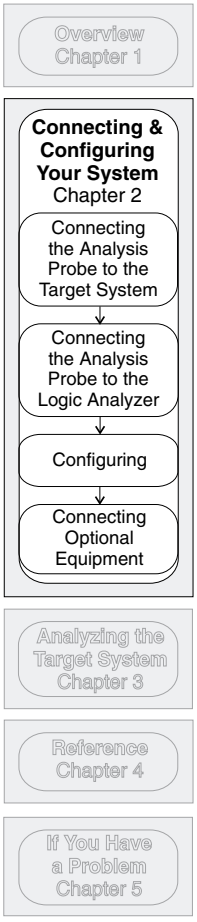
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2

Connecting and Configuring Your System

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Connecting and Configuring Your System



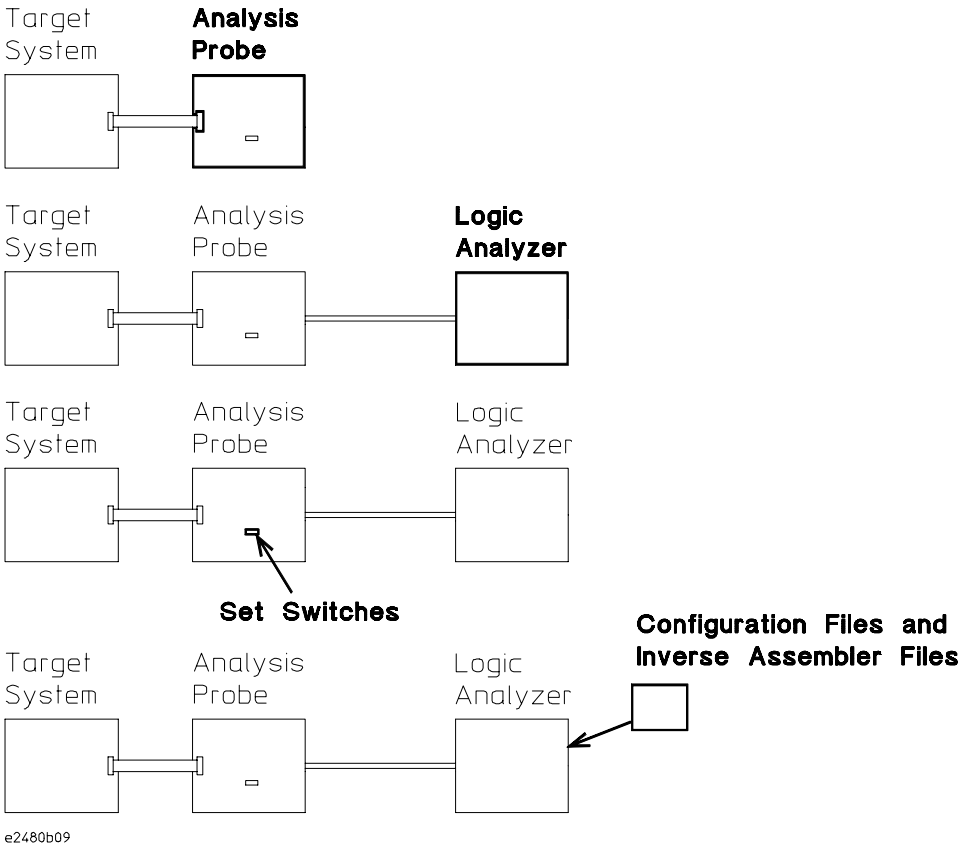
This chapter shows you how to connect the logic analyzer to the target system through the analysis probe.

Follow the instructions given on-screen in the Setup Assistant for connecting and configuring your system. Use this manual for additional information, if desired. Refer to chapter 1 for a description of Setup Assistant. This chapter is divided into the following sections; the order shown here is the recommended order for performing these tasks:

- Read the power on/power off sequence
- Connect the analysis probe to the target system
- Connect the analysis probe to the logic analyzer
- Configure the analysis probe
- Configure the logic analyzer
- Connect optional equipment

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Read the power on/power off sequence.



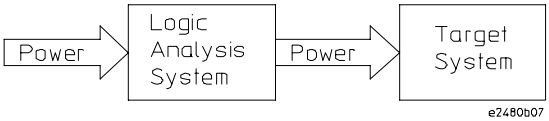
Connection Sequence

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Power-on/Power-off Sequence

Listed below are the sequences for powering on and off a fully connected system. Simply stated, your target system is always the last to be powered on, and the first to be powered off.

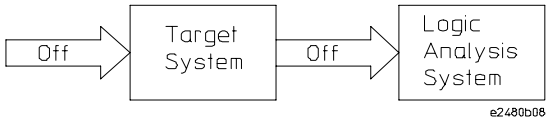
To power on Agilent Technologies 16700-series logic analysis systems



Ensure the target system is powered off.

1. Turn on the logic analyzer. The Setup Assistant will guide you through the process of connecting and configuring the analysis probe.
2. When the analysis probe is connected to the target system and logic analyzer, and everything is configured, turn on your target system.

To power off

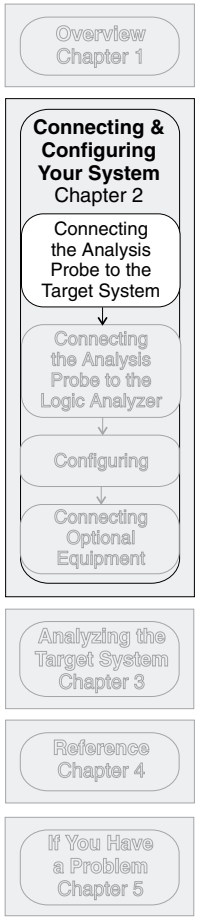


Turn off power to your system in the following order:

1. Turn off your target system.
2. Turn off your logic analysis system.

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Connecting the Analysis Probe to the Target System



This section explains how to connect the Agilent Technologies E2487C analysis probe to the target system. Connecting the analysis probe to the target system consists of the following tasks:

- Connect the probe adapter to the target system.

  Refer to the Installation Guide included with your probe adapter.
- Connect the analysis probe to the probe adapter.

The remainder of this section describes these general tasks in more detail.

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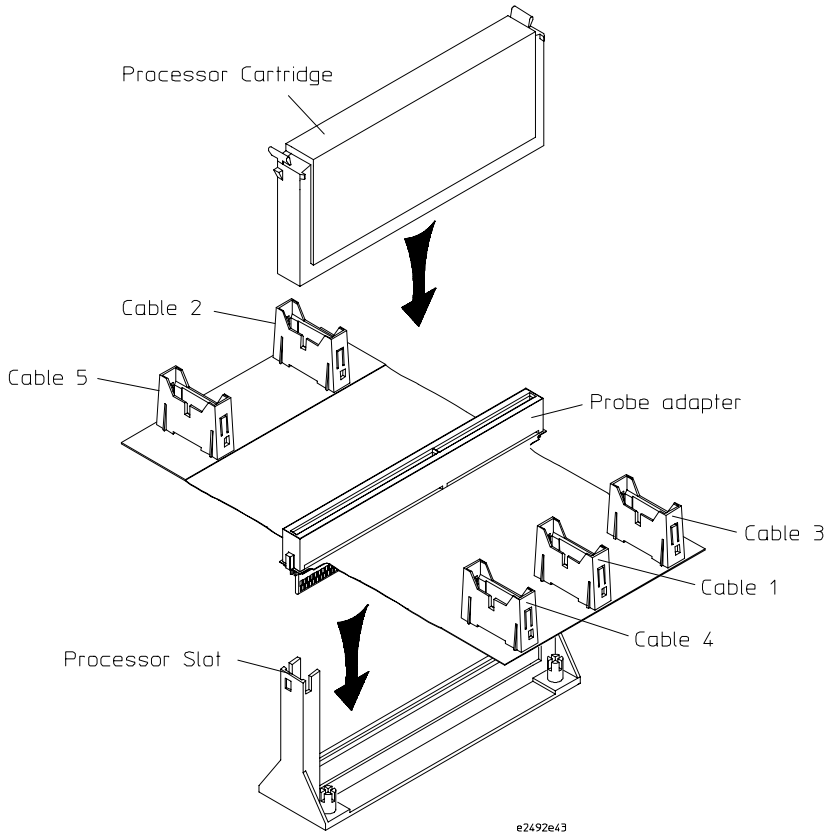
To connect the probe adapter to the target system

CAUTION

Equipment Damage. To prevent equipment damage, remove power from the target system and make sure no logic analyzer cables are connected to the analysis probe.

The probe adapter connects to the target system, and the analysis probe connects to the probe adapter.

1. To prevent equipment damage, remove power from both the logic analyzer and the target system.
2. Follow the instructions in the Installation Guide that came with your probe adapter to connect the probe adapter to the target.



Connecting Probe Adapter to the Target System

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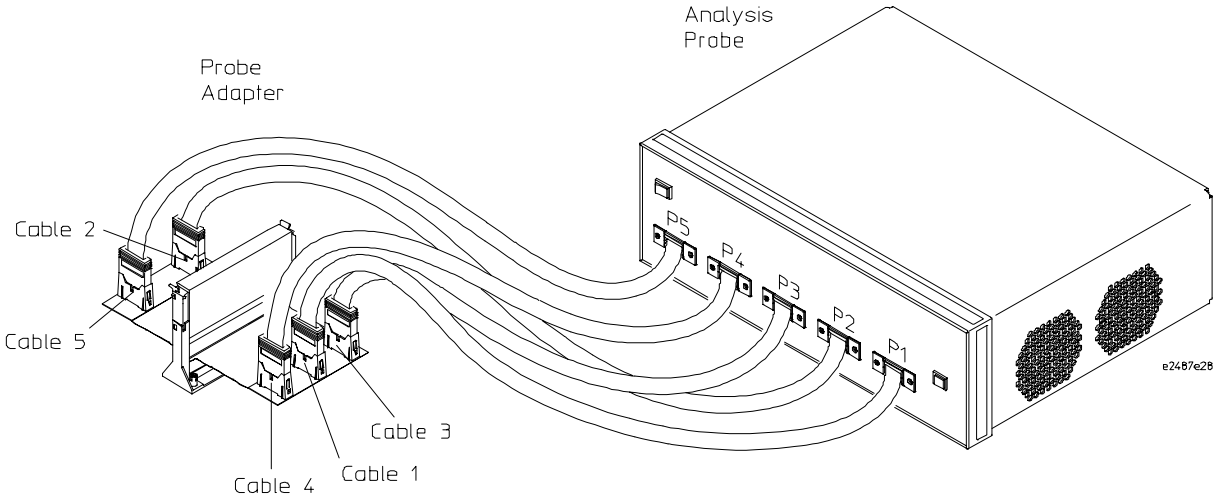
To connect the analysis probe to the probe adapter

CAUTION

Equipment Damage. To prevent equipment damage, remove power from the target system and make sure no logic analyzer cables are connected to the analysis probe.

The front of the analysis probe contains five connectors (10 pods) for connecting to the probe adapter. The illustration below shows the cables on the analysis probe hardware.

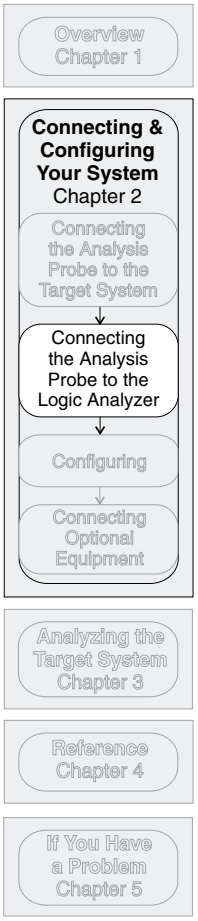
1. To prevent equipment damage, remove power from both the logic analyzer and the target system.
2. Refer to the probe adapter Installation Guide for information on connecting the probe adapter cables to the correspondingly-numbered analysis probe cables.



Connecting the Analysis Probe to the Probe Adapter

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Connecting the Analysis Probe to the Logic Analyzer



The following sections show the connections between the logic analyzer pod cables and the analysis probe cables. Use the appropriate section for your logic analyzer. The configuration file names for each logic analyzer are located at the bottom of the connection diagrams.

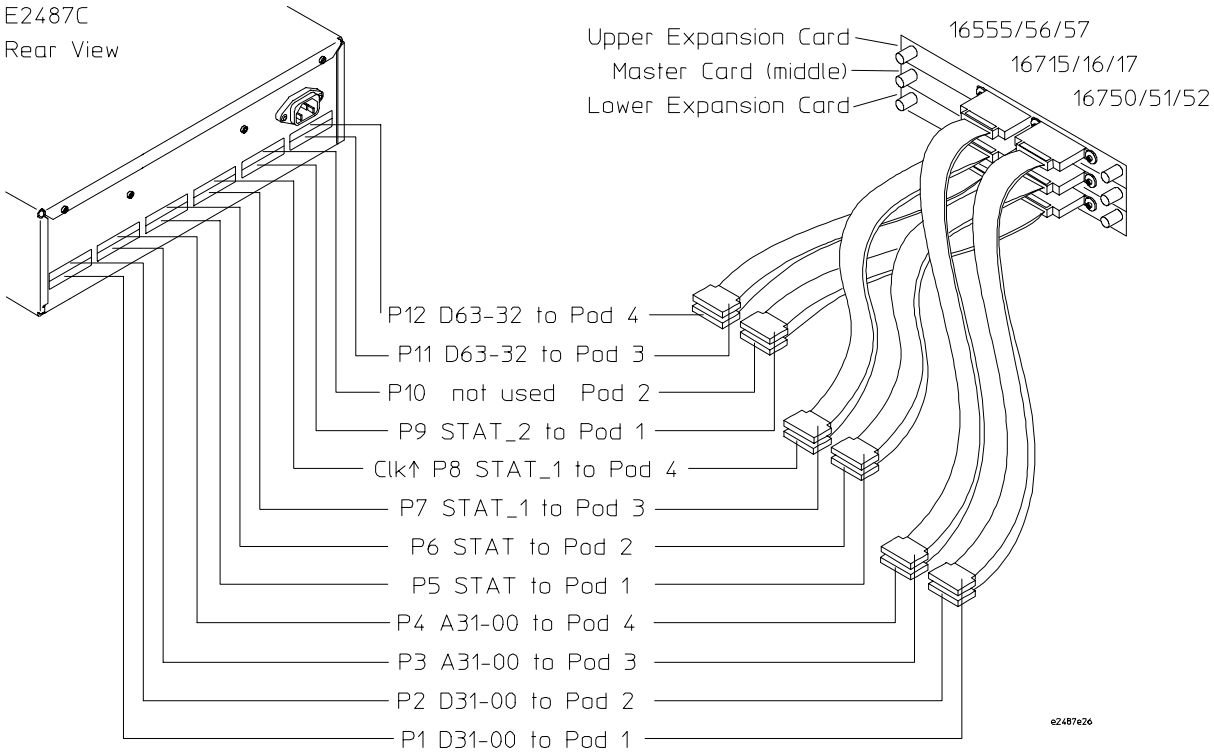
This section shows connection diagrams for connecting the analysis probe to the Agilent Technologies logic analyzers listed below:

- 16555/56/57 logic analyzers (3 or 5 cards)
- 16715/16/17 logic analyzers (3 or 5 cards)
- 16750/51/52 logic analyzers (3 or 5 cards)

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To connect to 16555/56/57, 16715/16/17, or 16750/51/52 three-card logic analyzers

Use the figure below to connect the analysis probe to the Agilent Technologies 16555/56/57, 16715/16/17, or 16750/51/52 logic analyzers.

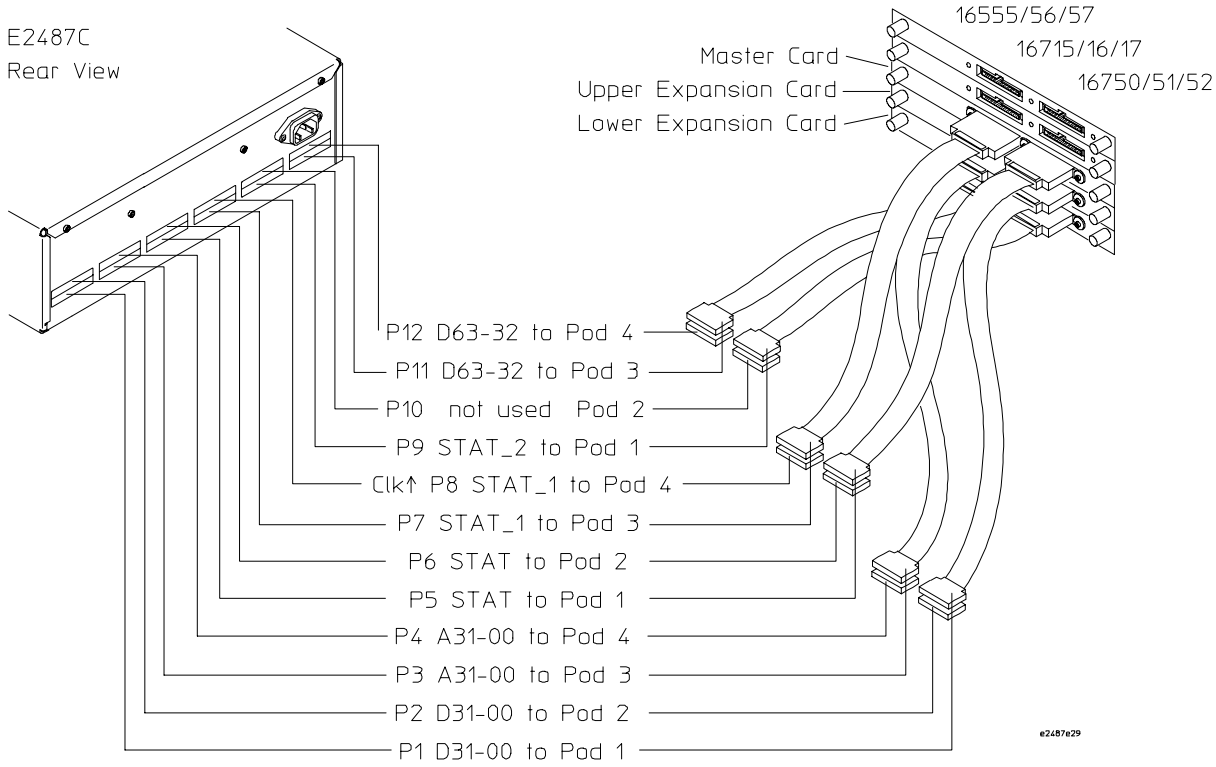


Configuration File
Use configuration file CP6K_1 for the Agilent Technologies 16555/56/57 16715/16/17, 1or 6751/51/52 logic analyzers.

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To connect to 16555/56/57, 16715/16/17, or 16750/51/52 five-card logic analyzers

Use the figure below to connect the analysis probe to the Agilent Technologies 16555/56/57, 16715/16/17, or 16750/51/52 logic analyzers.



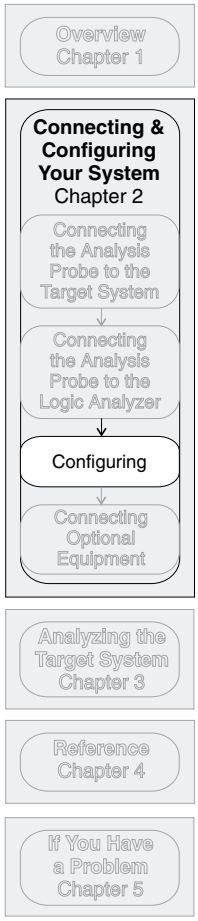
Configuration File
Use configuration file CP6K_1 for the Agilent Technologies 16555/56/57, 16715/16/17, or 16750/51/52 logic analyzers.

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Configuring

This section shows you how to configure the Agilent Technologies E2487C Analysis Probe and the logic analyzer. It consists of the following tasks:

- Configuring the analysis probe
- Configuring the logic analyzer



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Configuring the Analysis Probe

Configuring the analysis probe consists of the following:

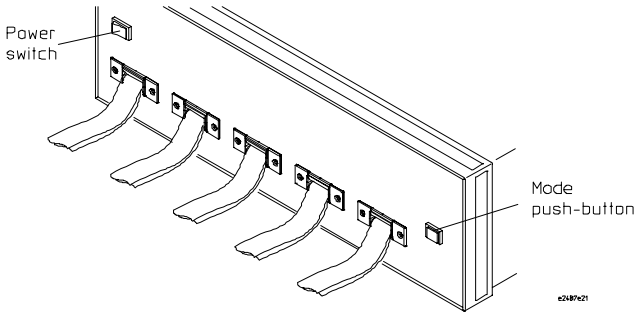
- Selecting the operating mode

To select the operating mode

The analysis probe can operate in two modes: .State-per-clock with Expanded Clock Qualifier and State-per-clock with Compacted Clock Qualifier. The mode push-button on the front panel is used to change the operating mode.

1 For State-per-clock with Exapnded Clock Qualifier (STATE/CLK EXPANDED) analysis, push the mode button in.

2 For State-per-clock with Compacted Clock Qualifier (STATE/CLK COMPACTED) analysis, push the mode button to the out position.



Mode Push-button

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Configuring the Logic Analyzer

You configure the logic analyzer by loading a configuration file. The information in the configuration file includes:

- Signal names and channel assignments for the logic analyzer
- Inverse assembler file name

The configuration file you use is determined by the logic analyzer you are using. The configuration file names are listed with the logic analyzer connection tables, and on the following page.

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To load configuration and inverse assembler files — 16700 logic analysis systems

If you did not use Setup Assistant, you can load the configuration and inverse assembler files from the logic analysis system hard disk.

1 Click on the File Manager icon. Use File Manager to ensure that the subdirectory /logic/configs/hp/pentiumII_E2487C/ exists.

> If the above directory does not exist, you need to install theIA-32 Processor Support Package. Close File Manager, then use the procedure on the CD-ROM jacket to install the IA-32 Processor Support Package before you continue.

2 Using File Manager, select the configuration file you want to load in the /logic/configs/hp/pentiumII_E2487C/ directory, then click Load. If you have more than one logic analyzer installed in your logic analysis system, use the Target field to select the machine you want to load.

The logic analyzer is configured for IA-32 analysis by loading the appropriate configuration file. Loading this file also automatically loads the inverse assembler.

3 Close File Manager.

Logic Analyzer Configuration Files

Analyzer Model	Analyzer Description	Configuration File
16752A (3 or 5 cards)	32/64 M states 400 MHz LA	CP6K_1
16751A (3 or 5 cards)	16/32 M states 400 MHz LA	CP6K_1
16750A (3 or 5 cards)	4/8 M states 400 MHz LA	CP6K_1
16717A (3 or 5 cards)	2 M states 333MHz LA	CP6K_1
16716A (3 or 5 cards)	512 k states 167 MHz LA	CP6K_1

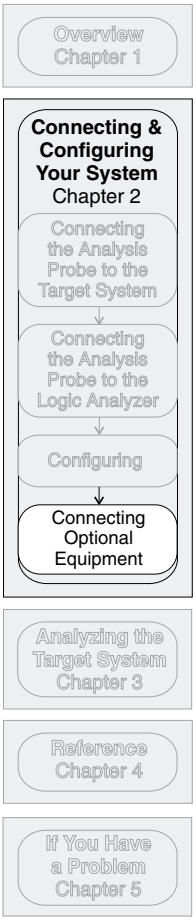
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Logic Analyzer Configuration Files (continued)

16715A (3 or 5 cards)	2M states 167 MHz LA	CP6K_1
16557D (3 card)	2M/4M states 250/500 MHz LA	CP6K_1
16556D (3 card)	2 M states 100/200 MHz LA	CP6K_1
16556A (3 card)	1 M states 100/200 MHz LA	CP6K_1
16555D (3 card)	2 M states 110/250 MHz LA	CP6K_1
16555A (3 card)	1 M states 110/250 MHz LA	CP6K_1

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Connecting Optional Equipment



The remaining portion of this chapter describes additional equipment you can use. At the time this manual was printed, the following optional equipment was available for use with the analysis probe.

- Instruction disassembly
- APIC signals

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To configure the processor for instruction disassembly

To get accurate instruction disassembly, configure your target processor to:

1. Enable Branch Trace Messages.
2. Disable instruction caches.

   An easy way to do this on processors with ITP voltage level greater than 1.5V is to use an emulator such as the Agilent Technologies E5900A #510 or E5901A #501.

To connect to the APIC signals

CAUTION

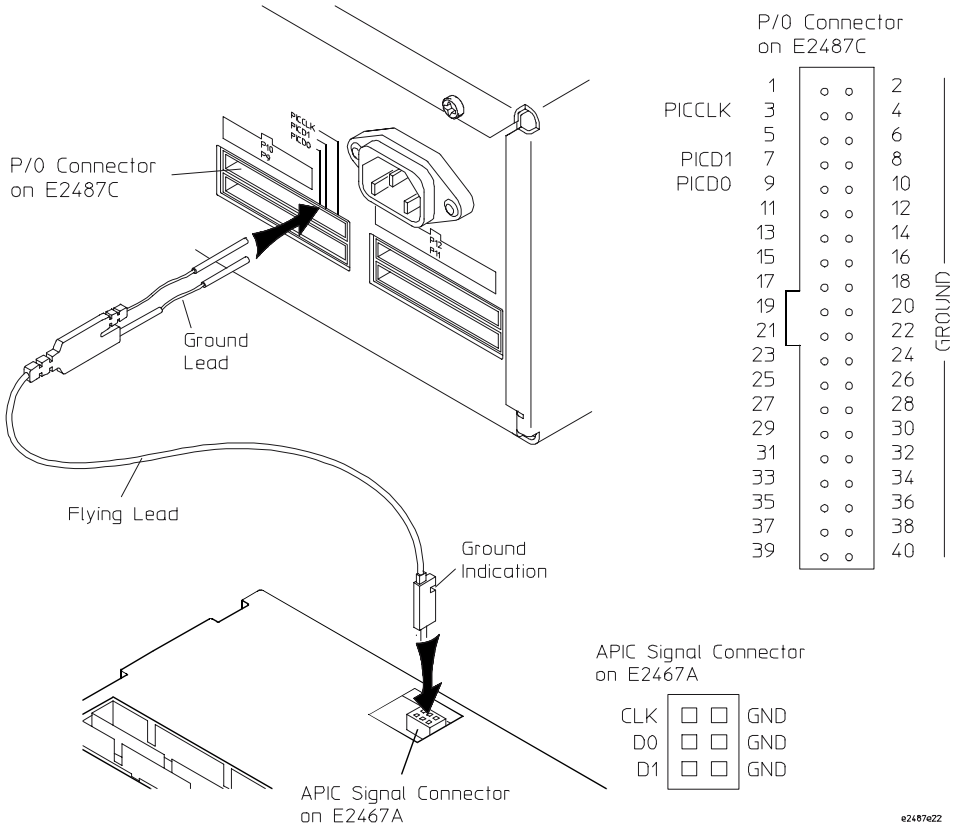
Equipment Damage. To prevent equipment damage, remove power from the target system and make sure no logic analyzer cables are connected to the analysis probe.

The APIC signals are routed to a 40-pin connector located on the back side of the Agilent Technologies E2487C analysis probe. These signals can be probed using the Agilent Technologies E2467A APIC Bus Analysis Probe.

1. To prevent equipment damage, remove power from both the logic analyzer and the target system.
2. Connect the flying leads of the Agilent Technologies E2467A to the P10 connector on the E2487C.

   The figure below shows the location of the connectors and the signal locations. These signals are buffered versions of the system bus signals; they are not latched by the bus clock.
3. Connect the ground leads of the Agilent Technologies E2467A to any of the ground pins of connector P10.

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Connecting APIC Signals

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3

Analyzing the Intel IA-32 Processor

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Analyzing the Intel IA-32 Processor

This chapter describes modes of operation for the Agilent Technologies E2487C Analysis Probe. It also describes analysis probe data, symbol encodings, and information about the inverse assemblers.

The information in this chapter is presented in the following sections:

- Displaying Information
- Using the Transaction Tracker
- Using the Inverse Assembler
- Reset Configuration Information
- Triggering Hints

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Displaying Information

This section describes how to display logic analyzer configuration information, state data captured by the analysis probe interface, and symbol information that has been set up by the analysis probe interface configuration software.

To display timing information

The Agilent Technologies E2487C does not support asynchronous timing analysis. However, you can view waveforms of timing relationships between signal transitions using the Waveform Display window. To capture these waveforms, set the operating mode to Sate-per-clock with Expanded Clock Qualifier, and turn off the clock qualifier using the Master Clock field in the Format menu.

To display the format specification

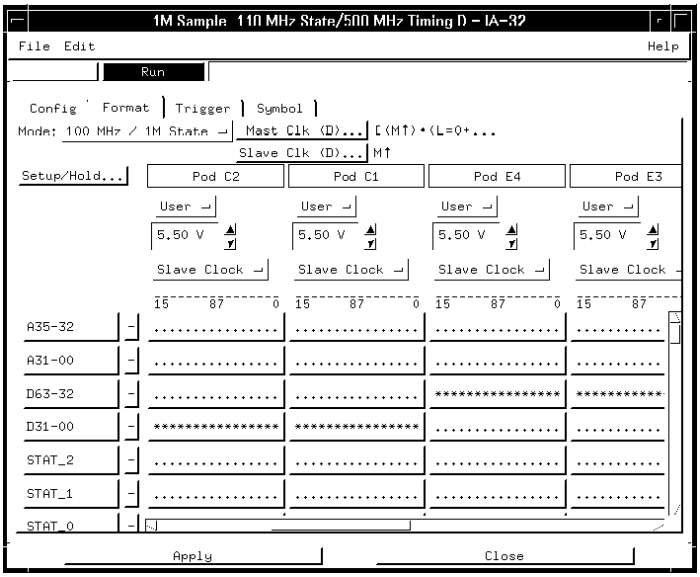
- **Using the mouse, right-click and hold on the instrument icon for the logic analyzer. In the pop-up menu, slide down to "Format...." then release the mouse button.**

  The Agilent Technologies E2487C configuration files contain predefined format specifications. These specifications include all labels for monitoring the microprocessor bus.

  Chapter 4 of this guide contains a table that lists the signals for the IA-32 processor and on which pod and probe line the signal comes to the logic analyzer. Refer to this table and to the logic analyzer connection information for your analyzer in chapter 1 to determine where the processor signals should be on the format specification screen.

  The format specification display shown in the following figure is from the Agilent Technologies 16700 logic analyzer. Additional labels and pod assignments are listed off the screen. Scroll vertically to view additional signals. Scroll horizontally to view other pot-bit assignments. There may be some slight differences in the display for your particular analyzer.

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Logic Analyzer Format Specification

To display the configuration symbols

- Using the mouse, right-click and hold on the instrument icon for the logic analyzer. In the pop-up menu, slide down to "Symbol..." then release the mouse button. Choose a label name from the "Label" list, then select "User Defined Symbols...." The logic analyzer will display the symbols associated with the label.

  The Agilent Technologies E2487C configuration software sets up symbol tables. The tables contain alphanumeric symbols which identify data patterns or ranges. Labels simplify triggering on specific IA-32 processor cycles. The label base in the symbols menu is set to hexadecimal to conserve display space.

  All IA-32 system bus signals are routed to the logic analyzer probe headers or to extra headers. Labels that begin with a lower case letter are signals that are created by the analysis probe hardware. Labels that begin with an uppercase letter and have lower case letters within them are signals that combine analysis probe generated signals and IA-32 processor signals.

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The first of the following tables describes the IA-32 processor signals that are captured by the analysis probe. The second table lists the label and symbol encodings defined by the logic analyzer configuration software.

Note

Under the heading "Polarity", negative means that the logic analyzer inverts the signal. Positive means that the logic analyzer does not invert the signal.

Signal/Label List

Label Name	Polarity	Number of bits	Description
A20M#	positive	1	Address bit 20 Mask signal
A35-32	negative	4	Address bus bits 35:32
A31-00	negative	32	Address bus bits 31:00
ADS#	positive	1	Address Strobe
AERR#	positive	1	Address Parity Error signal
AP#	positive	2	Address Parity signals
BCLK	positive	1	Bus Clock signal
BERR#	positive	1	Bus Error signal
BINIT#	positive	1	Bus Initialization signal
BNR#	positive	1	Block Next Request signal
BP3#	positive	1	Breakpoint signal
BP2#	positive	1	Breakpoint signal
BPM1#	positive	1	Breakpoint and Performance Monitor signal
BPM0#	positive	1	Breakpoint and Performance Monitor signal
BPRI#	positive	1	Priority Agent Bus Request signal
BR#	positive	4	Symmetric Agent Bus request signals
D63-32	negative	32	Data bus bits 63:32
D31-00	negative	32	Data bus bits 31:00
DBSY#	positive	1	Data Bus Busy signal
DEFER#	positive	1	Defer signal
DEP#	positive	8	Data bus ECC/Parity signals
DRDY#	positive	1	Data Ready signal
FERR#	positive	1	Floating-point Error signal
FLUSH#	positive	1	Flush signal

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Label Name	Polarity	Number of bits	Description
FRCERR	positive	1	Functional Redundancy Check Error signal
HIT#	positive	1	Snoop Hit signal
HITM#	positive	1	Snoop Hit Modified signal
IERR#	positive	1	Internal Error signal
IGNNE#	positive	1	Ignore Numeric Error signal
INIT#	positive	1	Initialization signal
INTR	positive	1	Interrupt Request signal
LINT	positive	2	Local Interrupt signals
LOCK#	positive	1	Bus Lock signal
NMI	positive	1	Non-maskable Interrupt signal
PRDY#	positive	1	Probe Ready signal
PREQ#	positive	1	Probe Request signal
RESET#	positive	1	Reset signal
RP#	positive	1	Request Parity signal
RS#	positive	3	Response Status
RSP#	positive	1	Response Parity signal
SMI#	positive	1	System Management Interrupt signal
STPCK#	positive	1	Stop Clock signal
TRDY#	positive	1	Target Ready signal

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The following table lists the transaction type symbol encodings defined by the logic analyzer configuration software for the TranTy label.

IA-32 Processor Transaction Type Symbols

Signal	Symbol
TranTy	"Branch Trace" "Code Read " "Data Read " "Defer Reply " "Int Ack/Spcl" "Invalidate " "I/O Read " "I/O Write " "Mem Write " "RSVD_1 " "RSVD_2 " "RSVD_3 " "RSVD_4 " "Writeback " "--- "

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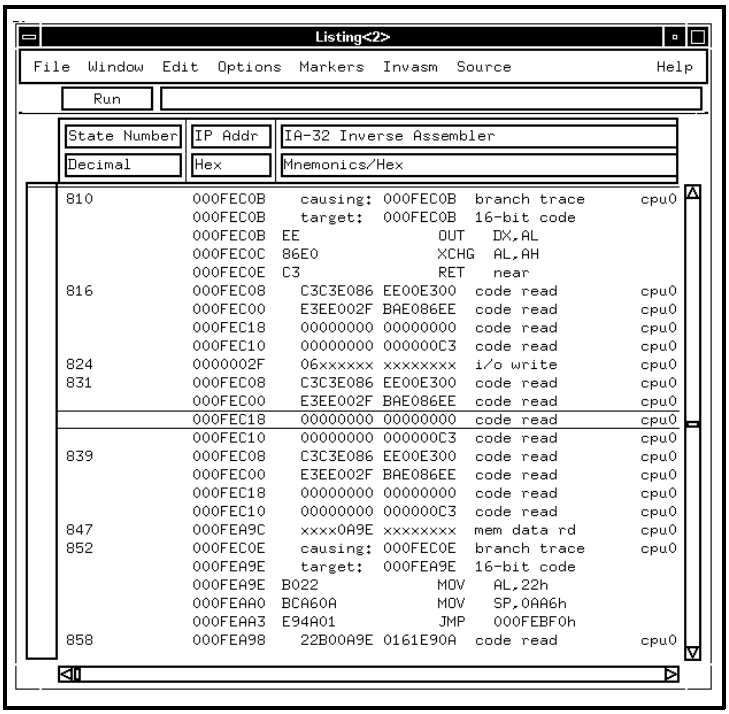
To display captured state information

The captured information is displayed in the Listing display.

- **Open the Listing display for your logic analyzer.**

  If your trace listing doesn't otherwise appear to be correct, make sure the logic analyzer is configured for state analysis and correctly connected. See Chapter 2 to review the logic analyzer connections, correct it if needed, and then run the trace again.

  The figure below shows the Listing display for the Agilent Technologies 16700 logic analyzer.



Logic Analyzer Listing Display

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Using the Transaction Tracker

This section discusses the general output format of the transaction tracker, and any processor-specific information you will need.

The transaction tracker supports many filter options based on type of states (start of a transaction, all of a transaction), transaction types, and transaction-agent ownership. The next few paragraphs describe the general output format of the transaction tracker.

Data Format

The transaction tracker processes the captured data in a transaction-based format.

Numeric Format

For the data bus values, the numeric output from the transaction tracker is in hexadecimal format. All other numbers are in decimal format.

Filter options

The transaction tracker supports many filter options based on phases (start of a transaction, all of a transaction), transaction types, and transaction ownership. The following is a list of the filter options available.

Filterable State	**Options**
Show Phases	
Request Phase A:	Show/Suppress
All Phases:	Show/Suppress
Agents	
CPU 0:	Show/Suppress
CPU 1:	Show/Suppress
CPU 2:	Show/Suppress
CPU 3:	Show/Suppress
Priority:	Show/Suppress

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Filterable State	Options
Show Transactions:	
Code Reads:	Show/Suppress
Memory Data Reads:	Show/Suppress
Mem Read & Invalidate:	Show/Suppress
Memory Writes:	Show/Suppress
Memory Writebacks:	Show/Suppress
I/O Reads:	Show/Suppress
I/O Writes:	Show/Suppress
Deferred Replies:	Show/Suppress
Interrupt Acknowledges:	Show/Suppress
Special Transactions:	Show/Suppress
Branch Trace Messages:	Show/Suppress

Show/Suppress

The Suppress/Show settings determine whether the various microprocessor operations are shown or suppressed on the logic analyzer display. The preceding section shows the microprocessor operations which have this option. The settings for the various operations do not affect the data which is stored by the logic analyzer, they only affect whether that data is displayed or not. The same data can be examined with different settings, for different analysis requirements.

This function gives you a better analysis display in two ways. First, unneeded information can be filtered out of the display. Second, particular operations can be isolated by suppressing all other operations. For example, I/O accesses can be shown, with all other operations suppressed, allowing quick analysis of I/O accesses.

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Transaction tracker messages

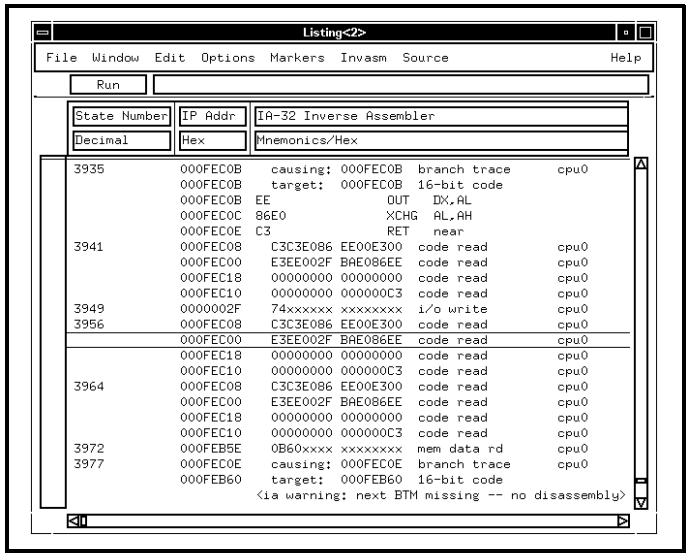
Any of the following messages may appear during analysis of your target software. Included with each message is a brief explanation.

Errors and warnings

The Agilent Technologies E2487C software contains error messages and warnings for both the transaction tracker and the inverse assembler. For a list and description of the messages, refer toChapter 5.

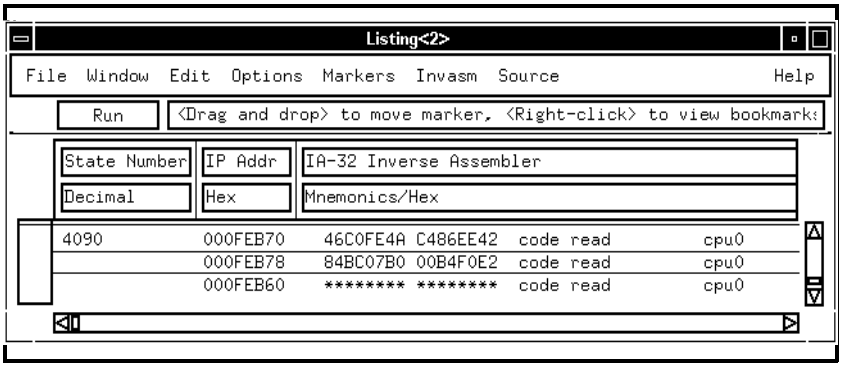
Reaching boundaries

If the transaction tracker internal search limit (8192 states per transaction) is exceeded, or if part of a transaction is not acquired at the end of the analyzer acquisition memory, error messages may be displayed. The figure below shows a warning message. On the next page, the figure shows the end of a boundary.



Listing Display with Boundary Error Message

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Listing Menu Showing End of Boundary

Protocol Violations

The transaction tracker displays a bus protocol violation when the maximum allowable outstanding transactions have been exceeded.

Protocol violations are followed with line:

"*** protocol violation detected ***"

The transaction tracker does not attempt to do a complete job of detecting protocol violations. Undetected protocol violations may cause the transaction tracker to display incorrect results.

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In addition to basic transaction tracking, the Agilent Technologies 16700 can display an accurate instruction execution trace of IA-32 processor target systems containing up to four processors. Instruction disassembly supports Intel's MMX technology. Disassembly requires the use of a separate run-control tool such as the Agilent Technologies E5900A #510 or E5901A #510 to disable all CPU caches and enable Branch Trace Message transactions.

Analysis features are determined by a combination of analysis probe operating mode settings and options selected in the Agilent Technologies 16700 Listing window under the "Invasm - Filter..." and "Invasm - Preferences..." menu pull-downs. The Filter dialog allows the user to show, suppress, or change the color of an entire acquisition state, whereas the Preferences dialog controls the display format for a state which is shown.

Disassembly is only possible when "Display Disassembly" is selected in the Preferences dialog and "Branch Trace Messages" are selected in the Filter dialog. Additionally, a run-control tool should be used to enable Branch Trace Messages and disable the instruction caches for all processors.

Operating mode

The inverse assembler software requires that the operating mode on the analysis probe hardware is set to one of the modes listed below.

- State-per-clock Mode with Expanded Clock Qualifier
- State-per-clock Mode with Compacted Clock Qualifier

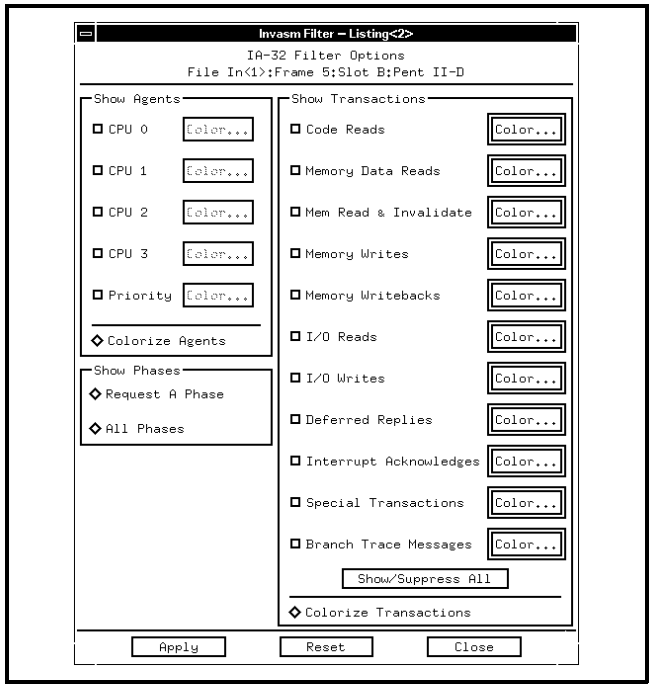
Refer to Chapter 1 for the mode selection procedure.

See Chapter 5 for a complete list of error messages.

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IA-32 filter dialog

Filter options are accessed from the Listing menu bar by clicking on Invasm and selecting Filter. The Filter dialog provides the ability to display only information for particular bus agents and/or transaction types. Colorization can be used to identify either transactions or processors. Show Phases allows you to show only the Request A Phase, which contains a summary of the entire transaction, or All Phases, which includes all captured states pertaining to each transaction. The figure below shows a sample Filter dialog.



Agilent Technologies 16700 IA-32 Filter Dialog

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IA-32 preferences dialog

Preferences options are accessed from the Listing menu bar by clicking on Invasm and selecting Preferences. The Preferences dialog controls the level of detail for states shown. The figure on the following page shows the Preferences dialog.

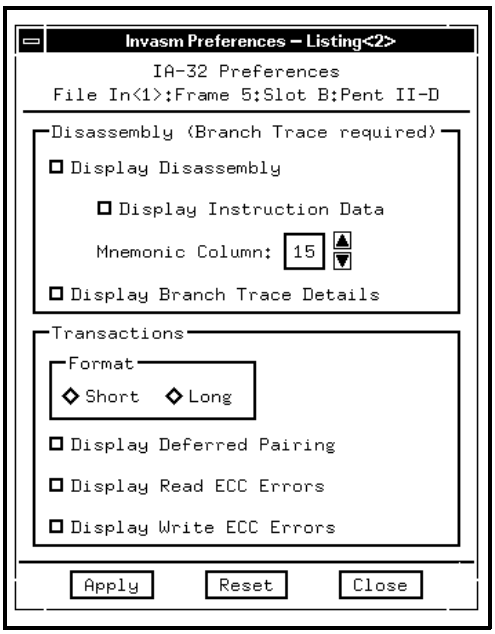
Disassembly

When "Display Disassembly" is selected, a block of instructions appears in the Listing window under each Branch Trace Message transaction or Memory Code Read from the reset vector (the instruction cache(s) must be disabled). "Display Instruction Data" turns on/off the display of data bytes corresponding to each instruction. "Display Branch Trace Details" shows the causing and target linear addresses contained in each Branch Trace Message transaction, along with the default address/operand size.

Transactions

The transaction Format can be set to "Short" to display one line per transaction data chunk (DRDY# asserted state), or "Long" for more extensive information about the phases. "Display Deferred Pairing" consolidates the deferred reply transaction information directly beneath the original deferred transaction. "Display Read/Write ECC Errors" examines the D[63:00]# and DEP[7:0]# signals during DRDY# asserted states and displays detected errors not on the data phase, but on the Request phase which started the transaction. Bad bits are identified for single-bit correctable errors. These ECC options should only be selected when data bus error-checking is enabled on the target system. While CPU agents usually drive DEP[7:0]#, non-CPU agents may or may not, so exercise judgment when turning on "Display Read ECC Errors".

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Agilent Technologies 16700 IA-32 Preferences Dialog

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Analysis techniques

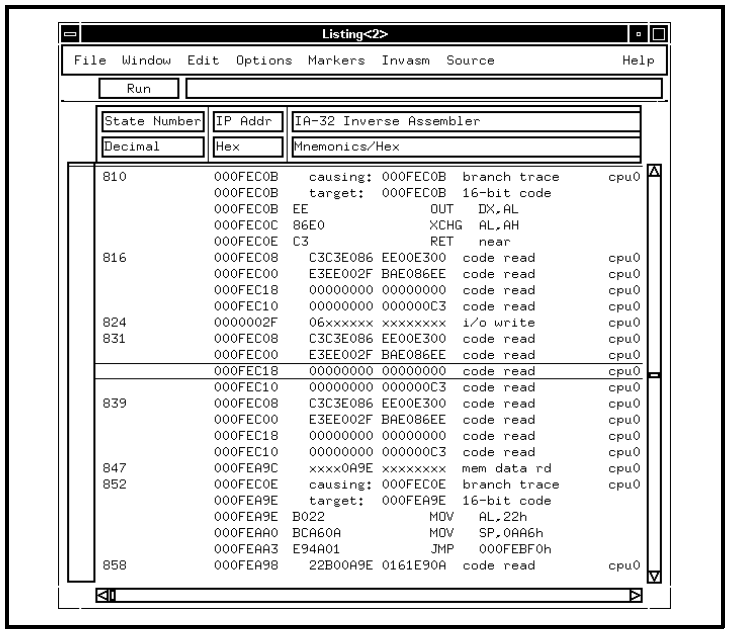
Suggested Settings

For software analysis, the settings below give a high-level view of the captured data. Remember to disable the processor instruction caches and enable Branch Trace Messages in order to get disassembly.

Operating Mode: State/Clock with Compacted Clock Qualifier.

Filter:	Show Agents	-- Show All
	Show Transactions	-- Show All
	Show Phases	-- Request A Phase

Preferences:	Display Disassembly	-- ON
	Display Branch Trace Details	-- ON
	Transaction Format	-- SHORT
	Display Deferred Pairing	-- ON
	Display Read ECC Errors	-- OFF
	Display Write ECC Errors	-- ON



Agilent Technologies 16700 Listing Window for Software Analysis

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For hardware analysis, the State Waveform display provides the most relevant details. If this display does not provide the level of detail required for your analysis needs, you might need the restricted version of the Agilent Technologies E2487C. Contact your Agilent Technologies Sales Office for information on obtaining the appropriate Intel non-disclosure forms for the restricted version.

Disassembler Behavior

To display instruction disassembly, use an IA-32 processor run-control tool such as the Agilent Technologies E5900A #510 or E5901A #510 to enable Branch Trace Messages and disable the processor instruction caches. Show "Branch Trace Messages" in the Filter dialog, and select "Display Disassembly" in the Preferences dialog.

When a processor executes a branching instruction, the prefetch queues are flushed, a Branch Trace Message (BTM) appears on the bus, and the processor begins fetching code at the branch target address. The disassembly software finds matching code reads between the current BTM and the next matching BTM, reorders any out-of-order bursts, then disassembles the code read data. In searching for code reads, any fetches which are deferred are automatically paired with their corresponding deferred replies to ensure that all code read data is found. This pairing is not affected by the "Display Deferred Pairing" setting in the Preferences dialog.

Physical vs. Linear Addresses

Branch Trace Messages give linear causing and target addresses. The addresses displayed for Memory Code Read transactions in the "IP Addr" column are physical. For real-mode programs, these linear and physical addresses are equivalent. For protected-mode programs with paging enabled, the address bits higher than A[11] will usually be different.

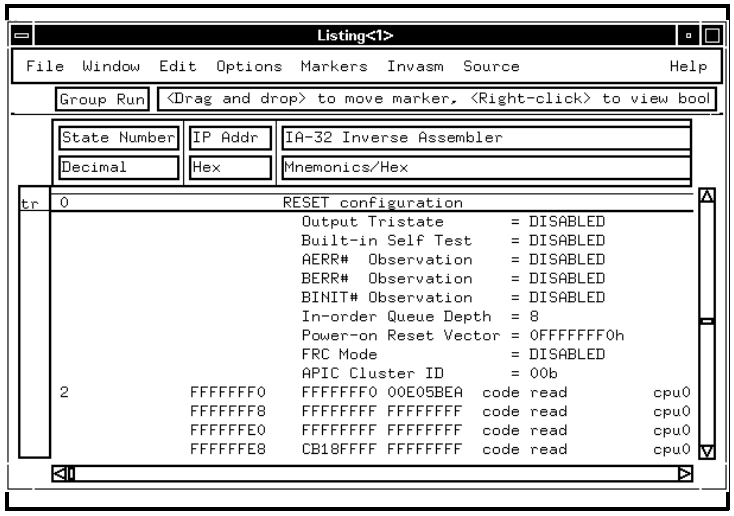
For disassembled instructions, linear addresses are shown in the "IP Addr" column of the Listing window.

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The following table describes the reset configuration information that is displayed at reset.

Reset Configuration

Signal at Reset	Configuration (asserted/deasserted)
FLUSH#	Output Tristate Enabled/Disabled
INIT#	Built-in Self Test Enabled/Disabled
A8#	AERR# Observation Policy Enabled/Disabled
A9#	BERR# Observation Policy Enabled/Disabled
A10#	BINIT# Observation Policy Enabled/Disabled
A7#	In-order Queue depth = 1/8
A6#	Power-on Reset Vector = 000FFFF0 or FFFFFFF0 hex
A5#	FRC Mode Enabled/Disabled
A[12:11]#	APIC Cluster ID (00, 01, 10, 11)



Reset Configuration

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Triggering Hints

Storage qualification

Clock qualification is a form of storage qualification. You can turn the clock qualifier off and capture all bus clocks; however, you should not attempt any other storage qualification using the trigger sequence, as that might result in error messages in the inverse assembly column in the Listing.

Triggering on address and transaction type

To trigger on a specific address and transaction type, use the A35-32, A31-00, and TranTy labels, together with the TranTy label symbols. The symbols identify each transaction type uniquely, except for Interrupt Acknowledge and Special Transactions, which are combined into one symbol.

Triggering on data and transaction type

There is no guaranteed method of triggering on a particular transaction type or address ANDed with a particular data value in a target system with overlapping transactions. Although the Listing displays a transaction type and 8-byte data value on the same line when Transaction Display Mode is set to Short, this alignment is the result of post-processing and cannot be used for triggering. The analysis probe hardware captures this information on different states. A trigger specification could be defined to find a certain transaction type in the Request A phase, then trigger on a data value qualified by DRDY# asserted; however, by the time the data pattern is found, it could belong to a different transaction.

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4

Reference

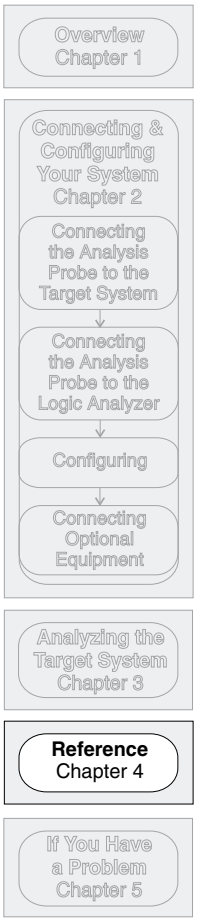
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Reference

This chapter contains additional reference information including the signal mapping for the Agilent Technologies E2487C analysis probe.

The information in this chapter is presented in the following sections:

- Operating characteristics
- Theory of operation and clocking
- Signal-to-connector mapping
- Circuit board dimensions
- Replaceable parts



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Operating characteristics

The following operating characteristics are not specifications, but are typical operating characteristics for the analysis probe.

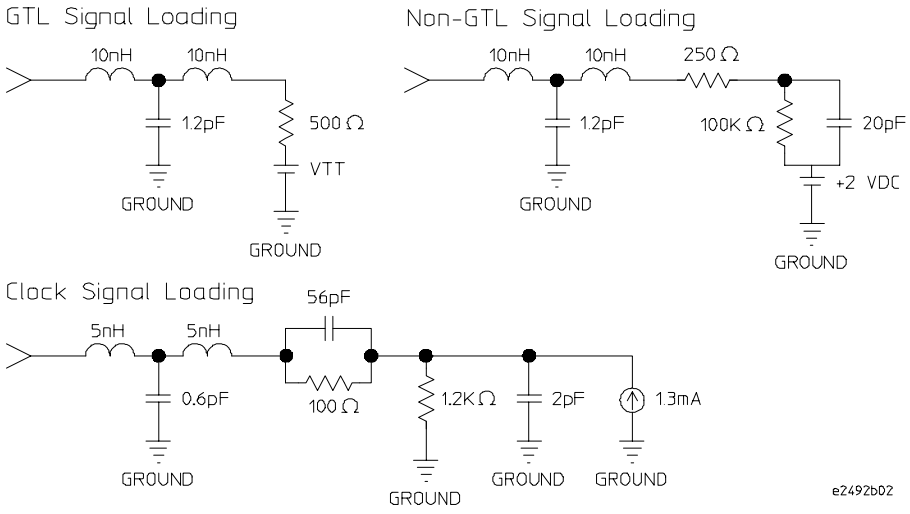
Operating Characteristics

Microprocessor Compatibility	Intel IA-32 microprocessors which use the Pentium Pro bus protocol, such as the Pentium II® processor and Pentium III® processor
Microprocessor Package	Pentium II-III® Slot 1, Pentium II-III® Xeon ™ Slot 2, Celeron® Slot 1, Celeron® PPGA, and Pentium III® FC-PGA Call Agilent Technologies for other processors/packages supported.
Clock Frequency	133 MHz maximum for external BCLK
Target Signal Amplitude	800 mV p-p minimum for all GTL+ signals
Logic Analyzers Supported	16715/16/17A (3 card) 16750/51/52A (3 card) 16557D (three card) 16556A/D (three card) 16555A/D (three card)
Accessories Required	Agilent Technologies E2492B, E2492C, or E2492E probe adapter. Call Agilent Technologies for ordering information.
Power Requirements	115/230 Vac, 200W Power supply is built into the analysis probe. CAT II, Pollution degree 2.
Pods Required	Eleven logic analyzer pods (180 channels) are required.
Signal Line Loading	Varies depending on probe adapter. The illustration on the following page shows signal line loading when the E2492B/C is used.
Environmental Temperature	Operating: 10 to 40 degrees C Nonoperating: -40 to +70 degrees C
Altitude	Operating: 4,600 m (15,000 ft) Nonoperating: 15,300 m (50,000 ft)
Humidity	Up to 80% noncondensing. Avoid sudden, extreme temperature changes which could cause condensation within the instrument.

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Signal Line Loading

The following schematics show the signal line loading for GTL, non GTL, and Clock. This loading model applies only when the Agilent Technologies E2487C is connected to the target using the Agilent Technologies E2492B/C.



Theory of operation and clocking

The analysis probe operates only in State-per-clock mode. The logic analyzer master clock is normally qualified with the "cqual#" signal from the analysis probe. This clock qualifier is set to either Compacted or Expanded. By eliminating idle clocks, the Compacted qualifier can potentially capture many more transactions than the Expanded qualifier. Refer to chapter 1 for information on configuring the analysis probe and logic analyzer for the desired mode of operation.

The analysis probe uses the BCLK rising edge to capture the signals from the IA-32 processor bus and to clock the logic analyzer. The PLDs in the analysis probe generate additional information about each clock. The PLD information along with the bus signals are sent to the logic analyzer and used by the transaction tracker and inverse assembler to produce the transaction display (see Block Diagram).

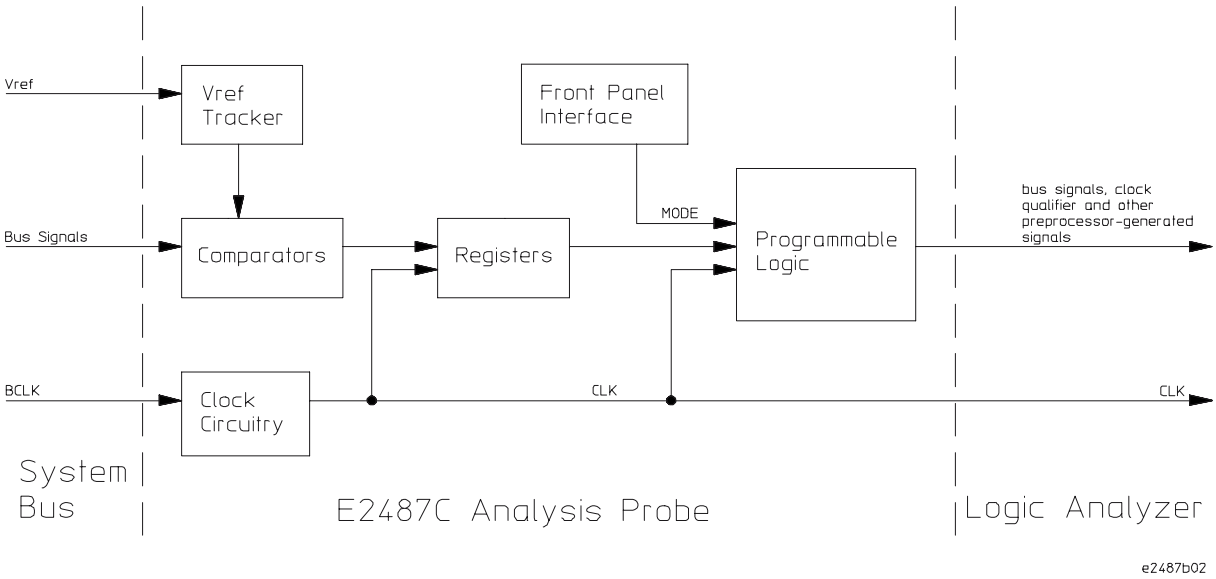
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IA-32 processor signals require a multi-clock latency to move the information from the processor pins to the logic analyzer memory. The first clock is used to capture all of the bus signals in latches on the analysis probe. Subsequent clocks move the bus signals through the PLDs and into the logic analyzer.

> The analysis probe captures but does not display the REQ[4:0]# bus signal group.

Clocking

The logic analyzer uses the master clock specification [(M↑) • (K = 0 or L=0)] to capture all pod data. Connector P8 carries BCLK (M ↑), which clocks the logic analyzer. Connectors P5 and P6 carry the "cqual1#" (J = 0) and "cqual2#" (K = 0) signals from the PLD, which is used to qualify the master clock to eliminate the acquisition of unnecessary data. The qualifier is highly recommended, but not required.



Block Diagram

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Signal-to-connector mapping

The following table describes the electrical interconnections implemented with the Agilent Technologies E2487C Analysis Probe. Since the pods on the logic analyzers are numbered differently than the analysis probe connectors, refer to the connection table in chapter 1 to correlate the pod numbers.

The signal list table column descriptions are as follows:

ANALYSIS PROBE CONNECTOR	NAME	The analysis probe connector that carries the signal.
	PIN	The pin within the analysis probe connector that carries the signal.
	BIT	The bit position of the signal within the analysis probe connector.
CPU	SIGNAL	The microprocessor signal name.
ANALYZER	LABEL(S)	The analyzer label assigned to the signal. Lower case letters indicate a analysis probe-generated signal.

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IA-32 Signal List

ANALYSIS PROBE CONNECTOR			CPU	ANALYZER
NAME	PIN	BIT	SIGNAL	LABEL(S)
P1	3	CLK1		
P1	7	D15	D15#	D31-00
P1	9	D14	D14#	D31-00
P1	11	D13	D13#	D31-00
P1	13	D12	D12#	D31-00
P1	15	D11	D11#	D31-00
P1	17	D10	D10#	D31-00
P1	19	D9	D09#	D31-00
P1	21	D8	D08#	D31-00
P1	23	D7	D07#	D31-00
P1	25	D6	D06#	D31-00
P1	27	D5	D05#	D31-00
P1	29	D4	D04#	D31-00
P1	31	D3	D03#	D31-00
P1	33	D2	D02#	D31-00
P1	35	D1	D01#	D31-00
P1	37	D0	D00#	D31-00

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IA-32 Signal List (Cont.)

ANALYSIS PROBE CONNECTOR			CPU	ANALYZER
NAME	PIN	BIT	SIGNAL	LABEL(S)
P2	3	CLK1		
P2	7	D15	D31#	D31-00
P2	9	D14	D30#	D31-00
P2	11	D13	D29#	D31-00
P2	13	D12	D28#	D31-00
P2	15	D11	D27#	D31-00
P2	17	D10	D26#	D31-00
P2	19	D9	D25#	D31-00
P2	21	D8	D24#	D31-00
P2	23	D7	D23#	D31-00
P2	25	D6	D22#	D31-00
P2	27	D5	D21#	D31-00
P2	29	D4	D20#	D31-00
P2	31	D3	D19#	D31-00
P2	33	D2	D18#	D31-00
P2	35	D1	D17#	D31-00
P2	37	D0	D16#	D31-00

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IA-32 Signal List (Cont.)

ANALYSIS PROBE CONNECTOR			CPU	ANALYZER
NAME	PIN	BIT	SIGNAL	LABEL(S)
P3	3	CLK1	AP1#	AP1#
P3	7	D15	A15#, BE7#	A31-00, BE#
P3	9	D14	A14#, BE6#	A31-00, BE#
P3	11	D13	A13#, BE5#	A31-00, BE#
P3	13	D12	A12#, BE4#	A31-00, BE#
P3	15	D11	A11#, BE3#	A31-00, BE#
P3	17	D10	A10#, BE2#	A31-00, BE#
P3	19	D9	A9#, BE1#	A31-00, BE#
P3	21	D8	A8#, BE0#	A31-00, BE#
P3	23	D7	A7#, EXF4#	A31-00, EXF#
P3	25	D6	A6#, EXF3#	A31-00, EXF#
P3	27	D5	A5#, EXF2#	A31-00, EXF#
P3	29	D4	A4#, EXF1#	A31-00, EXF#
P3	31	D3	A3#, EXF0#	A31-00, EXF#
P3	33	D2	A2#	A2#
P3	35	D1	A1#	A1#
P3	37	D0	A0#	A0#

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IA-32 Signal List (Cont.)

ANALYSIS PROBE CONNECTOR			CPU	ANALYZER
NAME	PIN	BIT	SIGNAL	LABEL(S)
P4	3	CLK1	AP0#	AP0#
P4	7	D15	A31#, ATTR7#	A31-00, ATTR#
P4	9	D14	A30#, ATTR6#	A31-00, ATTR#
P4	11	D13	A29#, ATTR5#	A31-00, ATTR#
P4	13	D12	A28#, ATTR4#	A31-00, ATTR#
P4	15	D11	A27#, ATTR3#	A31-00, ATTR#
P4	17	D10	A26#, ATTR2#	A31-00, ATTR#
P4	19	D9	A25#, ATTR1#	A31-00, ATTR#
P4	21	D8	A24#, ATTR0#	A31-00, ATTR#
P4	23	D7	A23#, DID7#	A31-00, DID#
P4	25	D6	A22#, DID6#	A31-00, DID#
P4	27	D5	A21#, DID5#	A31-00, DID#
P4	29	D4	A20#, DID4#	A31-00, DID#
P4	31	D3	A19#, DID3#	A31-00, DID#
P4	33	D2	A18#, DID2#	A31-00, DID#
P4	35	D1	A17#, DID1#	A31-00, DID#
P4	37	D0	A16#, DID1#	A31-00, DID#

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IA-32 Signal List (Cont.)

ANALYSIS PROBE CONNECTOR			CPU	ANALYZER
NAME	PIN	BIT	SIGNAL	LABEL(S)
P5	3	CLK1	RP#	RP#
P5	7	D15	RESET#	RESET#
P5	9	D14	BINIT#	BINIT#
P5	11	D13	RSP#	RSP#
P5	13	D12	RS2#	RS#
P5	15	D11	RS1#	RS#
P5	17	D10	RS0#	RS#
P5	19	D9		
P5	21	D8	REQ4#	REQ#
P5	23	D7	REQ3#	REQ#
P5	25	D6	REQ2#	REQ#
P5	27	D5	REQ1#	REQ#
P5	29	D4	REQ0#	REQ#
P5	31	D3	A35#	A35-A32
P5	33	D2	A34#	A35-A32
P5	35	D1	A33#	A35-A32
P5	37	D0	A32#	A35-A32

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IA-32 Signal List (Cont.)

ANALYSIS PROBE CONNECTOR			CPU	ANALYZER
NAME	PIN	BIT	SIGNAL	LABEL(S)
P6	3	CLK1	cQual2	cQual2
P6	7	D15	BPRI#	BPRI
P6	9	D14	BR3#	BR#
P6	11	D13	BR2#	BR#
P6	13	D12	BR1#	BR#
P6	15	D11	BR0#	BR#
P6	17	D10	BNR#	BNR#
P6	19	D9	AERR#	AERR#
P6	21	D8	BERR#	BERR#
P6	23	D7	TRDY#	TRDY#
P6	25	D6	DRDY#	DRDY#
P6	27	D5	DBSY#	DBSY#
P6	29	D4	ADS#	ADS#
P6	31	D3	DEFER#	DEFER#
P6	33	D2	HIT#	HIT#
P6	35	D1	HITM#	HITM#
P6	37	D0		

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IA-32 Signal List (Cont.)

ANALYSIS PROBE CONNECTOR			CPU	ANALYZER
NAME	PIN	BIT	SIGNAL	LABEL(S)
P7	3	CLK1	cQual1	cQual1
P7	7	D15	IGNNE#	IGNNE#
P7	9	D14	A20M#	A20M#
P7	11	D13	STPCLK#	STPCLK#
P7	13	D12	SMI#	SMI#
P7	15	D11	LINT1, INTR	LINT1, INTR
P7	17	D10	LINT0, NMI	LINT0, NMI
P7	19	D9	SLP	SLP
P7	21	D8	FRCERR#	FRCERR#
P7	23	D7	FLUSH#	FLUSH#
P7	25	D6	INIT#	INIT#
P7	27	D5	PREQ#	PREQ#
P7	29	D4	PRDY#	PRDY#
P7	31	D3	BP3#	BP3#
P7	33	D2	BP2#	BP2#
P7	35	D1	BPM1#	BPM1#
P7	37	D0	BPM0#	BPM0#

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IA-32 Signal List (Cont.)

ANALYSIS PROBE CONNECTOR			CPU	ANALYZER
NAME	PIN	BIT	SIGNAL	LABEL(S)
P8	3	CLK1	BCLK	BCLK
P8	7	D15		
P8	9	D14	ppmode	ppmode
P8	11	D13	*	
P8	13	D12		
P8	15	D11		
P8	17	D10	*	
P8	19	D9	*	
P8	21	D8	*	
P8	23	D7	*	
P8	25	D6	*	
P8	27	D5	*	
P8	29	D4	*	
P8	31	D3	*	
P8	33	D2	*	
P8	35	D1	*	
P8	37	D0	*	

* These signals are generated by the analysis probe.

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IA-32 Signal List (Cont.)

ANALYSIS PROBE CONNECTOR			CPU	ANALYZER
NAME	PIN	BIT	SIGNAL	LABEL(S)
P9	3	CLK1	PWR-GOOD	PWR-GOOD
P9	7	D15	LOCK	LOCK
P9	9	D14	TCK	TCK
P9	11	D13	TDI	TDI
P9	13	D12	TDO	TDO
P9	15	D11	TMS	TMS
P9	17	D10	TRST#	TRST#
P9	19	D9	IERR#	IERR#
P9	21	D8	FERR#	FERR#
P9	23	D7	DEP7#	DEP#
P9	25	D6	DEP6#	DEP#
P9	27	D5	DEP5#	DEP#
P9	29	D4	DEP4#	DEP#
P9	31	D3	DEP3#	DEP#
P9	33	D2	DEP2#	DEP#
P9	35	D1	DEP1#	DEP#
P9	37	D0	DEP0#	DEP#

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IA-32 Signal List (Cont.)

ANALYSIS PROBE CONNECTOR			APIC
NAME	PIN	BIT	SIGNAL
P10	3	CLK1	PICCKL
P10	7	D15	PICD1
P10	9	D14	PICD0
P10	11	D13	
P10	13	D12	
P10	15	D11	
P10	17	D10	
P10	19	D9	
P10	21	D8	
P10	23	D7	
P10	25	D6	
P10	27	D5	
P10	29	D4	
P10	31	D3	
P10	33	D2	
P10	35	D1	
P10	37	D0	

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IA-32 Signal List (Cont.)

PREPROCESSOR CONNECTOR			CPU	ANALYZER
NAME	PIN	BIT	SIGNAL	LABEL(S)
P11	3	CLK1	FANFAIL	FANFAIL
P11	7	D15	D47#	D63-32
P11	9	D14	D46#	D63-32
P11	11	D13	D45#	D63-32
P11	13	D12	D44#	D63-32
P11	15	D11	D43#	D63-32
P11	17	D10	D42#	D63-32
P11	19	D9	D41#	D63-32
P11	21	D8	D40#	D63-32
P11	23	D7	D39#	D63-32
P11	25	D6	D38#	D63-32
P11	27	D5	D37#	D63-32
P11	29	D4	D36#	D63-32
P11	31	D3	D35#	D63-32
P11	33	D2	D34#	D63-32
P11	35	D1	D33#	D63-32
P11	37	D0	D32#	D63-32

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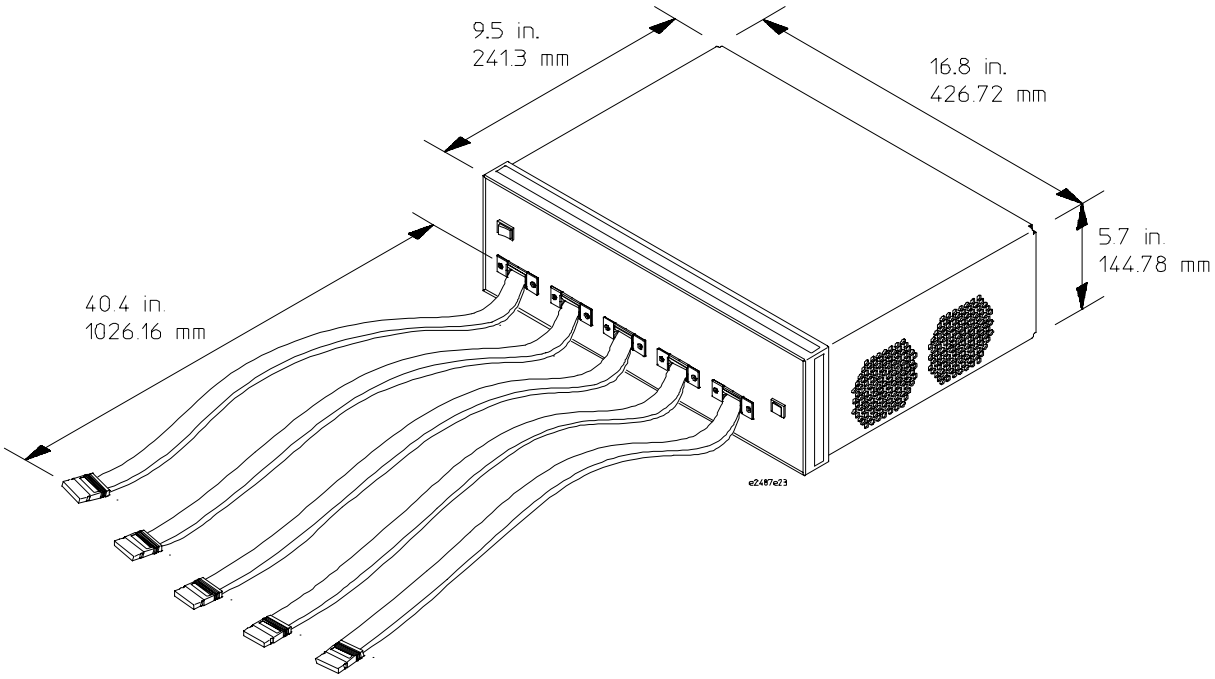
IA-32 Signal List (Cont.)

PREPROCESSOR CONNECTOR			CPU	ANALYZER
NAME	PIN	BIT	SIGNAL	LABEL(S)
P12	3	CLK1		
P12	7	D15	D63#	D63-32
P12	9	D14	D62#	D63-32
P12	11	D13	D61#	D63-32
P12	13	D12	D60#	D63-32
P12	15	D11	D59#	D63-32
P12	17	D10	D58#	D63-32
P12	19	D9	D57#	D63-32
P12	21	D8	D56#	D63-32
P12	23	D7	D55#	D63-32
P12	25	D6	D54#	D63-32
P12	27	D5	D53#	D63-32
P12	29	D4	D52#	D63-32
P12	31	D3	D51#	D63-32
P12	33	D2	D50#	D63-32
P12	35	D1	D49#	D63-32
P12	37	D0	D48#	D63-32

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Analysis probe dimensions

The following illustration gives the dimensions for the analysis probe assembly. The dimensions are listed in inches and millimeters.



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Replaceable parts

The repair strategy for this analysis probe is board replacement. However, the following table lists some mechanical parts that may be replaced if they are damaged or lost. Contact your nearest Agilent Technologies Sales Office for further information on servicing the board.

Exchange assemblies are available when a repairable assembly is returned to Agilent Technologies. These assemblies have been set up on the "Exchange Assembly" program. This allows you to exchange a faulty assembly with one that has been repaired, calibrated, and performance verified by the factory. The cost is significantly less than that of a new assembly.

Replaceable Parts

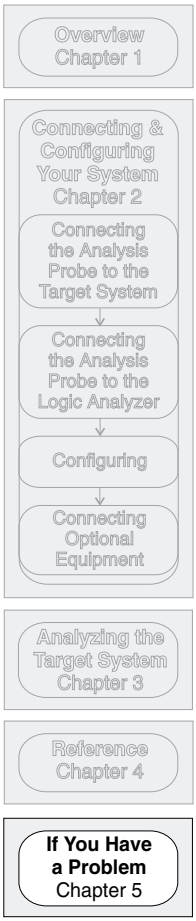
Agilent Part Number	Description
E2487-69005	Rebuilt analysis probe assembly
E2474-61601	Probe cable

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If You Have a Problem

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If You Have a Problem



Occasionally, a measurement may not give the expected results. If you encounter difficulties while making measurements, use this chapter to guide you through some possible solutions. Each heading lists a problem you may encounter, along with some possible solutions.

The information in this chapter is presented in the following sections:

- Logic analyzer problems
- Analysis probe problems
- Inverse assembler problems
- Intermodule measurement problems
- Messages
- Cleaning the instrument

If you still have difficulty after trying the suggestions in this chapter, contact your local Agilent Technologies Service Center.

CAUTION

When you are working with the analyzer, be sure to power down both the analyzer and the target system before disconnecting or connecting cables, probes, and analysis probes. Otherwise, you may damage circuitry in the analyzer, analysis probe, or target system.

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Analyzer Problems

This section lists general problems that you might encounter while using the analyzer.

Intermittent data errors

This problem is usually caused by poor connections, incorrect signal levels, or marginal timing.

- ☐ **Remove and reseat all cables and probes, ensuring that there are no bent pins on the analysis probe or poor probe connections.**
- ☐ **Adjust the threshold level of the data pod to match the logic levels in the system under test.**
- ☐ **Use an oscilloscope to check the signal integrity of the data lines.**

  Clock signals for the state analyzer must meet particular pulse shape and timing requirements. Data inputs for the analyzer must meet pulse shape and setup and hold time requirements.

See Also

See “Capacitive loading” in this chapter for information on other sources of intermittent data errors.

Unwanted triggers

Unwanted triggers can be caused by instructions that were fetched but not executed.

- ☐ **Add the prefetch queue or pipeline depth to the trigger address to avoid this problem.**

  The logic analyzer captures prefetches, even if they are not executed. When you are specifying a trigger condition or a storage qualification that follows an instruction that may cause branching, an unused prefetch may generate an unwanted trigger.

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No activity on activity indicators

- ☐ Check for loose cables, board connections, and analysis probe connections.
- ☐ Check for bent or damaged pins on the analysis probe.

No trace list display

If there is no trace list display, it may be that your trigger specification is not correct for the data you want to capture, or that the trace memory is only partially filled.

- ☐ Check your trigger sequencer specification to ensure that it will capture the events of interest.
- ☐ Try stopping the analyzer; if the trace list is partially filled, this should display the contents of trace memory.

Analyzer won't power up

If the logic analyzer power is powered down when it is connected to a powered-up target system, the logic analyzer may not be able to power up. Some logic analyzers are inhibited from powering up when they are connected to a target system that is already powered up.

- ☐ Disconnect all logic analyzer cabling from the analysis probe. This will allow the logic analyzer to power up. Reconnect logic analyzer cabling after power up.

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Analysis Probe Problems

This section lists problems that you might encounter when using an analysis probe. If the solutions suggested here do not correct the problem, you may have a damaged analysis probe. Contact your local Agilent Technologies Sales Office if you need further assistance.

Target system will not boot up

If the target system will not boot up after connecting the analysis probe, the microprocessor (if socketed) or the analysis probe may not be installed properly, or they may not be making electrical contact.

- ☐ Ensure that you are following the correct power-on sequence for the analysis probe and target system.

  1 Power up the analyzer and analysis probe.

  2 Power up the target system.

  If you power up the target system before you power up the analysis probe, interface circuitry in the analysis probe may latch up and prevent proper target system operation.

- ☐ Verify that the microprocessor and the analysis probe are properly rotated and aligned so that the index pin on the microprocessor (pin 1 or pin A1) matches the index pin on the analysis probe.

- ☐ Verify that the microprocessor and the analysis probe are securely inserted into their respective sockets.

- ☐ Verify that the logic analyzer cables are in the proper sockets of the analysis probe and are firmly inserted.

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Erratic trace measurements

There are several general problems that can cause erratic variations in trace lists and inverse assembly failures.

- ☐ **Do a full reset of the target system before beginning the measurement.**

  Some analysis probe designs require a full reset to ensure correct configuration.

- ☐ **Ensure that your target system meets the timing requirements of the processor with the analysis probe installed.**

  See “Capacitive Loading” in this chapter. While analysis probe loading is slight, pin protectors, extenders, and adapters may increase it to unacceptable levels. If the target system design has close timing margins, such loading may cause incorrect processor functioning and give erratic trace results.

- ☐ **Ensure that you have sufficient cooling for the microprocessor.**

  Some microprocessors generate substantial heat. This is exacerbated by the active circuitry on the analysis probe board. You should ensure that you have ambient temperature conditions and airflow that meet or exceed the requirements of the microprocessor manufacturer.

Capacitive loading

Excessive capacitive loading can degrade signals, resulting in incorrect capture by the analysis probe, or system lockup in the microprocessor. All analysis probes add additional capacitive loading, as can custom probe fixtures you design for your application.

Careful layout of your target system can minimize loading problems and result in better margins for your design. This is especially important for systems that are running at frequencies greater than 50 MHz.

- ☐ **Remove as many pin protectors, extenders, and adapters as possible.**

- ☐ **If multiple analysis probe solutions are available, use one with lower capacitive loading.**

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Inverse Assembler Problems

This section lists problems that you might encounter while using the inverse assembler.

When you obtain incorrect inverse assembly results, it may be unclear whether the problem is in the analysis probe or in your target system. If you follow the suggestions in this section to ensure that you are using the analysis probe and inverse assembler correctly, you can proceed with confidence in debugging your target system.

No inverse assembly or incorrect inverse assembly

This problem may be due to incorrect alignment, modified configuration files, incorrect connections, or a hardware problem in the target system. A locked status line can cause incorrect or incomplete inverse assembly.

- ☐ **Ensure that each logic analyzer pod is connected to the correct analysis probe connector.**

  There is not always a one-to-one correspondence between analyzer pod numbers and analysis probe cable numbers. Microprocessor interfaces must supply address (ADDR), data (DATA), and status (STAT) information to the analyzer in a predefined order. The cable connections for each analysis probe are often altered to support that need. Thus, one analysis probe might require that you connect cable 2 to analyzer pod 2, while another will require you to connect cable 5 to analyzer pod 2. See Chapter 2 for connection information.

- ☐ **Check the activity indicators for status lines locked in a high or low state.**

- ☐ **Verify that the STAT, DATA, and ADDR format labels have not been modified from their default values.**

  These labels must remain as they are configured by the configuration file. Do not change the names of these labels or the bit assignments within the labels. Some analysis probes also require other data labels. See Chapter 3 for more information.

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- ☐ **Verify that all microprocessor caches and memory managers have been disabled.**

  In most cases, if the microprocessor caches and memory managers remain enabled you should still get inverse assembly. It may be incorrect because a portion of the execution trace was not visible to the logic analyzer.

- ☐ **Verify that storage qualification has not excluded storage of all the needed opcodes and operands.**

Inverse assembler will not load or run

You need to ensure that you have the correct system software loaded on your analyzer.

- ☐ **For the Agilent Technologies 16600/700 logic analysis systems, the inverse assembler must be installed on the hard drive using the procedures listed on the jacket for the CD-ROM. Re-install the Processor Support Package for this product, then try loading the configuration file again.**

- ☐ **For other logic analyzers, ensure that the inverse assembler is on the same disk as the configuration files you are loading.**

  Configuration files for the state analyzer contain a pointer to the name of the corresponding inverse assembler. If you delete the inverse assembler, rename it, or use the File Manager Copy command to copy it to the Agilent Technologies 16600/700 logic analysis systems, the configuration process will fail to load the inverse assembler.

  See Chapter 3 for details.

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Intermodule Measurement Problems

Some problems occur only when you are trying to make a measurement involving multiple modules.

An event wasn't captured by one of the modules

If you are trying to capture an event that occurs very shortly after the event that arms one of the measurement modules, it may be missed due to internal analyzer delays. For example, suppose you set the oscilloscope to trigger upon receiving a trigger signal from the logic analyzer because you are trying to capture a pulse that occurs right after the analyzer's trigger state. If the pulse occurs too soon after the analyzer's trigger state, the oscilloscope will miss the pulse.

- ☐ **Adjust the skew in the Intermodule menu.**

  You may be able to specify a skew value that enables the event to be captured.

- ☐ **Change the trigger specification for modules upstream of the one with the problem.**

  If you are using a logic analyzer to trigger the scope, try specifying a trigger condition one state before the one you are using. This may be more difficult than working with the skew because the prior state may occur more often and may not always be related to the event you are trying to capture with the oscilloscope.

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Analyzer Messages

This section lists some of the messages that the analyzer displays when it encounters a problem.

". . . Inverse Assembler Not Found"

This error occurs if you rename or delete the inverse assembler file that is attached to the configuration file. Ensure that the inverse assembler file is not renamed or deleted.

For the Agilent Technologies 16700 logic analysis systems, the inverse assembler must be installed on the hard drive using the procedures listed on the jacket for the CD-ROM.

For other logic analyzers, if you have copied the files to the logic analyzer hard disk, ensure that the inverse assembler is located in the same directory as the configuration file.

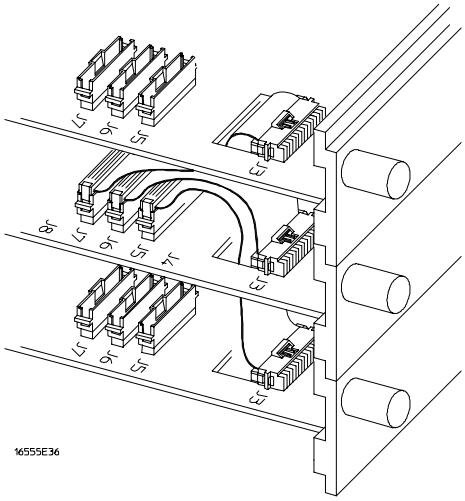
". . . Does Not Appear to be an Inverse Assembler File"

This error occurs if the inverse assembler file requested by the configuration file is not a valid inverse assembler. Use the Install procedures listed on the jacket of the CD-ROM to re-install the files for this product.

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"Measurement Initialization Error"

The following diagrams show the correct cable connections for one-card, two-card, and three-card installations on Agilent Technologies 16555A/D, and 16556A/D logic analysis cards. Ensure that your cable connections match the silk screening on the card, and that they are fully seated in the connectors. Then, repeat the measurement.



Cable Connections for Three-Card Agilent Technologies 16555/56/57 Installations

See Also

The Agilent Technologies 16555A 110-MHz State/250-MHz Timing Logic Analyzer Service Guide.

The Agilent Technologies 16556A 100-MHz State/400-MHz Timing Logic Analyzer Service Guide.

The Agilent Technologies 16557D 135-MHz State/500-MHz Timing Logic Analyzer User's Reference

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"No Configuration File Loaded"

This is usually caused by trying to load a configuration file for one type of module/system into a different type of module/system.

- ☐ Verify that the appropriate module has been selected from the Load {module} from File {filename} in the Agilent Technologies 16500A/B/C disk operation menu. Selecting Load {All} will cause incorrect operation when loading most analysis probe configuration files.

See Also Chapter 2 describes how to load configuration files.

"Selected File is Incompatible"

This occurs when you try to load a configuration file for the wrong module. Ensure that you are loading the appropriate configuration file for your logic analyzer.

"Slow or Missing Clock"

- ☐ This error message might occur if the logic analyzer cards are not firmly seated in the logic analysis system mainframe. Ensure that the cards are firmly seated.
- ☐ This error might occur if the target system is not running properly. Ensure that the target system is on and operating properly.
- ☐ If the error message persists, check that the logic analyzer pods are connected to the proper connectors on the analysis probe. See Chapter 2 to determine the proper connections.

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"Time from Arm Greater Than 41.93 ms"

The state/timing analyzers have a counter to keep track of the time from when an analyzer is armed to when it triggers. The width and clock rate of this counter allow it to count for up to 41.93 ms before it overflows. Once the counter has overflowed, the system does not have the data it needs to calculate the time between module triggers. The system must know this time to be able to display data from multiple modules on a single screen.

"Waiting for Trigger"

If a trigger pattern is specified, this message indicates that the specified trigger pattern has not occurred. Verify that the triggering pattern is correctly set.

- When analyzing microprocessors that fetch only from word-aligned addresses, if the trigger condition is set to look for an opcode fetch at an address not corresponding to a word boundary, the trigger will never be found.

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Cleaning the Instrument

If this instrument requires cleaning, disconnect it from all power sources and clean it with a mild detergent and water. Make sure the instrument is completely dry before reconnecting it to a power source.

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Glossary

Analysis Probe A probe connected to the target microprocessor. It provides an interface between the signals of the target microprocessor and the inputs of the logic analyzer.

Connector Board A board whose only function is to provide connections from one location to another. One or more connector boards might be stacked to raise a probe above a target micoprocessor to avoid mechanical contact with other components installed close to the target microprocessor.

Elastomeric Probe Adapter A connector that is fastened on top of a target microprocessor using a retainer and knurled nut. The conductive elastomer on the bottom of the probe adapter makes contact with pins of the target microprocessor and delivers their signals to connection points on top of the probe adapter.

Emulation Module An emulation module is installed within the mainframe of a logic analyzer. It provides run control within an emulation and analysis test setup. See Emulation Probe.

Emulation Probe An emulation probe is a stand-alone instrument connected to the mainframe of a logic analyzer. It provides run control within an emulation and analysis test setup. See Emulation Module.

Flexible Adapter Two connection devices coupled with a flexible cable. Used for connecting probing hardware on the target microprocessor to the analysis probe.

General-purpose Flexible Adapter A cable assembly that connects the signals from an elastomeric probe adapter to an analysis probe. Normally, a male-to-male header or transition board makes the connections from the general-purpose flexible adapter to the analysis probe.

High-Density Adapter Cable A cable assembly that delivers signals from an analysis probe hardware interface to the logic analyzer pod cables. A high-density adapter cable has a single Mictor connector that is installed into the analysis probe, and two cables that are connected to corresponding odd and even logic analyzer pod cables.

High Density Termination Adapter Cable Same as a High Density Adapter Cable, except it has a termination in the Mictor connector.

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Jumper Moveable direct electrical connection between two points.

Mainframe Logic Analyzer A logic analyzer that resides on one or more board assemblies installed in an Agilent Technologies 16500B/C, 1660xA, or 16700A mainframe.

Male-to-male Header A board assembly that makes point-to-point connections between the female pins of a flexible adapter or transition board and the female pins of an analysis probe.

Preprocessor Interface See Analysis Probe.

Preprocessor Probe See Analysis Probe.

Probe adapter See Elastomeric Probe Adapter.

Processor Probe See Emulation Probe and Emulation Module.

Prototype Analyzer The Agilent Technologies 16505A prototype analyzer acts as an analysis and display processor for the Agilent Technologies 16500B/C logic analysis system. It provides a windowed interface and powerful analysis capabilities.

Setup Assistant A software program that guides you through the process of connecting and configuring an analysis probe and logic analyzer to make measurements on a specific microprocessor.

Shunt Connector. See Jumper.

Stand-alone Logic Analyzer A stand-alone logic analyzer has a predefined set of hardware components which provide a specific set of capabilities. It is designed to perform logic analysis. A stand-alone logic analyzer differs from a mainframe logic analyzer in that it does not offer card slots for installation of additional capabilities, and its specifications are not modified based upon selection from a set of optional hardware boards that might be installed within its frame.

Transition Board A board assembly that obtains signals connected to one side and re-arranges them in a different order for delivery at the other side of the board.

1/4-Flexible Adapter An adapter that obtains one-quarter of the signals from an elastomeric probe adapter (one side of a target microprocessor) and makes them available for probing.

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DECLARATION OF CONFORMITY

according to ISO/IEC Guide 22 and EN 45014

Manufacturer's Name: Agilent Technologies

Manufacturer's Address: 1900 Garden of the Gods Road
Colorado Springs , CO 80907
U.S.A.

Declares, that the product

Product Name: Analysis Probe

Model Number(s): Agilent Technologies E2487C

Product Options: All

Conforms to the following Product Specifications:

Safety: IEC 1010-1:1990+A1 / EN 61010-1:1993
UL 3111
CSA - C22.2 No. 1010.1:1993

EMC: CISPR 11:1990 /EN 55011:1991 Group 1, Class A
IEC 555-2:1982 + A1:1985 / EN 60555-2:1987
IEC 555-3:1982 + A1:1990 / EN 60555-3:1987 + A1:1991
IEC 801-2:1991 /EN 50082-1:1992 4 kV CD, 8 kV AD
IEC 801-3:1984 /EN 50082-1:1992 3 V/m, {1kHz 80% AM, 27-1000 MHz}
IEC 801-4:1988 /EN 50082-1:1992 0.5 kV Sig. Lines, 1 kV Power Lines

Supplementary Information:
The product herewith complies with the requirements of the Low Voltage Directive 73/23/EEC and the EMC Directive 89/336/EEC, and carries the CE-marking accordingly.
This product was tested in a typical configuration with Agilent Technologies test systems.

Colorado Springs, 12/9/98

Ken Wyatt, Quality Manager

European Contact: Your local Agilent Technologies Sales and Service Office or Agilent Technologies GmbH, Department ZQ/Standards Europe, Herrenberger Strasse 130, D-71034 Böblingen Germany (FAX: +49-7031-14-3143)

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Product Regulations

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CSA-C22.2 No.1010.1:1993

EMC This Product meets the requirements of the European Communities (EC) EMC Directive 89/336/EEC.

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N279
LR 93772C

Emissions EN55011/CISPR 11 (ISM, Group 1, Class A equipment), IEC 555-2 and IEC 555-3

Immunity EN50082-1	Code	Notes
IEC 801-2 (ESD) 8kV AD	1	1
IEC 801-3 (Rad.) 3V/m	3	
IEC 801-4 (EFT) 1kV	1	

Performance Codes:
1 Pass - Normal operation, no effect.
2 Pass - Temporary degradation, self recoverable.
3 Pass - Temporary degradation, operator intervention required.
4 Fail - Not recoverable, component damage.

Notes:
1 The user cable assembly is sensitive to ESD events. Use standard ESD preventative practices to avoid component damage.

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