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HP E2925A 32 Bit, 33 MHz PCI Exerciser and Analyzer

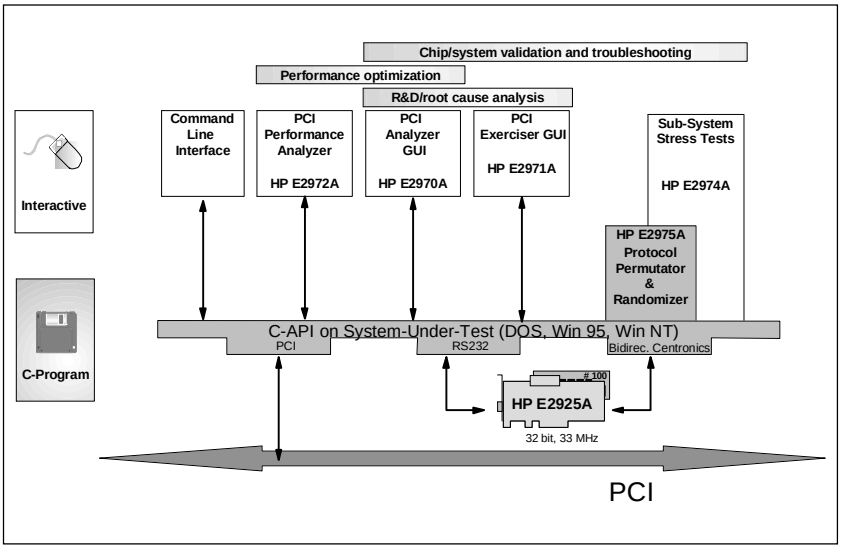
Technical Specifications

HP E2920 Computer Verification Tools, PCI Series

Part of the HP E2920 Computer Verification Tools, PCI Series, the HP E2925A 32 bit, 33 MHz PCI Exerciser and Analyzer is a fully programmable PCI master and target with an on-board PCI state logic analyzer, a PCI protocol observer and built-in test functions.

Integrates into your test environment
With its C-Application Programming Interface (C-API), the fully in-system programmable HP E2925A 32 bit, 33 MHz PCI Exerciser & Analyzer Card can be completely integrated into your test software for validating chips, cards and systems. The card is fully programmable either via PCI from the system-under-test, or via RS232/bi-directional Centronics from an external test controller.

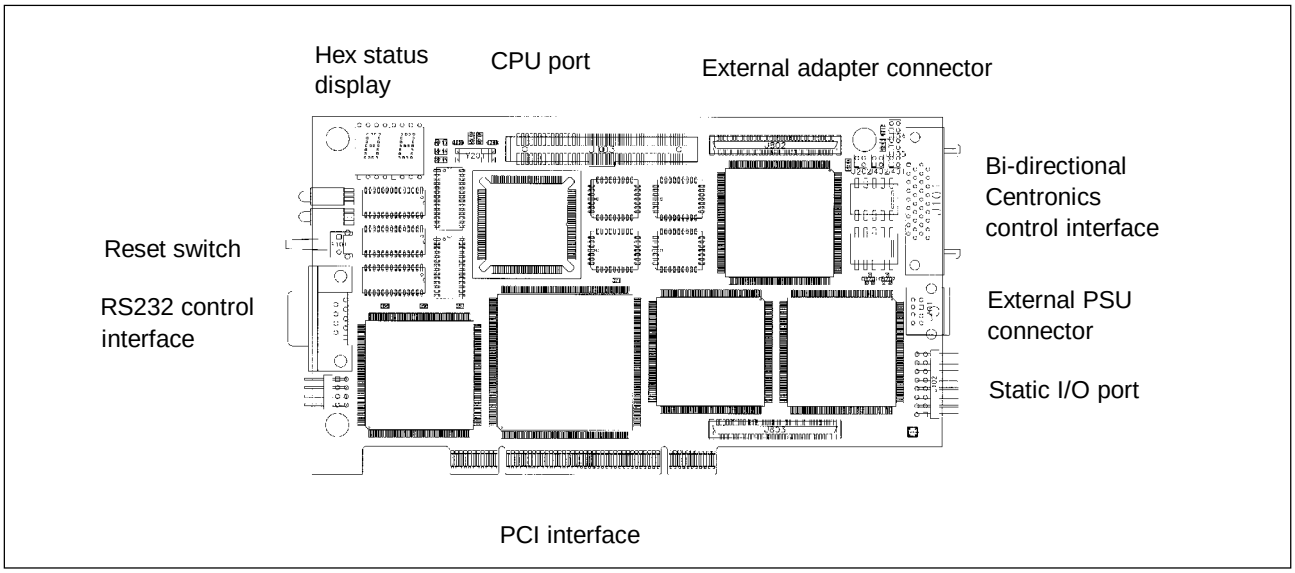
Tailored solutions for all validation processes
Choose from the Windows 95/NT Graphical User Interface and software products also available in the HP E2920 PCI Series of Computer Verification Tools to tailor the exerciser and analyzer card to meet your interactive debugging, system validation or PCI performance analysis needs.



Key Features

- Control of master and target protocol and traffic behavior for traffic emulation and debugging.
- 32 k/1 M (optional) state PCI logic analyzer with PCI-oriented triggering and storage qualification for convenient traffic analysis.
- Optional trigger sequencer with 64 branches to trigger, store data, decrement and pre-load counter.
- PCI protocol checker monitors 25 protocol rules in real-time for capturing violations.
- On-board 128 kB PCI memory and/or I/O space for emulating master and target resources.
- Programmable configuration space/expansion EEPROM.
- On-board CPU with built-in test functions for system data integrity testing.
- C-API programming library for complete integration into your test environment.
- Control over RS232, PCI, or bi-directional Centronics.
- CPU port and static I/O signals to read and write DUT registers and signals beyond PCI.
- Add-on comprehensive GUIs for convenient, interactive debugging performance analysis.
- Add-on, ready-to-run stress tests and protocol permutation library to intensify tests.

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For interactive debugging and root cause analysis, use the:

- HP E2970A PCI Analyzer GUI or
- HP E2971A PCI Exerciser GUI.

For PCI performance evaluation and optimization, you need the:

- HP E2972A PCI Performance Analyzer.

To intensify testing with easy-to-run test functions during system validation, use the:

- HP E2974A Sub-System Stress Tests.

For exhaustive PCI protocol verification, you need the:

- HP E2975A PCI Protocol Permutator and Randomizer.

Master capabilities

The HP E2925A provides a programmable PCI master for emulating missing device traffic and generating protocol and traffic variations. You can completely control:

- The number and type of master data transfers which should take place, by setting up pages of master block transfers.
- The transaction and protocol behavior which should be used during the data transfer, on a phase-by-phase basis, by setting up master protocol attributes.
- The run control conditions for the block transfers.
- The data content of write transfers from the on-board data memory.

Master block transfers

A master block transfer defines the transfer of a block of data.

PCI command type	0000\b - 1111\b (except DAC)
Target PCI address	32 bit
Number of data transfers	1 to 32 k
Byte enables	0000\b - 1111\b
Data offset in data memory	00000\h - 1ffff\h
Protocol behavior page pointer	0 - 255
Compare flag	0, 1
Compare offset in data memory	00000\h - 1ffff\h

You can define up to sixteen pages of master block transfers, and each page can contain up to sixteen individual transfers. When you run a page of transfers, all block transfers in that page will be run sequentially by the on-board CPU.

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The master will sequentially move the required number of data transfers, using the defined PCI command type and byte enables, from the internal data memory to the target PCI address in the case of a write command, and vice-versa in the case of a read command. For data integrity testing, by setting a compare flag, the transferred data can be compared with expected reference data stored in the internal data memory at the compare offset address.

The master automatically continues after any target disconnect or retry until the defined block transfer or page of transfers is completed. A pointer to the protocol behavior pages allows each block transfer to exhibit different behavior.

The master protocol behavior, such as the number and length of transactions used, wait states or parity, is defined separately from the data transfer using the master protocol attributes.

Master Protocol Attributes

You can define the master protocol behavior by setting up sequences of protocol attributes, up to a maximum of 8 k independent entries. Each entry controls the protocol behavior for a single phase (address or data) during a block transfer, and the entries are used sequentially for each phase until the block transfer is complete.

Attributes are available to:

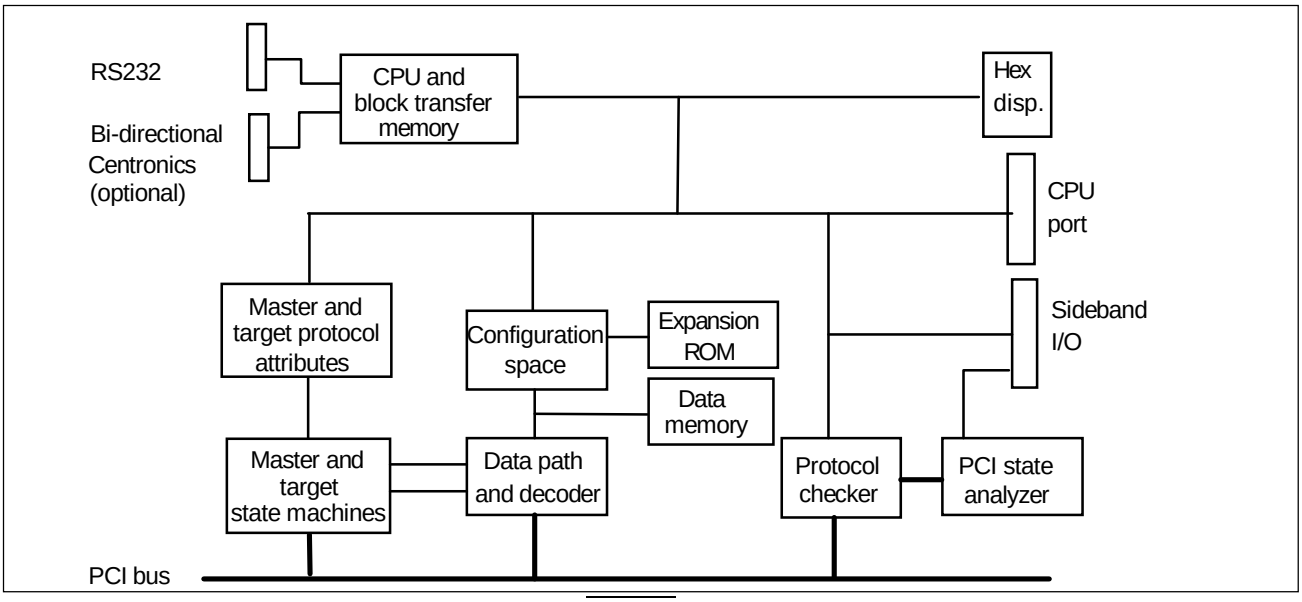
- force SERR# if address phase,
- invert PAR if address phase,
- perform four address steps, toggling address, if address phase,
- control LOCK (no, lock, hide, unlock),
- insert 0 - 31 master wait states,
- force PERR# during data phase,
- force SERR# during data phase,
- invert PAR,
- perform four data steps, toggling data,
- force master to terminate burst and continue with new address phase,
- release REQ# during data phase,
- loop back to the start of the current page.

The protocol attribute sequence is divided into 256 pages of 32 entries to allow different entry points for different block transfers and looping.

Master latency timer
The master latency timer is programmable from 0 to 255 clocks and can be disabled.

Master run control
Once the master block transfers and protocol behavior are set up, you can run the exerciser to generate the required traffic. In addition, you can control the start and repeat conditions for the traffic.

Master trigger pattern
You can define a 0/1/x pattern to trigger the master traffic. The pattern can include any of the PCI bus signals, ext. trigger I/O signals, protocol violation signal, and decoded bus state signals. This trigger pattern is independent of the PCI analyzer trigger and qualification patterns.



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Delay counter
You can set a 16 bit delay counter to delay the master traffic by a number of PCI clocks following the master trigger.

Run mode
The master can be set to run once or to repeat in an infinite loop until you stop it. The start can be controlled by a trigger pattern and the delay counter.

Data Memory

The on-board data memory provides 128 kB of read/write memory. The master uses this memory to store data from read transfers and as a data source for master write transfers, using an internal address range of 00000\h to 1ffff\h. The target makes it available as read/write memory or as I/O space on the PCI bus. This makes it possible for other PCI masters to provide data for the exerciser's master.

Target Capabilities

The HP E2925A provides a programmable PCI target for emulating missing devices and generating protocol and traffic variations. You can completely control:

- The target protocol behavior which is used during the data transfer, on a phase-by-phase basis, by setting up target protocol attributes.
- The target memory and/or I/O address by setting up the target decoders directly, or the base address registers in the configuration space.
- The data content of read transfers from the on-board data memory.

Target Decoders

The target provides two independently-controllable address decoders.

	Decoder 1	Decoder 2
Decode speed	Medium or slow	Medium or slow
Commands accepted	Memory only	Memory or I/O
PCI address space	4 kB to 16 MB	16 B to 64 kB
PCI address	Assigned via configuration space base address registers	
Internal address offset	00000\h	10000\h

If the address space assigned to Decoder 1 is greater than the available 128 kB on-board memory, the memory is mirrored.

Target Protocol Attributes

You can define the target protocol behavior by setting up a sequence of protocol attributes, up to a maximum of 8 k independent entries. Each entry in a sequence controls the protocol behavior for a single data phase during an access to the target. Attributes are used sequentially for each phase during a transfer until the access is complete. The protocol attribute sequence is divided into logical pages of 32 entries to allow looping. You can also choose whether the target automatically restarts at the beginning of the current page each time it is accessed (new master address phase) or continues with the next entry.

Attributes are available to:

- insert 0 - 31 target wait states,
- terminate transaction (no, retry, disconnect, abort),
- force SERR#,
- force PERR#,
- invert PAR,
- perform four data steps, toggling data,
- loop back to the start of the last page.

Configuration Space

The HP E2925A provides a fully programmable PCI configuration space. Default values are stored in the EEPROM of the on-board CPU and are used to initialize the configuration space following power-up. The defaults can also be reprogrammed with modified values. The configuration space can be disabled, making the card invisible to BIOS or O/S configuration routines.

Status register
As well as the standard PCI status register in the configuration space, there is an additional register to provide card status information:

- master running,
- target active,
- protocol checker running,
- analyzer running,
- protocol error occurred,
- data compare error,
- functional error,
- interrupt timer exceeded,
- interrupt asserted (A, B, C, D),
- self-test failed.

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Mailbox registers
The user configuration space also has two mailbox registers, designed to allow an external test controller program (connected via RS232 or bi-directional Centronics) to communicate with a test program running on the system-under-test.

Expansion ROM

A 64 kB EEPROM is provided as a PCI expansion ROM. The ROM decoder reacts to a 256 kB address space, from the start address written to the expansion ROM base address register, so that the EEPROM is mirrored four times. The EEPROM is fully programmable, allowing you to test BIOS handling of expansion ROM data, or provide a test code to the system CPU during the boot process.

Protocol checker

Protocol state machines continuously monitor 25 protocol rules in real-time. Each rule can be individually suppressed using a bit mask to disable the detection of known problems. As well as providing an "any error" output for triggering purposes, registers are used to both latch the first error to occur and to accumulate all errors which occur.

The protocol checker status can be displayed on the on-board hex display.

State analyzer

The on-board PCI state analyzer provides a 32 k/1 M (optional) state logic analyzer optimized for observing the PCI bus, with visibility of:

- All 32 bit PCI address/data and control signals.
- Protocol error signal from masked protocol checker for triggering on protocol errors.
- Decoded bus state signals, time-aligned to the bus signals for easy triggering on address, data, idle, and other bus states.
- Master and target active signals, aligned to the bus signals for easy identification of transactions involving the HP E2925A.
- Four input signals from the external trigger I/O connector for external triggering, in or out.

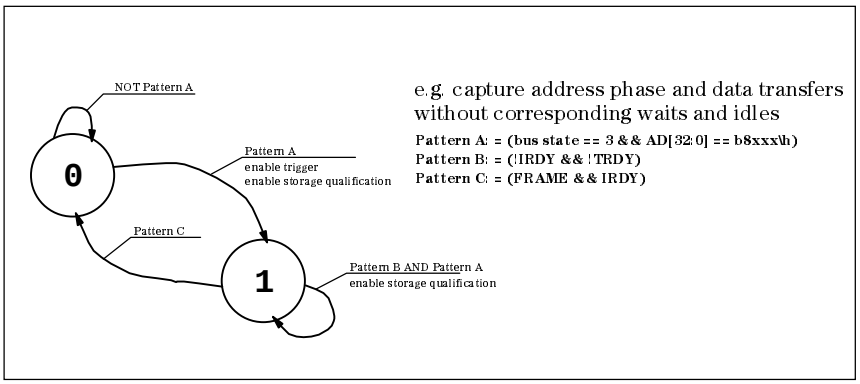
Triggering
You can set up one 0/1/x trigger pattern to trigger the analyzer and one 0/1/x compare pattern to qualify whether the state should be stored. The aligned bus state signals allow the easy identification of the bus state for triggering and filtering.

Flexible trigger points
For maximum flexibility, the trigger can be placed in any position in the trace memory.

Trigger sequencer with 64 branches and termination counter
The HP E2925A option 100 enhances the standard trigger capabilities by allowing 64 branches to trigger, store data, decrement and pre-load a 32 bit termination counter. It features a state machine providing four states, which can handle four pattern terms and counter status. Therefore, it overcomes the limitations of a traditional n-level trigger sequencer by allowing only IF - ELSE and nested loops. The state machine allows the easy handling of multiple branches or the simultaneous handling of different pattern terms, while keeping a state. Each branch is reflected by a state machine transition and can simultaneously enable/disable the analyzer trigger and the storage qualification, and pre-load or decrement the termination counter.

The important information, e.g. not all accesses, but every 16th access to the I/O register, can be easily filtered by pre-loading and decrementing the termination counter.

The transition conditions of up to four pattern terms are set by any logical expression (AND, OR, EXOR, negation) and feature the status of the termination counter.



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Additional I/O Ports

Static I/O signals
Eight static I/O pins are available for observing or controlling additional signals beyond PCI as part of the test. Each pin can be configured as an input, a totem pole, or as an open drain output. The outputs can be set under program control as either high or low.

External trigger I/O
The external trigger I/O consists of three input pins, observed by the analyzer and available as part of its trigger, storage, and master run control qualification patterns. There is one external trigger output.

CPU port
The CPU port is designed to allow the test program to control and initialize registers in a device or system-under-test via a simple Intel parallel bus interface. It provides:

- 16 bit address bus,
- 16 bit data bus,
- two byte enables,
- two chip select signals,
- write enable,
- read enable,
- ready,
- reset,
- interrupt,
- CPU clock (16 MHz).

Built-in Test Functions

The on-board CPU makes a number of built-in test functions available, designed to quickly and easily intensify existing tests by adding additional asynchronous background traffic to the system.

- **Make Traffic**: master generates bursts of various lengths to its own target in order to load the arbiter and decrease the available bandwidth for other PCI masters without influencing the system's resources.

- **Write/Read/Compare**: this test function continuously writes a block of data from the on-board memory to an external target, reads it back, and can compare (as an option) the results with the original data. The test stops on miscompare.

- **Block Move**: this test function continuously reads a block of data from one target address and writes it to another using the on-board memory as an intermediate buffer.

C-Application Programming Interface

The C-Application Programming Interface (C-API) is a library of C functions which provides a programming interface for setting up and controlling the HP E2925A as part of your own test programs. The test program can be running on the system-under-test itself or on an external controller because the C-API can control the HP E2925A via its PCI, RS232, or optional bi-directional Centronics interface. Drivers are provided for each interface, which allow the C-API to be used under DOS, Windows NT 3.51 and 4.0, or Windows 95.

	Windows 95	Windows NT	DOS
RS232	Yes	Yes	Yes
PCI	No	Yes	Yes
Option 002 Centronics	Yes	Yes	Yes

The library functions are divided into groups which allow you to set up and control the various capabilities of the HP E2925A.

Session and interface functions
These functions allow your program to start controlling an HP E2925A card by allocating resources and setting up the control path (RS232, PCI, or bi-directional Centronics). A handle to identify this particular card when using the other functions is also provided.

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Master block property functions
These functions set up, run, and stop the master block transfers which define the transfer of a block of data.

Master protocol behavior functions
These functions set up the sequence of protocol attributes which are to be used by the master when running the master block transfers.

Master generic property functions
These set up the following generic properties of the master:

- trigger pattern,
- delay counter,
- run mode,
- latency timer.

Target decoder functions
These set up the two target decoders:

- switch decoder on or off,
- select memory or I/O (Decoder 2),
- set decoder size (also modifies "read only" bits in configuration BAR),
- set decoder base address (also modifies configuration BAR).

Target protocol behavior functions
These functions set up the sequence of protocol attributes which are to be used by the target when accessed.

Protocol checker functions
These set up and monitor the protocol checker:

- enable/disable checker,
- set up error mask,
- read or reset first error, accumulated error, and checker status registers,
- read an error description string for a particular error number.

Analyzer and trigger functions
These set up and control the PCI state analyzer:

- select trigger mode,
- set trigger and qualification patterns,
- read analyzer status,
- read trace memory data,
- run/stop control.

Host to PCI access functions
Higher level functions allow a test program quick and direct access to the system-under-test's PCI resources (memory, I/O, or configuration spaces) without having to program specific block transfers or protocol behavior. Used, for example, to download the test code to the system memory, to dump the memory's contents, or to read/modify particular registers.

- Fill a block of data to a specified system address.
- Dump a block of data from a specified system address.
- Set or get any single byte, word, or Dword in memory, I/O, or configuration space.

Static I/O functions
The static I/O functions set up and control the static I/O pins:

- configure pin as input, totem pole, or open drain output,
- set output as high or low.

CPU port functions
These functions set up the CPU port and perform write and read accesses via the port.

Configuration space functions
These set up and control the card configuration space:

- enable/disable the configuration space decoder,
- write or read the current register setting within the configuration space,
- store current settings as defaults to be used after the next power cycle.

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Expansion ROM functions
These functions write or read a byte within the expansion EEPROM.

Status functions
These read or clear the user status register.

Mailbox functions
You can exchange data between the system-under-test and the external controller via the mailbox registers.

Hex display functions
These functions:

- set the hex display mode either to display protocol checker errors or to be program-controlled,
- program the two digit hex display directly.

Power-up functions
The power-up functions define the power-up behavior of the HP E2925A by defining the power on the following settings:

- protocol checker enable/disable,
- run analyzer.

Test functions
You can call the built-in test functions as part of your test program:

- make traffic,
- write/read/compare,
- block move.

In addition, the following functions quickly set up the card as the protocol monitor and store the analyzer's results for later analysis.

- Protocol error detect: sets up the protocol checker to trigger the analyzer if a protocol error occurs.

- Dump result: stores the analyzer's and protocol checker's status to a file, including the trace memory. The file can then be analyzed later using the HP E2970A PCI Analyzer Graphical User Interface for Windows 95/NT.

Command Line Interface

The HP E2925A is supplied with a Command Line User Interface (CLI) which runs under Windows 95/NT. This allows you to interactively control the HP E2925A from an external PC by entering command functions which correspond with the functions provided by the C-API. The CLI can also process batch files of concatenated command functions. The CLI is intended to provide a programmer with a means of controlling the card interactively, while developing test programs using the C-API.

Ordering Information

The HP E2925A 32 bit, 33 MHz PCI Exerciser and Analyzer includes:

- 32 bit, 33 MHz PCI Exerciser and Analyzer Card,
- C-Application Programming Interface software,
- Command Line Interface (CLI) software for Windows 95/NT,
- software ID module to enable CLI software and add-on software products, whether ordered now or later.

In addition, the following options are available.

External Power Supply (001)
For applications where the exerciser & analyzer card should be transparent to the system, you can connect this external power supply to prevent the card from drawing power from its slot.

Fast Host Interface (002)
For applications requiring extensive data download/upload from an external test controller to the system-under-test, you can improve the data throughput through the exerciser & analyzer card by using the bi-directional Centronics interface instead of the RS232 interface. This option includes an ISA bi-directional Centronics interface card for your controlling PC and the appropriate cable to connect it to the HP E2925A. Windows NT on the controlling computer is required.

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HP Logic Analyzer Adapter (003)
This add-on daughter card provides all of the on-board PCI analyzer signals with the appropriate terminations and connectors to connect straight to an external HP Logic Analyzer. This is useful if you want to observe the PCI bus state in context with other busses or interfaces in the system-under-test.

Generic Logic Analyzer Adapter (004)
This Generic Logic Analyzer Adapter provides all of the on-board PCI analyzer signals to connect directly to any external logic analyzer. Appropriate terminators, depending on the selected logic analyzer, have to be added.

1 M Memory/Performance Board (100)
This option enhances the HP E2925A by providing:

- 1 M trace memory,
- Four real-time counters and one reference counter with virtual, infinite depth,
- trigger sequencer with 64 branches to trigger, store data, decrement and pre-load a 32 bit termination counter,
- four pattern storage qualifiers.

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HP E2925A PCI Specifications

The following specifications use the outline of the PCI Rev 2.1 specification.

2. Signal definition	All 32 bit PCI bus signals (except JTAG) and internal state information can be observed by the logic analyzer and used by the pattern recognizor to trigger the analyzer or exerciser.
2.2.6. Interrupts pins (optional)	INTA# - INTD# can be asserted.
2.2.7. Cache support pins (optional)	SBO#, SDONE sampled by the analyzer but not actively implemented/supported.
2.2.8. Additional signals	PRSNT# pins: hardwired for 15 W max.: PRSNT1# = open. PRSNT2# = GND1. CLKRUN#: not supported, since not defined for connector.
2.2.9. 64 bit bus extension pins (optional)	64 bit PCI not supported.
2.2.9. JTAG/boundary scan pins (optional)	Not supported. TDI is hardwired to TDO, TCK, TMS, and TRST# open.
2.3. Sideband signals	Three external trigger input pins are provided, which are observed by the PCI analyzer and can be used for triggering purposes. One external trigger output pin is provided to trigger an external device driven by the trigger pattern for the on-board analyzer.
3.1. Bus commands, master	All command types, including "reserved", can be generated, except for dual address cycle. Reserved commands 0100 and 1000 are treated as read commands. Reserved commands 0101 and 1001 are treated as write commands. It is up to the user to ensure that when using cacheline related commands, the number of data transfers correlates to the cacheline size. Data is written from the on-board memory for write commands and read into the on-board memory for read commands.
3.1. continued Bus commands, target	Provides a configuration space and two decoders for the on-board memory, which can all be individually enabled or disabled. Decoder 1 responds to all types of memory cycles, if enabled. Decoder 2 can be configured to respond to either I/O cycles or all memory cycles. Configuration space responds to type 0 configuration cycles, if enabled. Target does not respond to interrupt acknowledge, special cycle, reserved commands or dual address cycles.
3.2.2. Addressing, master	Supports 32 bit addressing, and always generates a linear address order within a burst, independent of AD[1:0] state.
3.2.2. continued Addressing, target	Programmable slow or medium decode speed. Decoder 1: decodes all types of memory cycles and has a programmable address range of 4 kB to 16 MB, starting from the address assigned in BAR 0 in the configuration space. If an address range >128 kB is used, the on-board memory is mirrored. Decoder 1 maps into the on-board memory starting at internal address 00000\h. Assumes linear, ordered bursts (AD[1:0] ignored). Decoder 2: decodes either all memory cycles or I/O cycles and has a programmable address range of 16 B to 64 kB, starting from the address assigned in BAR 1 in the configuration space. AD [3:0] is not decoded, so I/O addresses are not decoded to the byte boundary. Decoder 2 maps into the on-board memory at address 10000\h. Note that if Decoder 1 has an address range >64 kB, it will overlap in the on-board memory with Decoder 2. Assumes linear, ordered bursts (AD[1:0] ignored). Configuration space: a single function (64 Dword) configuration space responds to configuration cycles, if enabled. All implemented registers are fully programmable, for example to change the size of the address range requested by a BAR or Vendor ID. Each register has a write enable mask to define which bits can be written by PCI configuration accesses, for example to protect read-only bits in BARs. Non-implemented registers will return 0000\h to a read and throw away data on a write. Bursts are not accepted and are disconnected.
3.2.3. Byte alignment	Master: any combination of byte enables can be programmed for a particular data transfer. The byte enables are maintained for all data phases within a block transfer, whether the transfer takes place as a single transaction or as multiple transactions due to target disconnects. Target: always returns all data bytes, independent of byte enables.

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3.2.6. Combining, merging, collapsing	Not supported.
3.3. Bus transactions	Any command can be programmed as burst or single transfer. 0 to 31 wait states can be generated in any master or target phase.
3.3.3.1. Master-initiated termination	Completion: the length of a burst is programmable. The maximum burst length is 32 kDwords (limited by the size of the on-board memory) if the protocol behavior is allowed to loop. The master completes when the defined data transfer is finished, or if the protocol behavior is set up to split the transfer into multiple transactions. Time-out: programmable latency counter (4 to 256 clocks) forces master to release bus if GNT# is de-asserted and if the counter has expired. REQ# will remain asserted if the programmed transfer is not yet completed. Master abort: six cycles after FRAME# is asserted, if target does not respond. In this case, the master abort detected bit is set in the configuration space status register.
3.3.3.2. Target-initiated termination	Master: retries a target-terminated access after a deterministic number of clocks, starting at the address of the next untransferred data and assuming a linear burst ordering. In the case of a target abort, the target abort received bit is set in the status register. Target: all target termination types can be programmed in any target data phase for memory and I/O accesses. The assertion of STOP# can be placed on a clock cycle basis using the "wait" parameter. Disconnect A/B: terminates after data transfer. Retry/disconnect C: terminates without data transfer. Target abort: terminates without data transfer and de-asserts DEVSEL#. The signaled target abort bit is set in the status register. Note that the target may also generate unprogrammed retries, for example if the on-board memory is currently being accessed by the on-board CPU from the user interface.
3.4. Arbitration	Master: REQ# is asserted as soon as the first address and data of the programmed transfer have been prepared. By default, REQ# remains asserted until the transfer has been completed, even if it consists of multiple transactions. This can be overridden by programming REQ# to be de-asserted during any address phase.
3.4.2. Fast back-to-back transactions	Master: not supported. Target: supports fast back-to-back. Fast back-to-back capable bit in status register is programmable.
3.4.3. Arbitration parking	**Bus parking is implemented.**
3.5.1. Target latency	Target initial latency: read cycles; four clocks, programmable up to 35. write cycles; two clocks, programmable up to 33. Target subsequent latency: programmable from 0 to 31 waits. Master data latency: programmable from 0 to 31 waits. Arbitration latency: latency counter implemented; see 3.3.3.1.
3.6. Exclusive access	Master: can start a locked access and complete it at the end of the next transaction or later. Target: locks its whole address range.
3.6.1. Starting an exclusive access	Master: releases LOCK# after master or target abort.
3.6.3. Accessing a locked agent	Master: withholds a locked access while another master has LOCK# asserted. Target: signals retry when locked and accessed with a non-exclusive access.
3.6.4. Completing an exclusive access	Master: LOCK# is released one clock cycle after the last data in a burst.
3.7.1. Device selection	Target can be programmed to perform slow or medium speed decode.
3.7.2. Special cycle	Master can generate single cycle special cycle command. Target does not support special cycles.
3.7.3. Address/data stepping	Address: One address step is implicated in all address phases; address will output following GNT# for one clock before FRAME# is asserted. Four fixed additional address steps with toggling address can be programmed. Data: Four fixed additional data steps with toggling data can be programmed in any data phase.

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3.7.4. Configuration cycles

Master can generate type 0 and type 1 configuration cycles and can access any configuration space if the motherboard connects IDSELx to address lines.

Target: if enabled, the configuration space will respond to type 0 configuration accesses when IDSEL is asserted. Always responds with a disconnect to force master to single cycles.

3.7.5. Interrupt acknowledge

Master: can generate an interrupt acknowledge cycle. The read interrupt vector is stored in on-board memory.

Target: does not respond to interrupt acknowledge cycles.

3.8.1. Parity

Address or data phases can be individually programmed to generate correct or wrong PAR bit. Parity is checked by the protocol checker for all bus traffic and can be used to trigger on-board analyzer.

3.8.2.1. PERR#

Master and target can assert PERR# two clock cycles after any read/write data transfer as part of the intended test.

Although parity errors are detected by the protocol checker, they are not used to automatically assert PERR#.

PERR# can only be asserted if the parity error response bit has been enabled in the command register.

If PERR# is asserted, the data parity error bit is set in the status register.

If PERR# is asserted during a master transaction, the detected parity error bit is also set in the status register.

3.8.2.2. SERR#

Master and target can assert SERR# two clocks after an address phase as part of the intended test.

SERR# can only be asserted if the SERR enable bit is set in the command register.

If SERR# is asserted, the signaled system error and detected parity error bits are set in the status register.

3.9. Cache support

Not implemented/supported. SBO# and SDONE are sampled by the on-board logic analyzer.

3.10. 64 bit bus extension

Not supported.

4.2. Component specification

PCI drivers are driven by Vio on the PCI connector and can be used in both 5 V and 3.3 V environments.

AD[31:0], C/BE[3:0], PAR and PERR are driven by PCI-compliant buffers of Altera Flex81500A2-304ARC FPGA.

FRAME#, IRDY#, REQ#, DEVSEL#, STOP# and TRDY# are driven by PCI-compliant buffers of Altera Flex81188A2-208AQP FPGA.

4.2.3.1. Clock specification

Operates at any frequency between DC and 33 MHz.

4.2.3.2. Timing parameters

Symbol	Min	Max	Notes
tval		12 ns	
ton	2 ns		
toff		28 ns	
tsu	7 ns		
tsu(ptp)	7 ns		
th	0 ns		

@ temperatures of -40 °C to +70 °C

4.4. Expansion board specification

4.4.1. Board pin assignment

PRSNT1# = open.
PRSNT2# = ground.
TDI connected to TDO.
Universal board pinout.

4.4.2.1. Decoupling

Unused 3.3 V power pins are decoupled.

4.4.2.2. Power requirements

Consumes <15 W from PCI slot, unless optional external power supply is used.

4.4.3.1. Trace length limits

Control signals: 2.0 to 2.5".
AD[31:0],C/BE[3:0],PAR: 1.0 to 2.9".

4.4.3.3. Impedance

60 - 100 Ohm typical.

4.4.3.4. Signal loading

CLK is loaded with two Altera inputs and one additional clock buffer (25 pF typical).

FRAME#, IRDY# and DEVSEL# are loaded with two Altera I/O pins (20 pF typical).

All other signals are loaded with a single Altera I/O pin (10 pF typical).

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HP E2925A PCI Specifications

5.2. Expansion card physical dimensions	Short, universal PCI card. Connector level: 20 degrees.
5.2.1. Connector physical description	**Universal 32 bit card edge connector**.
6. Configuration space	The HP E2925A has a complete, fully programmable, single function configuration space which responds to type 1 configuration accesses. Bits and values which are normally fixed in a standard PCI device can be programmed.
6.2.1. Device identification	Vendor ID, device ID, revision ID, header type, and class code are programmable.
6.2.3. Device status	Signaled, received, and detected bits will be set according to status. 66 MHz, UDF, fast back-to-back, and DEVSEL bits are programmable, although default values represent true capabilities of the HP E2925A.
6.2.4. Miscellaneous functions	Cacheline size can be programmed to four or eight Dwords for latency timer time-out purposes. Latency timer can be programmed from 0 to 255 clocks. MIN_GNT and MAX_LAT are programmable. Sub-system IDs are programmable.
6.2.5. Base addresses	
6.3. Expansion ROM	64 kB EEPROM is available as expansion ROM and is mapped (repeated four times) into a 256 kB address space, starting at the address assigned in the expansion ROM BAR. The EEPROM is fully programmable and retains its contents if power is cycled.
6.6. System reset	The HP E2925A can be programmed to respond to RST# in two ways. Reset all: the card is completely reinitialized, all state machines are reset and all hardware settings returned to default conditions (except for expansion EEPROM contents). Reset state machines: only state machines are reset. All settings, such as protocol behavior and target address decoder are maintained.
7. 66 MHz PCI	Not supported.
Operating temperature	-40 ºC to +70 °C.

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Related HP Literature

- HP E2920 Computer Verification Tools, PCI Series, brochure, p/n 5965-4723E.
- HP E2970A PCI Analyzer Graphical User Interface for Windows 95/NT, technical specifications, p/n 5965-4726E.
- HP E2971A PCI Exerciser Graphical User Interface for Windows 95/NT, technical specifications, p/n 5965-4725E.
- HP E2972A PCI Performance Analyzer, technical specifications, p/n 5965-8008E.
- HP E2974A Sub-System Stress Tests, technical specifications, p/n 5965-8009E.
- HP E2975A PCI Permutator and Randomizer, technical specifications, p/n 5965-8010E.

For more information:
http://www-europe.hp.com/dvt

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Japan:
Hewlett-Packard Japan Ltd.
Measurement Assistance Center
9-1, Takakura-Cho, Hachioji-Shi,
Tokyo 192, Japan
Tel: (81-426) 56-7832
Fax: (81-426) 56-7840

Latin America:
Hewlett-Packard
Latin American Region Headquarters
5200 Blue Lagoon Drive
9th Floor
Miami, Florida 33126
U.S.A.
Tel: (305) 267-4245
Tel: (305) 267-4220
Fax: (305) 267-4288

Australia/New Zealand:
Hewlett-Packard Australia Ltd.
31-41 Joseph Street
Blackburn, Victoria 3130
Australia
1 800 629 485

Asia Pacific:
Hewlett-Packard Asia Pacific Ltd
17-21/F Shell Tower, Times Square,
1 Matheson Street, Causeway Bay,
Hong Kong
Tel: (852) 2599 7777
Fax: (852) 2506 9285

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