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HP E2926A 32/64 Bit, 33 MHz PCI Exerciser and Analyzer

Technical Specifications

HP E2920 Computer Verification Tools, PCI Series

The HP E2926A 32/64 bit, 33 MHz PCI Exerciser and Analyzer is a fully controllable PCI master and target card used for system verification, design bring-up and debug, compliance test and performance measurement of PCI systems in the computer and semiconductor industry.

State of the art design verification
Featured with an on-board PCI state logic analyzer, PCI real-time protocol observer and traffic generation capabilities, the HP E2926A is a universal verification tool in research and development and quality assurance laboratories. The application tailored software packages of the HP E2920 PCI Series make it easy-to-use in the complete design and verification cycle and to communicate design problems between teams.

A product family used in the entire design cycle
Choose from the Windows 95/NT® Graphical User Interface and software products also available in the HP E2920 PCI Series of Computer Verification Tools to tailor the exerciser and analyzer card to meet your debugging, system validation or PCI performance analysis needs.

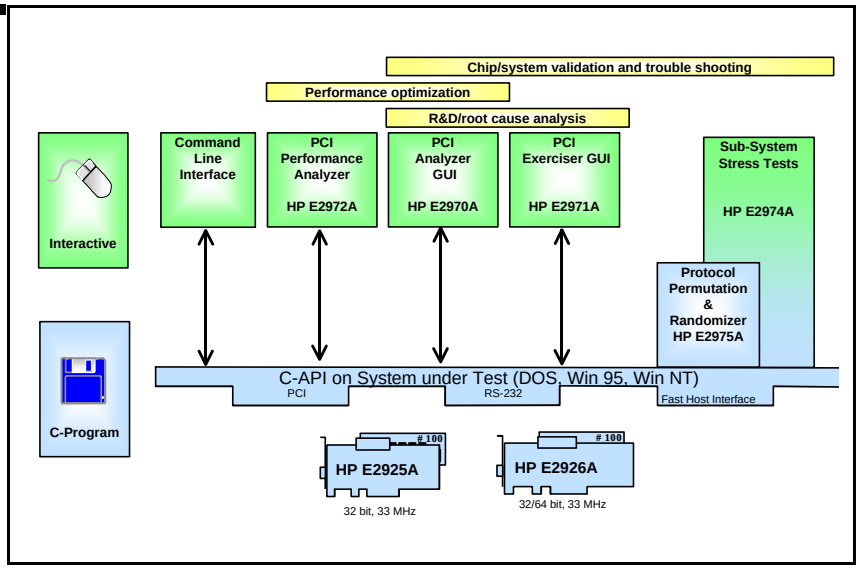


Figure 1. The HP E2920 PCI Series

Key Benefits

- Predictable test environment to verify computer systems under various stress conditions.
- Faster design verification at corner cases.
- Simplified analysis of PCI traffic and protocol violations.
- Integral part of a test environment.

Key Features

- Fully programmable PCI master and target.
- Full 64 bit data/address support (master, target, analyzer).
- 512 KB on-board data memory.
- 64 K/4 M (optional) state PCI logic analyzer trace memory.
- 24 pattern terms.
- 64-level trigger sequencer.
- Real-time protocol check.
- 8 real-time counters.
- Real-time data compare.
- C-Application Programming Interface.
- On-board CPU with built-in test functions.
- Application oriented graphical user interfaces and software packages addressing the complete design cycle available.
- In-system programmable by PCI.
- External control by RS232 or optional 4 MB/s fast host interface.

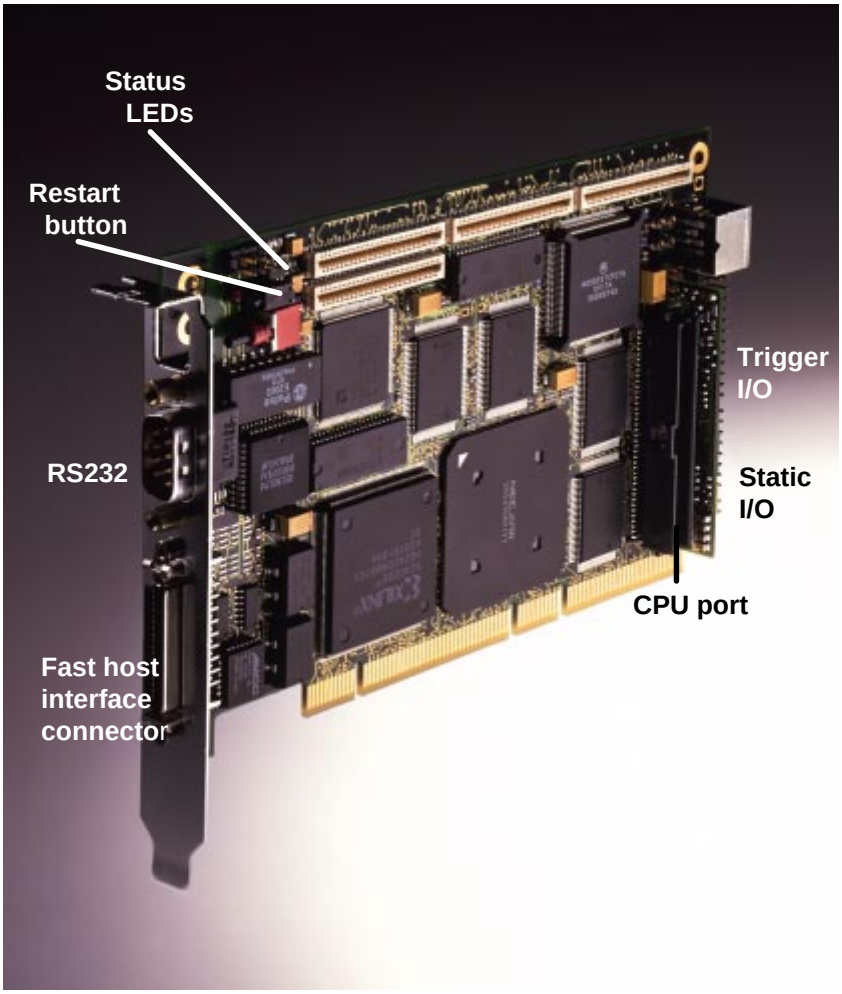


Figure 2. The HP E2926A PCI Exerciser and Analyzer

For interactive debugging, use the:

- HP E2970A PCI Analyzer GUI,
- HP E2971A PCI Exerciser GUI,
- HP E2972A PCI Performance Analyzer GUI.

To intensify testing with easy-to-run test functions and for exhaustive PCI protocol verification during system validation in research and development and quality assurance, use the:

- HP E2974A Sub-System Stress Tests,
- HP E2975A PCI Protocol Permutator and Randomizer.

Bring-up and debug PCI designs
During bring-up and debug phases, the analyzer part of the HP E2926A is used to seamlessly observe design behavior, detect protocol violations or to analyze performance. The exerciser is used to set up controlled bus transfers when isolating problem cases.

PCI based design verification
For in-depth verification of PCI chips, cards or systems, a fully controllable PCI master and target simplifies the debug and verification process. Rather than waiting until corner cases suddenly appear by plugging standard PCI cards back and forth, the HP E2926A's exerciser capabilities force the needed test scenarios in a deterministic and repeatable way. It also concurrently monitors and captures failures or performance data, at real-time when needed.

Integrates into your test environment
With its C-Application Programming Interface (C-API), the fully in-system programmable HP E2926A can be completely integrated into your test software for validating chips, cards and systems. The card is fully programmable via PCI from the system-under-test, or via RS232 or the optional fast host interface from an external test controller.

Analyzer Capabilities

The HP E2926A features real-time protocol check, real-time performance counters and built-in logic analyzer capabilities to analyze a system through the PCI bus, as well as the PCI bus itself. Controlled by the C-API or by one of the optional HP E2920 PCI series software packages, the HP E2926A acquires the data needed for PCI protocol compliance check, as well as for in-depth system analysis.

PCI protocol checker
The HP E2926A simultaneously monitors 53 PCI protocol rules in real-time. Each rule can be individually masked to suppress the triggering of known problems. The 53 rules are defined to find practically any thinkable misbehavior of the PCI protocol, based on PCI Spec Rev. 2.1 Chapter 3 'Bus Operation' and Appendix C 'Operating Rules'.

When a protocol violation is detected, the protocol checker can:

- directly trigger the state analyzer trace memory,
- store the rule number of the first (non-masked) violated rule,
- count protocol errors.

Real-time counters
To count at real-time up to seven individual events and eight counters are supported. All counters have virtually infinite depth.

PCI state analyzer
The on-board PCI state analyzer provides a 64K/4 M (optional) state logic analyzer optimized for monitoring and capture on the PCI bus, with visibility of:

- all PCI bus signals, except JTAG signals,
- protocol error,
- data miscompare,
- decoded bus state signals, time-aligned to the bus signals,
- master and target active signals, aligned to the bus signals for easy identification of transactions involving the HP E2926A,
- twelve input signals from the external trigger I/O connector.

Pattern terms
24 pattern terms monitor:

- all PCI bus signals, except JTAG signals,
- 12 input signals from the external trigger I/O connector,
- all static I/O lines,
- protocol error,
- data miscompare,
- all bus observer signals.

To set up a standard pattern, each individual bit can be masked 0/1/x. For bit fields ,such as C/BE, all bit combinations can be defined individually. Addresses can be specified as a range.

Easy triggering
The HP E2926A bus observer provides very easy triggering setup using only one pattern term for most PCI transactions. The bus observer automatically detects:

- idle bus cycles,
- (dual) address phases,
- decode cycles and decode speed,
- wait and data cycles,
- where a data burst is interrupted,
- how data phases are terminated,
- back-to-back transfers,
- dword ordering,
- the type of command used,
- exclusive access,
- 64 bit data transfer requests,
- the actual PCI address used.

Whether the detected state should be stored is defined with the additional 0/1/x compare or the transitional pattern term.

64-level trigger sequencer
For extended trigger scenarios, the HP E2926A features a trigger machine, which flexibly handles up to eight pattern terms, one termination counter and up to 64 levels of trigger sequencing.

Sequence levels	Available Patterns/Counter
1	up to 8
2	up to 7
3..4	up to 6
5..8	up to 5
9..16	up to 4
17..32	up to 3
33..64	up to 2

Pattern terms can be combined by the logical operations AND, OR, EXOR and NEGATION. The termination counter can be pre-loaded and decrement.

Flexible trigger points
For maximum flexibility, the trigger can be placed in any position in the trace memory.

Exerciser Capabilities

The HP E2926A can emulate and force practically any thinkable behavior of a PCI device - except blatant protocol violations.

Target and master can handle:

- 32/64 bit data and 64 bit addressing,
- fast decode,
- fast back-to-back,
- exclusive access,
- programmable delay between transactions,
- burst lengths from 1 to 2,000,000,000 dwords,
- all 16 PCI command types,
- real-time data compare.

Target capabilities
The HP E2926A provides a programmable PCI target for emulating missing devices and generating protocol and traffic variations. You can completely control the following:

- The protocol behavior per data phase.
- The data content of read transfers from the on-board data memory.
- The decoders to map any PCI address to the on-board data resources as data memory, configuration space, mailbox registers, expansion ROM and programming registers.

Target decoders
Six individual target decoders can be programmed. Each can map any PCI address range to the on-board data memory, data compare memory, configuration space, expansion ROM, internal mailbox or programming registers, CPU port one or two, and static I/O port.

The decoders support:

- 32/64 bit address space,
- 0/1/x masks for address ranges,
- programmable subset of commands,
- fast/medium/slow decode speed.

In addition, one decoder is provided to decode each of the following:

- expansion ROM,
- configuration type 0,
- configuration type 0/1,
- subtractive decoding.

Target protocol attributes
You can define the target protocol behavior to any data memory access by setting up linear sequence/repeat loops of protocol attributes. A maximum of 255 independent entries is allowed. Each entry in a sequence controls the protocol behavior for a single data phase during access to the target. Attributes are either used sequentially for each phase or permutated during a transfer. You can also choose whether the target automatically restarts at the beginning each time it is accessed (new master address phase) or continues with the next entry to simulate the behavior of FIFOs.

Attributes are provided to:

- accept or don't accept 64 bit data,
- force SERR# associated to the data phase, the second clock of the dual address cycle or the address cycle,
- insert 0 - 30 target wait states or hanging TRDY#,
- terminate transaction (no, retry, disconnect, abort),
- force PERR#,
- invert PAR and/or PAR64 in the data phase.

Target latencies
The HP E2926A target accepts zero wait state writes. It also accepts zero wait state reads when the transaction address follows the address of the last dword read from the target, readings from the HP E2926A require six waits or the initial data phase otherwise.

Master	Direct	Address follows last transaction (prefetch)	Min. initial latencies	Min. subsequ. latencies
Idle	Write	Don't care	0	0
	Read	Yes	1	0
		No	7	0
	Write compare	Yes	1	0
		No	7	0
Transfer intended	Don't care		<16, typ 8	0

Master capabilities
The HP E2926A provides a programmable PCI master, which is capable of generating practically any thinkable PCI protocol and traffic behavior or traffic variation. You can completely control the following:

- The number and type of master data transfers which should take place, by setting up a sequence of master block transfers.

- The transaction and protocol behavior which should be used during the data transfer, on a phase-by-phase basis, by setting up master protocol attributes.
- A single, repetitive or conditional start of the block transfer.
- The data content of write transfers from the on-board data memory.

Master block transfers
A master block transfer defines which PCI address space is accessed, and where data is moved to.

Up to 255 block transfers can be defined and are performed in a linear sequence. Each block transfer specifies:

- the PCI command type to be used (0000\b to 1111\b),
- dual address cycle (yes/no),
- the 32/64 bit PCI address to be accessed,
- the number of dwords (1 to 2,000,000,000 equivalent to 8 GB) which can be transferred,
- if a fixed byte enabled value (C/BE[3::0]/C/BE[4::7]) is used, or if a sequence of byte enabled values should be used during the transfer,
- the internal data memory dword address to be used for read/write or compare data,
- which protocol behavior is to be used.
- The time between two block transfers is user programmable. The minimum is 15 clock cycles.

Master attributes
Master protocol behavior can be specified per address/data phase, by setting up linear sequences/ repeat loops of protocol attributes. Up to 255 attribute entries are allowed. Attributes are available to:

- perform 32 or 64 bit address and/or data access,
- try fast back-to-back transaction,
- perform 0-15 address steps,
- control LOCK (no, lock, hide, unlock),
- insert 0 to 2,000,000 clock delay between transactions
- re-assert REQ# 2 to 127 clock cycles after a target termination,
- release REQ# 0 to 14 cycles after the address/data phase or keep it asserted,
- force SERR# associated to the address phase, the second clock of the dual address phase or the data phase,
- invert PAR and/or PAR64 during the address phase, the second clock of the dual address phase or the data phase,
- insert 0 - 30 master wait states or hanging IRDY#,
- force PERR# during the data phase,
- force master to terminate burst and continue with a new address phase.

Data Memory

The HP E2926A features a 512 KB programmable read/write data memory (organized 64K x 2 dwords). Master and target share the memory. Multiple address decoders can selectively address it.

The data memory can:

- store data from read/write transfers,
- be mapped to any PCI address space,
- be utilized for hardware data compare with current content when data is written to this memory.

Configuration Space

The HP E2926A provides a fully programmable PCI configuration space. Default values (customizable) are stored in the EEPROM of the on-board CPU and are used to initialize the configuration space following power-up. The configuration space can be disabled, making the card invisible to BIOS or O/S configuration routines.

Mailbox registers

The HP E2926A features two 32 bit mailbox registers, designed to allow an external test controller program (connected via RS232 or optional fast host interface) to communicate with a test program running on the system-under-test.

Additional I/O Ports

Static I/O signals
Eight static I/O pins are available for observing or controlling additional signals beyond PCI as part of the test. Each pin can be configured as an input, a totem pole, or as an open drain output. The outputs can be set under program control as either high or low.

External trigger I/O
12 trigger I/O signals provide a way to synchronize between multiple HP E2926A modules and REQ#/GNT# lines of other PCI devices or other test equipment. Programmed as input pins, they are observed by the analyzer and available as part of its pattern terms. The trigger sequencer controls output signals.

CPU port
The CPU port is designed to allow the test program to control and initialize registers in a device or system-under-test via a simple parallel bus interface. It provides:

- 16 bit address bus,
- 16 bit data bus,
- two byte enables,
- two chip select signals,
- write enable,
- read enable,
- ready,
- reset,
- interrupt,
- CPU clock (16 MHz).

Built-in Test Functions

The on-board CPU makes a number of built-in test functions available, designed to quickly and easily intensify existing tests by adding additional asynchronous background traffic to the system.

- **Make Traffic**: master generates bursts of various lengths to its own target in order to load the arbiter and decrease the available bandwidth for other PCI masters without influencing the system's resources.
- **Write/Read/Compare**: this test function continuously writes a block of data from the on-board memory to an external target, reads it back, and can, as an option, compare the results with the original data. The test stops on miscompare.
- **Block Move**: this test function continuously reads a block of data from one target address and writes it to another using the on-board memory as an intermediate buffer.
- **Protocol Error Detect**: sets up the protocol checker to trigger the analyzer if a protocol error occurs.
- **Dump Result**: stores the analyzer's and protocol checker's status to a file, including the trace memory. The file can then be analyzed later using the HP E2970A PCI Analyzer Graphical User Interface for Windows 95/NT.

C-Application Programming Interface

The C-Application Programming Interface (C-API) is a library of C functions which provides a programming interface for setting up and controlling the HP E2926A as part of your own test programs. The test program can be running on the system-under-test itself or on an external controller because the C-API can control the HP E2926A via its PCI, RS232, or optional 4MB/s fast host interface. Drivers are provided for each interface, which allow the C-API to be used under DOS, Windows NT 3.51 and 4.0, or Windows 95.

	Windows 95®	Windows NT®	DOS
RS232	Yes	Yes	Yes
PCI [1]	Yes [2]	Yes	Yes
Fast host interface	Yes [2]	Yes	No

[1] Works @ PCI clock of ≥ 32.5 MHz.
[2] Available in Q4 1998.

The library functions are divided into groups, which allow you to set up and control the various capabilities of the HP E2926A, such as:

- connection functions,
- master block transfer functions,
- master protocol behavior,
- master generic property functions,
- target decoder functions,
- target protocol behavior functions,
- protocol checker functions,
- state analyzer functions,
- host to PCI access functions,
- static I/O functions,
- CPU port functions,
- configuration space functions,
- expansion ROM functions,
- status functions,
- mailbox functions,
- built-in test functions.

Command Line Interface

The HP E2926A is supplied with a Command Line User Interface (CLI) which runs under Windows 95/NT. This allows you to interactively control the HP E2926A from an external PC by entering command functions that correspond with the functions provided by the C-API. The CLI can also process batch files of concatenated command functions. The CLI is intended to provide a programmer with a means of controlling the card interactively, while developing test programs using the C-API.

General PCI Specifications

Bit size: 32/64 bit PCI bus.
Power: operates from DC to 33 MHz.

Timing specifications: Meets PCI Spec 2.1

	Min.	Max.
Tval	2 ns	11 ns
Ton	2 ns	
Toff		28 ns
Tsu	7 ns	
Tsu(ppt)	7 ns	
Th	0 ns	
@ temperatures of-40°C to +50°C		

Signaling environment: supports 5 V and 3.3 V.
Decoupling: unused 3.3 V power pins are decoupled.
Power requirements: consumes < 25 W from the PCI slot, unless the optional external power supply is used.
Trace length limits: meets PCI specifications.
Signal loading: 10 pF.
Operating temperature:-40°C to +50°C.
Mechanical dimensions: standard PCI short card, occupying one slot. In conjunction with the HP logic analyzer adapters (003/004), the neighbor slot is blocked and not accessible.

Static I/O signals and CPU port: 3.3V CMOS 74LVT I/O drivers, compatible to 5V TTL.
Flat cable connector.

Ordering Information

The HP E2926A 32/64 bit, 33 MHz PCI Exerciser and Analyzer includes:

- 32/64 bit, 33 MHz PCI Exerciser and Analyzer Card,
- C-Application Programming Interface software,
- Command Line Interface (CLI) software for Windows 95/NT.

In addition, the following options are available.

4 MB/s Fast Host Interface (002)
For applications requiring extensive data download/upload from an external host, controlling the system-under-test. This option includes a PCI card to be plugged into the controlling host PC and a cable to be connected between the HP E2926A, external host and software drivers. Requires one free 32 bit PCI slot and Windows NT.

HP Logic Analyzer Adapter (003)
This add-on daughter card provides all of the on-board PCI analyzer signals with the appropriate terminations and connectors to connect straight to an external HP Logic Analyzer. This is useful if you want to observe the PCI bus state in context with other buses or interfaces in the system-under- test.

Generic Logic Analyzer Adapter (004)
This Generic Logic Analyzer Adapter provides all of the on-board PCI analyzer signals to connect directly to any external logic analyzer. Appropriate terminators, depending on the selected logic analyzer, have to be added.

4 M Memory Board (100)
This option enhances the HP E2926A by providing 1 M trace memory for the PCI State Logic Analyzer. The board is customer installable and is required when using the HP E2972A PCI Performance Analyzer software package. Option 002 is also recommended.
(Available in the fourth quarter of 1998)

Related HP Literature

- HP E2920 Computer Verification Tools, PCI Series, brochure, p/n 5965-4723E.
- HP E2920 PCI Performance Multimedia CD, p/n 5965-5882E.
- HP E2970A PCI Analyzer Graphical User Interface for Windows 95/NT, technical specifications, p/n 5965-4726E.
- HP E2971A PCI Exerciser Graphical User Interface for Windows 95/NT, technical specifications, p/n 5965-4725E.
- HP E2972A PCI Performance Analyzer, technical specifications, p/n 5965-8008E.
- HP E2974A Sub-System Stress Tests, technical specifications, p/n 5965-8009E.
- HP E2975A PCI Permutator and Randomizer, technical specifications, p/n 5965-8010E.
- HP E2925A 32 Bit, 33 MHz PCI Exerciser and Analyzer, p/n 5965-4724E.
- HP E2924A PCI Host Interface Adapter, technical specifications, p/n 5966-4828E.
- HP E2979A Software License for Multiple Test Benches, p/n 5966-4759E.

For more technical information on C-API programming, application notes, and technical documentation, please refer to:
http://www.hp.com/go/dvt

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