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Agilent E2925B 32 bit, 33 MHz

PCI Exerciser and Analyzer

Technical Overview

Agilent E2920 Computer Verification Tools, PCI Series

The Agilent Technologies E2925B PCI Exerciser and Analyzer is a single-slot 3U card, offering a complete PCI state analyzer, real-time protocol check, timing check, and bus performance statistics. The optional on-board exerciser contains a fully controllable PCI master and target.

State of the art design verification

The E2925B is a ready-to-use solution for PCI system bring-up, system verification, and performance measurements. The application tailored software of the E2925B makes it easy to use.

Fast and easy to use

An intuitive Windows 98/2000 Graphical User Interface allows easy and fast operation. A hierarchical structure, from higher-level transaction-oriented listers down to a logic analyzer known-waveform viewer, makes the PCI Exerciser and Analyzer suitable for hardware designers as well as for software developers.

Fully scalable solution

The E2925B are fully scalable from just an analyzer to a complete exerciser and analyzer system. Trace memory can be expanded up to 155 x 4MB. PCI load is always <10pF, and thus does not alter timing analysis.

Analyzer Capabilities

The E2925B configuration supports:

- Short PCI form factor
- 33 MHz PCI Analyzer
- Full 32 respectively 32/64 bit PCI data/address and command support
- Real-time PCI protocol check
- Real-time timing check
- Setup and hold time analysis with 250ps resolution
- Real-time bus performance statistics
- 64K PCI state logic analyzer
- 24 pattern terms
- 64-level trigger sequencer
- PCI Analyzer Graphical User Interface

PCI protocol checker

Fifty-three PCI protocol rules are simultaneously monitored in real time. This includes 32 as well as 64 bit-related signals and PCI commands.

Each rule can be individually masked to suppress the triggering of known problems. The 53 rules are defined to find any thinkable misbehavior of the PCI protocol, based on PCI Spec Rev. 2.1 Chapter 3 “Bus Operation” and Appendix C “Operating Rules.”

When a protocol violation is detected, the protocol checker can:

- directly trigger the state analyzer trace memory,
- store the rule number of the first (non-masked) violated rule,
- list all found protocol errors, and
- accumulate the number of violated rules.

Key features

E2925B/E2926B basic configuration:

- Full 32 respectively 32/64 bit data/address support
- 33 MHz PCI Analyzer
- Supports all PCI signals
- 155 x 64K PCI state logic analyzer trace memory
- 24 pattern terms
- 64-level trigger sequencer
- Real-time protocol check
- Timing check and analysis with 250ps resolution
- Performance analysis
- External controlled by RS-232 or 4MB fast parallel interface
- In-system controllable through PCI

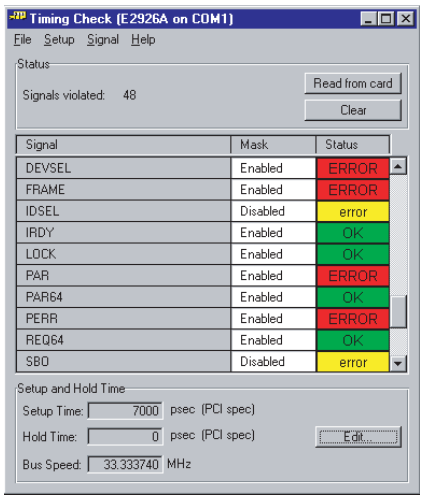
Optional:

- On-board 33 MHz PCI Exerciser
- Fully programmable PCI master and target
- 512 KB on-board data memory
- 155 x 4M trace memory
- C-Application Programming Interface
- PCI Protocol Permutation
- System Validation Pack
- PCI Performance optimizer

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Timing Checker



The timing checker observes all 32 respectively 32/64 PCI signal and checks for setup and hold time violations. It works simultaneously but independently of the protocol check.

It supports:

- direct trigger of the state analyzer trace memory,
- storage of the rule number of the first (non-masked) violated rule,
- listing of all found timing violations,
- 250ps accuracy (typ.),
- simultaneous checks of all 32 and 64 bit PCI signals,
- automatic checks against PCI timing specification of 7 ns setup time at 33 MHz PCI clock and 0 ns hold time, and
- manual adjust of setup and hold time reference point by ±2ns, in 250ps steps.

The ability to manually adjust the setup and hold time in 250ps steps allows margin tests, concurrently on all PCI signals.

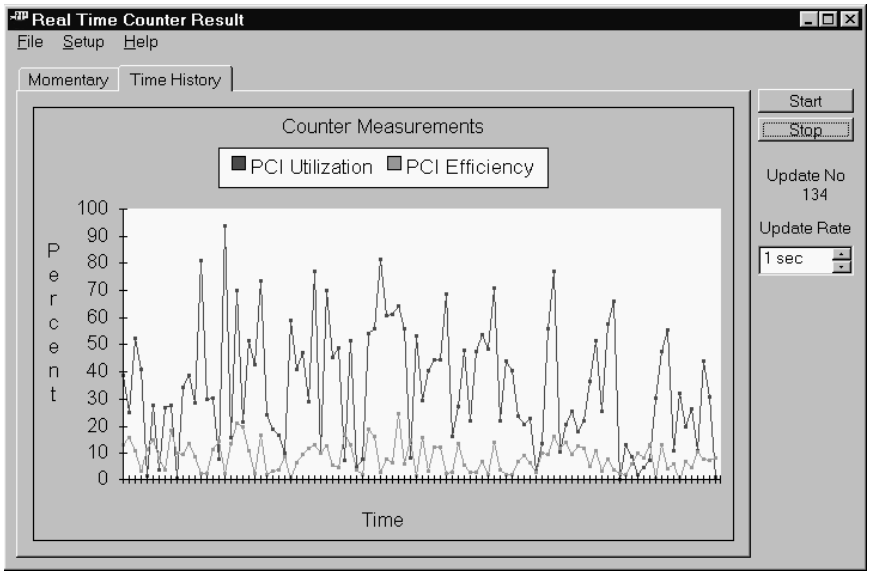
Real-time bus performance statistics

The Agilent PCI Analyzer offers four predefined ready-to-run bus performance measures:

- PCI throughput
- PCI bus utilization
- PCI efficiency
- retry rate

In addition, customer-defined measures can be setup. Measurements from simple event counting to comprehensive measurements using the Analyzer trigger sequencer capabilities are possible.

All performance measures are based on virtual infinite depth counters, allowing non-interrupted long-time measures.



PCI state analyzer

The on-board PCI state analyzer observes all signals (except JTAG) specified by the PCI specification for a 32 respectively 32/64 bit PCI system. In detail, the analyzer captures:

- all 32 respectively 32/64 bit PCI address/data signals,
- PCI protocol error,
- PCI timing violation,
- data miscompare,
- decoded bus state signals, time-aligned to the bus signals,
- master and target active signals, aligned to the bus signals for easy identification of transactions involving the exerciser, and
- 12 input signals from the external trigger I/O connector.

A simple push-button storage qualification selects storage qualifiers to tune the use of the state analyzer memory, depending on the level of detail you need. You can, for example:

- store all states,
- store only particular bus transactions by command type, or combinations thereof,
- suppress idle cycles,
- suppress wait cycles,
- suppress data transfers.

Pattern terms

Twenty-four pattern terms can be monitored:

- all PCI bus signals, except JTAG signals
- all trigger inputs
- the protocol checker error signals
- data miscompare
- the bus observer

To set up a standard pattern, each individual bit can be masked 0/1/x. For bit fields, such as C/BE, all bit combinations can be defined individually. Addresses can be specified as a range.

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Easy triggering

The bus observer allows easy analyzer triggering for most applications by defining only one simple pattern term. The bus observer automatically detects:

- idle bus cycles,
- (dual) address phases,
- decode cycles and decode speed,
- wait and data cycles,
- where a data burst is interrupted,
- how data phases are terminated,
- fast back-to-back transfers,
- dword ordering,
- the type of command used,
- exclusive access,
- 64 bit data transfer requests, and
- the actual PCI address used.

Whether the detected state should be stored is defined with the additional 0/1/x compare or the transitional pattern term.

64-level trigger sequencer

For extended trigger scenarios, the Exerciser features a trigger machine, which flexibly handles up to eight pattern terms, one termination counter, and up to 64 levels of trigger sequencing.

Sequence levels	Available Patterns/Counter
1	up to 8
2	up to 7
3..4	up to 6
5..8	up to 5
9..16	up to 4
17..32	up to 3
33..64	up to 2

Pattern terms can be combined by the logical operations AND, OR, EXOR, and NEGATION. The termination counter can be preloaded and decremented.

Flexible trigger points

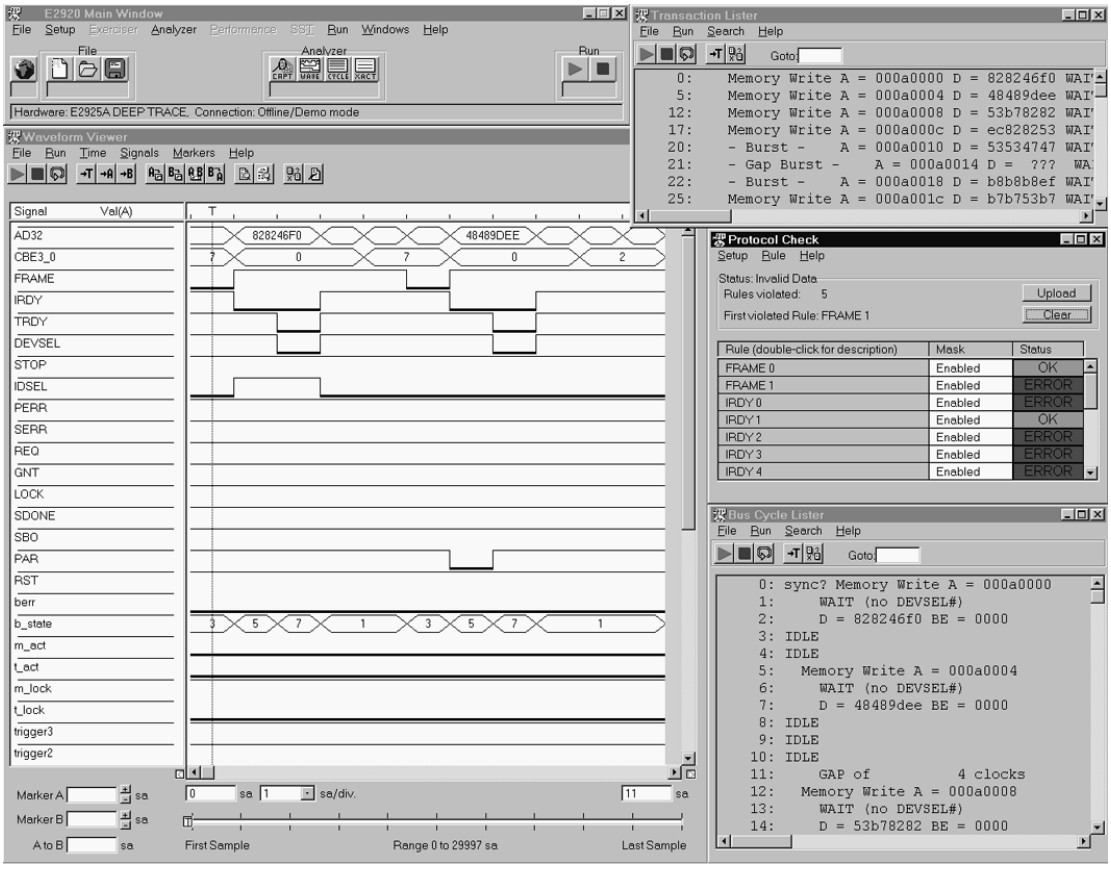
For maximum flexibility, the trigger can be placed in any position in the trace memory.

Configuration Space

The PCI Analyzer provides a fully programmable PCI configuration space. Default values (customizable) are stored in the EEPROM of the on-board CPU and are used to initialize the configuration space following power-up. The configuration space can be disabled, making the card invisible to BIOS or O/S configuration routines.

External trigger I/O

Twelve trigger I/O signals provide a way to synchronize between multiple Agilent PCI Exerciser and Analyzer cards, REQ# and GNT# lines of other PCI devices, or other test equipment. Programmed as input pins, they are observed by the analyzer and available as part of its pattern terms. Trigger I/Os are controlled through Command Line Interface (CLI).



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PCI Performance Optimizer (option 200)

In addition to the standard real-time performance measurements provided by the Agilent E2925Ban optional software package is available, which extends the performance measurement capabilities by combining real-time measurements with in-depth post processed statistical performance analysis. For this analysis, one or multiple bus snapshots are taken by the PCI analyzer.

Optimize system performance

Statistical PCI Performance analysis makes it easy to select the best PCI cards and components, detect and locate PCI performance bottlenecks, and balance system settings so that the overall performance of the system is optimized.

A hierarchical approach to analyzing real-time and post-processing performance measurements is used. This means that the E2925B can move swiftly from high-level throughput numbers to, for example, PCI command usage and latency measurements, as required. It is therefore simple to identify design issues and analyze their causes. Overall, this approach reduces the effort required in revealing design problems.

- Graphical and text-based presentation
- In-depth performance analysis through post-processing
- Differential storage qualifier to optimize trace memory usage
- Incorporates the E2925B standard real-time measures for:
  - PCI efficiency
  - PCI throughput
  - PCI utilization
  - Retry rate
- Latency measurement
- First word latency of split transaction (PCI spec 2.1)
- Activity lister with time stamp
- Reveals target, master, and arbiter contribution to performance measurement results
- Measures overall traffic and selective for master/target pair
- Report generation
- Cross-references to PCI Analyzer Graphical User Interface

Post-Processed Data Analysis

The E2925B can carry out an in-depth performance analysis of sampled PCI transactions by using the PCI Analyzer to acquire data.

To optimize the usage of trace memory, the differential storage qualifier is set up to automatically select the data needed for the performance measurement.

Basic bus statistics

To obtain an overall picture of the PCI performance, the PCI bus is analyzed for:

- PCI throughput
- PCI utilization
- non-retry utilization
- PCI efficiency
- PCI non-retry efficiency
- PCI data efficiency
- retry overhead

A bus efficiency chart provides an overview of how efficiently the traffic was handled between different bus agents.

Bus utilization

The bus utilization analysis shows how the PCI bus was used by:

- data transfer
- overhead
- retry

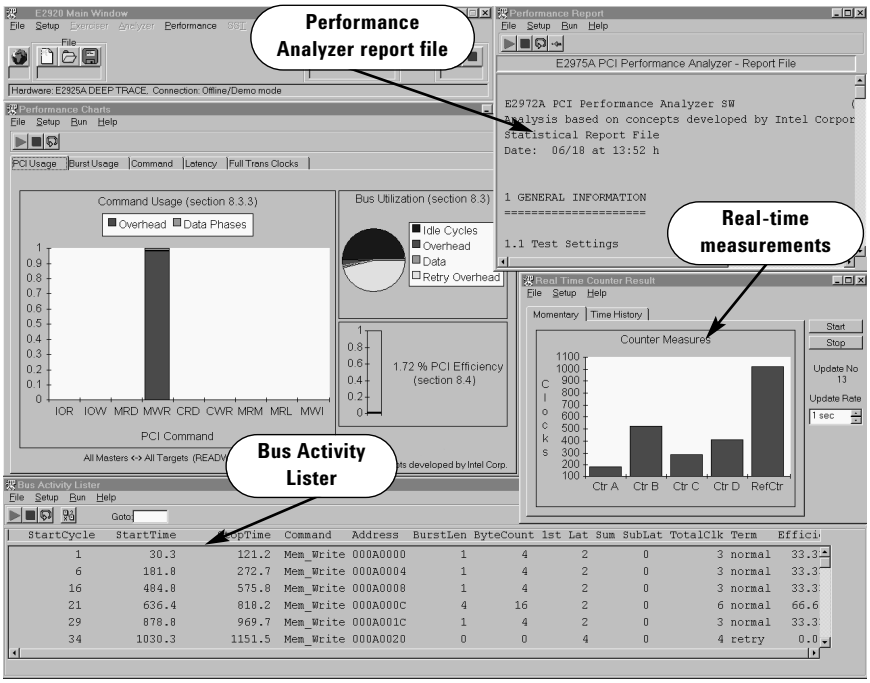
A utilization chart shows how the different bus agents used the bus.

Interrupt latency

Interrupt latencies are evaluated in detail by measuring:

- average interrupt latency; individually for INT A, B, C, D, and
- overall interrupt latency; the interrupt latency is calculated as a weighted average of INT A, B, C, and D.

An interrupt latency histogram shows the distribution of the individual interrupts over clock cycles.



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Master/Target Performance
Post-processing allows the analysis of customer-selected master/target combinations so that specific master/target performance behavior can be analyzed in depth. By evaluating the critical agents using the real-time measurements and basic bus statistics, the in-depth master/target analysis provides an "inside view" of how to optimize single agents.

Master/target bus usage
The bus usage measurements show:

- Master was waiting for GNT# but bus was idle.
- Master was waiting for GNT# but bus was busy.
- Bus occupation by selected master/target, split into retry overhead, transfer overhead, and data phases
- Data phase statistics, showing the distribution of byte enable
- Average byte enable efficiency
- Average decode speed

Wait cycle histogram
A wait cycle histogram shows wait cycles caused by the master and target.

Burst length distribution
As well as displaying the average overall burst length, this histogram also shows the distribution of burst length over PCI commands. Again, this provides an "inside view" into performance bottlenecks in PCI systems.

Command usage chart
The command usage chart lists the usage of different PCI commands so that performance issues caused by inefficient command usage are revealed.

Master/target efficiency
A further important indication for PCI system performance is how efficiently a certain master/target pair uses the occupied bus time. Thus, the software examines:

- master/target overall efficiency of transferred data,
- non-retry efficiency, and
- efficiency over burst length.

Termination statistics
The PCI termination statistics indicate:

- the average number of retries needed,
- termination by arbiter in favor of other bus agents, and
- termination over burst length.

Latency distribution
This histogram shows the following (over clock cycles):

- first word latency
- average latency
- arbiter latency
- bus access latency
- first word retry

Report and Result ASCII-File
All results are available as an ASCII report file for further analysis and customer post-processing.

The different segments are:

1 GENERAL INFORMATION
  1.1 Test Settings
  1.2 Statistical Base

2 BASIC BUS STATISTICS

3 BUS THROUGHPUT STATISTICS

4 EFFICIENCY STATISTICS
  4.1 Master Target Efficiency

5 BUS UTILIZATION STATISTICS
  5.1 Master Target Utilization

6 BUS USERS OVERVIEW

7 INTERRUPT STATISTICS
  7.1 Interrupt Latency Histogram

8 MASTER - TARGET PAIR: All Masters <-> All Targets (Read/ Write)
  8.1 Statistical Basis
  8.2 Bus Usage
  8.3 Bus Occupation
    8.3.1 Data Phase
    8.3.2 Time Overhead
    8.3.3 Command Usage
    8.3.4 Command Termination
    8.3.5 Wait Histogram
    8.3.6 Burst Length over Command
  8.4 Efficiency Statistics
    8.4.1 Efficiency over Burstlength
  8.5 Termination Statistics
    8.5.1 Termination Burst Histogram
  8.6 Latency Histogram

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PCI Exerciser (option #300)

The E2925B has an optional on-board 32/64 bit PCI exerciser. The exerciser operates at up to 33 MHz, and can emulate and force practically any thinkable behavior of a PCI device—except blatant protocol violations.

The exerciser comes with a graphical user interface (GUI) and a command line interface (CLI).

Target and master can handle:

- 32 respectively 32/64 bit data
- 64 bit addressing
- fast back-to-back
- exclusive access
- programmable delay between transactions
- burst lengths from 1 to 2,000,000,000 dwords
- all 16 PCI command types
- real-time data compare

Target capabilities

The PCI Exerciser provides a programmable PCI target for emulating missing devices and generating protocol and traffic variations. You can completely control:

- the protocol behavior per data phase,
- the data content of read transfers from the on-board data memory, and
- the decoders to map any PCI address to the on-board data resources as data memory, configuration space, mailbox registers, expansion ROM, and programming registers.

Target decoders

Six individual target decoders can be programmed. Each can map any PCI address range to the on-board data memory, data compare memory, configuration space, expansion ROM, internal mailbox or programming registers, CPU port one or two, and static I/O port.

The decoders support:

- 32/64 bit address space
- 0/1/x masks for address ranges
- programmable subset of commands
- fast/medium/slow decode speed

In addition, one decoder is provided to decode each of the following:

- expansion ROM
- configuration type 0
- configuration type 0/1
- subtractive decoding

Target protocol attributes

You can define the target protocol behavior to any data memory access by setting up linear sequence/repeat loops of protocol attributes. A maximum of 256 independent entries is allowed. Each entry in a sequence controls the protocol behavior for a single data phase during access to the target. Attributes are either used sequentially for each phase or permutated during a transfer. You can also choose whether the target automatically restarts at the beginning each time it is accessed (new master address phase) or continues with the next entry to simulate the behavior of FIFOs.

Attributes are provided to:

- force SERR# associated to the data phase, the second clock of the dual address cycle or the address cycle,
- insert 0–30 target wait states or hanging TRDY#,
- terminate transaction (no, retry, disconnect, abort),
- force PERR#, and
- invert PAR and/or PAR64 in the data phase.

Target latencies

The Exerciser accepts zero wait state writes. It accepts zero wait state reads when the transaction address follows the address of the last dword read from the target. Otherwise reads require six waits or the initial data phase. (See Table 1, Target Latency.)

Master capabilities

The Exerciser provides a programmable PCI master, which is capable of generating practically any thinkable PCI protocol and traffic behavior or traffic variation. You can completely control:

- The number and type of master data transfers which should take place, by setting up a sequence of master block transfers.
- The transaction and protocol behavior which should be used during the data transfer, on a phase-by-phase basis, by setting up master protocol attributes.
- A single, repetitive or conditional start of the block transfer.
- The data content of write transfers from the on-board data memory.

Table 1. Target Latency

Exerciser Master	Direction	Address follows last transaction (Prefetch)	Minimum initial latencies	Minimum subsequent latencies
Idle	Write	Don't care	0	0
	Read	Yes	1	0
		No	7	0
	Write compare	Yes	1	0
		No	7	0
Transfer intended	Don't care		<16, typically 8	0

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Master block transfers

A master block transfer defines which PCI address space is accessed, and where data is moved to.

Up to 256 block transfers can be defined and are performed in a linear sequence. Each block transfer specifies:

- the PCI command type to be used (0000\b to 1111\b),
- dual address cycle (yes/no),
- the 32/64 bit PCI address to be accessed,
- the number of dwords to be transferred (1 to 2,000,000,000),
- if a fixed byte enable value (C/BE[3::0] / C/BE[4::7] is used, or if a sequence of byte enable values should be used during the transfer,
- the internal data memory dword address to be used for read/write or compare data, and
- which protocol behavior is to be used.

The time between two block transfers is user programmable. The minimum is 15 clock cycles.

Master attributes

Master protocol behavior can be specified per address/data phase, by setting up linear sequences/repeat loops of protocol attributes. Up to 256 attribute entries are allowed.

Attributes are available to:

- perform 32 or 64 bit address and/or data access,
- try fast back-to-back transaction,
- perform 0–15 address steps,
- control LOCK (no, lock, hide, unlock),
- insert 0 to 2,000,000 clock delay between transactions,
- reassert REQ# 2 to 127 clock cycles after a target termination,
- release REQ# 0 to 14 cycles after the address/data phase or keep it asserted,
- force SERR# associated to the address phase, the second clock of the dual address phase, or the data phase,
- invert PAR respectively PAR and/or PAR64 during the address phase, the second clock of the dual address phase, or the data phase,
- insert 0–30 master wait states or hanging IRDY#,
- force PERR# during the data phase, and
- force master to terminate burst and continue with a new address phase.

Data Memory

The E2925B features a 512 KB programmable read/write data memory (64K x 2 dwords). Master and target share the memory. Multiple address decoders can selectively address it. The data memory can:

- store data from read/write transfers,
- be mapped to any PCI address space, and
- be utilized for hardware data compare with current content when data is written to this memory.

Exerciser Graphical User Interface

The graphical user interface gives you an easy way to setup and control the exerciser. In conjunction with the Bus Transaction Description Language, you have a convenient way to force dedicated test cases by stimulating the needed PCI traffic.

PCI Bus Transaction Description Language (BTDL)

The BTDL gives you complete control over the traffic and protocol behavior of the exerciser. Optional parameters minimize your programming effort.

Master Transaction Editor

Use the transaction editor to set up a linear sequence of bus transactions. Choose between high-level block transfer commands or low level per data phase commands for the right level of abstraction or detail.

Block transfer command

This facilitates the movement of large blocks of data. Optionally, the underlying protocol can be specified in the master attribute editor.

Block parameter	Description
Busaddr	Start address on bus
Buscmd	PCI command used
Byten	C/BE[] in data phases
Nod	Number of transferred Dwords
Intaddr	Address of internal data memory
Compflag	Enables data compare
Compoffs	Internal address offset of reference data for comparison
Attrpage	Pointer to protocol behavior set

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Data phase commands

These are optimized for clear and easy control over the protocol behavior. They let you specify protocol attributes and data values per data phase, yet defaults can be set for a whole block transfer.

Protocol attribute	Description
stepmode	Generates four address steps with toggling AD[]
awrpar	Generates wrong PAR in address phase
aperr	Asserts SERR for address phase
lock	Generates exclusive access
relreq	De-asserts REQ#
waits	Inserts 0 to 31 wait cycles
waitmode	Generates data steps with toggling data
Dwrpar	Sets wrong PAR in data phase
Dperr	Asserts PERR in data phase
Dserr	Asserts SERR in data phase
Last	Terminates a transaction
ACK64	Accept 64 bit data transfer
REQ64	Request 64 bit data transfer

Master Attribute Editor

Use the master attribute editor to set up protocol behavior sets that are used during block transfers. Protocol attributes can be specified per data phase. When the end of a behavior set is reached, it jumps back to the start again.

Master Conditional Start

The master conditional start window lets you set up the start conditions for the master traffic. Following a run command, the master can be programmed to start:

- immediately
- triggered by a pattern
- delayed additionally by a number of PCI clock cycles

Data Memory Editor

The data memory editor lets you view and modify the contents of the PCI exerciser's on-board memory. This allows you to define the data content for master write transfers or target read accesses to the card, as well as to view the data received from master read transfers or target write accesses. The data can be viewed in hex format, big or little endian, and 8, 16, 32, or 64 bit size.

Target Attribute Editor

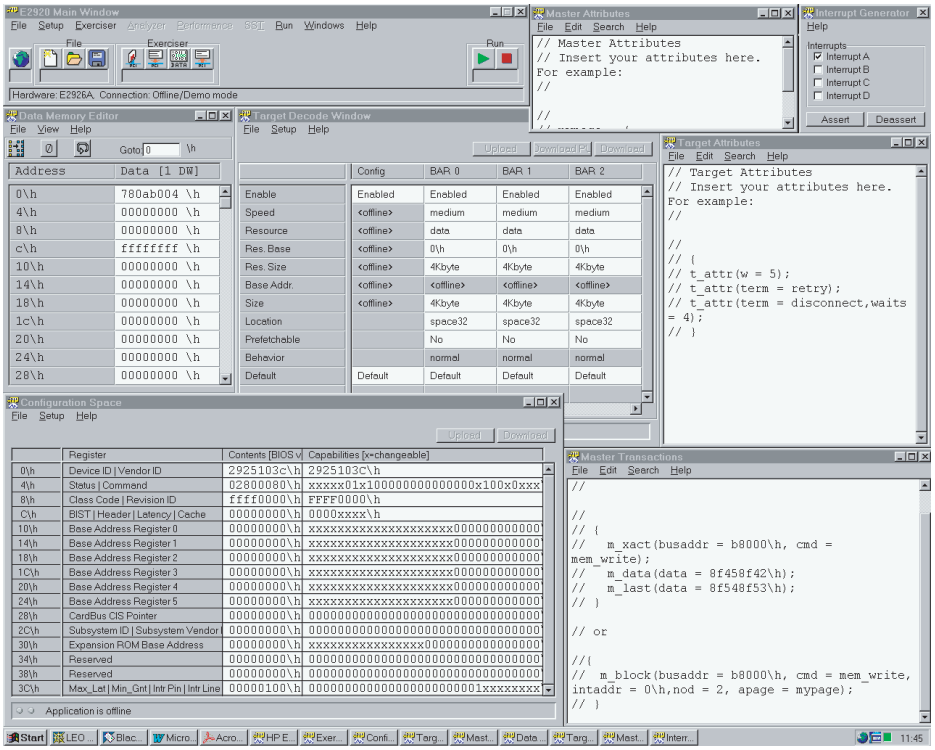
The target attribute editor lets you define the target's protocol behavior on a phase-by-phase basis. When the target is accessed, the attributes are used sequentially for each data phase. When the end is reached, it jumps back to the start. You can select whether the target should restart with each new transaction, or continue in the linear sequence.

Target Decode Window

The target decode window lets you configure the target address decoders. As well as configuring the programmable decoders for the exerciser's on-board memory, you can individually enable or disable the decoders for configuration space and expansion ROM.

Configuration Window

The configuration window lets you view and modify the current configuration space settings of the PCI exerciser and analyzer card. You can also store the current settings as defaults, which will then be used following all subsequent power cycles or PCI resets.



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Agilent System Validation Package #310

The System Validation Package is a ready-to-use software package, which performs system stress tests during the validation of servers, workstations, PCs, or other PCI/PCI-X based systems.

With its easy-to-use Windows-based GUI, it simplifies test development on setup for engineers and allows easy test execution by technicians.

Choosing the Agilent E2925B, E2928A, E2940A, E2929B option #310 adds the System Validation Package to your hardware order.

Target application

The System Validation Package programs and controls multiple PCI/PCI-X Exerciser and Analyzer test cards of the E2920 PCI Series to create realistic application system traffic. The test card approach allows you to set up fully predictable traffic scenarios and gives you measurable test coverage and test predictability. Used for validation of PCI/PCI-X based systems and silicon, it enhances the traditional test method of using off-the-shelf PCI/PCI-X cards.

Outstanding test coverage

Today's validation test methods typically lack time efficiency and repeatable execution of critical system traffic scenarios. Hot mock-up tests, which use off-the-shelf PCI cards to load a system-under-test and wait until an error occurs, are the typical test approaches used today. Now the E2976A executes such types of system critical tests within minutes, simply with a mouse click.

PPR, the key technology

Agilent's Protocol Permutation and Randomizing (PPR) technology is the key to predictable and repeatable test coverage. PPR is technology that allows permutation of the PCI/PCI-X protocol and traffic in a pseudo random way. Thus, system critical test patterns are not only transferred between different system components, but also automatically permutated to achieve all possible traffic scenarios.

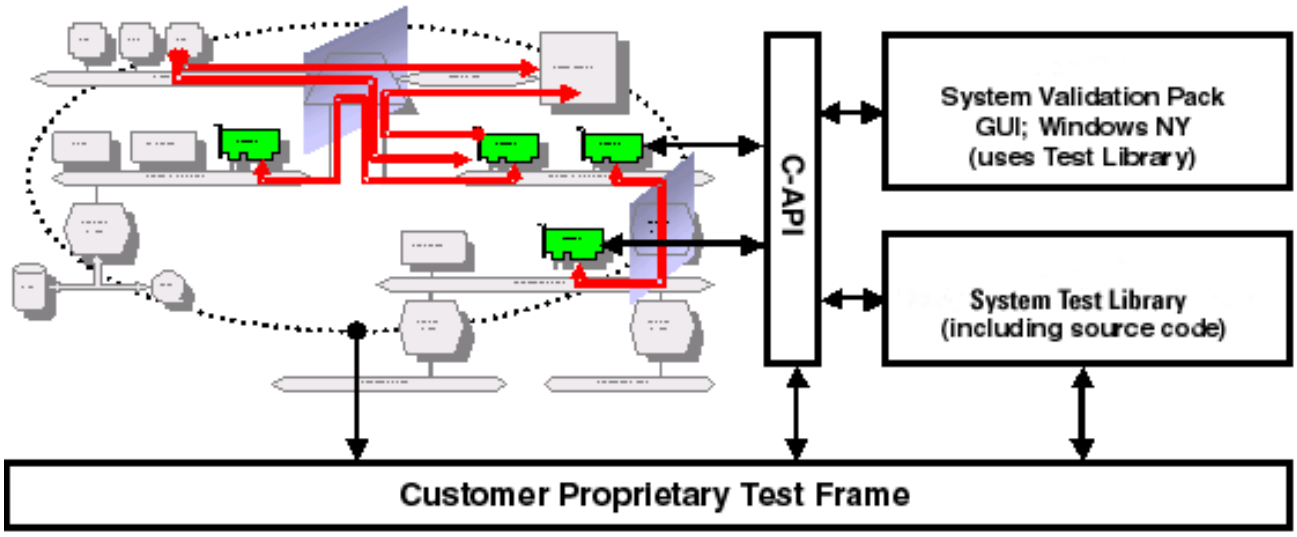
Stress all critical data paths

Just by plugging the PCI/PCI-X Exerciser and Analyzer test cards in each individual PCI/PCI-X bus of your system under test, the software is able to automatically test and stress data paths within your system (see system architecture diagram).

A small executable running on the system CPU(s) allows testing within the whole system, not only the I/O system.

System Validation Package/System Test Library benefits

- Fully controlled test environment for validation of servers, workstations and PCs
- Predictable test coverage
- Repeatable test scenarios
- Documented test results



System Architecture

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Test method

The Agilent System Validation Package allows automatic tests and stress data paths from:

- CPU and Exerciser to system memory
- Exerciser to system memory
- CPU to Exerciser memory space
- CPU to Exerciser I/O space
- Peer to peer traffic
- Master to target traffic

While testing, the setup emulates typical traffic scenarios in a PCI system. For example, data CPU to SCSI card, LAN to LAN card traffic, concurrent system memory access from LAN card and CPU (see Figure 2).

So far, these have been typical traffic scenarios and have been generated within the so-called hot mock-up test. Now the Agilent verification solution significantly extends this validation process by:

- Increasing test coverage through increased number of variations, when dealing with system traffic.
- Being programmable to force the system's most critical traffic conditions.
- Being repeatable for failure analysis and failure regression tasks.
- Being comparable, to achieve measurable quality improvements.
- Producing log files to catch the problems before the system hangs.
- Creating test reports to document system quality.
- Making an easy link to R&D's debug environment.

Any access from an Agilent Exerciser is permutated using PPR, varying block sizes, memory commands (write, read, write-invalidate, read line, read multiple), alignments, and byte-enables (meaning all variations of dword, word, and byte read/write accesses are used).

Protocol variations on all system actions include all possible waits (master and target), all possible terminations except target aborts (target only), both 64 bit and 32 bit accesses (master only) as well as acceptance/non-acceptance of 64 bit access (target only).

Automatic test setup

When starting the validation software on a system under test, it automatically scans the system for Agilent PCI/PCI-X Exerciser and Analyzer cards. Based on the available test cards, the operator can select various tests, define the test duration and start the test.

Customer configurable tests

All tests are configurable by the customer. The System Validation Package GUI shows all parameters, and all setups are simply done with a mouse click.

Thus, using different Exercisers to test between different buses, e.g. 33 MHz PCI and 133 MHz PCI-X, is easy. With each test, you just select the path to test, and define the data to be used. The software automatically communicates with the test card plugged into the corresponding bus and tells you which protocol/traffic parameters you may vary.

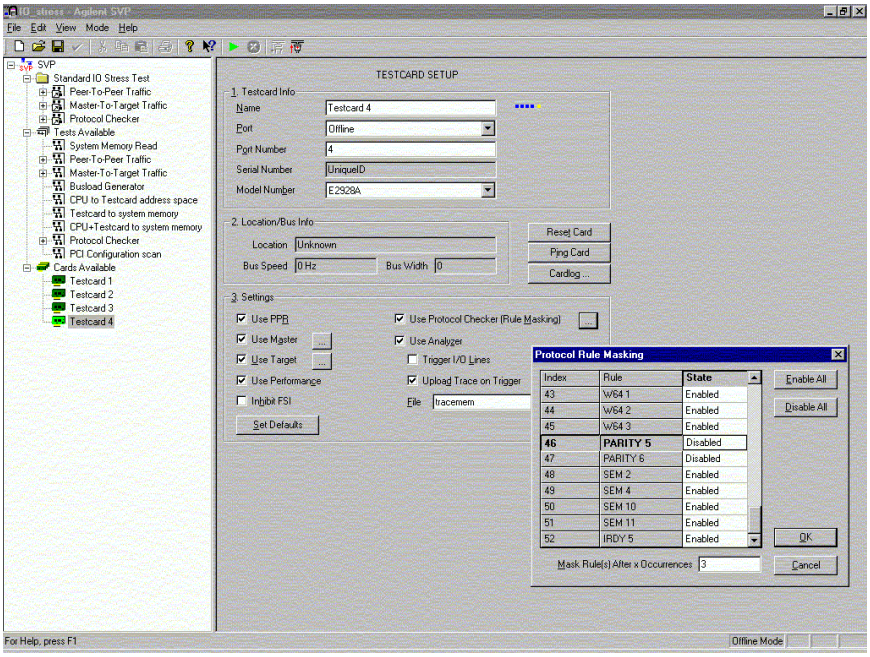


Figure 2. Test card setup

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Tests Available

PCISIG Compliance Tests

The Agilent System Validation Package includes a series of tests defined by the PCI Special Interest Group (PCI-SIG). Agilent Technologies has been working closely together with the PCI-SIG to provide compliance tests, which are utilized, for testing PCI and PCI-X systems at each PCI-SIG Compliance workshop. Agilent supplies the hardware and software to perform PCI-SIG compliance testing, including a PCI-SIG Compliance Test Library. The tests are used to verify that devices and systems are compliant to the PCI and PCI-X specifications. The tests are set up and run via the System Validation Package combined with either the PCI or PCI-X exerciser/analyzer test cards. These tests are in addition to the standard tests included or part of the System Validation Package option.

Description of the compliance tests:

- MLT - Master Latency Test
This test is not implemented as a special test within SVP but can be carried out manually. To do this, carry out the PCI configuration scan test (see "PCI Configuration Scan" on page 50) and examine the latency settings to determine the result of this test.

· SIG Post Test

This test is utilized to initialize the Base Address registers and to verify the address assignments. To do this, the test card is defined as target.

· SIG Interrupt Routing Test

The exerciser asserts an interrupt on request from the analyzer mailbox. To do this, the test card is defined as a master.
The SVP software requests an interrupt from the card and verifies that the interrupt was received and processed correctly.

· CPU to Test card Address and Test card to System Memory Address

This test accesses either the memory space or the I/O space of the test card from the CPU. To do this, the test card is defined as a target.
This test also accesses the system memory from the PCI or PCI-X bus. To do this, the test card is defined as a master and sends different write and read commands from/to the analyzer.

· SIG Card Test

The SIG Card test performs a number of tests. This includes testing for:
· Correct values and operation for the Command Register.
· The Status register.
· Appropriate values for other configuration registers.
The configuration register contents are displayed during the SIG Card test in the SVP Reporting window that opens when you run the test.

· PMTEST - Power Management Test

· TYPE1 - Type 1 Test

The Type 1 test verifies correct configuration transaction decoding by the device.

· DISCARD - Discard Test

This test verifies that the card correctly repeats retried PCI transactions.

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This test verifies that the card correctly repeats retried PCI transactions.

For more information about the PCI-SIG Compliance Program and the Agilent System Validation Package, please refer to www.agilent.com/find/pci_SVP or to www.pcisig.com

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Further Tests

Test description

The following list describes all tests available for the System Validation Package. All tests are customer configurable (see Table 2, page 12), and stress one data path. All tests can be performed concurrently to increase and maximize stress conditions. The PPR capabilities vary from Exerciser model to Exerciser model. For example, different protocol variations are available for PCI and PCI-X. Please refer to the corresponding technical data sheet of the Exerciser used for a list of available protocol variations.

CPU and Exerciser to system memory

Access system memory space via virtual memory from CPU and from PCI/PCI-X bus (Exerciser acting as master). The same address range with interleaved addresses is used in order to stress cache controller.

- **Tested data paths:** CPU to host memory; Exerciser to host bridge to system memory.
- **Tested devices:** Host bridge and host bridge configuration, host memory controller, and arbitration unit.

W/R/C to System Memory

Access the system memory from the PCI/PCI-X bus, and perform data write/data read/data compare.

- **Tested data paths:** Exerciser to host bridge to system memory
- **Tested devices:** Host bridge, host bridge configuration, host memory controller, and arbitration unit

Read from memory

This test reads repetitively from a customer-defined physical address to check accessibility and to stress the data path:

- **Tested data paths:** Exerciser to host bridge to system memory
- **Tested devices:** Host bridge, host bridge configuration, host memory controller, and arbitration unit

Peer-To-Peer Traffic

Two PCI Exerciser cards access each other's memory or I/O space. Master-target traffic in both directions is set up. Two test cards on different buses are used to test the bridges and bridge configuration.

- **Tested data path:** Exerciser #1 to bridge(s) to Exerciser #2
- **Tested devices:** Bridges, bridge configuration, and arbitration units

Master Target Traffic

Two PCI Exerciser cards access each other's memory or I/O space with unidirectional master-target traffic. Two test cards on different buses are used to test the bridges and bridge configuration.

- **Tested data path:** Exerciser #1 to bridge(s) to Exerciser #2
- **Tested devices:** Bridges, bridge configuration, arbitration units

CPU to test card

This test accesses either the test cards memory or I/O space via virtual memory from the CPU.

- **Tested data paths:** CPU to host bridge to test card
- **Tested devices:** Host bridge, host bridge configuration, host memory controller, and arbitration unit

Bus Load Generation

An Exerciser is set up to generate self-traffic and therefore saturate a bus with a defined level of traffic. This kind of test stresses other devices on the same bus by limiting the available time a certain device can get access to the bus. Also the arbitration unit can be verified under controlled bus load conditions.

Error Analysis

The Analyzer of an E2920 Series test card can be set up to check for:

- Protocol violations
- Data transfer errors
- Parity errors
- Bus hang-ups/bus locks
- Bus load measurements

Detected problems are logged in a report file. Optionally, a trace memory waveform file is generated for in-depth root cause analysis. All PCI/PCI-X devices on the bus are passively observed.

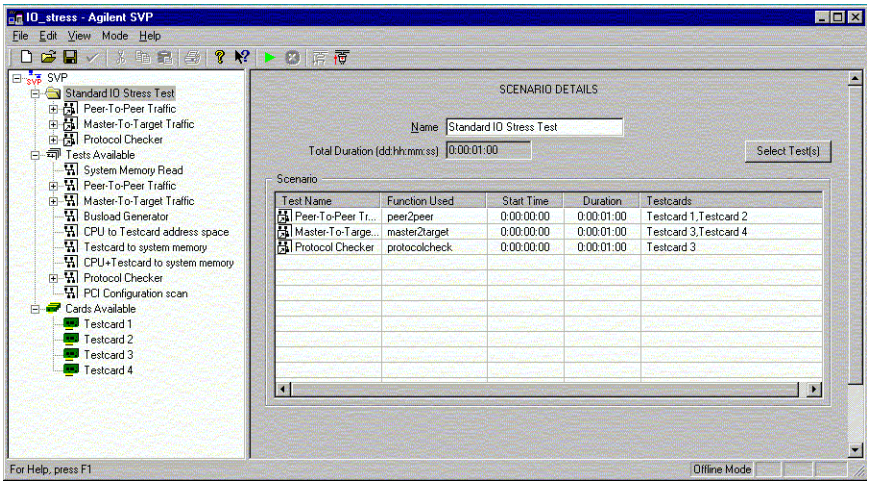


Figure 3. Test scenario setup window

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PCI/PCI-X Configuration Scan
Automatic scanning and reporting of the whole configuration space of the PCI/PCI-X bus allows proper documentation of test conditions during the test run. As PCI/PCI-X configuration space may change with each system reboot, this is an incredible help when looking for sporadic errors.

Link into debugging environment
In error cases, the trace memory and the dumped trace memory file can be analyzed with the Analyzer Graphical User Interface. To upload the Analyzer data, an external PC running the Analyzer Graphical User Interface will be connected to the Exerciser and Analyzer cards, even if the system under test hangs. Trigger I/0's of cards can be connected to generate "snapshots" of bus status error on individual PCI/PCI-X buses.

In-system Programmable
The Agilent System Validation Package can be installed and executed on the system-under-test itself. In this case, the Exerciser and Analyzer are programmed through the PCI and the PCI-X interface.

External Control
Alternatively, the whole test can also be controlled from an external host PC, which runs the System Validation Package. The Exerciser and Analyzer are connected via an appropriate external interface (RS-232, 4MB fast host interface). To execute a test that requires the FSI (see Table 2), the FSI must be installed on the system under test.

Working with non-Windows
Two options are available to verify a system that does not use Windows.

Use an external controlling host PC
In this case, any test which does not require the FSI can be executed immediately. To use the other test, the FSI, which is only a small C-program, must be compiled for the appropriate OS. The FSI is delivered as executable for Windows, DOS, and in source code.

Table 2. Customer Configurable Test Parameter

			Customer configurable test parameters						Usable mechanisms to detect errors			
	# of cards	FSI[2]	Band-width	PPR	Address Space	Address Prefetch	Address	Memory Size	Data Compare	Protocol Check	Protocol Error Mask	Capture Waveform on Error[3]
CPU and Test Card to System memory	1	yes	1..100%	√	Memory	n/a	by OS	0..512KB/ 0..1MB[1]	√	√	√	√
Peer to Peer Test	2	no	1..100%	√	Memory or I/O	true or false	by BIOS/ OS	0..512KB/ 0..1MB[1]	√	√	√	√
Master/Target Traffic	2	no	1..100%	√	Memory or I/O	true or false	by BIOS/ OS	0..512KB/ 0..1MB[1]	√	√	√	√
CPU to Test Card	≥1	yes	1..100%	√	Memory or I/O	true or false	by BIOS/ OS	0..512KB/ 0..1MB[1]	√	√	√	√
Write/Read/ Compare to System Memory	≥1	yes	1..100%	√	Memory	n/a	by OS	Dword value 0..4Kbyte	√	√	√	√
Read From System Memory	≥1	yes	1..100%	√	Memory	n/a	Address Value	Dword value 0..4Gbyte	√	√	√	√
Bus Load Generation (self traffic)	≥1	no	1..100%	√	Memory or I/O	n/a	by BIOS/ OS	0..512KB/ 0..1MB[1]	—	√	√	√

1. The memory can be specified for the selected Exerciser. 512KB data memory is available on E2925B, E2928A, and E2940A. 1MB data memory is available on E2929B and System Test Library.
2. The FSI (Front Side Interface) is a small executable table which must run on the system under test CPU(s).
3. Requires option 100 for the E2929B. Not supported for System Test Library.

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Porting the System Test Library
The other alternative is to import the complete System Test Library to your preferred OS. Therefore, the System Test Library comes with source code.

Optionally, special porting support is offered, helping you to incorporate the System Test Library test capabilities into your proprietary test environment.

Required E2920 Series Exerciser/Analyzer
The System Validation Package requires a full Exerciser/ Analyzer (see Table 3).

Ordering Information

The System Validation Package can be ordered as option #310 of the E2925B, E2928A, and E2929B, E2240A
The system test is also available as a system test library to be integrated in customer proprietary test frames.

Refer to System Test Library technical specifications (5968-3500E) for more information.

Table 3. Minimal Exerciser/Analyzer Configuration Needed for Option #310/System Test Library

	Option #310	System Test Library
E2929B PCI-X Protocol Checker	•	•
#100 (Analyzer)	•	•
#300 (Exerciser)	•	•
#320 (C-API)		•
E2925B/E2928A/E2940A PCI	•	•
#300 (Exerciser)	•	•
#320 (C-API)		•
E2922B PCI-X Master Target Test Cards	Not Supported	• [1, 2]

1. For error detection, the E2922B supports PCI-X protocol and data compare only. Other analyzing capabilities like waveform capture, trigger I/O, or bus load measures require the E2929B.
2. The E2922B does not support external interfaces and must be in-system programmed through PCI-X.

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C-API/PR Library (option #320)

The optional C-Application Programming Interface (C-API) provides a programming interface for setting up and controlling the Exerciser and Analyzer.

Option #320 comes with a library of C functions to facilitatecontrol of the Excerciser and Analyzer.

Option #320 also comes with a PCI Protocol Permutation and Randomizing library.

The test program can run on the system-under-test itself or on an external controller. If the program runs on an external host, the Agilent E2925B connects via RS232 or fast parallel port to the external host. If the test program runs on the system under test, the PCI interface itself is used. Drivers are provided for each interface, which allow the C-API to be used under Windows NT 4.0® or Windows 95/98®.

	Win
98/2000®	NT®
RS232	Yes
PCI	Yes
Parallel	Yes

The library functions are divided into groups, which allow you to set up and control the various capabilities of the Agilent E2925B such as:

- session and interface functions,
- master block property transfers,
- master protocol behavior,
- master generic property functions,
- target decoder functions,
- target protocol behavior functions,
- protocol checker functions,
- analyzer and trigger functions,
- host to PCI access functions,
- configuration space functions,
- expansion ROM functions,
- status functions,
- mailbox functions,
- built-in test functions.

Built-in Test Functions

The on-board CPU makes a number of built-in test functions available, designed to quickly and easily intensify existing tests by adding additional asynchronous background traffic to the system.

- **Make Traffic**: master generates bursts of various lengths to its own target in order to load the arbiter and decrease the available bandwidth for other PCI masters without influencing the system's resources.

- **Write/Read/Compare:** this test function continuously writes a block of data from the on-board memory to an external target, reads it back, and can compare (as an option) the results with the original data. The test stops on miscompare.

- **Block Move:** this test function continuously reads a block of data from one target address and writes it to another using the on-board memory as an intermediate buffer.

- **Protocol Error Detect:** sets up the protocol checker to trigger the analyzer if a protocol error occurs.

- **Dump Result:** stores the analyzer's and protocol checker's status to a file, including the trace memory. The file can then be analyzed later using the Analyzer Graphical User Interface for Windows 95/98/NT®.

Command Line Interface

The PCI Exerciser and Analyzer supports a Command Line User Interface (CLI) which runs under Windows 98/2000®. This allows you to interactively control the PCI Exerciser and Analyzer from an external PC by entering command functions that correspond with the functions provided by the C-API. The CLI can also process batch files of concatenated command functions. The CLI is intended to provide a programmer with a means of controlling the card interactively, while developing test programs using the C-API.

Protocol Permutation and Randomization (PPR)

The PPR library extends the C-API by offering dedicated functions to setup PCI protocol permutation in a pseudo random sequence. It allows easy to setup transfers of contiguous blocks of data with as many PCI protocol variations as possible.

Therefore, the PPR software calculates which variations are covered, and after how many data transfers, by permutating the possible protocol variations. It determines whether the coverage, within programmed constraints, can be achieved under given test circumstances, and calculates the test time required performing the data transfers.

To expose the device-under-test to the protocol variations, PPR uses the exerciser to perform a series of master and target protocol variations. The information used in the transfer and the protocol variations are stored in the hardware. The software programs the hardware so that it is guaranteed that all desired protocol permutations will be executed.

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Generating permutations

The user-defined protocol constraints can be easily set by specifying lists of protocol variations which must occur, for example, which different burst lengths, wait cycles, memory read/write commands, etc.

Then, PPR automatically moves simultaneously through the lists. With each step, that is, with each permutation, the next value in this list is combined with the next values in the other lists. The software proceeds in this way until each value of each list is combined with all values of the other list, and thus all combinations are covered. In this way, the repetition or omission of combinations is avoided.

Documented test coverage

A printable report tells you to which protocol variation the device has been exposed. It explicitly reports which protocol attributes are permutated against which other protocol attributes, and after how many data transfers.

Optimized test time

The values to be varied can be specified for each master and target attribute separately. Thus, focusing on interesting cases can optimize testing time.

By carrying out these protocol permutations at real-time within the PCI exerciser hardware, these tests run much more quickly than any other CPU-based test program.

Effective test generation

The exhaustive C-library makes it simple to focus on test structuring, partitioning and the specification of protocol constraints. This means that an appropriate and valuable test for PCI protocol verification with meaningful results can quickly be obtained.

Once started, the test can be easily extended to incorporate newly gained experiences or to address testing needs for newly invented PCI features.

Deterministic test conditions

In contrast to PCI traffic generated by other PCI cards, the generated variations are completely deterministic and reproducible.

PCI protocol check

The comprehensive analyzing capabilities of the Agilent PCI test hardware can be used concurrently with the PCI protocol permutation. Thus, by using either the C-API commands or the PCI Analyzer GUI, root cause analysis and error localization, including real-time PCI protocol check, can be carried out.

Even in case of bus hang-up, the last block of transferred data can be identified for a simple repetition of error conditions.

Supported Protocol Variations

The Agilent PCI Exerciser and Analyzer allows the variation constraints for the PCI transfer, PCI master and PCI target behavior to be specified. All specified constraints can be permutated against each other, and up to 100 constraints can be maintained per list.

PCI transfer variations

- Start address alignment; a list of arbitrary address alignments to start PCI transfers at given offsets (e.g. 1 dword) relative to the given address granularity (e.g. 32 byte boundary).
- Byte enables; a list of selected values for the C/BE lines during the address phase.
- Block size; a block describes a contiguous range in memory available to be transferred. A list of up to 100 different block sizes (from 4 to 128 KByte) to be transferred can be selected.
- Bus commands; a list of selected PCI bus commands. All selected commands are permutated with other selected constraints, as appropriate, for the specified transfer direction and PCI specifications.

Master attribute variations

- Burst length; a list of selected burst lengths ranging from 1 to 32 kDwords.
- Address stepping.
- Request line release; a list of different values of when the REQ# line has to be released.

Target attribute variations

- Termination; allows a list of different termination modes for use to be specified, i.e. no termination, termination with retry, with disconnect, and with target abort.

Master/target attribute variations

- Wait cycles; a list of selected wait cycles ranging from 0 to 31.
- Data stepping.
- Parity/system errors; lists specifying how PERR/PAR/ SERR should be considered for permutations.

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General Specifications

PCI specifications:
PCI bus: 32/64 bit respectively
Addressing: 32/64 bit, DAC

PCI Clock range:
Analyzer: 0 to 66.7 MHz
Exerciser: 0 to 33 MHz

Timing specifications:

	Min.	Max.
T_{val}		11 ns
T_{on}	2 ns	
T_{off}		28 ns
T_{su}	7 ns	
$T_{su(ppt)}$	7 ns	
T_h	0 ns	
@ temperatures of -40°C to +70°C		

Drivers: can be used in both 5 V and 3.3 V environments.

Decoupling: unused 3.3 V power pins are decoupled.

Power requirements: consumes < 25 W from Compact PCI slot.

Trace length limits:
meets Compact PCI specifications.

Signal loading: 10 pF.

Operating temperature:
-40°C to +70°C.

Mechanical dimensions:
3U Compact PCI card, occupying one slot.

Static I/O signals: 3.3V CMOS 74LVT I/O drivers, compatible to 5V TTL Flat cable connector

Ordering Information

The Agilent E2925B base product includes:
· 32 or 32/64 bit respectively, 33 MHz Analyzer ,
· Analyzer Graphical User Interface, single user license for Windows,
· RS-232 cable,
· 4Mb fast host interface
· Software media CD.

Option #200, Performance Optimizer includes
- Single user liceense for Windows 98/2000

Option #300, PCI Exerciser includes:
- On-board 32 or 32/64 bit respectively , 33 MHz Exerciser
- Exerciser Graphical User Interface, single user license for Windows

Option #310, System Validation Package Includes:
- Graphic User Interface, single user license for Windows The PCI Exerciser (option #300) must be installed

Option #320 C-API interface/PPR library
- single user license.

To use PPR or C-API exerciser commands, the PCI exerciser option #300 must be installed/

Accessories:

Agilent E2991A: External Power Supply

The External Power Supply supports applications where the Exerciser and Analyzer card should be transparent to the system, you can connect this external power supply to prevent the card from drawing power from its slot.

Agilent E2993A: External Agilent Logic Analyzer Adapter, terminated

This add-on "daughter" card provides all of the on-board PCI analyzer signals with the appropriate terminations and connectors to connect straight to an external Agilent Logic Analyzer. This is useful if you want to observe the PCI Bus State in context with other busses or interfaces in the system-under-test.

Agilent E2994A: Universal Logic Analyzer Adapter, non- terminated

This Generic Logic Analyzer Adapter provides all of the on-board PCI analyzer signals to connect directly to any external logic analyzer. Appropriate terminators, depending on the selected logic analyzer, must be added.

Agilent E2995A: 4M Memory Board

This enhances the Agilent E2925B by providing 155 x 4M trace memory for the PCI State Logic Analyzer.

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Overview PCI/PCI-X E2920 Series

	PCI Analyzer -protocol checker - 64K state PCI logic analyzer -4MB fast host interface - timing checker -real-time performance measures -GUI - RS-232 interface	**E2940A** compact PCI 32/64 bit 66MHz	**E2925B** PCI 32 bit 33 MHz	**E2928A** PCI 32/64 bit 66 Mhz	**E2929B** PCI-X 32/64 bit 133 MHz -protocol checker -RS-232/USB interface - GUI
Opt.100					**PCI-X Analyzer** - 2M state PCI logic analyzer -4MB fast host interface -real-time performance measures - GUI
Opt..200	**PCI Performance Optimizer**	4M trace memory recommended please order separately		32/64 bit 66 MHz	**PCI-X Performance Optimizer** -post processed and real-time performance analyzer -performance report - GUI
Opt.300	**PCI Exerciser** - master and target -GUI - CLI -512 KB on-board memory	32/64 bit 33 MHz	32 bit 33 MHz	32/64 bit 66 MHz	PCI-X Exerciser - master - target - GUI - 1MB onboard data memory
Opt. 310	**System validation package**	- peer-to-peer test -system memory test - system load test - protocol load test - protocol check - GUI			
Opt.320	**C-API/PPR**	- C-programming interface library -protocol permutation and randomization library			

PCI-PCI-X Bundle:

With the E2997A Agilent also offers a great price on the purchase of the E2928A PCI Card and the E2929B PCI-X card.

Master Target Test Card

The E2922B PCI-X Master target Test card provides validation engineers in the semiconductor industry a fast and predictable way to set up PCI-X protocl compliance of first silicon.

Accessories Agilent Products	**E2940A**	**E2925B**	**E2928A**	**E2929B**
E2991A External power supply		•	•	•
E2993A External Agilent Logic Analyzer Adapter		•	•	
E2994A External general purpose Logic Analyzer Adapter		•	•	
E2995A 155 x 4M trace memory		•	•	
E2996A 155 x 4M trace memory	•	•		
System test library	•	•	•	•





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Related Agilent Literature

- Agilent E2928A 32/64bit, 66 MHz, PCI Exerciser & Analyzer, technical overviews, p/n 5968-3506E
- Agilent E2929B PCI Exerciser & Analyzer, technical overview, P/n 5968-8984E
- Agilent E2922B PCI-X Master Target Card, technical overview, p/n 5968-9577E
- Agilent E2940A CompactPCI Exerciser & Analyzer, technical overview, P/n 5968-1915E
- Agilent System Validation Pack, Agilent System Test Library, technical overview, p/n 5968-3500E
- Agilent E2920 Computer Verification Tools, PCI Series, brochure, p/n 5968-9694E
- Intel discusses basic concepts of PCI performance and efficient use of PCI with the Agilent E2920 series, case stuy, p/n 5988-0448ENDE
- HP NSD stabilizes server designs quickly and completely with the Agilent E2920 PCI Series, case study, p/n 5968-6948E
- HP HSTC speeds high-end server testing and reduces engineering costs with the Agilent E2920 PCI Series, case study, p/n 5968-6949E
- Agilent E2920 Verification Tools, PCI Series gives Altera Corporation competitive Advantage, case study, p/n 5968-4191E

You can find the current literature and software at:
www.agilent.com/find/pci_products

For more information, please visit us at:
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