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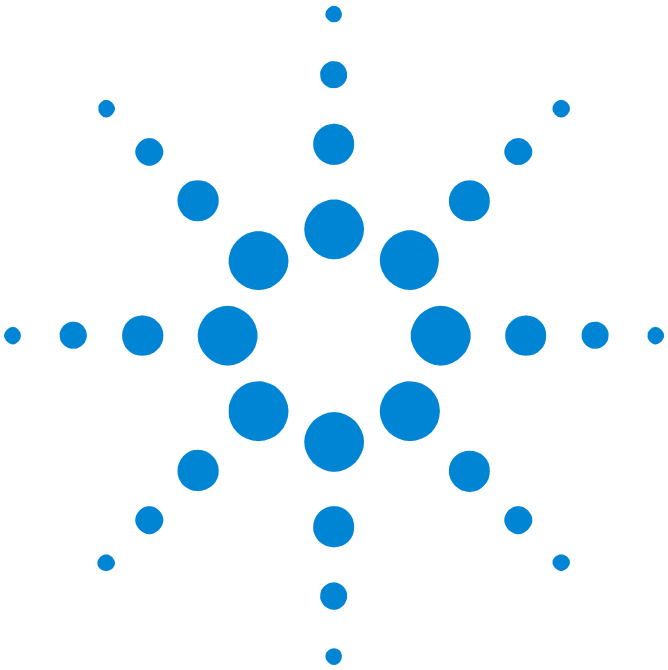
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# Agilent E2929A/B PCI-X

## Getting Started Guide



Agilent Technologies

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## Important Notice

All information in this document is valid for both Agilent E2929A and Agilent E2929B testcards.

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# Documentation Overview

This section shows you the different types of documents offered by Agilent Technologies and gives you an overview of which documents are available when you work with the Agilent E2929A/B PCI-X Exerciser and Analyzer.

All documents are valid for both Agilent E2929A and Agilent E2929B testcards. The following documents are available:

Getting Started Guide

- **Getting Started Guide**

  Introduces standard analysis features and provides an example of how to set up the protocol observer.

  This guide also gives detailed information about the hardware and interfaces.

User's Guides

- **Agilent E2929A/B Opt. 300 PCI-X Exerciser User's Guide**

  Provides information on programming the testcard as an initiator and/or target device. It shows you how to actively stimulate the PCI-X bus.

  This guide shows how to:

  – Initiate data transfers on the PCI-X bus (act as requester-initiator).

  – Act as completer-target.

  – Handle split completion transactions (act as completer-initiator).

  – Handle open requests (act as requester-target).

- **Agilent E2929A/B Opt. 100 PCI-X Analyzer User's Guide**

  Provides information on how to examine the behavior of a PCI-X device on the bus and shows how to perform functional tests such as data compares.

- **Agilent E2929A/B Opt. 200 PCI-X Performance Optimizer User's Guide**

  Provides all features that are needed to evaluate and optimize any device under test in terms of the performance.



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### GUI and C-API/PPR References

- **Agilent E2929A/B Windows and Dialog Boxes Reference**

  Provides reference information on all windows and dialog boxes of the Agilent E2920 graphical user interface (GUI).

- **Agilent E2929A/B Opt. 320 C-API/PPR Reference**

  Describes all C functions, types and definitions of the application programming interface of the Agilent E2929A/B PCI-X testcard.

  This reference also provides the commands and abbreviations that are used in the command line interface (CLI) of the graphical user interface.



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# System Overview

This section introduces the features, interfaces and options of the Agilent E2929A/B testcard:

- *"A Window to the System" on page 8* describes the use models and scenarios in which the testcard and its options are intended to be used.
- *"User Interface" on page 10* provides an overview of the user interface software, which is delivered with the testcard, and lists the testcard's basic features.
- *"Hardware and Interfaces" on page 15* identifies the most important elements on the testcard.

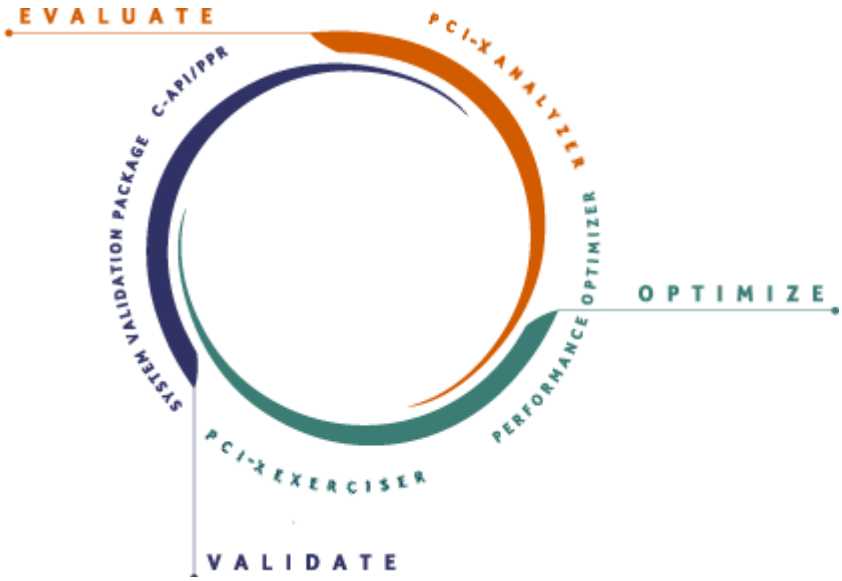


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# A Window to the System

The Agilent E2929A/B testcard is your window to the system during product development, giving you access to almost all of the system components located on the PCI-X bus, as well as devices and adapters on secondary buses such as ISA.

The options available for the testcard support you in all phases of the design cycle—and all along the value chain of the computer industry.






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This is how you can use the testcard in the individual phases:

- When bringing up and debugging a PCI-X-based system, device, or firmware, the **PCI-X Analyzer** (option #100) lets you **evaluate** its behavior on the PCI-X bus.

  While tools like oscilloscopes and logic analyzers focus on problems *on your device* (for example, signal integrity), the PCI-X Analyzer allows you to examine the device's behavior *on the bus*, as well as to perform functional tests like data compares.

  For example, when testing LAN interface testcards telecom switches, you can sample the data packages and compare incoming and outgoing data.

- When optimizing a system or a device to improve its performance, the **Performance Optimizer** (option #200) gives you in-depth post-processed performance analysis and hints for performance optimization.

  The Agilent E2920 PCI-X software also features real-time performance measurement, using predefined, standardized measures like efficiency, throughput, and utilization.

- The **PCI-X Exerciser** (option #300) allows you to overcome the passive role in monitoring the PCI-X bus. With the PCI-X Exerciser, the testcard can be programmed to behave as an initiator and/or target device. The PCI-X Exerciser features:

  – Two requester-initiator queues.

  – One completer-target.

  – Four completer-initiator queues to handle independent split transactions.

  – One requester-target to handle open requests.

  With the PCI-X Exerciser you can set up complex PCI-X scenarios and worst case test patterns quickly and in a repeatable way.

  Using these features, you can **optimize for reliability**, by ensuring that your system or device will handle even worst-case PCI-X conditions.

  You can also run functional tests, directing the PCI-X Exerciser to generate and transmit large blocks of data in specified time intervals, thus testing how much PCI-X traffic your device can handle.



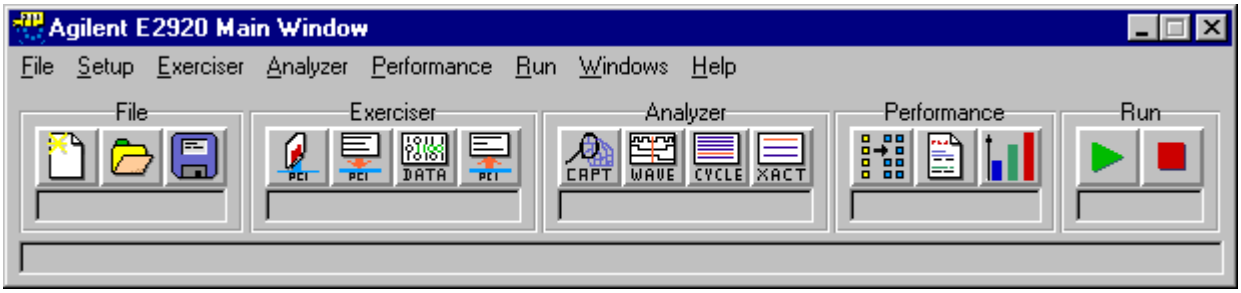
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- To proceed even further and validate that your PCI-X design works under all real-life conditions, the **System Validation Pack** (option #310) provides a sophisticated user interface and pre-defined tests.
- Finally, the **C-API/PPR** (option #320) programming interface provides full flexibility for integrating the testcard into existing test environments and controlling all details on the testcard.

  Agilent's unique **PCI-X Protocol Permutator and Randomizer** (PPR) prepares the PCI-X Exerciser to transfer a single block of data with as many protocol variations as possible, giving you the **optimum test coverage** in the minimum amount of time.

# User Interface

The Agilent E2929A/B testcard comes with graphical user interface software, which provides a basic framework and the controls for the PCI-X Exerciser and PCI-X Analyzer. The options available for the testcard also use this framework, expanding it by their own specific features.




**Buttons** The most important features are available via the framework buttons. For example, for the PCI-X Analyzer you can set up the data capture and display the results in different formats—all by means of the buttons.

**Menus** All these features and more are available via the menus of the framework window, as well.



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# Analyzer Overview

For the PCI-X Standard Analysis, the software provides:

- the protocol check

  The protocol observer continuously monitors the PCI-X bus to detect protocol errors.

  For more information, refer to *"Analyzing Protocol Violations" on page 33*.

For the PCI-X Analyzer (option 100), the software provides:

- the capture control

  The PCI-X Analyzer allows you to specify exactly when and which data is to be captured from the PCI-X bus, thus making optimum use of the available trace memory.

  For more information, refer to the *Agilent E2929A/B Analyzer User's Guide*.

- the result windows: waveform viewer, bus cycle lister, and transaction lister

  The result windows interpret and display the captured data using different levels of abstraction (from signal level to transaction level).

  For more information, refer to the *Agilent E2929A/B Analyzer User's Guide*.

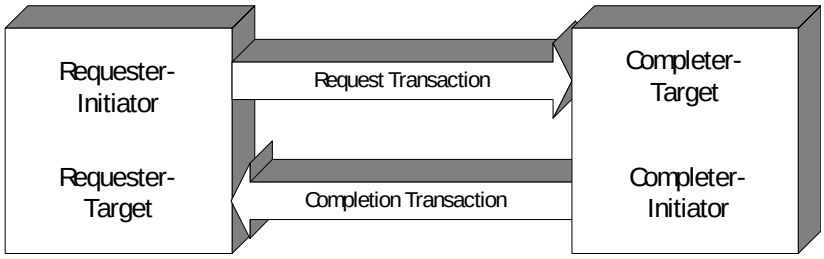


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# Exerciser Overview

The Agilent E2929A/B testcard can act as an initiator or a target device on the PCI-X bus to generate any kind of PCI-X transfer.

Because PCI-X allows you to perform split transactions, initiator and target have been subdivided. This is shown in the following figure:




For the **requester-initiator,** you can specify:

- The transactions to be performed.
- The protocol behaviors to be used with the transactions.
- Data to be used for the transactions.
- Conditions to be fulfilled before the transactions are started.

For the **completer-target,** you can specify:

- The Protocol behaviors to be used during the transactions.
- Which addresses are to be decoded (target decode, configuration space, expansion ROM, split decode).
- How received data is to be handled.
- The data to be transferred on request.

For the **completer-initiator**, you can specify:

- How to handle independent split-transactions.
- Completer-initiator behaviors to be used for the split-transactions.
- Conditions to be fulfilled before the transactions are started.

For the **requester-target** you can specify:

- How to handle open requests.
- The requester-target behaviors to be used for transactions.

Furthermore, you have full control over the testcard's **configuration space.**

The Agilent E2929A/B testcard is also able to generate any **PCI-X interrupt** INTA# ... INTD#.



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# Performance Overview

**Post-Processed Performance**

If the PCI-X Performance Optimizer option has been installed and enabled, features for post-processed performance analysis and optimization are provided:

- The Performance Setup

  For the Performance Optimizer, you can set up the structure of the report to be generated, identify master and target devices to be considered, and control the capture for performance analysis.

- The Performance Chart

  The performance charts show graphical representations of the performance-relevant aspects found in the captured PCI traffic.

- The Performance Report

  The performance report summarizes the results in a hierarchical way, so you can focus on your level of detail.

**Real-Time Performance**

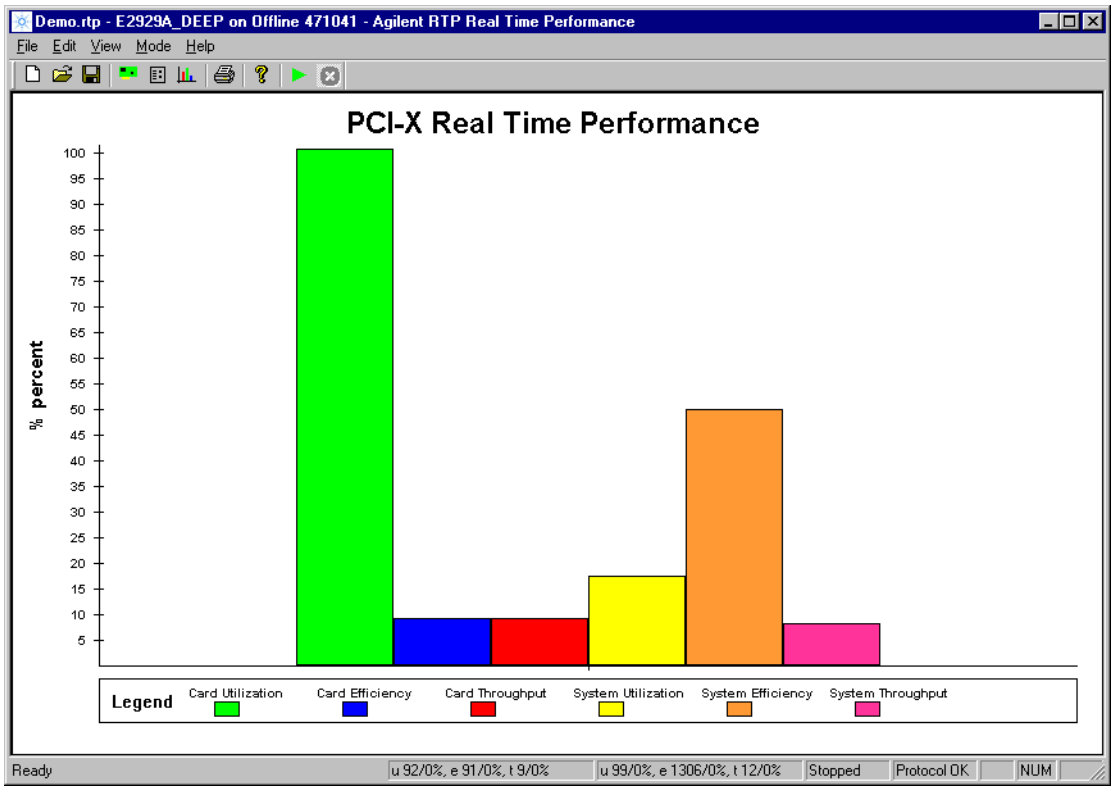
The Agilent E2920 PCI-X software provides additional features for real-time performance measurements. These features are available via a separate GUI, which can be accessed by selecting:

```
Start > Programs > Agilent E2920 PCI-X > PCI-X Real Time
Performance GUI
```



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The user interface for the RTP Real Time Performance measurements looks as follows:



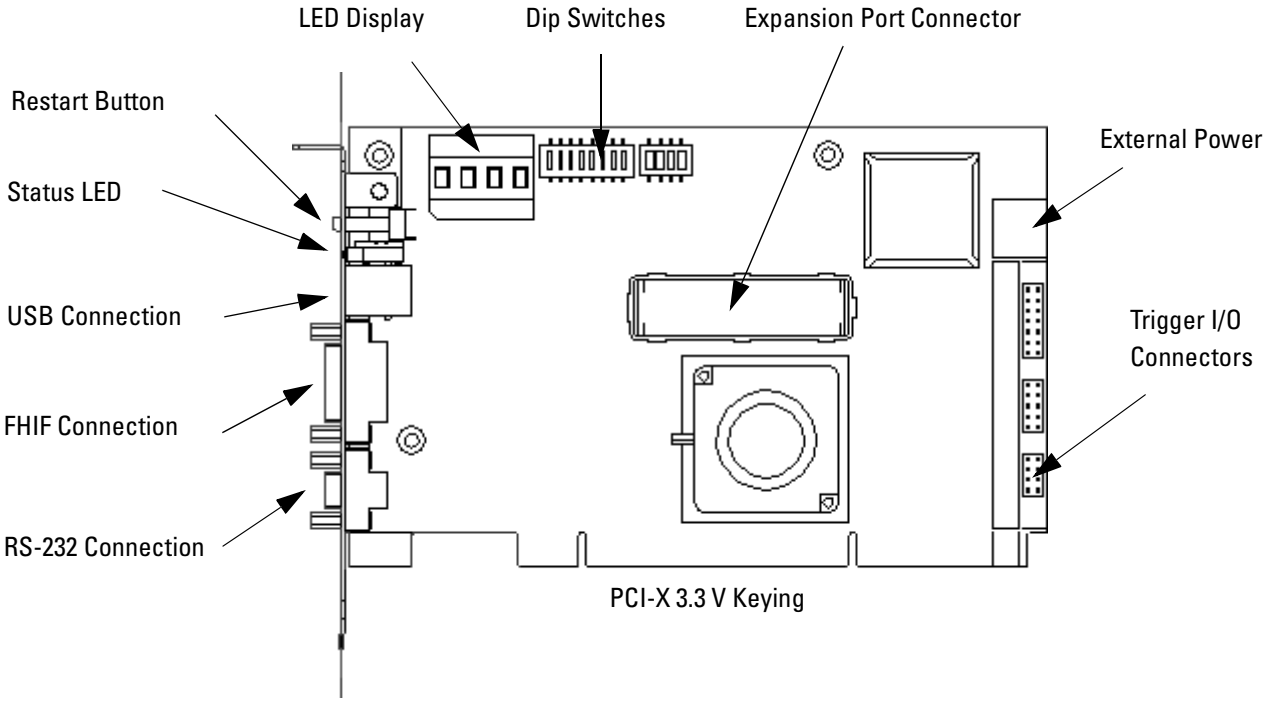

For information about using the PCI-X Performance Optimizer, please refer to *Agilent E2929A/B PCI-X Performance Optimizer User's Guide*.



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# Hardware and Interfaces

The following figure shows an overview of the interfaces provided by the Agilent E2929A/B testcard.




The following list roughly describes the most important interfaces of the testcard.

- The **Restart Button** clears all protocol observer errors currently.
- The **Status LEDs** shows the testcard's status and are visible even if the testcard is plugged into a closed system. For more details, refer to *"LEDs on the Testcard" on page 49*.



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- The **LED Display** is used
  - to identify multiple testcards in a system,
  - to show an error number, and
  - to display system status.
- The **USB**, **FHIF and RS-232 ports** are the control interfaces used to connect the testcard to the user interface software running on a host PC. The FHIF is used in combination with the Fast Host Interface testcard plugged into the host PC. For more details, refer to *"Connecting to the Testcard" on page 29*.
- The **Trigger I/O** pins provide access to the testcard's trigger I/O lines. For more details, refer to *"Trigger I/O Connectors" on page 44*.
- The **PCI-X 3.3 V Keying** is used to plug the testcard into the system under test. If the user interface software is running on the system under test, this connector can also be used as control interface.
- The **Dip Switches** can be used to override the PLL range automatically selected or to turn the PLL completely off for using the testcard at HW-emulation speed. For more details, refer to *"Dip Switches" on page 47*.
- The **Expansion Port Connector** is an interface (400-pin connector) to a piggyback board. For more details, refer to *"Analyzer Interface" on page 50*.
- The Agilent E2929A/B provides an **External power** connector. If the power supply is connected, the testcard automatically draws its current from the external power supply.



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# Running A Sample PCI-X Getting Started Session

The following application example explains how the testcard can be used in analyzing protocol violations. After seeing how to prepare for the sample session, you will find the following guided tour:

- Guided Tour: Analyzing Protocol Violations

## PCI-X Standard Analysis Scenarios

For standard analysis, the PCI-X testcard helps you, if you are:

- designing a PCI-X chip and you need to do bring-up or debugging,
- using a third party PCI-X chip on your motherboard or adapter card that you need to check for PCI-X protocol rule violations,
- writing and debugging low-level software (for example, BIOS code, device drivers).

It gives you the possibility to monitor the PCI-X bus to find out whether your device under test reacts correctly at the protocol level.

If the PCI-X Analyzer (option 100) is licensed with your testcard, the 2-MB state PCI-X logic analyzer allows you to capture PCI-X traffic and view it as a state waveform, a bus cycle listing or as a transaction listing. The following examples show you how to set up the PCI Analyzer and how to interpret the results.



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# Preparing for the Guided Tour

The example described in the guided tour is designed to be performed in Offline/Demo Mode (without hardware).

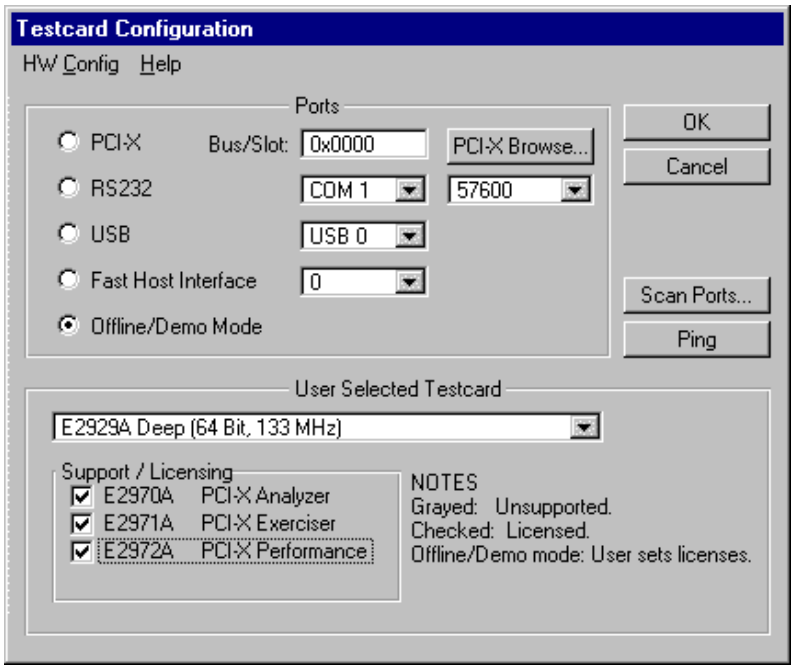
All the setup files (*.bst) and logic analyzer trace files (*.wfm) that are mentioned in the following text can be found under <your_installation_directory>\samples\demo. If you did not change the default setting during installation, <your_installation_directory> will be `c:\Program Files\Agilent\E2920 PCI-X Series`.

To prepare for the guided tour:

1 Launch the Agilent E2920 software.

2 From the *Setup* menu, choose *Testcard Configuration*.

3 In the Testcard Configuration window, select *Offline/Demo Mode*.



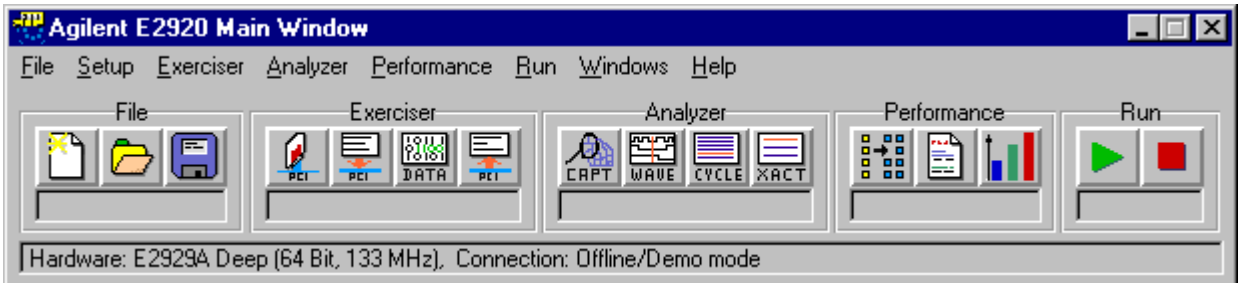

4 Now choose *Agilent E2929A/B (64 bit, 133 MHz)* from the *User Selected Testcard* list, and select all licenses in the *Support/Licensing* group.

Your display should look like the window shown above.



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**5** Click *OK* and the main window should look like this.




You are now ready to start the guided tour.

# Guided Tour: Analyzing Protocol Violations

In this example, the protocol observer of the testcard is used in conjunction with the built-in logic analyzer to trigger on a protocol violation that occurred during an access to a device's I/O space. You can load the setup for this example from `protocol.bst`, and the trace data from `protocol.wfm` (load `protocol.bst` with *Load* from the *File* menu in the main window, and `protocol.wfm` with *Load* from the *File* menu in the waveform viewer).

The protocol observer of the Agilent PCI-X Analyzer monitors 53 PCI-X protocol rules and Agilent rules in real time and flags the violation of an error with an LED on the rear panel of the board.



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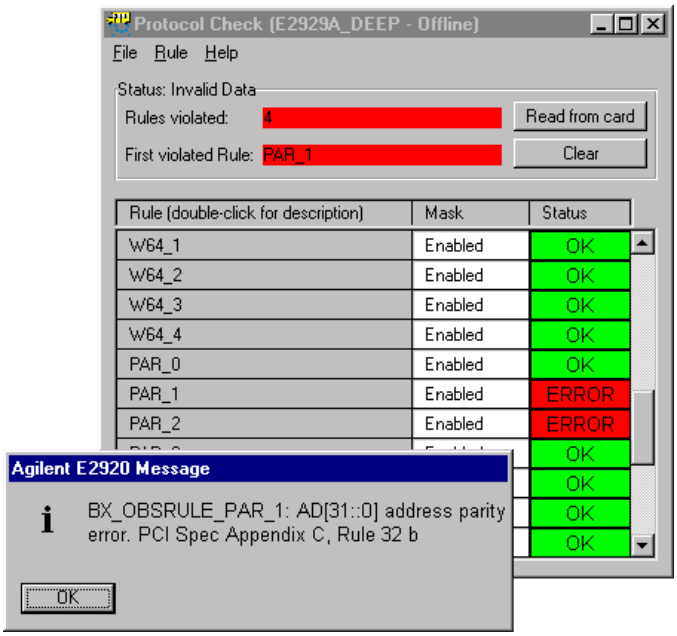
# Setting Up the Protocol Observer

From the user interface, the status of the protocol observer can be checked by opening the protocol check window:

1 From the *Analyzer* menu select *Protocol Check*.

The Protocol Check window indicates the first rule that was violated, as well as the total number of violated rules. Each rule can be individually enabled or disabled to prevent flagging of known errors.

In demo mode, the software displays random errors to give you an idea of how it works. You can double-click on any rule name field to get an explanation of what that rule checks.



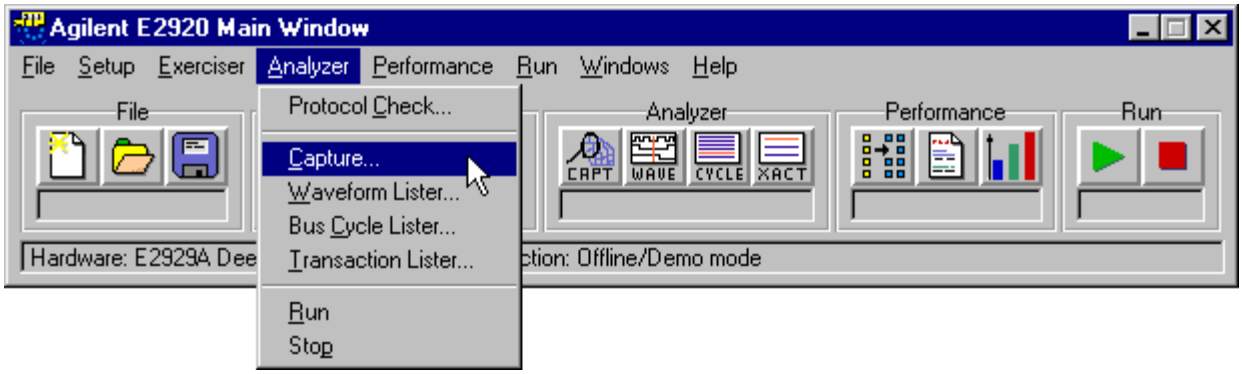



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# Triggering on Protocol Errors

In order to analyze a protocol violation and find out which PCI-X device caused the violation, you can set up the built-in logic analyzer to trigger on protocol errors:

1 Use the Capture button  in the icon bar of the main window, or choose *Capture* from the *Analyzer* menu.




2 In the Capture dialog box, select the *Trigger* tab.

3 Choose the *Trigger on:* option.

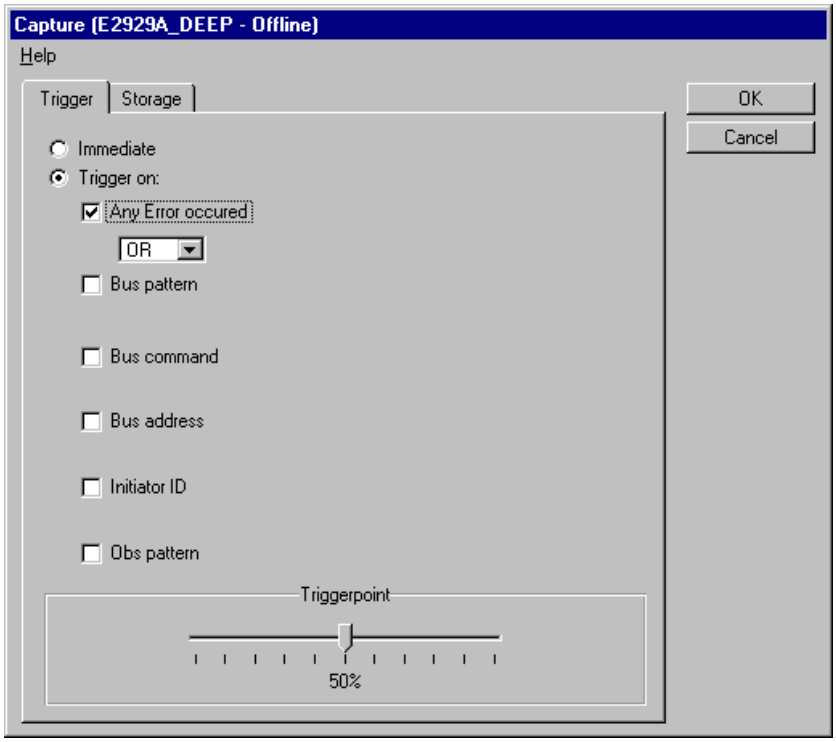
4 Select the *Any Error occurred* check box.

5 Click *OK*.



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The Capture window should now look like this.




Press *OK* in the Capture window, and the logic analyzer is ready to run.

**6** Run the analyzer to trigger on protocol errors.



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# Analyzing the Captured Waveforms

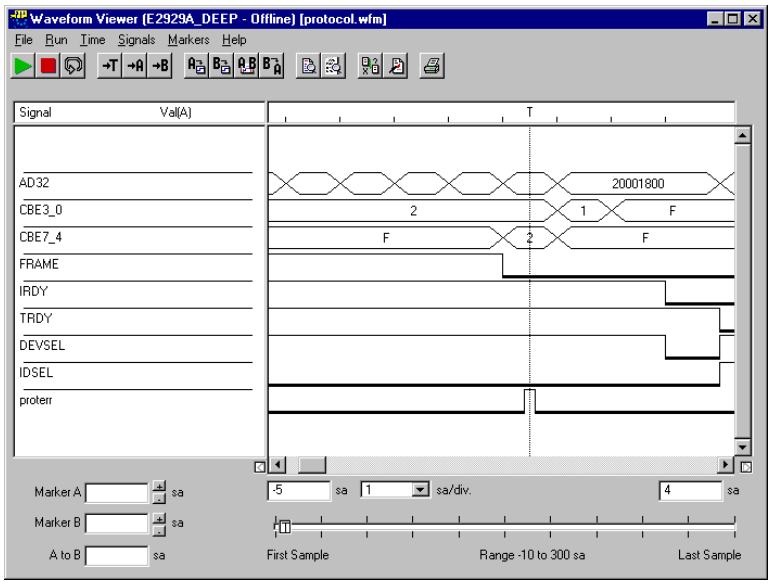
When the analyzer is started and the previously mentioned device is accessed, the analyzer triggers when any violation occurs. To view the results, proceed as follows:

1 Open the waveform viewer.

Your display will look different than that shown, but you can add and move signals within the display using the *Arrange* item from the *Signals* menu.

2 From the *File* menu in the Waveform Viewer window select *Load from file* and load the trace file `protocol.wfm`.

The signal *proterr* is asserted at the triggerpoint. The errors in this particular case are address parity errors in AD[31::0] and AD[63::32] (PAR1 and PAR2).

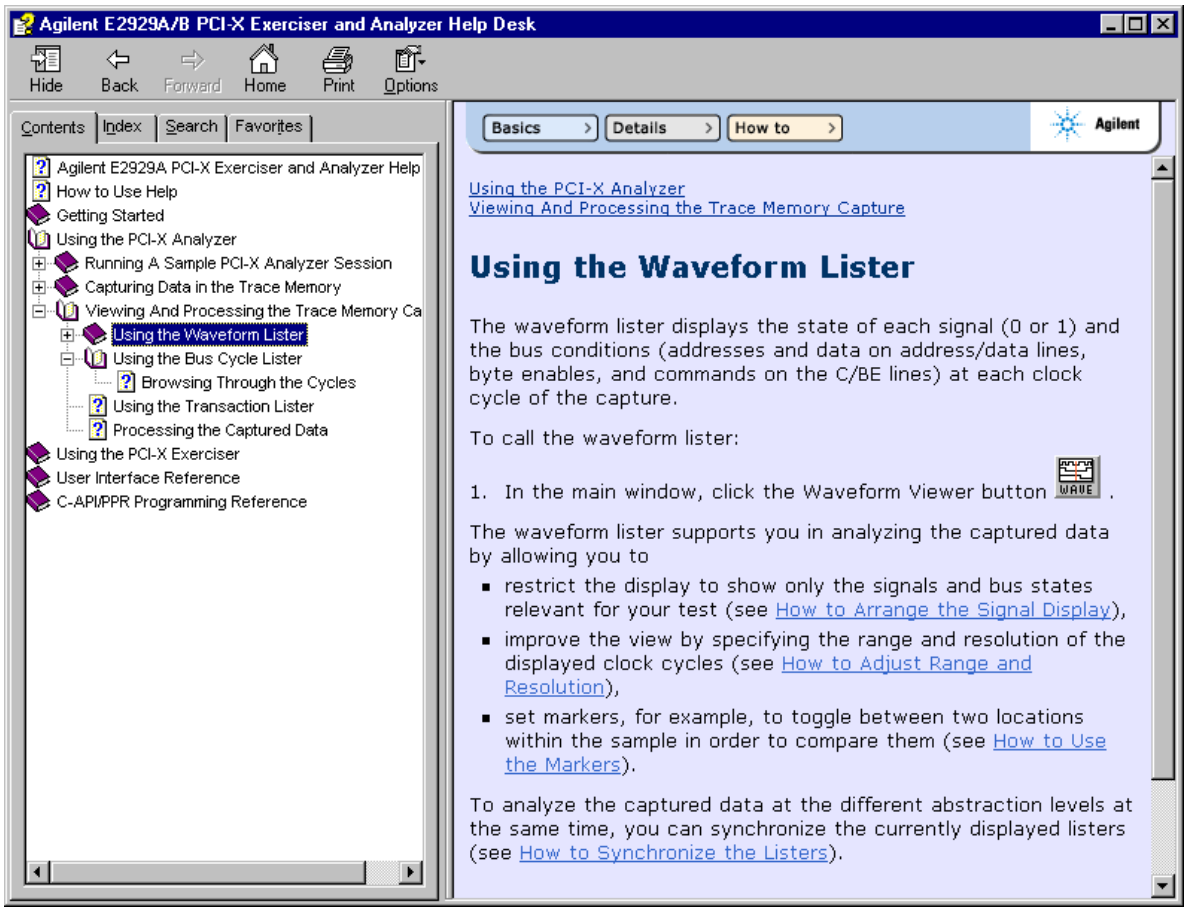





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# Getting Help

With the cursor in any Analyzer window, pressing the keyboard's **F1** key brings up context sensitive help.




Starting from here, you can use the signposts on top of the topic to find more information:

- Use the *Basics* signpost to find related basic and background information.
- Use the *Details* signpost to find more advanced information and reference data.
- Use the *How to* signpost to find procedural information and instructions for using the currently selected window.

**NOTE** The online help requires Internet Explorer 4.0 or higher to work. The on-line help is also currently focussed on Analyzer and Exerciser functions. Additional on-line help will be added for other features in future software releases.



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# Setting Up a PCI-X Standard Analysis Test

Setting up a PCI-X standard analysis test includes the following steps:

- According to your test requirements, you need to decide for one of the basic PCI-X standard analysis configurations.
- You need to establish the connection between the user interface software and the testcard.

NOTE For information on how to insert the testcard into the system under test, please refer to the installation instructions shipped with the testcard.



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# Possible PCI-X Configurations

The Agilent E2929A/B PCI-X testcard basically consists of two components:

- the testcard
- the graphical user interface software

The *testcard* plugs into the PCI-X bus of the system to be tested—or of the system hosting the device to be tested. The *software* can be run either on a remote system (a dedicated Control PC) connected via a fast host interface, or directly on the system under test.

This configuration provides the following benefits:

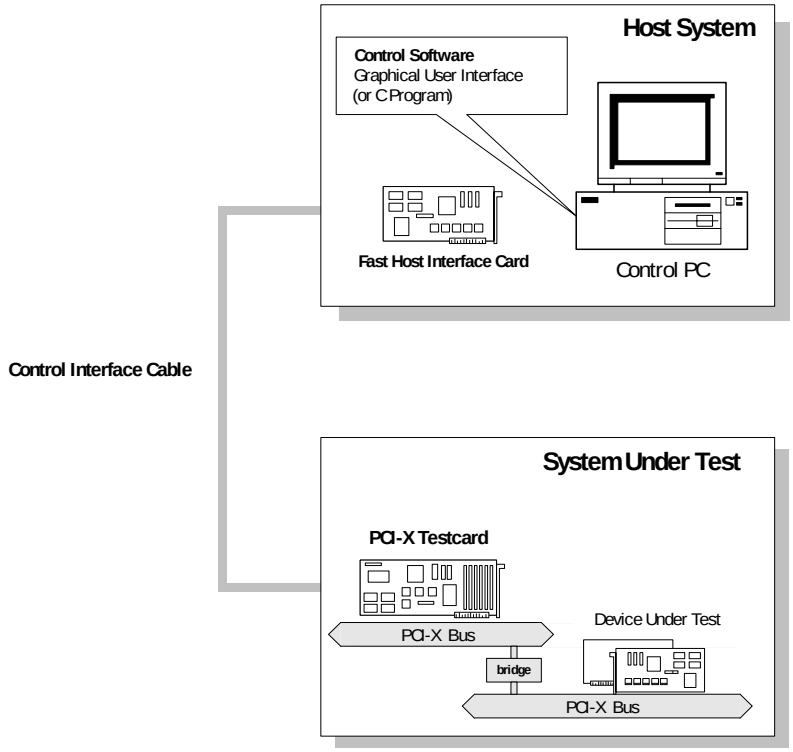
- The user interface software does not interfere with the traffic generated to examine the system or device behavior.
- You can easily switch between different systems under test by just moving the testcard from one system to another.
- Different devices under test can easily be exchanged without changing the setup of the Control PC.



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# Running a Test on an External System

The following figure shows a typical configuration where the user interface software is running on the Control PC and controls the testcard plugged into the system under test.




When running extensive tests using more than one testcard, you only need one Control PC, which can be connected to each testcard, one at a time. There is no need for a permanent connection between testcard and user interface software. While the test on one testcard is still running, the Control PC can connect to another testcard.

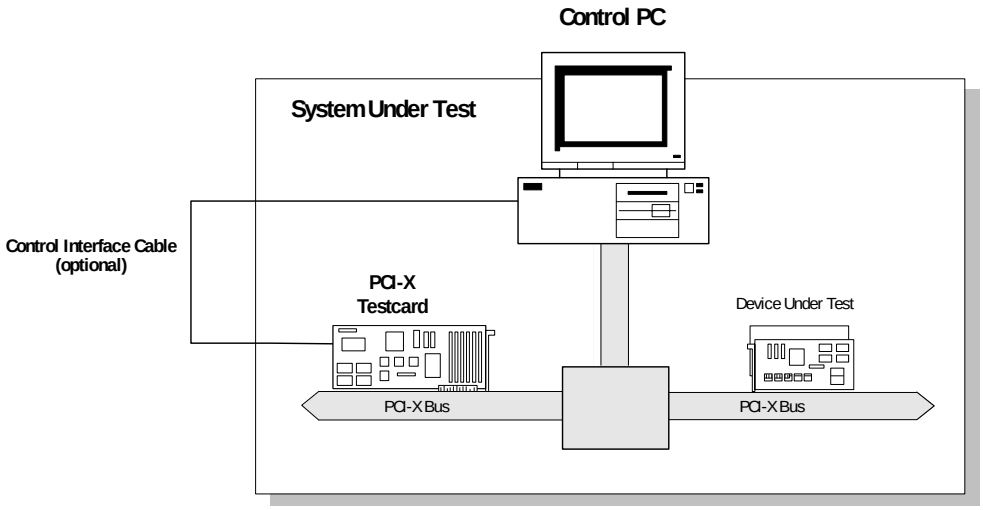


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# Running a Test Internally

The following figure shows a configuration where the user interface software is running on the system under test itself. Thus, there is no extra Control PC required.

The PCI-X software usually connects to the testcard directly via the PCI-X bus. However, you can also use the fast host interface or the serial interface for connection.




If there is more than one testcard installed in the system, all testcards can be reached directly via the PCI-X bus.



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# Concealing the Testcard from the System

Concealing the testcard is useful, for example, to monitor a system only for protocol errors or with the PCI-X Analyzer without influencing and interfering with the system. You can run the PCI-X testcard to see what is happening on the PCI-X bus.

A dip switch on the testcard allows you to switch off all decoders to conceal the Agilent E2929A/B testcard from the system under test before you run your test.

The testcard will not reply to any configuration access from BIOS and will, therefore, be completely invisible for the system.

For more information about location and required position of the specific dip switch, refer to *"Dip Switches" on page 47*.

# Connecting to the Testcard

To transfer control information between control software and testcard, the testcard's control interfaces are used. The Agilent E2929A/B testcard features the following control interfaces:

- Fast Host Interface

  This is the fastest connection to a testcard plugged into a remote system under test. The Fast Host Interface card coming with the PCI-X Analyzer must be plugged into the Control PC and connected to the parallel port on the testcard using the included bi-directional Centronics cable.

- PCI-X Port

  The PCI-X port can be used for in-system analysis (when the software is running on the system under test). No cable or hardware is required.



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- RS-232 Port

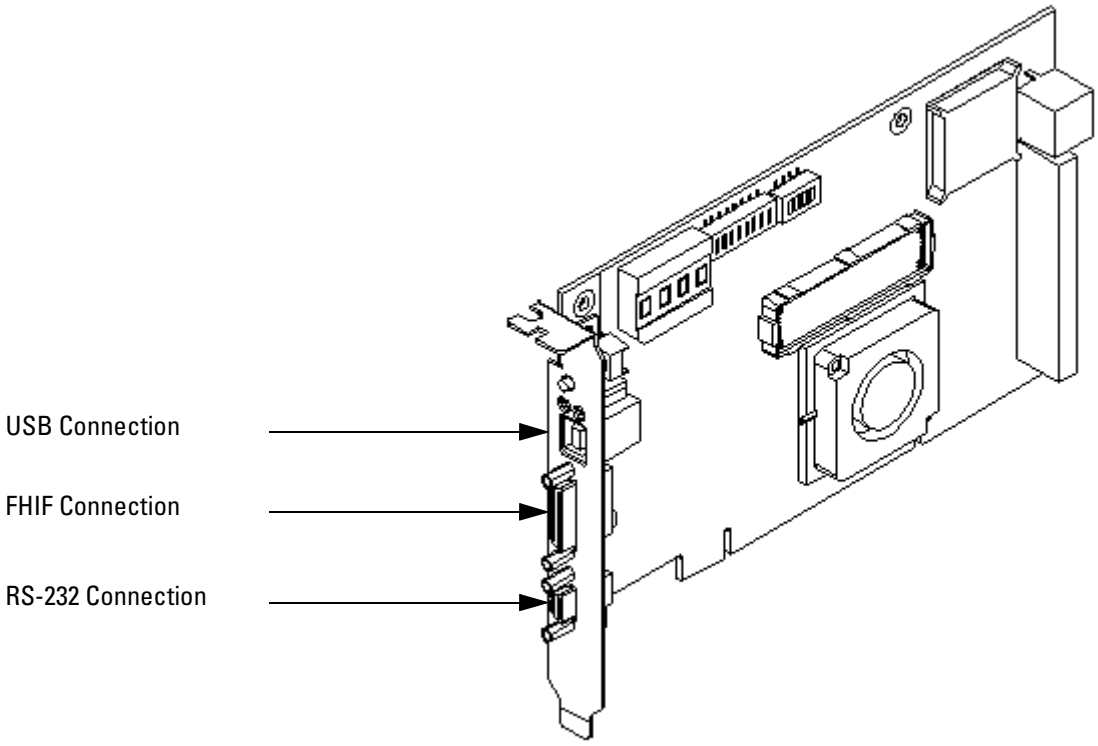
  The RS-232 port of the testcard can be connected to the serial interface of the Control PC using the included RS-232 cable.

  The Agilent E2929A/B testcard supports the baud rates 9600, 19200, 38400 and 57600 Bit/s. The actual value depends on the maximum baud rate supported by the serial interface of the Control PC.

  The RS-232 port must be used when updating the onboard firmware.

- USB Port

  The USB port of the testcard can be used in order to connect more than 4 testcards to one host without using PCI-X connections. With an USB hub, as much as 256 PCI-X testcards can be controlled simultaneously.




**NOTE** Note that some of the control interfaces are not supported by all operating systems running on the Control PC:

- The Fast Host Interface is not supported by DOS.
- The USB interface is not supported by DOS and Windows NT.



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Different testcards can be connected to the control software simultaneously using different control interfaces, and activated alternately.

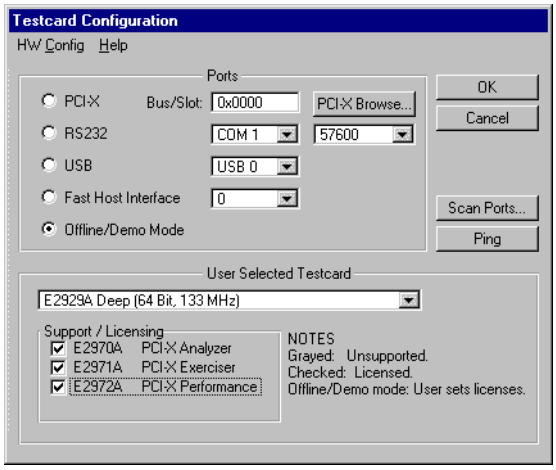
**NOTE** The user interface software also provides an Offline/Demo Mode. In this mode, all features of the software can be used without hardware, for example, for analysis of previously stored data or test preparation without hardware. No connection is established in this case.

## How to Select the Connection

After the hardware connection has been established, the user interface software supports you in identifying the available testcards and selecting the connection.

To connect to a testcard:

**1** From the *Setup* menu, select *Testcard Configuration*.




**2** Click the *Scan Ports* button.

The software scans all available control interfaces and lists the testcards available at the associated ports.

**3** Select one of the listed ports by double-clicking the entry in the list.

If no error messages occur, the connection has been established successfully, and your selection will be displayed in the Testcard Configuration dialog box.



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**NOTE** In case of any problem, refer to *"Connection Troubleshooting"* below.

Using the *PCI-X Browse* button in the Testcard Configuration dialog box, you can select from a list of devices found on the PCI-X bus of the Control PC.

Using the *Ping* button, you can check the connection between the user interface software and the testcard on the selected port.

# Connection Troubleshooting

If the selected connection cannot be established, an error message is displayed. Read the error message carefully and follow the steps described in the error message to eliminate the problem.

The following table provides additional information:

**Table 1 Troubleshooting Tips**

| Error Message | Reason | Help |
|---|---|---|
| Version mismatch ... | Version conflict. | Refer to *"Updating the Testcard" on page 41*. |
| Port is not connected ... | Cable loose or disconnected. | Ensure that the cable is properly connected. |
| | Wrong type of RS-232 cable or adapter. | Use an adapter shipped with the testcard. |
| | Wrong bi-directional Centronics cable. | Use the cable shipped with the testcard. |
| | Wrong port settings. | Correct the port settings in the Testcard Configuration dialog box. |

You can check the connection at any time while tracking down the error by selecting *Check Connection* from the *Setup* menu.



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# Analyzing Protocol Violations

When bringing up or debugging devices or complete systems, you have to check whether all devices keep to the protocol rules defined by the PCI-X Specification.

The Agilent PCI-X testcard provides an on-board protocol observer that monitors the PCI-X bus in real time to detect any protocol violations.

## Protocol Observation

The Agilent E2929A/B testcard provides a hardware-implemented protocol observer that monitors the PCI-X bus to detect protocol violations.

### Operation Principles

The protocol observer monitors the PCI-X bus in real time with 100 % observation time. The PCI-X bus is monitored continuously while the testcard is powered.

The protocol observer monitors 53 protocol rules simultaneously. These rules refer to the rules of the PCI-X specification. Each rule can be individually masked to disable its observation. For a list of monitored protocol rules, refer to the *Agilent E2929A/B C-API/PPR Reference*.

Multiple violations may occur in a sequence because a protocol violation of a PCI-X device will often cause malfunctions of other devices. Therefore, the protocol observer stores the first protocol violation and also counts and lists subsequent violations.

### Processing Protocol Violations

A detected protocol violation can be used as input for pattern terms (*proterr* signal), for example, to trigger a data capture.



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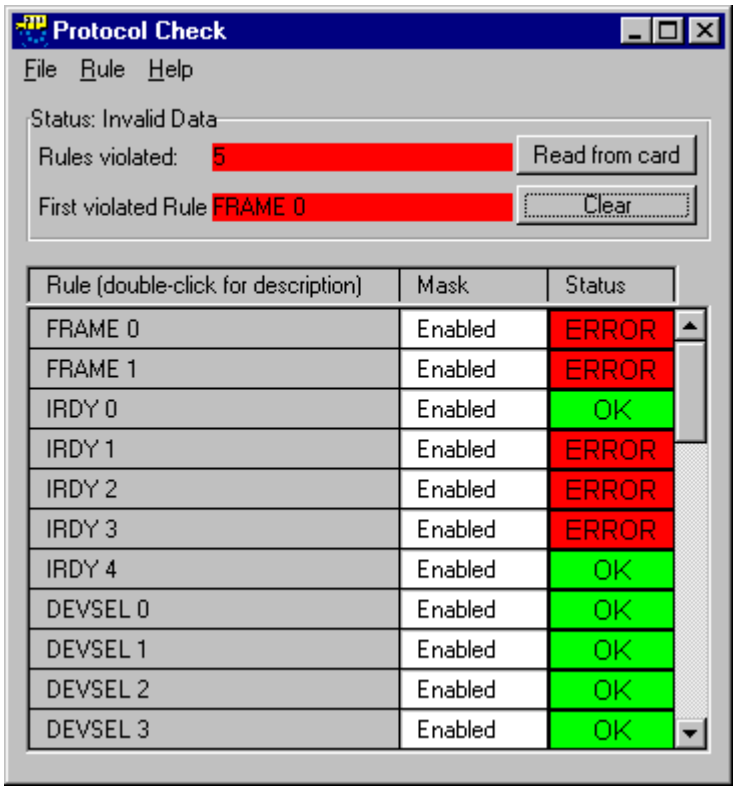
# How to Set Up the Protocol Observer

The protocol observer is controlled from the Protocol Check window. This window allows you to mask and unmask rules, and displays the contents of the error register.

To set up the protocol observer:

1 From the *Analyzer* menu, select *Protocol Check*.

The current observation settings and results are uploaded from the testcard and displayed in the window.




The *Status* group provides a result summary, showing the number of rules that were violated and identifying the rule that was violated first. The *Status* column in the *Rule* table shows error flags for each individual rule.

**NOTE** Double-clicking an entry in the *Rule* column pops up a description of that rule.



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2 Select the rules to be monitored for your test by masking those rules that are not relevant.

The current status for the individual rules is shown in the *Mask* column. To modify the mask:

– Click an entry in the *Mask* column to toggle its state (enabled/disabled).

– From the *Rule* menu, select *Enable All* or *Disable All* to set the state for all rules at once.

3 To restart the test, reset the protocol observer. For more information, see *"How to Reset the Protocol Observer" on page 36*.

**NOTE** If the rule mask has been changed, you need not reset the protocol checker explicitly, because a change in the mask column will remove all displayed errors.

# Watching the Protocol Observer

The protocol observer monitors the PCI-X bus continuously while the testcard is powered. The results displayed in the Protocol Observer window, however, are only updated on demand. Therefore, there is the need to upload the result data from the testcard, and maybe to reset the observer (that is, to clear the results).

## How to Upload Protocol Observer Results

The results of the protocol observer are not automatically uploaded to be displayed in the Protocol Observer window.

To upload the current state of the testcard registers to the display:

1 If the Protocol Check window is not displayed yet, select *Protocol Check...* from the *Analyzer* menu.

2 Click the *Read from card* button.

The current data will be uploaded from the testcard and be displayed in the window.



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## How to Reset the Protocol Observer

To restart a test, for example, for detecting the repeated occurrence of a protocol violation, you can reset the protocol observer.

To reset the protocol observer:

1 If the Protocol Check window is not displayed yet, select *Protocol Check...* from the *Analyzer* menu.

2 Click the *Clear* button.

This sets all rule states to OK, the total of *Rules violated* to 0, and clears the *First violated* rule. The protocol observer continues immediately. If a protocol violation cannot be cleared, this indicates that the violation is still present on the bus.

**NOTE** You can set the run options to clear the protocol check results with each start of a data capture.



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# Saving and Re-Using the Setups

The setups entered during a session can be saved to disk when exiting the program.

Because you might need different settings for different tests, you can also store the settings in separate test setup files.

## Re-Using Test Setups

The test setup files (.bst) contain all information required to repeat a test later-on, for example, the setups for the PCI-X Exerciser's initiator and target devices (if the PCI-X Exerciser option has been installed).

The functions for handling setup files can quickly be accessed via the buttons in the *File* group:






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# Upgrading the Testcard

If you have purchased software options for your PCI-X testcard, they need to be enabled after installation.

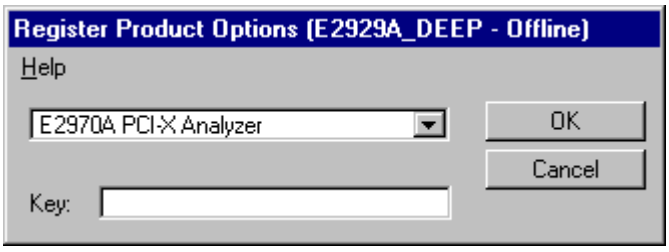
If you have added the PCI-X Exerciser option, the PCI-X state logic analyzer with 2-MB state trace memory and/or the C-API/PPR option subsequently, the testcard hardware needs to be upgraded.

## How to Install Software Options

To enable software options for the PCI-X testcard:

1 From the *Setup* menu, select *Testcard Configuration*.

2 From the *HW Config* menu, select *Register Product Options*.




Repeat the following steps for each software add-on to be enabled:

1 Select the software option from the list.

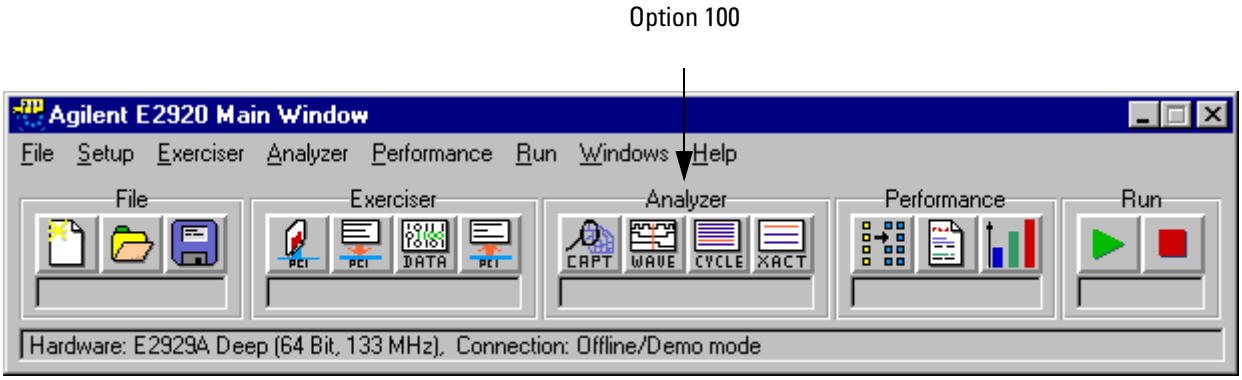
2 Enter the license key printed on the software certificate in the *Key* text field.

3 Click *OK*.



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The software options providing additional user interface features will become visible in the main window:




NOTE Store the software certificates in a safe place.

# Upgrading the Testcard Hardware

If you have added the PCI-X Exerciser option, the PCI-X state logic analyzer with 2-MB state trace memory and/or the C-API/PPR option subsequently, the testcard hardware needs to be upgraded.

For upgrading the testcard hardware, send the testcard to the address specified in the papers shipped with your testcard.

After upgrading the hardware you need to enable the new software options as described in *"How to Install Software Options" on page 39*.



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# Updating the Testcard

After a software update, a version conflict with the on-board firmware can occur. In this case, the hardware must be updated.

## How to Check the Hardware

When connecting to the card and during program start, the hardware check is performed automatically. You can also start the hardware check on your own (for example, if you changed to another testcard without restarting the software):

- From the *Setup* menu, select *Check Hardware*.

A message shows whether or not a hardware update is required.

## How to Update the Testcard Hardware

To perform the hardware update:

1. From the *Setup* menu, select *Update HW*.
2. In the *Port* section, select the control interface to be used and enter the required parameters for that control interface.
3. Click *OK*.

   The flashing red/green indicator will show the progress of the update. A message will appear after the hardware update has been completed successfully.
4. From the *Setup* menu, select *Check Hardware* to verify that hardware and software are compatible now.



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# Application Interfaces

The application interfaces can be used to exchange data between the Agilent E2929A/B testcard and external devices.

## PCI-X Interface

**I/O Buffers**

The I/O buffers provide the following features:

- The I/O buffers are fully compliant to the PCI-X Specification, (timing and loading). The V/I curve corresponds to AGP.
- The connector keying (3.3V) is performed to prevent damage.

**Clocking**

The clocking stands out for:

- In PCI mode: Any frequency from DC to 33 MHz is supported.
- In PCI-X mode: The frequencies DC, 33 MHz, 66 MHz, 100 MHz and 133 MHz are supported with automatic detection.

  These frequencies are automatically detected using the RST# encoding of TRDY#, DEVSEL# and STOP#. This selects the PLL range. You can override this selection by using the dip switches (see *"Dip Switches" on page 47*.)

  If the needed frequency is between 33 MHz and 133 MHz, you have to set the PLL by using the dip switches.
- In PCI and PCI-X mode: You can use a dip switch to turn the PLL completely off for using the testcard at HW-emulation speed (down to DC).



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# Trigger I/O Connectors

The Agilent E2929A/B testcard provides four trigger-in/ trigger-out signals.

**Trigger-In**

The trigger-in pins can be used:

- to synchronize the traffic generation of the testcard to an external trigger event.
- to synchronize multiple testcards among themselves.

**NOTE** If the input is used as a clock accurate input, the trigger-input signal must meet the input timing requirements of PCI-X at this pin.

The trigger signal can also change the status at any point in time if an uncertainty of 1 clock is acceptable. In this case, the minimum pulse width is one PCI-X clock period plus 2 nsec. Double buffering is implemented to avoid instability. The input level specification is identical to PCI-X.

As default, after power up, the pins are set as input pins only.

**Trigger-Out**

The trigger-out pins can be used:

- to trigger an external ocilloscope or logic analyzer
  - on a data miscompare, or
  - on a protocol violation, or
  - when the built-in analyzer triggers.
- to trigger other testcards on the involvement of this testcard in a particular transaction.

The output timing is identical to PCI-X output signals.

The trigger port features the following:

- 3.3V LVTTL outputs (Vohmin = 2.4 V can also drive 5 V TTL inputs)
- 3.3V LVTTL inputs (Vihmax = 3,6 V)

The outputs of the trigger port can withstand a short and are disabled after power up.



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## Trigger Port Connector and Pin Configuration

The following figure shows the connector and pin configuration:

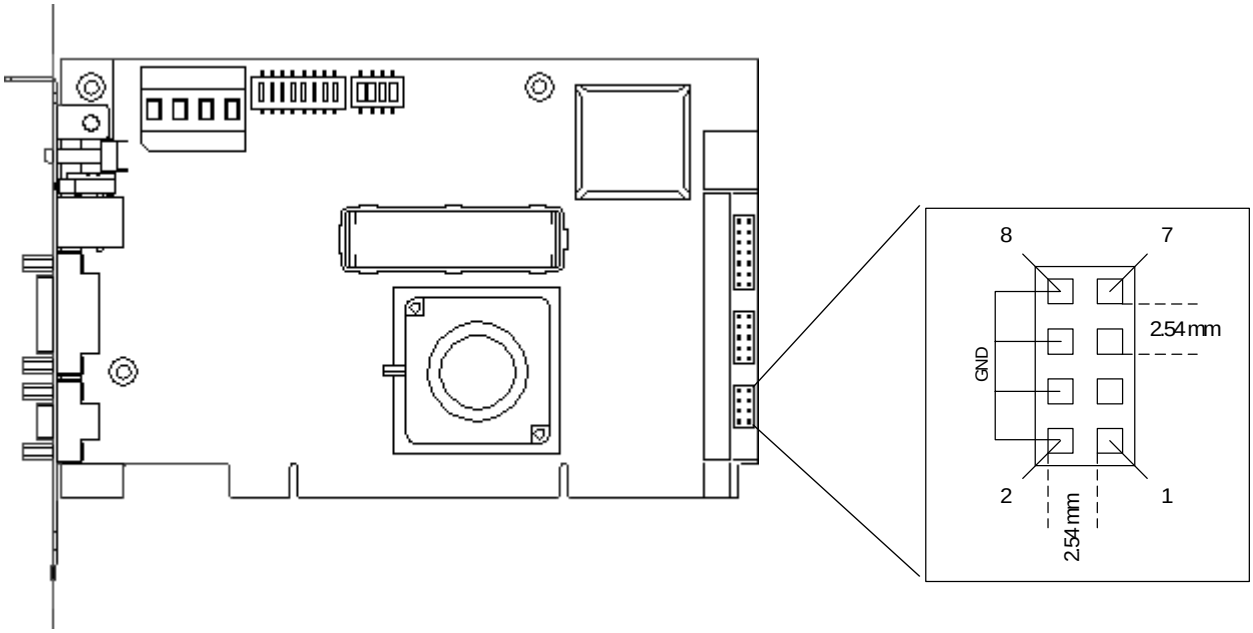



**Table 2 Trigger I/O Pin Configuration**

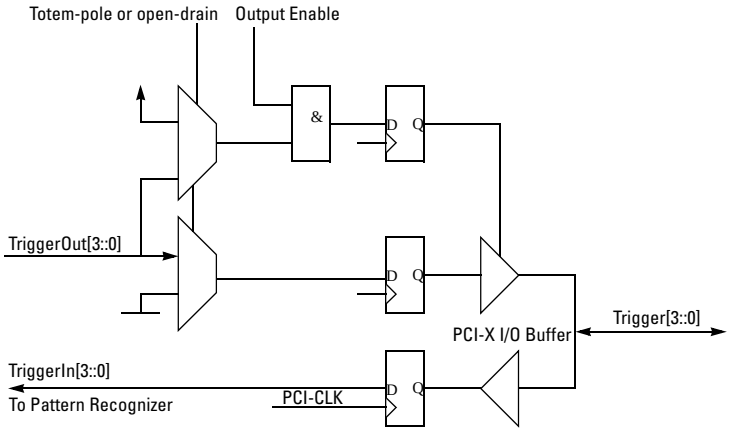
| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | Trigger[0] | 2 | GND |
| 3 | Trigger[1] | 4 | GND |
| 5 | Trigger[2] | 6 | GND |
| 7 | Trigger[3] | 8 | GND |



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## Trigger Port Block Diagram

The figure below shows the block diagram of the trigger port.






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# Dip Switches

There are twelve dip switches organized into a large block and a short block on the testcard, whose functions are described in the following tables:

**Table 3 Large DIP Switch**

| Switch # | Position | Function | Description on the Testcard |
|---|---|---|---|
| 1 | On (default) | Configuration space decoder is enabled. | VISIBLE |
| | Off | Configuration space decoder is disabled. The configuration space and the whole testcard is completely invisible to the system configuration SW. This is useful in pure analyzer applications. | |
| 2 | On (default) | Loading default setup is enabled. | USR SETTNG |
| | Off | Loading default setup is disabled. In case the programmed decoder setting is not understood by the BIOS, the factory default can be loaded to bring the testcard back into a delivered state, and thus you can get access to the testcard again. | |
| 3 | On (default) | The testcard boots firmware and is in normal operating mode. | STD/RECOVR |
| | Off | The testcard stays in core mode. This is a recover mode that allows you to reprogram the firmware of the testcard. This will be helpful in case the testcard does not respond or boot correctly into the standard operating mode. | |
| 4 | On (default) | reserved | AUX0 |
| | Off | | |
| 5 | On (default) | reserved | AUX1 |
| | Off | | |
| 6 | On (default) | reserved | AUX2 |
| | Off | | |
| 7 | On (default) | reserved | AUX3 |
| | Off | | |
| 8 | On (default) | reserved | AUX4 |
| | Off | | |



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The small dip switch controls the internal clock mode settings of the testcard. For internal clock mode, see *"Short Dip Switch" on page 48*.

**Table 4 Short Dip Switch**

| Switch 1 2 3 4 | Function |
|---|---|
| 0 0 0 0 | PLL Off |
| 1 0 0 0 | 37 MHz to 66 MHz |
| 1 0 0 1 | 50 MHz to 88 MHz |
| 1 0 1 0 | 75 MHz to 133 MHz |
| 1 1 1 1 | Auto Range Select |

# PCIXCAP Jumper

The PCIXCAP jumper defines the behavior of the PCIXCAP pin on the PCI-X connector.

| Name | Position | Function |
|---|---|---|
| P701 | Closed | PCI-X 66 |
| | Open | PCI-X 133 |

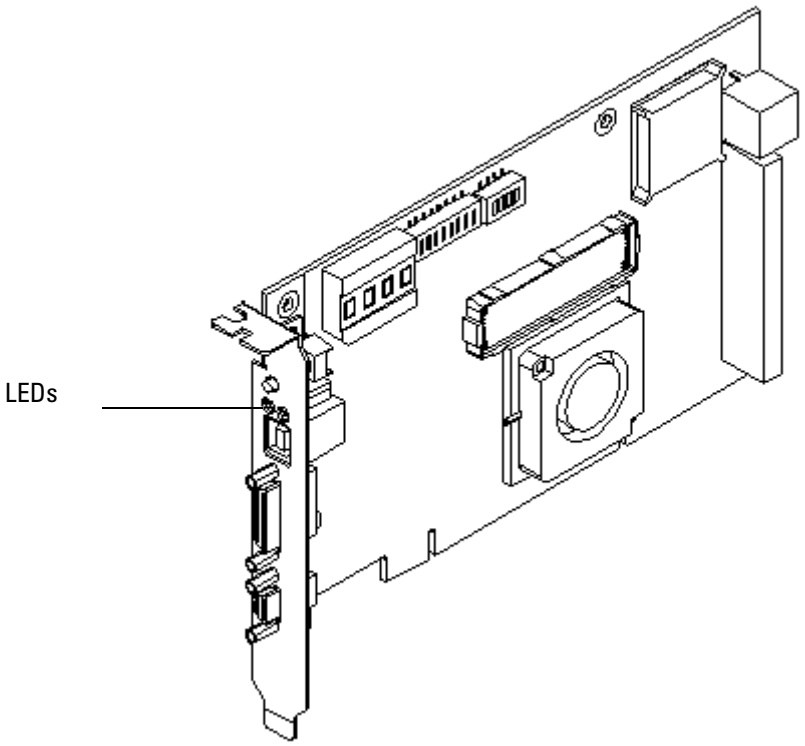


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# LEDs on the Testcard

The LEDs on the Agilent E2929A/B testcard show the testcard's status.

The following figure shows the position of the LEDs on the testcard:






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The following table shows the meaning of the LEDs:

**Table 5 Meaning of the LEDs**

| LED | State | Information |
|---|---|---|
| Exception LED (red) | off | The testcard is working properly. |
| | on | The testcard is booting. |
| Run Indicator LED (green) | off | No power. |
| | on | Power good. |

If the red LED and the green LED are alternatingly flashing with 3 Hz, a **fatal error** has occurred. Both LEDs also flash after use of the Ping button in the Testcard Configuration dialog box (simultaneously, 1 Hz).

# Analyzer Interface

The mainboard contains an interface (400-pin connector) to a piggyback board. This interface can either be connected to a piggyback board that contains a built-in logic analyzer or has connections for an external Agilent logic analyzer.

## I/F to Piggyback with Built-In Analyzer

The piggyback analyzer is a 2 MB state logic analyzer capable of tracing PCI-X signals. The PCI-X signals include:

- Bus state information
- Error conditions as protocol error violations
- Data miscompare
- Data incomplete errors

Additionally the external trigger signals are seen in the trace memory.



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# I/F to External Agilent Logic Analyzer

This piggyback board contains connectors to a standard Agilent logic analyzer. The board has the following properties:

- All PCI-X signals, the bus state and external trigger signals can be observed.
- The board has ready termination for LA Agilent 16700A series.
- Signals are always propagated, independent of the exerciser status.
- The signals are registered and a few clocks delayed to the original PCI-X clock.



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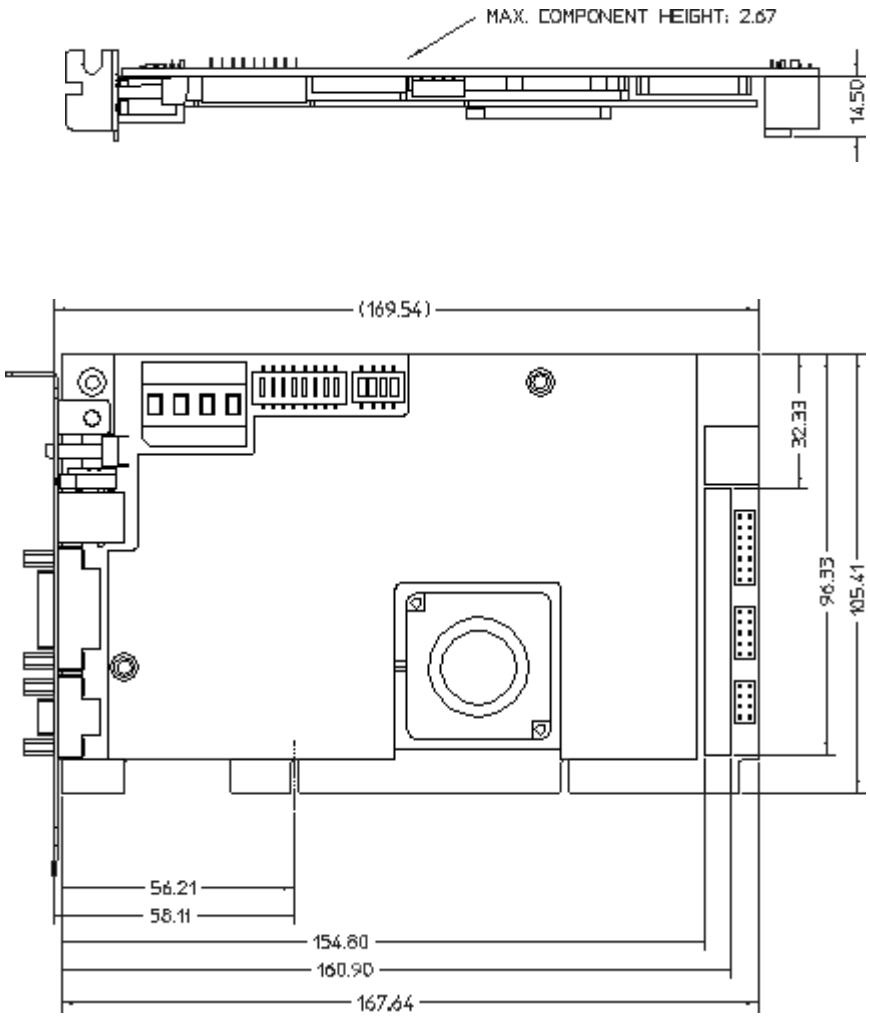
# Dimensions of the Agilent E2929A/B Testcard

This section give information about the real hardware dimensions of the testcard. It shows the dimensions of the testcard first with option 100, then without.



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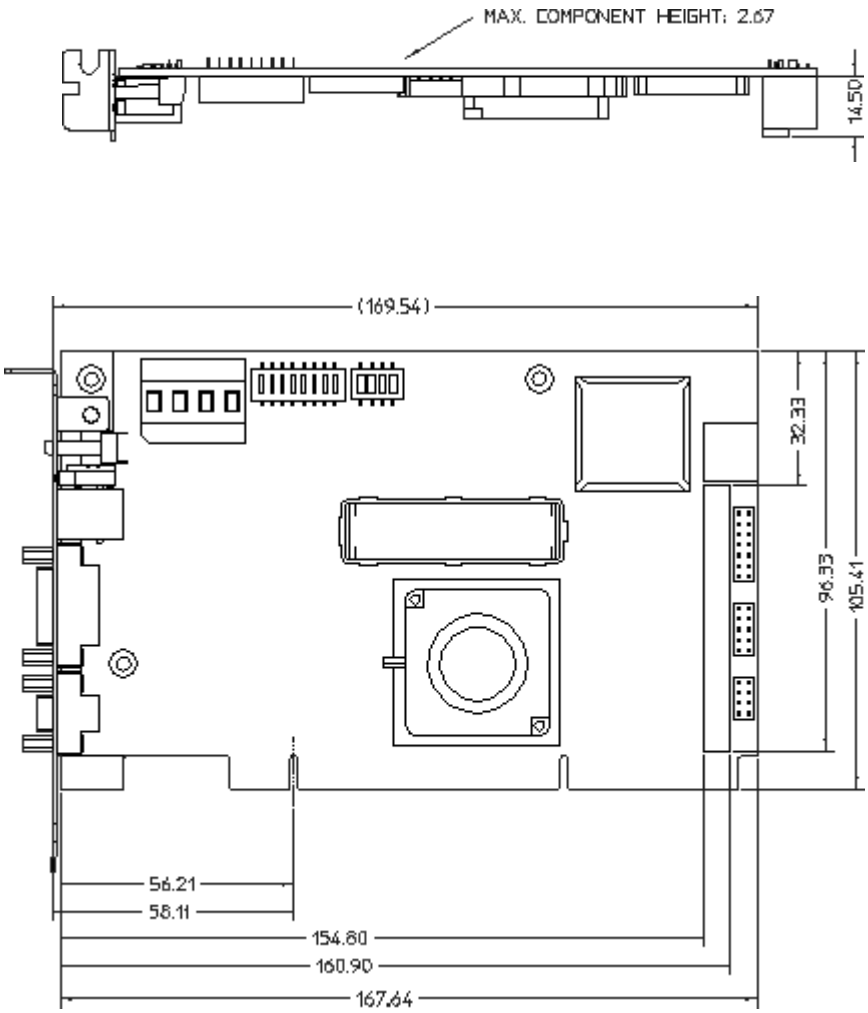
## Dimensions for E2929A/B with Option 100 (E2929A/B Deep)






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## Dimensions for E2929A/B without Option 100 (E2929A/B)






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## Dimensions of the Agilent E2929A/B Testcard



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# Glossary

This glossary contains terms used to describe and explain the functions and capabilities of the testcard. It contains a short explanation of each term.

If you do not find a term in this glossary, you can also look in the index of this manual, or in the glossary of the PCI-X Specification.

## A

### ADB (allowable disconnect boundary)

A naturally aligned 128-byte boundary. Initiators and targets are permitted to disconnect burst transactions only on ADBs.

### Alignment

Alignment occurs in multiple contexts:

- **Sample alignment in the trace memory**

  The samples in the trace memory are aligned to ensure that information that occurred simultaneously (that is: in the same clock) is aligned according to time. For example, command and address are latched, and aligned to data.

- **PCI-X bus address alignment**

  When transferring data via the PCI-X bus, the address alignment must often meet certain requirements for certain transfers. For example, when using cacheable resources, data must be aligned to cache line size.

  When accessing the testcard's data memory via the PCI-X bus for fast transfers, the internal address and the PCI-X bus address are to be aligned equally.

### Application Interface

The application interfaces are used by applications (external software or hardware) for exchanging information with the testcard.



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### Attribute

The 36-bit field contained on C/BE[3::0]# and AD[31::00] during the attribute phase of a PCI-X transaction. Used for further definition of the transaction.

### Attribute Phase

The clock after the address phase(s). The lower bus halves (C/BE[3::0]# and AD[31::00]) contain the attributes. The upper bus halves (C/BE[7::4]# and AD[63::32]) are reserved and driven high by 64-bit initiators.

## B

### Block Transfer

See Requester-Initiator Block Transfer.

## C

### Clock Cycle

A clock cycle is the smallest granularity in the PCI-X protocol.

### Control Interfaces

These are the testcard's interfaces for transferring control data and test results between the software and the testcard. The testcard can be controlled via the Fast Host Interface, RS-232, or by programming registers from PCI-X, which can be mapped into user configuration space or into another PCI-X address space.

See *"Connecting to the Testcard" on page 29*.

### Control PC

This PC runs the software controlling the testcard.

## D

### Data Memory

See Memory.

### Data Transfer

See Transfer.

### Decoder

The decoders of the testcard determine whether or not the testcard's target should claim a transaction on the bus. The decoders recognize programmed address ranges, translate them into an internal address range of an internal resource (such as data memory) and call the testcard's target unit to process the transaction.



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### E Exerciser

The PCI-X Exerciser functions enable the testcard to emulate a PCI-X requester-initiator, completer-target, completer-initiator or requester-target:

- As a **requester-initiator** device, it initiates data transfers on the PCI-X bus, allowing it to test target devices by exposing them to the initiator's attempts to transfer data to or from the target devices.
- As a **completer-target** device, it reacts to a initiator's attempts to transfer data to or from it.
- As a **completer-initiator** device, it handles split completion transactions.
- As a **requester-target** device, it handles open requests.

### H Host

Same as Control PC.

### I Interrupt

The PCI-X bus provides dedicated PCI-X interrupt lines. The testcard both recognizes and issues PCI-X interrupts.

### M Memory

The testcard provides different types of memory:

- **Data Memory**

  The data memory holds received test data, and data to be transferred by the testcard. It is shared between the PCI-X requester-initiator and the PCI-X target, and it can be set up or read out with host access functions. It also provides a data compare unit to compare incoming data with previously stored reference data.

- **Trace Memory**

  The trace memory is part of the testcard's Analyzer. It stores all PCI-X signals along with extensive bus state and Exerciser state information. All this information is aligned.

Furthermore, the testcard provides memory to store test setups, programming parameters, etc. (for example, behavior memories and block transfer memory).



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## P

### Pattern Term

The pattern terms are programmable for recognizing bus events (signal patterns on the bus). They are part of the testcard's Analyzer.

The output of pattern terms (always 1 or 0) can be used in Analyzer functions, for example, to trigger trace memory or to count bus events.

### PCI-X Analyzer

The testcard's Analyzer queries for information on the PCI-X bus, the state of the Exerciser, or the external trigger inputs, so that it can check capture traffic.

### PCI-X Status

The testcard queries the status of the PCI-X bus and provides registers to request information about the life status, reset, clock frequency, bus activity, the involvement of the testcard's Exerciser, and error states.

### Protocol Behavior

The PCI-X transfers performed by the testcard can be equipped with protocol behaviors, for example, parity errors. This allows you to see whether the system under test can handle these behaviors. How the behaviors are to be applied is stored in the behavior memories of the testcard.

The behavior memories contain a series of behaviors for the testcard's requester-initiator, completer-target, completer-initiator and requester-target.

The behaviors are programmed per intended transaction. The behaviors are used sequentially, and can be programmed to contain random protocol variations (only with C-API/PPR option).



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## R Requester-Initiator Block Transfer

A requester-initiator block transfer specifies a requester-initiator operation for the testcard's Exerciser. The Exerciser needs the following information to execute a requester-initiator operation:

- bus command
- bus address
- internal address
- number of bytes to be transferred
- the queue into which the block is put
- the data resource

A block transfer may need one or more transactions to complete, depending on the specified initiator and target behaviors, for example, disconnect or retry.

The block transfer settings are stored in the requester-initiator block transfer memory, which contains a linear series of block transfers for the requester-initiator.

## S Storage Qualifier

Storage qualifiers are used by the Analyzer when storing samples in the trace memory. The trace memory stores samples of bus states for post-processed analysis. To exclude unnecessary samples from being stored, the Analyzer provides storage qualifiers.

### Split Transaction

A single logical transfer containing an initial transaction (the Split Request) that the target (the completer or a bridge) terminates with Split Response, followed by one or more transactions (the Split Completions) initiated by the completer (or bridge) to send the read data (if a read) or a completion message back to the requester.

For further information, refer to the PCI-X Specification.

### System under Test

The system under test is the PCI-X system into which the testcard is plugged.



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## T

### Transaction

A transaction consists of an address phase, an attribute phase, a target response phase and a series of one or more data phases (burst).

### Transfer

Data transfers are those clocks within a data phase in which data is actually transferred (when both IRDY# and TRDY# are asserted).

### Trigger

The testcard provides different types of triggers:

- **Trace Memory Trigger**

  The trace memory trigger is part of the Analyzer. The trace memory stores samples of bus states for post-processed analysis. To control the start of the sampling, the Analyzer provides the trace memory trigger.

- **External Trigger (Trigger Input and Output)**

  The testcard provides input lines to be used as trigger input and output.

  As input, they can be used in pattern terms just like PCI-X signals.

  As output, they can be used to trigger other devices.



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