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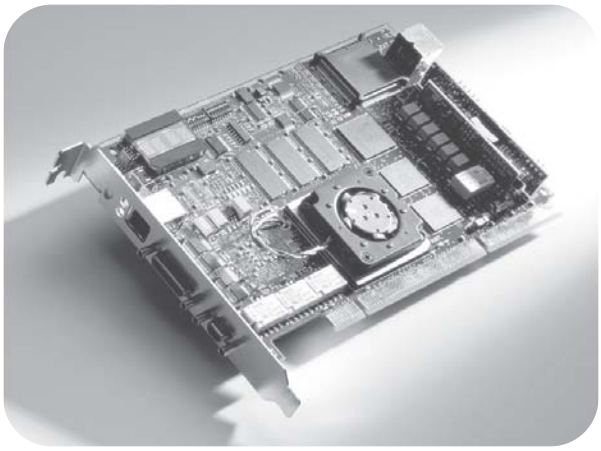
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Agilent Technologies E2930B Exerciser and Protocol Analyzer for PCI-X 2.0

Technical Overview



Key Specifications

- **Support for PCI-X Mode 1 and 2 (Mode 2 up to 266 MT/s DDR)**
- **64 bit data and addressing**
- **Exerciser (option #300) with full capabilities, including split transactions, 4 MB of data memory (512K x 64 bit) and real-time data generator**
- **Unidirectional data path verification**
- **Real time data compare**
- **PCI-X Mode 1 and 2 compliant**
- **64 PCI-X protocol rules**
- **USB 2.0**
- **Controllable in-system through PCI-X interface**
- **PCI-X state analyzer with 4M state trace memory**
- **Realtime performance analysis**
  System Validation Pack (option #310) with compliance tests
- **C-API (command application programmming interface)**
- **GUI (Graphical User Interface)**
- **Tcl interface**
- **Agilent Patented Protocol Permutator and Randomizer Technology**

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Agilent E2930B Exerciser and Protocol Analyzer for PCI-X 2.0

The Exerciser and Protocol Analyzer for PCI-X 2.0 Mode 1 and Mode 2 provides R&D and QA engineers with a fast and predictable way to debug, optimize and validate PCI-X based designs, like servers, motherboards, chip-sets, RAID systems or network interface cards. The modular test card combines a PCI-X protocol checker, a PCI-X exerciser (option #300) with full requester and completer capabilities to generate any kind of PCI-X transfer and a PCI-X state logic analyzer.

Individual software modules address specific needs during design bring up, design validation and compliance testing.

Verification of PCI-X protocol compliance

The E2930B features a PCI-X protocol checker, which runs constantly, checking for PCI-X protocol rule violations in real-time. In total, 64 protocol rules are checked concurrently. All rules are derived from the PCI-X 2.0 specification. Thus, simply plugging the E2930B into a PCI-X system allows you to check for PCI-X protocol compliance. The E2930B reports a list of all the errors that have occurred. For the purpose of debugging, the protocol checker can be used to trigger either the state logic analyzer or an external logic analyzer. Also, each individual protocol rule can be masked.

Bring Up and Debug

With its capabilities in generating PCI-X 2.0 traffic and simultaneously analyzing the generated traffic, the E2930B is perfectly suited for bring up and debug of PCI-X 2.0 and PCI-X 1.0 systems. The analyzer displays, with several levels of hierarchy, the captured trace and helps the engineer to debug and understand what is happening in the system. The graphical user interface supports the user in setting up various types of transactions and programming the analyzer.

Predictable System and Chip Validation

The E2930B PCI-X Exerciser (option #300) features a fully controllable requester and completer, real-time data compare and hardware support for the Agilent patented Protocol Permutation and Randomizing technique and the patented undirectional data verification method. This allows engineers to validate and stress the PCI-X system with specific and fully repeatable test cases.

The testcard can autonomously and repeatedly generate a series of programmable transactions, whilst generating protocol permutations in hardware and checking for data integrity errors and protocol violations. Key capabilities for this use model are:

- Generates deterministic traffic
- Exhaustive coverage of protocol corner cases through a patented Protocol Permutator and Randomizer (PPR,Option #320) technology
- Checks for data integrity and protocol errors.

The benefits of using this approach are:

- The state of bridges is not affected through traffic that may be needed to setup the testcard, because the testcard can run tests autonomously and predictably.
- Very high coverage through HW permutation of testcases (more than 100 000 testcases or transactions per second).
- Very short test execution time. Multiple testcards can be synchronized across multiple buses or even across multiple systems by using bus event based triggering or external trigger cabling.

Efficient design debugging

To get an insight into your system, a simple click of the mouse is all that is needed to setup a specific trigger or the state analyzer. The state analyzer offers impressive trigger and storage qualifier capabilities making it easier to find complex error conditions.

Besides conventional pattern terms for all PCI-X 2.0 signals, an additional bus observer makes the current bus status (e.g. address phase, attribute phase, data phase, idle phase etc.) transparent, and thus simplifies the setup of trigger conditions. Combining additional error pattern terms, external trigger inputs and trigger sequencer capabilities, the E2930B gives you the ultimate power to capture the data you need.

System Benefits

Easy PCI-X 2.0 system evaluation

- Ability to work in PCI-X mode 1 and mode 2
- Windows based GUI for interactive use
- State analyzer for PCI-X 2.0
- Exerciser for PCI-X 2.0 stresses your system's corner cases predictably and repeatedly
- Easy system validation using ready-to-run tests
- Over 1,000,000 test cases in less than 5 seconds[1]
- Programmable In-System
- C-Application Programming Interface
- TCL interface

System Overview

The E2930B is a short PCI card, which can simply be plugged into the system under test. It is controlled by an interactive Graphical User Interface from a custom-written C program, or from a TCL interface (Option #320 required). The software can either be installed on the system under test itself - controlling the card through the PCI-X 2.0 system bus, or on an external host - controlling the card by USB 2.0, designed for a high data transfer speed.

1 test case @133MHz = (50 clocks delay + avg. 250 clocks for 2k bursts) *7.5ns = 2.5us. Thus, 1,000,000 test cases need = 2.5s + 2s setup time.

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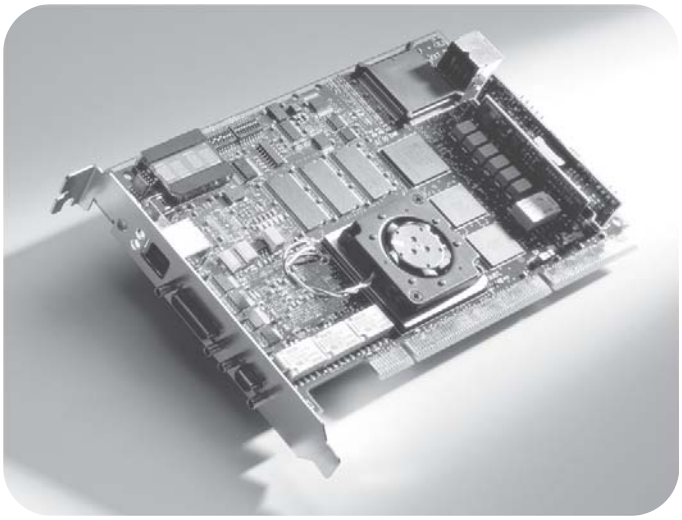


Figure 1. E2930B

PCI-X Protocol Checker

The E2930B basic configuration supports the PCI-X 2.0 protocol checker which checks over 64 protocol rules in real-time. Each rule can be individually masked to suppress the triggering of known problems. The rules are derived from the PCI-X 2.0 specification[2], and are designed to find any possible violations of the PCI-X 2.0 protocol. When a protocol violation is detected, the protocol checker can:

- store the rule number of the first (non-masked) violated rule
- list all found protocol errors
- accumulate the number of violated rules
- directly trigger the PCI-X 2.0 state analyzer's trace memory.
- trigger externally connected logic analyzer or additional E2930B cards (or even E2929Bs for cross bus trigger ing if necessary).

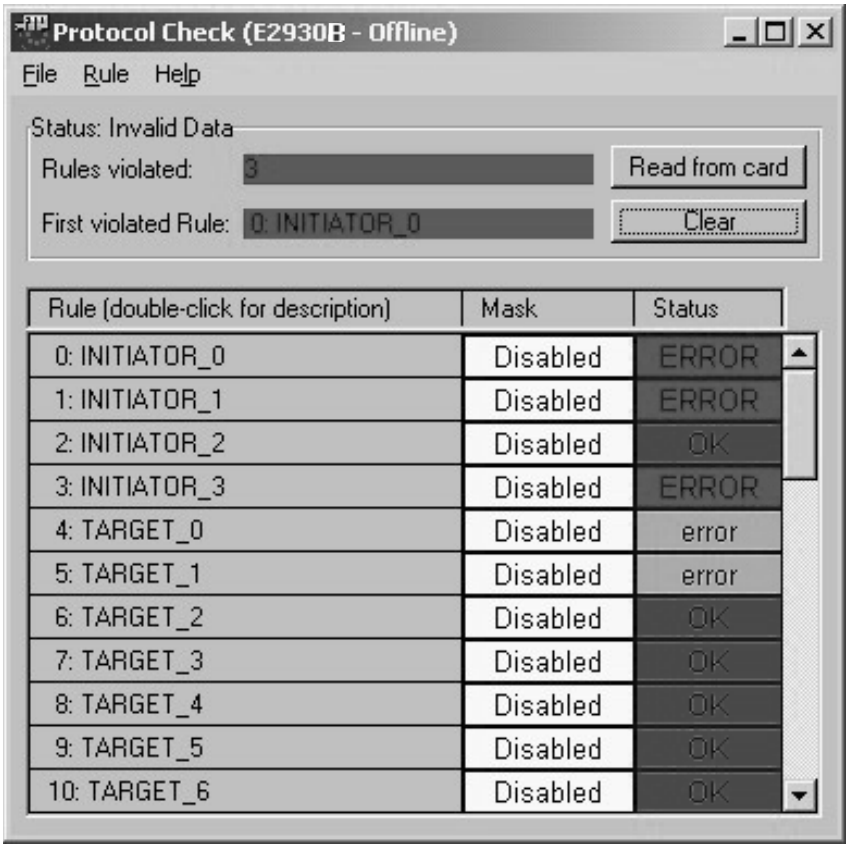


Figure 2. Protocol Checker

2 PCI-X Addendum to the PCI Local Bus Specification Revision 2.0, July/29/2002

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State analyzer

The PCI-X 2.0 state analyzer observes all signals (except JTAG) specified by the PCI-X 2.0 specification for a 64 bit 66/100/133 MHz system.
In detail, the analyzer captures:

- 4M samples
- all 64 bit PCI-X address/data signals
- PCI-X 2.0 protocol errors
- bus observer to decoded bus state signals, time aligned to the bus signals
- active requester and completer signals, aligned with the bus signals for easy identification of transactions involving the exerciser
- 4 signals from the trigger I/O connector.

Storage qualification

A simple push-button storage qualifier selects storage to optimize the use of the state analyzer memory, depending on the level of detail you need. For example:

- store all states
- suppress idle cycles
- suppress wait cycles
- suppress data transfers
- by pattern term.

The storage qualification can also be user programmed, using the trigger sequencer.

11 Pattern terms

The E2930B provides a total of 11 pattern terms:

- 4 pattern terms monitoring all PCI-X 2.0 bus signals (excluding JTAG signals) and trigger inputs
- 1 pattern term monitoring the protocol checker error signals, spilt transaction errors and data compare errors
- 6 pattern terms monitoring the bus observer.

To set up a pattern, each individual bit can be masked 0/1/X. For bit fields, such as C/BE, all bit combinations can be defined individually.

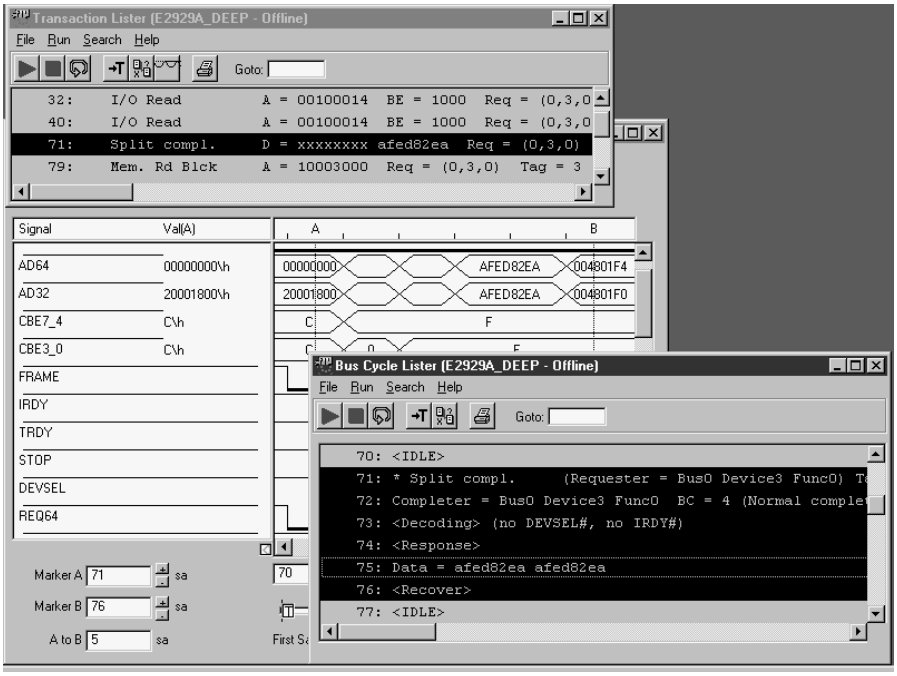


Figure 3. Waveform viewer: Bus cycle lister and transaction lister with cross references.

Bus observer for easy triggering

The bus observer allows easy triggering for the engineer's daily tasks by defining one simple pattern term. The bus observer automatically detects:

- idle bus cycles
- address cycles, the 1st and 2nd half of dual address cycles respectively
- attribute phase
- transactions to 32 or 64 bit address space
- decode cycles, decode speed A/B/C/subtractive
- data cycles
- 32 or 64 bit transfers
- target responses as claim transactions, single data phase disconnection, disconnection of next address boundary, abort
- split transactions/response
- waits and retries
- master aborts
- terminated unsuccessful transactions.
- PCI-X mode

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16 level trigger sequencer

For extended trigger scenarios, the E2930B features a trigger state machine, which handles up to eleven pattern terms, one termination counter (pre-load and decrement) and up to 16 levels of trigger sequencing Pattern terms can be combined with logical operations AND, OR and NEGATION. The termination counter can be pre-loaded and decrement.

Flexible trigger points

For maximum flexibility, the trigger can be placed at any position in the trace memory.

External trigger I/O

4 trigger I/O signals provide a way to synchronize between multiple PCI/PCI-X test cards of the E2920 Series or other test equipment like a general-purpose logic analyzer. Programmed as input pins, they are observed by the state analyzer and are available as part of the pattern terms.

GUI/C-API control or tcl scripting language interface

The PCI-X 2.0 state analyzer comes with a Windows based GUI (Graphical User Interface), a CLI (Command Line Interface) and a TCL interpreter window. The Command Line Interface (CLI) and the TCL interpreter window allows you to interactively control the PCI Exerciser and Analyzer by entering command functions that correspond with the functions provided by the C-API. The CLI can also process batch files of concatenated command functions.

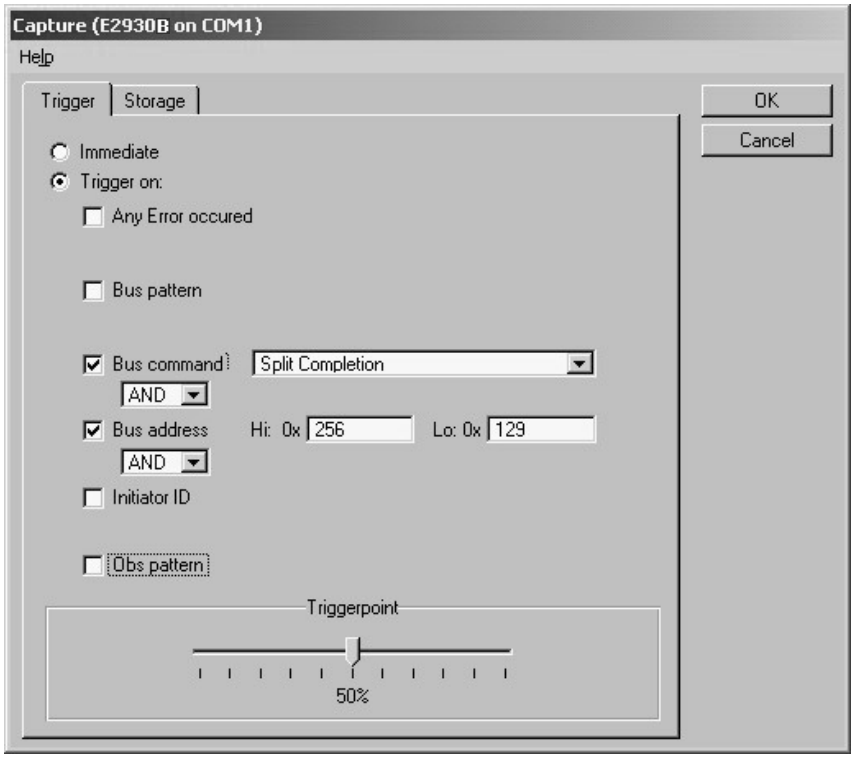


Figure 4. Trigger GUI

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Exerciser (option #300)

The Agilent E2930B has an optional on-board 64 bit PCI-X 2.0 exerciser. The exerciser operates in Mode 1 and Mode 2 with DDR and can emulate and force practically any behavior of a PCI-X 2.0 device imaginable - including blatant protocol violations. This means that the exerciser is able to send and respond to specific traffic patterns including test error recovery systems. The exerciser comes with a graphical user interface (GUI), a command line interface (CLI) and a TCL interface. As an option, the exerciser can be controlled from a C-API (option #320).
The exerciser features:

- one requester-initiator with two requester queues
- one completer with four completer queues to handle independent split-transactions
- one requester-target handling up to 32 open requests.

Requester and completer are fully programmable, operate independently of each other and are able to handle:

- 32/64 bit data transfers
- 32/64 bit addressing
- programmable delays between transactions
- block length up to 4Gbyte
- all 16 PCI-X 2.0 command types, including Device ID Messaging commands.

Configuration space

The E2930B provides configuration space, which is fully programmable. Default values (customizable) are stored in an EEPROM on-board and are used to initialize the configuration space when the power is switched on. The configuration space can be disabled, making the card invisible to BIOS or O/S configuration routines. Thus, analysis tests are possible without having any effect on the device or system under test. The E2930B has the full 4096 Bytes of configuration space required by the PCI-X 2.0 specification.

Architectural overview

The exerciser is based on two main ideas. Firstly, defining requester initiator data blocks, describing “what” data should be transferred and secondly, defining a requester initiator behavior, describing “how” the transfer should be executed.

For the requester initiator, up to 256 blocks of data transfers can be set up . In addition, requester initiator behaviors are set up, specifying how the requester initiator intends to transfer the data blocks over the PCI-X 2.0 bus. If any completer target replies to a transfer and requests a split transaction, the requester initiator data block attributes are moved internally to a split transaction map for further use. The transaction map can manage up to 32 open split transactions. When completing split transactions, the requester target behaviors are used to control the transfer.

The completer target behavior attributes define how the completer target of the E2930B acts. The completer target can manage up to 4 split transaction queues. It is also possible to fully control initiating the completion of split transactions. The completer initiator behavior attributes are used to program this. The programmable transaction scheduler decides whether completer or requester transaction is performed. All data comes or goes through the on-board data memory or from the on-board real-time data generator.

Requester Initiator data block

The requester initiator data block settings define which address space is accessed, and to where data is moved. Up to 256 block transfers can be defined and performed in a linear sequence by one of the two transfer queues. Each block specifies:

- the bus command seen on C/BE[3::0] in the address phase. All valid PCI-X commands are supported
- the 64 bit bus address
- the byte enable value (C/BE[3::0] / C/BE[4::7]
- the start address of the internal data memory
- the number of bytes to be transferred (1byte to 4GB)
- if the real-time data compare for incoming data should be activated
- the start condition for the transfer (immediately or wait for event)
- which transfer queue the data is passed through.

Requester Initiator behavior

The requester initiator behaviors are set to specify the PCI-X transfer behavior per sequence. Up to 256 attribute entries, which can be setup as linear sequence or repeat loops, are allowed.
The attributes control:

- 32 or 64 bit data access
- insertion of 1 to 65535 clock cycles delay between transactions
- the transfer queue to be used
- if an automatic or customer defined tag (0..31) is used the specific sequence length for the transfer (1 to 4096 byte) automatically rounded up to the next qword boundary
- the n-th ADB where the requester initiator disconnects (1 to 32)
- perform 0 to 4 address steps
- how many clock cycles after the address phase REQ# is de-asserted (0 to 2047)
- how often the current transfer attributes are used (repeat value 1 to 256).

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Latencies between requester initiator transactions

The latencies between transactions can be varied using requester initiator behavior property. The minimum latency is in general ≤2 clock cycles (for mode 1 ≤1 clock cycle) - including any sequences of read/write where real-time data compare is involved. A possible exception is if the most recent transaction is a read/write transfer into data memory and the subsequent transaction is a write out of data memory. In this particular case, the latency is 10 to 20 clock cycles. Please note that it is assumed that the master does not need to disconnect before the byte count of the current sequence is transferred and that wait cycles are added if required by the PCI-X specification.

Requester target behavior

The requester behavior attributes are set to specify the PCI-X 2.0 transfer behavior per transaction if a completer requests the completion of a split transaction from a requester initiator. Up to 256 attribute entries, which can be setup as linear sequence or repeat loops, are allowed.
The attributes control:

- the decode speed used (A[3] /B/C)
- acknowledgement of 64 bit data transfers
- the number of initial latency clock cycles (3 to 34)
- the behavior after initial latencies, either accept transfer, disconnect, signal retry or abort
- how often the current behavior is applied (repeat value 1 to 65536).

Completer Target behavior attributes

The completer target behavior attributes give full control over the E2930B completer target behavior, and define how it reacts to a request. Up to 256 attribute entries, which can be setup as linear sequences or repeat loops, are allowed. The attributes control:

[3]Decode speed A is supported up to 66 MHz

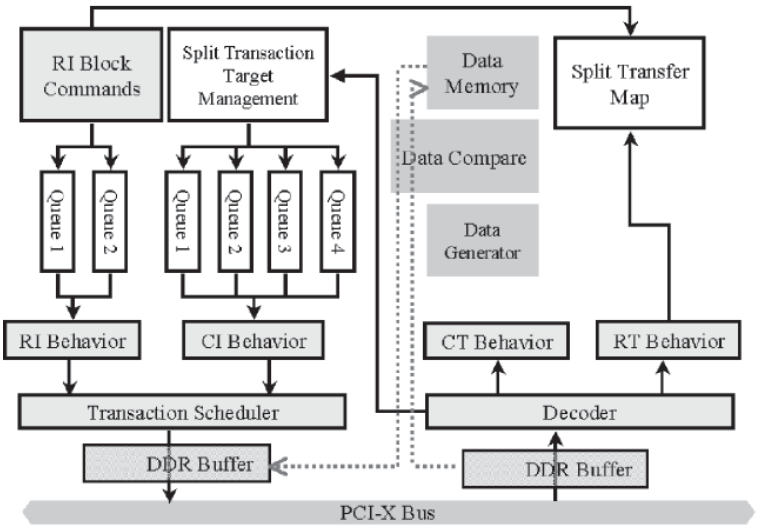


Figure 5. E2930B option #300 PCI-X exerciser architecture

- the decode speed used (A[3] /B/C)
- acknowledgement of 64 bit data transfers
- the number of initial latency clock cycles (0 to 31)
- the behavior after initial latencies, either accept transfer, signal a single data phase, retry or abort
- the behavior in subsequent data phases, either accept all subsequent data phases, disconnect after 1 to 2047 data phases
- signaling a split response, either by identifying an address value or range in the address phase, the decoder accessed, or by a subset of all 16 possible PCI-X commands
- the split transaction queue to be used
- how often the current behavior is applied (repeat value 1 to 65536).

Configuration space and decoders

In total, the E2930B features 6 decoders:

- one standard configuration space decoder, fully customer programmable
- One Device ID Message decoder
- Three programmable target decoders (six bars) that can either hold up to three memory spaces (64 bit) or two memory spaces and two I/O spaces simultaneously
- Decoders can decode up to 4 Gig of address space
- One decoder to access the 64Kbyte expansion ROM
- Additional 4K extended config space

All decoders can be switched off by a dip-switch on the E2930B, making the card completely invisi ble to the system under test.

Completer Initiator behavior

The completer initiator behavior attributes are set to specify the PCI-X transfer behavior per transaction if a completer starts to complete a split transaction. Up to 256 behavior entries, which can be setup as linear sequence or repeat loops, are allowed.

The attributes control:

- the split transaction queue to be served
- the start condition for this transfer
- 32 or 64 bit data transfer
- the number of clock cycles inserted before REQ# is asserted (1 to 65535)
- the number of clock cycles before REQ# is de-asserted (1 to 2047)
- the number of address steps (2 to 6)
- how often the current transfer attributes are used (repeat value 1 to 256)
- disconnect at n-th ADB (1 to 32).

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Completer target latencies

The initial latencies can be programmed with the completer target behavior attributes. Depending on the selected decode speed and address phases, the test card automatically adds the needed number of wait states to achieve the defined initial latency. A minimum of one wait cycle is always added when using decode speed B or C and a minimum of two wait cycles are needed with decode speed A.

Data memory

The E2930B Exerciser option #300 features a 4MB (152K x 64 bit) programmable read/write data memory. Requester and completer share the memory. The address decoders can selectively address it. The data memory can:

- store data from read/write transfers
- be mapped to any PCI-X address space.

Data generator

Instead of using the data memory, the on-board data generator can be used. Without initial latencies, the generator can generate a data pattern, deterministically linked to the data address.

Combined with a second exerciser card and the real-time data compare feature, long-term load stressing on any data path can be performed while errors are detected in real-time (figure 3). The generator features the following patterns:

- walking ones or zeros
- ground bounce
- count up (unique data)
- pseudo random pattern (unique data).The count up and pseudo random pattern are unique up to the length of 1M quad words (4MB). The data uniqueness is derived out of the lower bit 2 to 22 of the bus address.

Real-time data compare

Real-time data compare can be performed either on:

- Memory: when data is written to the memory it is compared against the actual memory content
- Data Generator: based on the data address the generator calculates the expected data and compares it with incoming data.

Exerciser Graphical User Interface

The Graphical User Interface gives you an easy way to setup and control the exerciser.

Master conditional start

The master conditional start window allows you to set up the start conditions for the master traffic. Following a run command, the master can be programmed to start:

- immediately
- triggered by a pattern.

Target decode window

The target decode window lets you configure the target address decoders. As well as configuring the programmable decoders for the exerciser's on-board memory, you can individually enable or disable the decoders for configuration space and expansion ROM. You can also store the current settings as defaults, which will then be used following all subsequent power cycles or PCI-X resets.

Error Injection Capabilities

The E2930B is capable of injecting error conditions into a system including generating inverted parity (PAR and PAR64), signalling a parity error (PERR#), a system error (SERR#) in a specified phase of the transaction, or ECC errors.

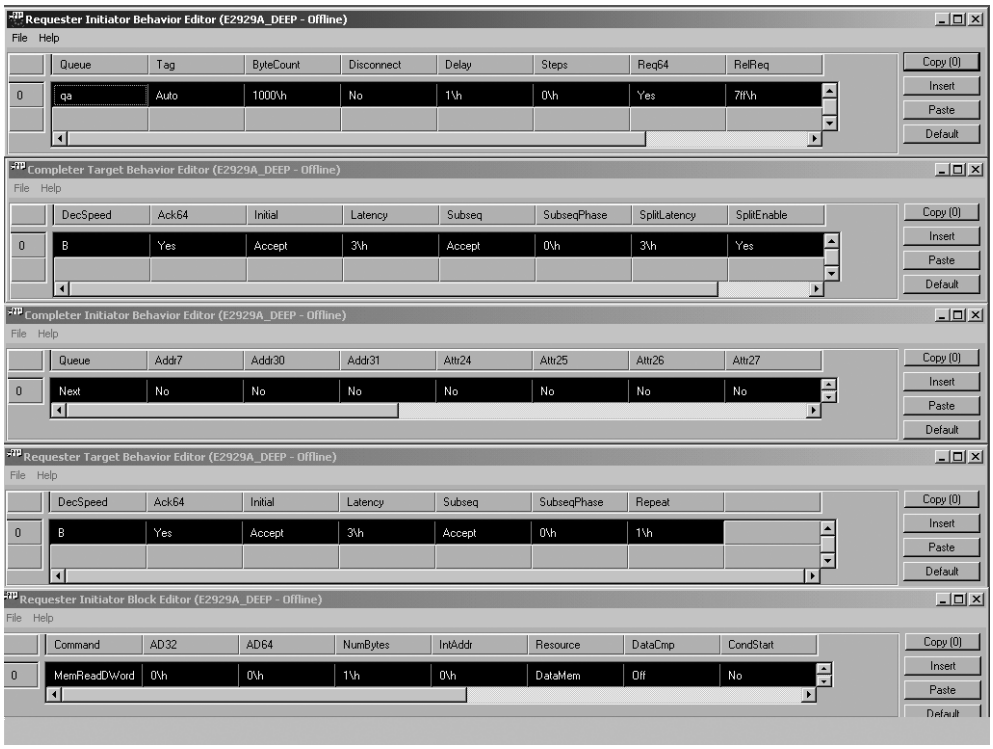


Figure 6. Exerciser GUI with all five different behavior editor windows

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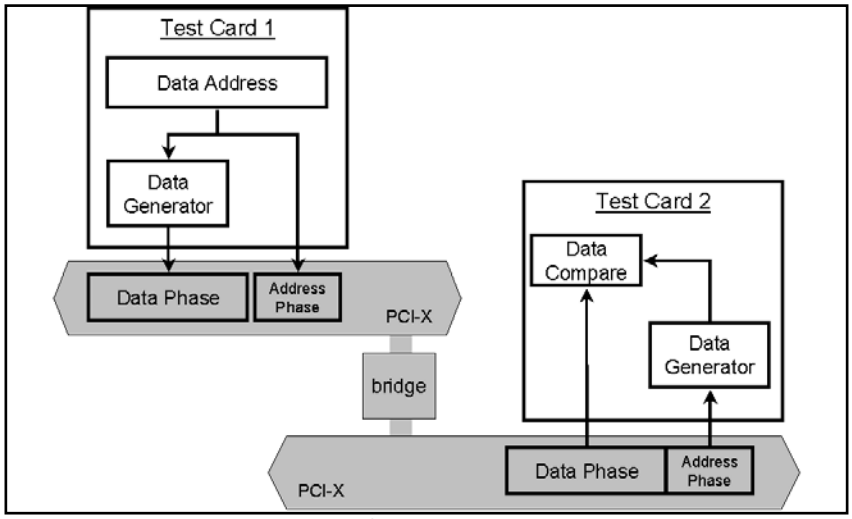


Figure 7. Undirectional data path verification

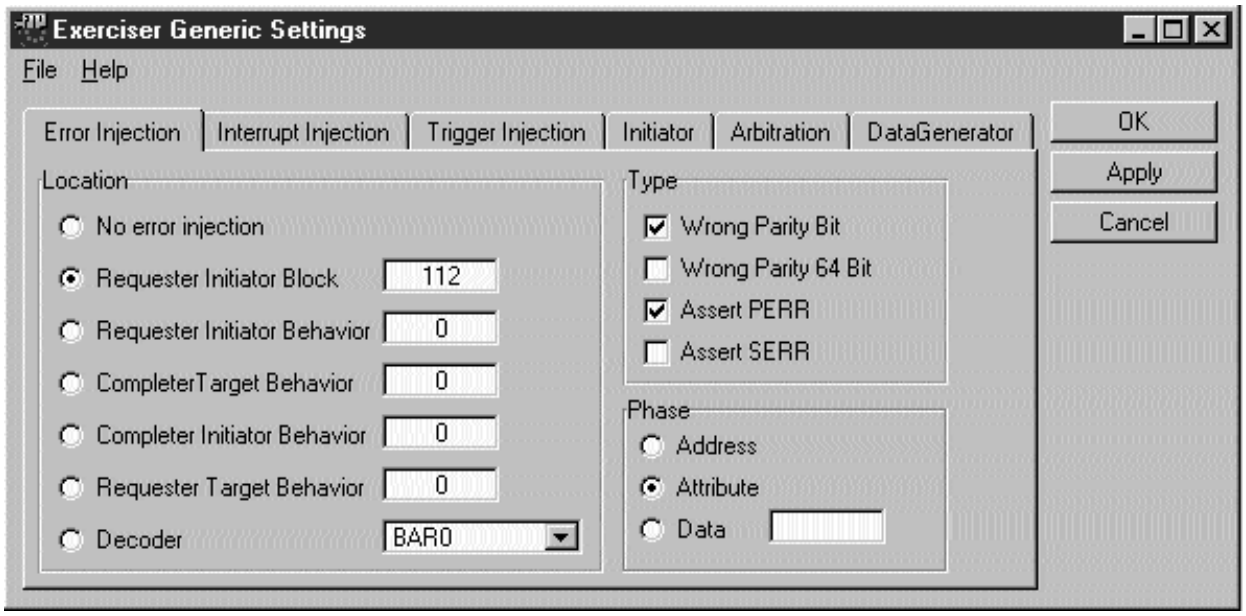


Figure 8. Exerciser Generic Settings

Configuration window

The configuration window lets you view and modify the current configuration space settings of the PCI-X 2.0 exerciser and analyzer card. You can also store the current settings as defaults, which will then be used following all subsequent power cycles or PCI-X 2.0 resets.

Data memory editor

The data memory editor lets you view and modify the contents of the exerciser's on-board memory. This allows you to define the data content for master write transfers or target read accesses to the card, as well as allowing you to view the data received from master read transfers or target write accesses. The data can be viewed in hex format, big or little endian, and 8, 16, 32 and 64 bit size.

Data generator setup window

The data generator setup window allows you to select the algorithm to be used for data generation.

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Agilent System Validation Package, SVP (Option #310)

The System Validation Package is ready-to-use software package, which performs system stress tests during the validation of servers, workstations, PCs, or other PCI/PCI-X based systems.

With its easy-to-use Windows-based GUI, it simplifies test development on setup for engineers and allows easy test execution by technicians.

Choosing the Agilent E2925B, E2928A, E2940A, E2929B and E2930B option #310 adds the System Validation Package to your hardware order.

Target application

The System Validation Package programs and controls multiple PCI/PCI-X Exerciser and Analyzer test cards of the E2920 PCI Series to create realistic application system traffic. The test card approach allows you to set up fully predictable traffic scenarios and gives you measurable test coverage and test predictability. Used for validation of PCI/PCI-X based systems and silicon, it enhances the traditional test method of using off-the-shelf PCI/PCI-X cards.

Outstanding test coverage

Today's validation test methods typically lack time efficiency and repeatable execution of critical system traffic scenarios. Hot mock-up tests, which use off-the-shelf PCI cards to load a system-under-test and wait until an error occurs, are the typical test approaches used today. Now the System Validation Package executes such types of system critical tests within minutes, simply with a mouse click.

PPR, the key technology

Agilent 's patented Protocol Permutation and Randomizing (PPR) technology is the key to predictable and repeatable test coverage.PPR is technology that allows permutation of the PCI/PCI-X protocol and traffic in a determinisitic way. Thus, system critical test patterns are not only transferred between different system components,but also automatically permutate to achieve all possible traffic scenarios.

Stress all critical data paths

By plugging the PCI/PCI-X Exerciser and Analyzer test cards in each individual PCI/PCI-X bus of your system under test, the software is able to automatically test and stress data paths within your system (see figure 9).

A small executable running on the system CPU(s)allows testing within the whole system, not only the I/O system, while tests are run from an external controlling host.

System Validation Package/System Test Library benefits

- Fully controlled test environment for validation of servers, workstations and PCs
- Predictable test coverage
- Repeatable test scenarios
- Documented test results.

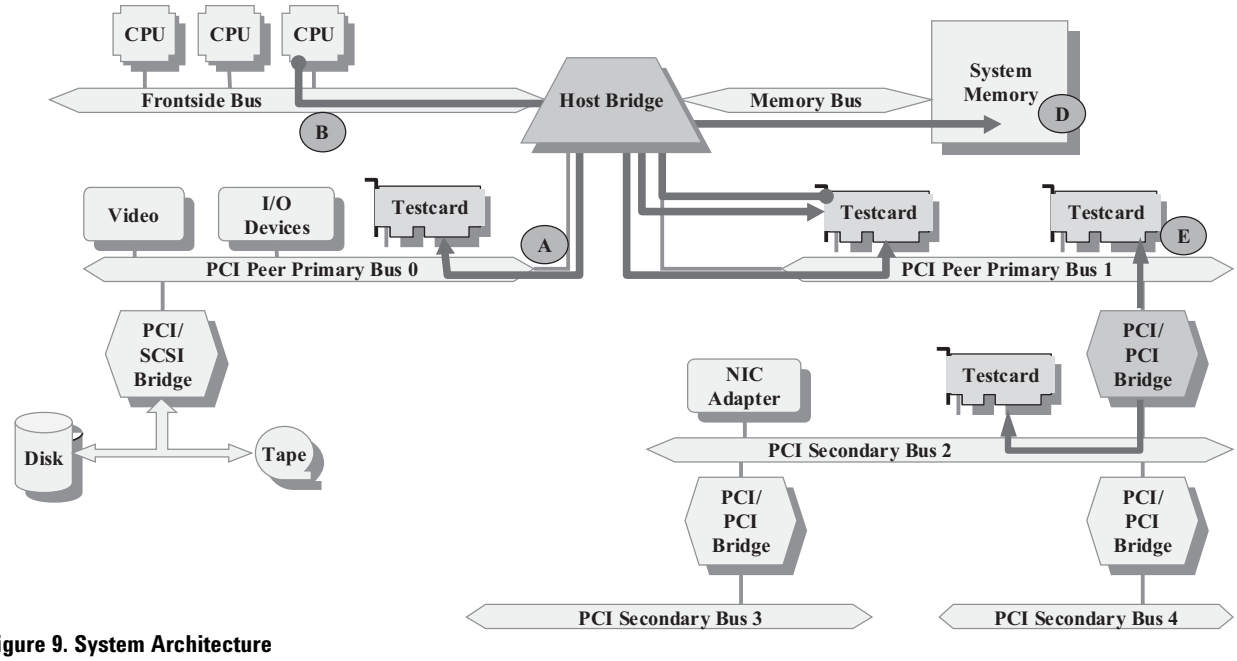


Figure 9. System Architecture

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Test method

The Agilent System Validation Package allows automatic tests and stresses data paths from:

- CPU and Exerciser to system memory
- Exerciser to system memory
- CPU to Exerciser memory space
- CPU to Exerciser I/O space
- Peer to peer traffic
- Master to target traffic
- Load generation.

While testing, the setup emulates typical traffic scenarios in a PCI system. For example, data CPU to SCSI card, LAN to LAN card traffic, concurrent system memory access from LAN card and CPU (see figure 10).

So far, these have been typical traffic scenarios and have been generated within the so-called hot mock-up test. Now the Agilent verification solution significantly extends this validation process by:

- Increasing test coverage through increased number of variations, when dealing with system traffic.
- Being programmable to force the system's most critical traffic conditions.
- Being repeatable for failure analysis and failure regression tasks.
- Being comparable, to achieve measurable quality improvements.
- Producing log files to catch the problems before the system hangs.
- Creating test reports to document system quality.
- Making an easy link to R&D's debug environment.

Any access from an Agilent Exerciser is permutated using PPR, varying block sizes, memory commands, alignments, and byte-enables (meaning all variations of dword, word, and byte read/write accesses are used). Protocol variations on all system actions include waits/latency, terminations, 64 bit and 32 bit access, address/data stepping and as well as acceptance/non-acceptance of 64 bit access.

Automatic test setup

When starting the validation software on a system under test, it automatically scans the system for Agilent PCI/ PCI-X Exerciser and Analyzer cards. Based on the available test cards, the operator can select various tests, define the test duration and start the test.

Customer configurable tests

All tests are configurable by the customer. The GUI shows all parameters, and all setups are simply done with a mouse click.

Thus, using different Exercisers to test between different buses, e.g. 33 MHz PCI and Mode 2 PCI-X, is easy. With each test, you just select the path to test. The software automatically communicates with the test card plugged into the corresponding bus and tells you which protocol/traffic parameters you may vary.

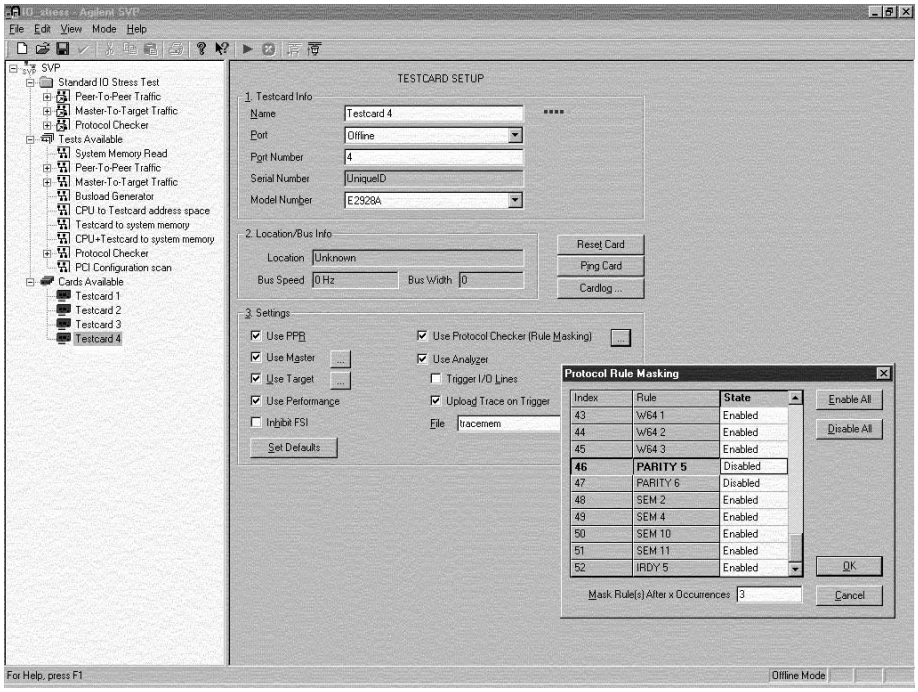


Figure 10. Test card setup

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Further Tests

The following list describes all tests available for the System Validation Package. All tests are customer configurable (see Table 2, page 13), and stress one data path. All tests can be performed concurrently to increase and maximize stress conditions. The PPR capabilities are customized for the different cards. For example, different protocol variations are available for PCI and PCI-X. Please refer to the corresponding technical data sheet of the Exerciser used for a list of available protocol variations.

CPU and Exerciser to system memory (W/R/C data[5])
Access system memory space via virtual memory from CPU and from PCI/PCI-X bus (Exerciser acting as master). The same address range with interleaved addresses is used in order to stress cache controller.

- **Tested data paths:** CPU to host memory; Exerciser to host bridge to system memory.
- **Tested devices:** Host bridge and host bridge configuration, host memory controller, and arbitration unit.

W/R/C to System Memory
Access the system memory from the PCI/PCI-X bus, and perform data write/data read/data compare.

- **Tested data paths:** Exerciser to host bridge to system memory
- **Tested devices:** Host bridge, host bridge configuration, host memory controller, and arbitration unit

Read from memory
This test reads repetitively from a customer-defined physical address to check accessibility and to stress the data path:

- **Tested data paths:** Exerciser to host bridge to system memory
- **Tested devices:** Host bridge, host bridge configuration, host memory controller, and arbitration unit.

Peer-To-Peer Traffic (W/R/C data)
Two PCI Exerciser cards access each other's memory or I/O space. Master-target traffic in both directions is set up. Two test cards on different buses are used to test the bridges and bridge configuration.

- **Tested data path:** Exerciser #1 to bridge(s) to Exerciser #2
- **Tested devices:** Bridges, bridge configuration, and arbitration units.

Master Target Traffic (W/R/C data)
Two PCI Exerciser cards access each other's memory or I/O space with unidirectional master-target traffic. Two test cards on different buses are used to test the bridges and bridge configuration.

- **Tested data path:** Exerciser #1 to bridge(s) to Exerciser #2
- **Tested devices:** Bridges, bridge configuration, arbitration units

CPU to test card (W/R/C data)
This test accesses either the test cards memory or I/O space via virtual memory from the CPU.

- **Tested data paths:** CPU to host bridge to test card
- **Tested devices:** Host bridge, host bridge configuration, host memory controller, and arbitration unit.

Bus Load Generation
An Exerciser is set up to generate self-traffic and therefore saturate a bus with a defined level of traffic. This kind of test stresses other devices on the same bus by limiting the available time a certain device can get access to the bus. Also the arbitration unit can be verified under controlled bus load conditions.

Error Analysis
The Analyzer of an E2920 Series test card can be set up to check for:

- Protocol violations
- Data transfer errors
- Parity errors
- Bus hang-ups/bus locks
- Bus load measurements.

Detected problems are logged in a report file. Optionally, a trace memory waveform file is generated for in-depth root cause analysis. All PCI/PCI-X devices on the bus are passively observed.

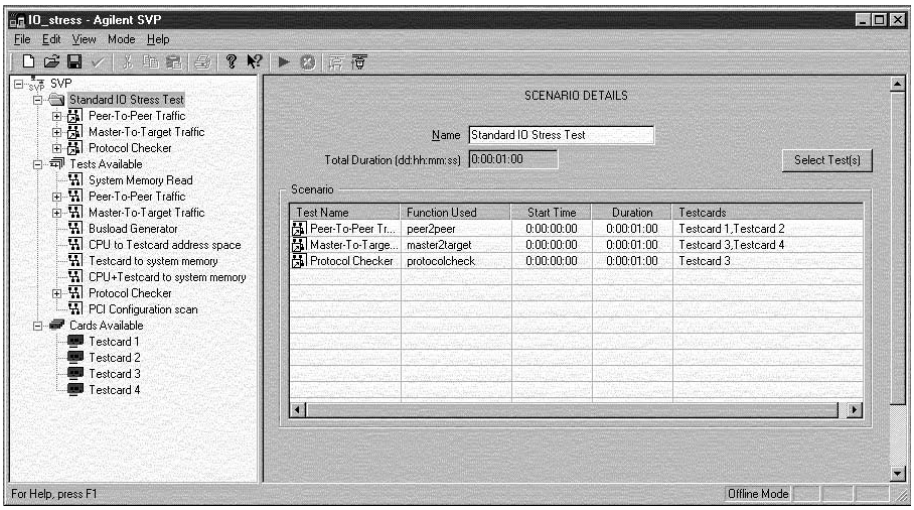


Figure 11. Test scenario setup window

[5] Write/Read/Compare data

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In-system Programmable

The Agilent System Validation can be installed and executed on the system-under-test itself. In this case, the Exerciser and Analyzer are programmed through the PCI or the PCI-X interface.

External Control

Alternatively, the whole test can also be controlled from an external host PC, which runs the System Validation Package. The Exerciser and Analyzer are connected via an appropriate external interface. To execute a test that requires the Front Side Interface (FSI, see Table 2), the FSI must be installed on the system under test.

Working with non-Windows OS

Two options are available to verify a system that does not use Windows.

Use an external controlling host PC

In this case, any test which does not require the FSI can be executed immediately. To use the other test, the FSI, which is only a small C-program, must be compiled for the appropriate OS. The FSI is delivered as executable for Windows DOS, and in source code.

Porting the System Test Library

The other alternative is to import the complete System Test Library to your preferred OS. Therefore, the System Test Library comes with source code.

Table 2. Customer Configurable Test Parameter

			Customer configurable test parameters						Usable mechanisms to detect errors			
	# of cards	FSI[2]	Band-width	PPR	Address Space	Address Prefetch	Address	Memory Size	Data Compare	Protocol Check	Protocol Error Mask	Capture Waveform on Error[3]
CPU and Test Card to System memory	1	yes	1..100%	√	Memory	n/a	by OS	0..512KB/ 0..1MB[1]	√	√	√	√
Peer to Peer Test	2	no	1..100%	√	Memory or I/O	true or false	by BIOS/ OS	0..512KB/ 0..1MB[1]	√	√	√	√
Master/Target Traffic	2	no	1..100%	√	Memory or I/O	true or false	by BIOS/ OS	0..512KB/ 0..1MB[1]	√	√	√	√
CPU to Test Card	≥1	yes	1..100%	√	Memory or I/O	true or false	by BIOS/ OS	0..512KB/ 0..1MB[1]	√	√	√	√
Write/Read/ Compare to System Memory	≥1	yes	1..100%	√	Memory	n/a	by OS	Dword value 0..4Kbyte	√	√	√	√
Read From System Memory	≥1	yes	1..100%	√	Memory	n/a	Address Value	Dword value 0..4Gbyte	√	√	√	√
Bus Load Generation (self traffic)	≥1	no	1..100%	√	Memory or I/O	n/a	by BIOS/ OS	0..512KB/ 0..1MB[1]	—	√	√	√

1. The memory can be specified for the selected Exerciser. 512KB data memory is available on E2925B, E2928A, and E2940A. 1MB data memory is available on E2929B and E2930B
2. The FSI (Front Side Interface) is a small executable table which must run on the system under test CPU(s).
3. Requires option 100 for the E2930B.

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Required E2920 Series Exerciser/Analyzer
The System Validation Package requires a full Exerciser/ Analyzer (see Table 3).

Ordering Information

The System Validation Package can be ordered as option #310 of the E2925B, E2940A, E2928A, E2929B and E2930B
The system test is also available as a system test library to be integrated in customer proprietary test frames. Refer to System Test Library technical specifications (5968-3500E) for more information.

Table 3. Minimal Exerciser/Analyzer Configuration Needed for Option #310/System Test Library

	Option #310	System Test Library
E2929B/E2930B PCI-X Protocol Checker	•	•
#300 (Exerciser)	•	•
#320 (C-API)		•
E2925B/E2940A/E2928A PCI	•	•
#300 (Exerciser)	•	•
#320 (C-API)		•
E2922B PCI-X Master Target Test Cards		• [1, 2]

1. For error detection, the E2922B supports PCI-X protocol and data compare only. Other analyzing capabilities like waveform capture, trigger I/O, or bus load measures require the E2929B or E2930B.
2. The E2922B does not support external interfaces and must be in-system programmed through PCI-X.

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C-API/PPR (Option #320)

The optional C-Application Programming Interface (C-API) provides a programming interface for setting up and controlling the exerciser and analyzer. Option #320 comes with a library of C functions to facilitate control of the exerciser and analyzer. Option #320 also comes with a PCI Protocol Permutation and Randomizing library.

The test program can run on the system-under-test itself or on an external controller. If the program runs on an external host, the Agilent E2930B connects via USB 2.0. If the test program runs on the system-under-test, the interface itself is used.

The library functions are divided into groups, which allow you to set up and control the various capabilities of the Agilent E2930B.

Recommended development environment: MS Visual C++ V. 6.0 or higher. Additional Tcl programming is possible.

Agilent Patented Protocol Permutation and Randomization (PPR) technology

The PPR library extends the C-API by offering dedicated functions to setup protocol permutation in a pseudo random sequence. It allows easy to set up transfers of contiguous blocks of data with as many protocol variations as possible. Therefore, the PPR software calculates which variations are covered, and after how many data transfers, by permutating the possible protocol variations. It determines whether the coverage, within programmed constraints, can be achieved under given test circumstances, and calculates the test time required to perform the data transfers.

Generating permutations

The user-defined protocol constraints can be easily set by specifying lists of protocol variations, which must occur. For example, which different burst lengths, wait cycles, memory read/write commands, etc. Then, PPR automatically moves sequentially through the lists. With each step, that is, with each permutation, the next value in this list is combined with the next values in the other lists. The hardware based permutation proceeds in this way until each value of each list is combined with all values of the other list, and thus all combinations are covered. In this way, the repetition or omission of combinations is avoided.

Documented test coverage

A printable report tells you which protocol variation the device has exposed. It explicitly reports which protocol attributes are permutated against which other protocol attributes, and after how many data transfers.

Optimized test time

The values to be varied can be specified for each master and target attribute separately. Thus, focusing on interesting cases can optimize testing time.

By carrying out these protocol permutations in real-time within the exerciser hardware, these tests run much more quickly than any other CPU-based test program.

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Effective test generation
The exhaustive C-library makes it simple to focus on test structuring, partitioning and the specification of protocol constraints. This means that an appropriate and valuable test for protocol verification with meaningful results can quickly be obtained. Once started, the test can easily be extended to incorporate newly gained experiences or to address testing needs for newly invented PCI-X 2.0 features.

Deterministic test conditions
In contrast to PCI-X 2.0 traffic generated by other PCI-X 2.0 cards, the generated variations are completely deterministic and reproducible.

Supported protocol variations
The exerciser and analyzer allow the variation constraints for the transfer, requester and completer behavior to be specified. All specified constraints can be permutated against each other and up to 100 constraints can be maintained per list.

Transfer variations
The generator features the following algorithms:
- Start address alignment; a list of arbitrary address alignments to start transfers at given offsets (e.g. 1 dword) relative to the qword boundaries
- Byte enables; a list of selected values for the C/BE lines during the address phase
- Block size; a block describes a contiguous range in memory available to be transferred. A list of up to 100 different block sizes (from 1 to 4096 byte) can be selected to be transferred
- Bus commands; a list of selected bus commands. All selected commands are permutated with other selected constraints, as appropriate, for the specified transfer direction and specifications
- Permutation of release ordering bit
- Permutation of no snoop bit.

Target behavior variations
The requester initiator allows for the variation of:
- byte count (1 to 4096)
- disconnect/initiator termination
- delay
- address stepping
- REQ64
- release REQ

The completer initiator allows for the variation of:
- Error message, yes/no
- partitioning
- delay
- address stepping
- REQ64
- release REQ.

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General Specifications

Specifications:
bus: 32/64 bit
Addressing: 32/64 bit

PCI Clock range:

PCI:	0-33 MHz
PCI-X1.0:	0-33 MHz
	50-100 MHz
	100-133 MHz
PCI-X 2.0:	50-100 MHz
	100-133 MHz

Timing:
The E2930B fully meets electrical and timing specifications for PCI-X Mode 2.

Electrical Specifications:
Automatically switches between mode 1 for a 3.3V environment and mode 2 for a 1.5V according to electrical sprecifications.

Power requirements: consumes less than 25 W from PCI-X slot.

Trace length limits: meets PCI-X specifications.

Signal loading: less than 10 pF, fully PCI-X compliant.

Operating temperature:
0°C to +45°C.

Mechanical dimensions:
short card, occupying one slot.

System Requirements:
Software supports Microsoft Windows 2000, 98 and XP.

Ordering Information

E2930B base product
Includes:
- PCI-X State Analyzer 4M samples
- Analyzer Graphical User Interface for Windows
- 4M trace memory
- 4MB/s fast parallel interface
- 32/64 bit, 133 MHz DDR PCI-X Mode 2 protocol checker
- USB 2.0
- Protocol Checker Graphical User Interface for Windows
- CLI interface
- Tcl interface
- Software media CD

Option #300, PCI-X Exerciser
Includes:
- Customer installable single card license
- Enables on-board 32/64 bit, 0..266 MHz Exerciser hardware
- Exerciser Graphical User Interface for Windows
- Software media CD

Option #310, System Validation Package
(Option #300 and option #320 recommended)
Includes:
- Single card license
- Graphical User Interface for Windows . The PCI-X Exerciser (option #300) must be installed
- Software media CD

Option #320, C-API / PPR Library
(Option #300 required)
- customer installable single card license
- enables PPR hardware and C-API interface for one test card
- the PCI-X exerciser option #300 must be installed
- drivers for Windows

When ordering without base product, S/N of the existing E2930B must be notified on purchase order.

Accessories

External Power Supply E2991A
The External Power Supply supports applications where the Exerciser and Analyzer card should be transparent to the system, you can connect this external power supply to prevent the card from drawing power from its slot.

Fast Host Interface Card
Available as Option #400

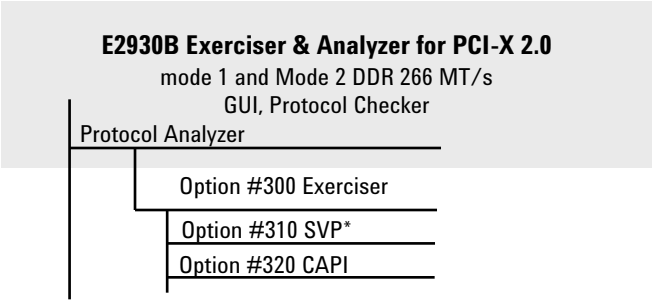


Figure 12. Recommended configuration

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Overview PCI/PCI-X E2920 Series

	PCI Analyzer -protocol checker -64K state PCI logic analyzer -4MB fast host interface- timing checker -real-time performance measures- GUI - RS 232 interface	**E2940A** compact PCI 32/ 64 bit 66MHz	**E2925B** PCI 32 bit 33 MHz	**E2928A** PCI 32/64 bit 66 MHz	**E2929B** PCI-X 32/64 bit 133 MHz -protocol checker -RS-232/USB interface - GUI	**E2930B** 32/64 bit 266 MT/s (DDR) -protocol checker -USB 2.0 - GUI -state PCI logoc analyzer -4MB fast host interface - real time performance measures -GUI
Opt100	N/A	N/A	N/A	N/A	**PCI-X Analyzer** - 2M state PCI logic analyzer - 4MB fast host interface - real-time- performance measures -GUI	N/A
Opt.200	**PCI Performance Optimizer**	4M trace memory recommended please order separately		32/64 bit 66 MHz	**PCI-X Performance Optimizer** -post processed and real-time performance analyzer- performance report -GUI	
Opt.300	**PCI Exerciser** - master and taget-GUI - CLI -512 KB on-board memory	32/64 bit 33 MHz	32 bit 33 MHz	32/64 bit 66 MHz	PCI-X Exerciser - master - target - GUI- 1MB onboard data memory	Exerciser for PCI-X 2.0 - master- target- GUI- 1MB onboard data memory
Opt.320	**System validation package**	- peer-to-peer -system memory test - systemload test - protocol load test - protocol check - GUI				
Opt.320	**C-API/PPR**	- C-programming interface library- protocol permutation and randomization library				

PCI-PCI-X Bundle

· With the E2997A Agilent also offers a great price on the purchase of the E2928A PCI Card and the E2929B PCI-X card.

Accessories Agilent products	**E2940A**	**E2925B**	**E2928A**	**E2929B**	**E2930B**
E2991A External power supply		-	-	-	-
E2993A External Agilent Logic Analyzer Adapter		-	-		
E2994A External general purpose logic Analyzer Adapter		-	-		
E2995A 155 x 4M		-	-		
E2996A 155 x 4M trace memory	-	-			

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Related Agilent Literature	**Publication Number**
· Agilent E2925B 32bit, 33 MHz, PCI Exerciser & Analyzer, technical specifications	5968-3501E
· Agilent E2928A 32/64bit, 66 MHz, PCI Exerciser & Analyzer, technical specifications	5968-3506E
· Agilent E2940A CompactPCI Exerciser & Analyzer, technical specifications,	5968-1915E
· Agilent E2922B PCI-X Master Target Card, technical overview	5968-9577E
· Agilent E2929B PCI Exerciser & Analyzer, technical specifications	5968-8984E
· Agilent System Validation Pack, Agilent System Test Library, technical overview	5968-3500E
· Agilent Technologies E2920, PCI series, PCI and PCI-X Design Verification, brochure	5968-9694E
· Intel discusses basic concepts of PCI performance and efficient use of PCI with the Agilent E2920 series, case study,	5988-0448ENDE
· Agilent NSD stabilizes server designs quickly and completely with the Agilent E2920 PCI Series, case study	5968-6948E
· Agilent HSTC speeds high-end server testing and reduces engineering costs with the Agilent E2920 PCI Series, case study,	5968-6949E
· Agilent E2920 Verification Tools, PCI Series gives Altera Corporation competitive Advantage, case study,	5968-4191E

You can find the current literature and software at:
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