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Serial Cell Generator and Analyzer HP E4859A

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Technical Data

Product Specifications and Characteristics

Characterization of TDMA and other burst-mode transmitters and receivers during research and development.

The HP E4859A serial cell generator and analyzer system is used in research and development to characterize the transmission performance of time division multiple access (TDMA) and other burst-mode transmitters and receivers used in communication system for local access, LAN, or military networks.

By measuring the error-performance of all types of burst-mode data under different line bit rates, cell timing, or cell length conditions, the cost and performance of the transmission system can be optimized.

Multiple serial cell generators can be set up to reproduce upstream data for a TDMA network, as shown in Figure 1. Variable cell lengths, cell content and cell timing allow the margins of the physical layer design, even for proprietary transmission formats, to be found. No other digital generators are needed to stimulate the devices, because the serial cell generator also produces control signals. The serial cell generator and analyzer system is easy to operate because it automatically compensates for the cell transfer delays of the test set-up. BER measurements can be automated and other test equipment connected via HP-IB.

Key features:

- bit-error-rate measurement of all types of burst-mode data
- up to 16 serial cell generators
- cells with up to 28 segments of mixed PRBS / user-defined pattern
- variable cell length and cell timing
- bit rate 170 kbit/s to 250 Mbit/s (opt. 660 Mbit/s)
- auto-adjust cell transfer delay

Features now available:

- clock input for analyzer with cell detect mode or bursted analyzer dock
- programming interface
- flexible control signals
- single-shot bursts
- continuous PRBS generation and BER measurement

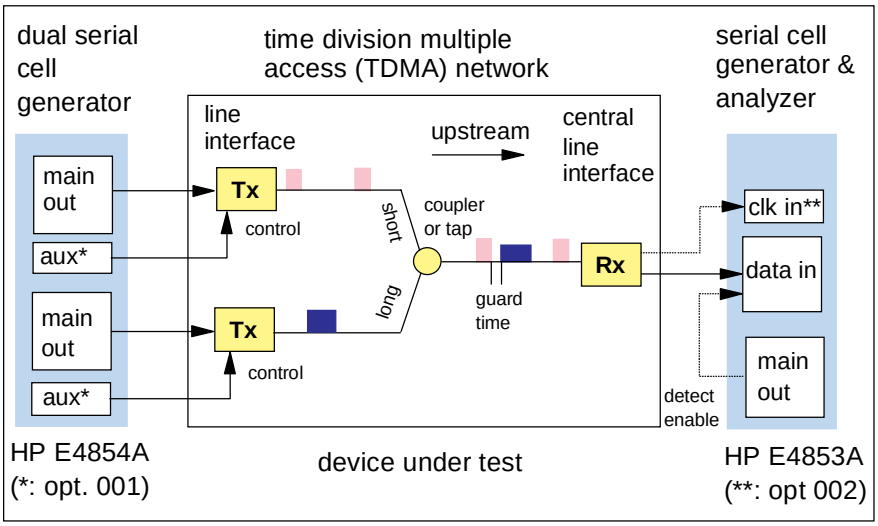


Figure 1: Test set-up for characterizing TDMA devices

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System description

HP E4859A serial cell generator and analyzer entry system

The HP E4859A is an entry level system, that comprises one burst-mode serial cell generator, a companion serial cell analyzer, a central clock source and nine free slots. Modules can be added for configurations requiring multiple generators or analyzers. The monitor, keyboard, and mouse are not included.

The HP E4859A serial cell generator and analyzer entry system is shown in Figure 2. The system comes factory installed with a 13-slot C-size VXI mainframe, embedded controller and disk, HP E4853A and E4805A modules, operating system, the user software and a TDMA license (See page 7 for details).

HP E4872A user software

The user software is required to operate the HP E4805A, E4853A, and E4854A modules. It provides a windows-based, color graphical user interface and a programming interface.

Save / recall: cells and complete settings can be saved and recalled
On-line help: provides context-sensitive help text
Configuration: multiple generators and analyzers can be controlled from the same user interface
Selftest: module and system selftests can be invoked
Software licenses: one node-locked on-line license and one off-line license is included (for operation via LAN connection)

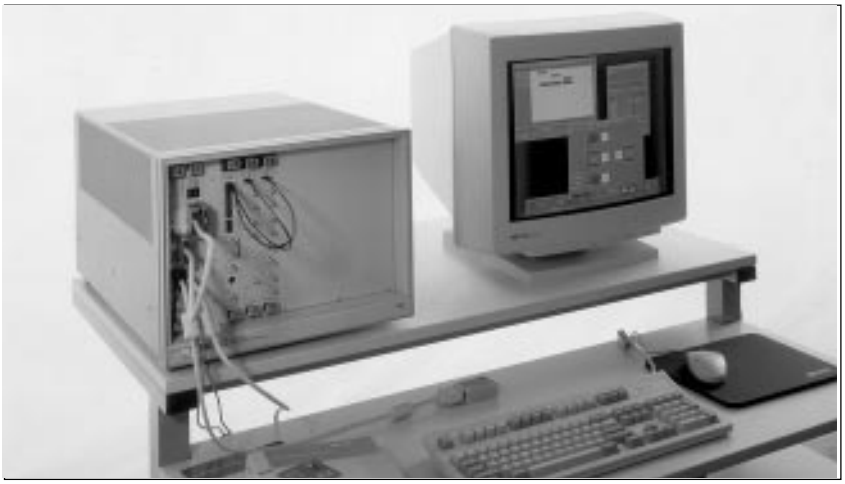


Figure 2: HP E4859A entry system with HP E4854A dual serial cell generator module and peripherals.

Programming interface: automated measurements can be made using a HP VEE, ANSI/C, or C++ program running on the embedded controller. Other test equipment can be connected and controlled via HP-IB.

HP E4856A TDMA license

For testing the BER of receivers and transmitters used in a TDMA network, specific features are provided. These are a connection window for a point-to-multipoint network, up / downstream burst-mode cell sequences for TDMA / TCM time slots, auto-adjust of generators and analyzers, compensation for cell transfer delays, and cell detect-mode for operation with an external analyzer clock. The TDMA license is included in the HP E4859A entry system.

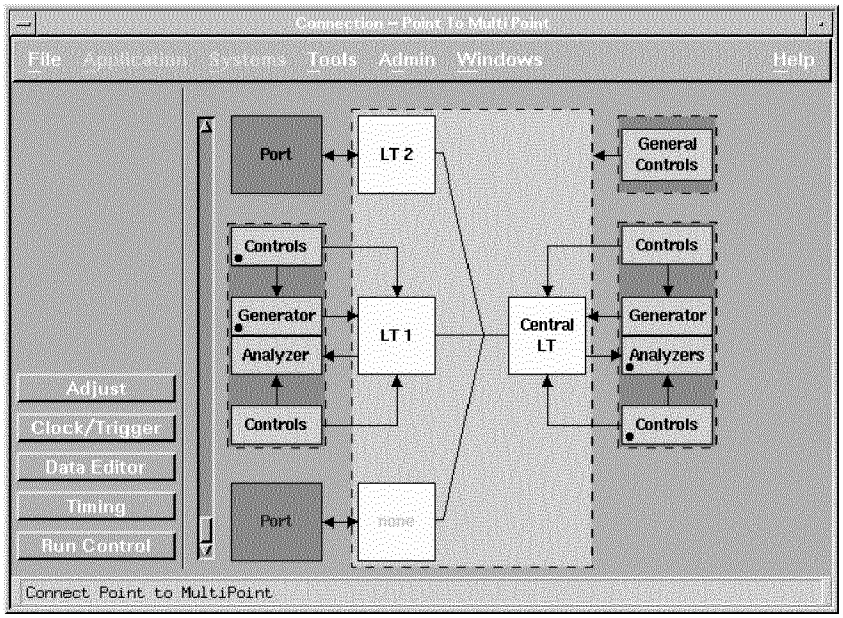


Figure 3: Connection window of the graphical user interface

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Module specifications

HP E4853A serial cell generator and analyzer and HP E4854A dual serial cell generator

The HP E4853A module provides one serial cell generator and one serial cell analyzer. The HP E4854A module provides two serial cell generators. Multiple generators and analyzers can be set-up.

DUT	Ports	Signal Type	← 1 frame →	HP E4853/4A outputs
Tx	Generator	Cell generator #1		Main
		Cell generator #2		Main
		Envelope #1		Main, Aux *)
		Bursted clock #1		Main, Aux *)
		Cont. clock		Main, Aux *)
		Reset pulse #2		Main, Aux *)
		Control cell #1		Main, Aux *)
Rx	Analyzer	Cells #1,#2		n/a
		Envelope #1,#2		Main
		Bursted clock #1,#2		Main
		Cont. clock		Main
		Reset pulse #1,#2		Main
any	General Controls	Control cell		Main, Aux *)

*) see descriptions on page 4

Figure 5: These signal types can be generated by one main output

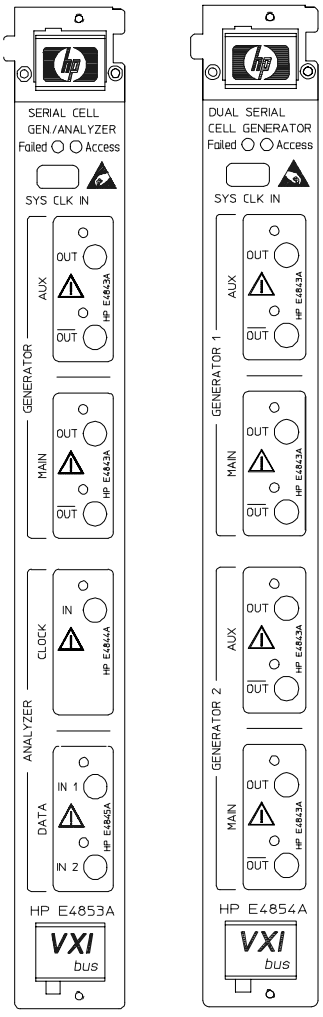


Figure 4: HP E4853A (left) and HP E4854A (right) shown with option 001 auxiliary outputs and option 002 clock input

Serial cell generator

Patterns and signals of the outputs

Each output can be used to provide one of the signal types shown in Figure 5.

Frame

The frame length is constant and all signals are repeated in each frame.
The frame can be repeated periodically or just once.
Frame repeat mode: repetitive and single. This allows:

- burst mode cells, repetitive
- burst mode cells, single-shot
- continuous mode PRBS

Cells

Each output only generates one cell. The cell is repeated n times per frame, n = 1 to 32.
(See Figure 5).
Cell structure: a cell consists of 1 to 28 segments of algorithmic and / or memory-based pattern.
(See Figure 6).
Cell sequence: supports TDMA (time division multiple access) time slots, and TCM (time compression multiplex) time slots for emulating data transmission in a point-to-multipoint network.
Pattern format: NRZ
Algorithmic pattern:

- **PRBS:** 2^n-1, n= 7, 9, 10, 11, 15, 17, 20, 21, 23, 31. (CCITT 0.151). Normal or inverted.
  Memory based pattern: 64 Kbit to 1024 Kbit memory per channel, dependent on bit rate; see Table 1, on the following page. Memory can be divided into segments of:
- user-defined pattern
- PRBS with zero / one substitution
- PRBS with error insertion
- PRBS with var. mark density
  Segment length: 1 bit to 64 Kbit, 1 to 16 bits resolution dependent on maximum bit rate; see Table 1. If the first or last segment in a cell is a user-defined pattern, this segment length has 1 bit resolution, independent of the bit rate.

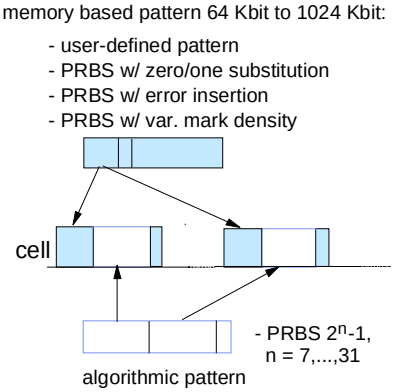


Figure 6: A cell consists of segments of memory-based pattern and algorithmic pattern

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Infinite segment length: PRBS segments can have an infinite length
Cell length: sum of segments

Control signals
These are used to stimulate the DUT (transmitter or receiver) or to trigger other test equipment. Multiple control signals can be set-up. The timing of the control signals is linked to cells generated, cells expected by the analyzer, or to the start of the frame. When control signals are linked to an analyzer, the cell transfer delays are taken into account.

Envelope
This generates a gating signal while the cell is active (e.g. can be used as laser on / off). The envelope pulse starts and stops 0 to ±24 ms before and after the cell which it is linked to (for AUX outputs 0 to +24 ms). The envelope pulse length can be varied with 1 bit resolution.

Reset pulse
This generates 1 pulse for each cell (can be used as reset-signal for the receiver).
Pulse format: NRZ
Reset-pulse position to cells: 0 to ±24 ms before / after cells, 1 bit resolution, ±100 ps bit typ. accuracy.

Bursted clock
The bursted clock starts and stops 0 to ± 24 bits before and after the cell which it is linked to (for AUX outputs 0 to +24 ms). The bursted clock length can be varied with 1 bit resolution.
Format: RZ, 50% duty cycle typical

Continuous clock
Format: RZ, 50 % duty cycle typ.
Clock / data delay: ± ½ clock period

Control cell
Format: NRZ
Position: starts 0 to ±24 ms before / after the cell which it is linked to or to start of frame. The resolution is 1 bit**.** For AUX outputs the control cell starts 0 to ±3 us before / after the associated MAIN output and the cell must have the same cell structure as the associated MAIN output.

HP E4853 / 4A option 001 auxiliary outputs

This option provides one auxiliary output for each main output.

AUX output
This is an auxiliary output which provides control signals, as shown in Figure 5, which are automatically linked to the cells of the main output of the same generator. If the MAIN output is used as an envelope, bursted clock, continuous clock, or reset pulse, the auxiliary output is disabled.

Timing parameters for MAIN and AUX outputs
These are measured with ECL-levels terminated with 50 Ω to GND.

Bit rate: 170 kbit/s to 250 Mbit/s, optional 660 Mbit/s for main outputs, auxiliary outputs are disabled >250 Mbit/s.

maximum bitrate	memory based pattern	algorithmic pattern	resolution of segment, frame
41.67 Mbit/s	64 Kbit	1 Mbit	1 bit
83.33 Mbit/s	128 Kbit	2 Mbit	2 bit
166.67 Mbit/s	256 Kbit	4 Mbit	4 bit
250 Mbit/s	512 Kbit	8 Mbit	8 bit
333.33 Mbit/s *	512 Kbit	8 Mbit	8 bit
660 Mbit/s *	1024 Kbit	16 Mbit	16 bit

* only with option 660

Table 1: Bit rate versus memory

Frame length: max. 24 ms, 1 to 16 bit resolution. Minimum frame length is cell length +0 to 30 bits (twice the frame length resolution - 2 bit). See Table 1.
Guard time between cells: 0 to framelength (max. 24 ms). Negative values are allowed. Transfer delay values are taken into account.
Guardtime resolution: 10 ps for cells coming from different generators.
Cell transfer delay: is the propagation delay through the device under test between the generator and analyzer. It can be entered manually or by auto-adjust.
Cell transfer delay ranges: for manual entry: < 24 ms, 10 ps resolution. For auto-adjust: <1.50 ms, 1/8 clock period resolution.
Delay range between main outputs: 0 to framelength (max. 24 ms), 10 ps resolution.
Data-jitter: <10 ps rms typical
Skew between outputs: ± 100 ps typical

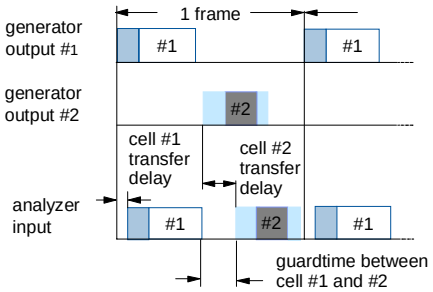


Figure 7: Timing relations between generators and analyzers

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Level parameters for MAIN and AUX outputs

Source impedance: 50 Ω
Output voltage: TTL, ECL (50 Ω to GND / to -2 V) , PECL (50 Ω to +3V). -2.00 to +3.00 V into 50 Ω terminated to GND. Can be varied real-time.
Voltage level accuracy: ±200 mV typical
Output amplitude: 0.30 to 2.50 V, 10 mV resolution
Termination voltage: -2.0 V to +3.0 V
Short circuit current: 120 mA maximum
Enable: each output is switched on / off individually by a relais
Normal / complement: differential outputs. Disable unused outputs for optimum pulse performance.
Connector: SMA (f) 3.5 mm.
Maximum external voltage: -2 V to +3 V
Transition times: 500 ps typical (between 10 % and 90 % of amplitude).
350 ps typical (20 % - 80 %)
Pulse performance: <5 % typical overshoot / preshoot / ringing. @ TLL levels <15 % droop typical**.**

Serial cell analyzer

Measurements: an analyzer measures all cells coming from one generator only:

- bit error ratio (BER) and error count of errored ones / zeroes / all
- number of received bits
- detect loss ratio for detect mode (ratio of non-detected cells to total number of transmitted cells)

Selectable segments: individual segments of a cell are measured. Others are ignored.

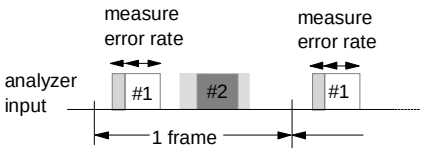


Figure 8: Individual cell segments can be measured, i.e. only payload

Multiple analyzers: simultaneous measurements of cells coming from different generators.
Max. measureable BER: 1 for synchronization modes 1 and 4
Reset measurement: resets error counter to 0
Measurement interval: 1 s to 100 days
Measurement modes: manual, single interval, repetitive intervals
Synchronization modes: the synchronization between the generator and analyzer can be achieved by using the:

1. system clock with constant cell transfer delays
2. external analyzer clock with cell detect-mode (only with option 002)
3. pure PRBS synchronization using an external analyzer clock (only with option 002)
4. bursted external analyzer clock (only with option 002)

Auto-adjust: automatically measures the cell transfer delay of a test-cell between each generator and each analyzer. It finds the start of the cell and sets the sampling point to typically 50 % of the eye-opening. The sampling point resolution is 1/8 bit period. A BER of up to 10^{-3} is tolerated during auto-adjust. During the auto-adjust procedure, a constant cell transfer delay is required and it cannot be done with an external analyzer clock.

HP E4853A option 002 clock input for analyzer

This provides a clock input for the serial cell analyzer to sample the recovered data bits with a clock provided by the device under test. For a BER measurement of the selected cell segments, each analyzed data bit requires a matching clock edge.

Timing parameters for CLOCK and DATA IN 1 / 2 inputs

Input frequency: 170 kHz to 250 MHz, with option 660: 660 MHz, 330 MHz when DATA IN1 is used (detect-mode). In detect-mode the clock period must be at least 20 ns @ frequency ≤ 41.67 MHz, and 10 ns, 5 ns, 2.5 ns @ ≤ 83.33 MHz, 166.67 MHz, 250 MHz respectively.
Analyzer clock: data is sampled with 1 sampling point per bit.

- system clock: used for all serial cell generators and analyzers.
- external analyzer clock: recovered clock from the DUT is used to sample data bits.

Input jitter / wander: eye-opening of data bits ≥50 % of bit period and >1 ns is required. With an external analyzer clock, an eye-opening >400 ps is required. Input frequency wander exceeding above requirements is not tolerated.
Clock / data delay: the phase of the internal sampling clock can be delayed while the measurement is running.

- with system clock: ±1 bit period, 1‰ resolution
- with external analyzer clock: between +5 ns and 8 ns after the rising of falling edge of the external analyzer clock. 10 ps resolution (See Figure 9.)

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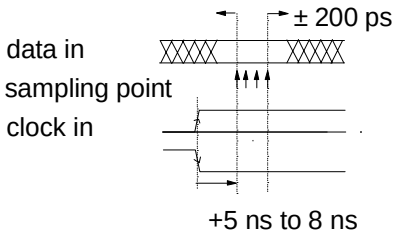


Figure 9: Relationship between clock, data, and internal sampling point.

Cell detect mode: the serial cell analyzer detects the start of each cell by using a detect word (or "unique word") in each cell transmitted. See Figure 10. The selected cell segments for BER measurement are compared only when the detect word has been properly detected. In cell detect mode, the external clock may be unstable before and after the measured cell segments. In burst-mode, the clock's phase is typically recovered and therefore unstable at the beginning of each burst (preamble). The detect enable signal is required to determine the time window where the start of the detect word is expected. This assures proper synchronization, even when PRBS segments are used, where the same pattern as the detect word occurs.

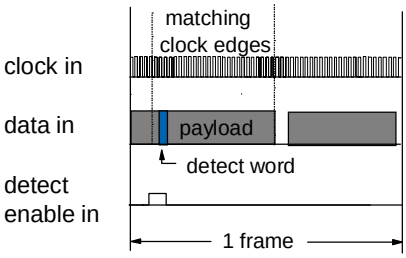


Figure 10: Input signals in cell detect mode

Detect word length: segment of 1 to 40 bits length
Detect enable signal: DATA IN 1; either gating or triggering. It can be provided by the DUT or a MAIN output of a serial cell generator.

Level parameters for CLOCK / DATA IN 1 / 2 inputs:

Input impedance: 50 Ω
Input threshold: -2.10 V to +5.10 V, 5 mV resolution, ±50 mV typical accuracy. Can be varied real-time.
Termination voltage: -2.10 V to +3.10 V
Input sensitivity: 200 mV @ frequencies >500 MHz: 300 mV
Normal / inverted: selectable
Enable: each input can be individually switched on and off. High impedance input will occur when disabled.
Connector: SMA (f) 3.5 mm
Maximum input voltage: -3 V to +6 V

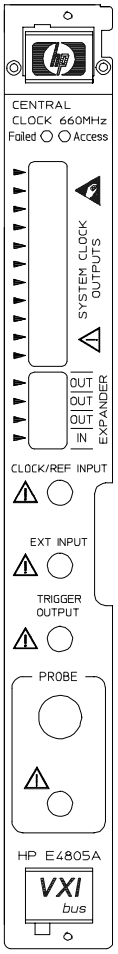


Figure 11: HP E4805A

HP E4805A central clock with option 001 high frequency resolution

This module synchronizes all other modules and generates a synthesized system clock.

System clock
Frequency range: 170 kHz to 660 MHz
Frequency resolution: 4 digits, 1 Hz with option 001
Frequency accuracy: ±50 ppm for internal PLL reference
Period jitter: < 10 ps rms typical for internal PLL reference
PLL reference: internal crystal, VXI-bus 10 MHz, or external 1, 2, 5, or 10 MHz
Clock / ref input
this input can be used as PLL reference or external bit rate for the system clock.
Input impedance: 50 Ω
Input sensitivity: 400 mV
Termination voltage: -2.10 V to +3.10 V
Input transitions: <20 ns
Input frequency: 170 kHz to 660 MHz
Required duty-cycle: 40...60 %
Connector: SMA (f) 3.5 mm
Maximum input voltage: -3 V to +6V
Trigger output
This is used to trigger other test equipment or an oscilloscope.
Trigger events: start before or after a selected cell or clock
Level: TTL (frequency <180 MHz), 1V/ GND, ECL (50 Ω to GND/ -2V), PECL (50 Ω to +3 V)
Output impedance: 50 Ω
Connector: SMA (f) 3.5 mm
Maximum external voltage: -2 V to +3V
External input: This input is not used
Probe: These connections are not used

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General system characteristics for the HP E4859A

HP E4859A entry system	
Entry system includes: (the entry systems are bundled products which come factory pre-installed. Monitor, keyboard, and mouse are not included)	HP E4805A#001, E4853A, E4872A user s/w, E4856A TDMA license, E1401B 13-slot VXI-C frame, E1497A#ANC embedded V743 controller, E4208B embedded disk, LAN transceiver, operating system HP-UX 9.0x, SICL, licenses, and documentation.
Number of free slots	9
Operating temperature	10 °C to 40 °C
Storage temperature	-20 °C to + 60 °C
Humidity	80 % rel. humidity @ 40 °C
Power requirements	100-240 Vac, ±10 %, 50-60 Hz; 100-120 Vac, ±10 %, 400 Hz
Electromagnetic compatibility	EN 55011/CISPR 11, Group 1, Class A +10 dB
Acoustic noise	48(56) dBA sound pressure at low (high) fan speed
Safety	IEC 348, UL1244, CSA 22.2 #231
Power consumption	see HP E1401B
Physical dimensions	W: 426 mm (16.8 ") H:310 mm (12.2 ") D:602 mm (23.7 ")
Weight net shipping	29 kg (63.9 lb) 50 kg (110.2 lb)
Battery	see HP E1497A (Lithium Matsushita Electr. BR-2325)
Interfaces	LAN AUI, dual RS-232, SCSI-2 for external drives, HP-IB, Trigger in/out, Mini-DIN connectors for keyboard and mouse, 1024x768 graphics output
Preset logical VXI address	HP E4208B: 16; HP E1497A: 0
Removeable media	3.5-inch floppy disk, and 21 MB floptical disk

Table 2: System characteristics

General module characteristics for the HP E4805A, HP E4853A, HP E4854A

	HP E4805A central clock	**HP E4853A serial cell generator & analyzer**	**HP E4854A dual serial cell generator**
Size	VXI-C-size, 1 slot	VXI-C-size, 1 slot	VXI-C-size, 1 slot
Module type	register-based	register-based	register-based
Weight net	1.1 kg (2.4 lb)	1.7 kg (3.7 lb)	1.7 kg (3.7 lb)
Module ID (hex)	0247	0245	0245
Current drawn from VXI bus +24 V +12 V +5 V -2 V -5.2 V -12 V Power dissipation Watts/slot	 0.1A 0.2 A 3.2 A 1.2 A 3 A 1.2 A 40.2 W	 0 A 0.5 A 4.0 A 0.8 A 2.4 A 0.4 A 44.4 W	 0 A 0.6 A 3.7 A 0.8 A 2.4 A 0.4 A 44.6 W

Table 3: Module characteristics

General Characteristics

Warranty: 3 years.
Recalibration period: 3 years recommended
ISO 9001: modules are produced according to ISO 9001 quality system.

Note: These specifications describe the instruments' warranted performance. Non-warranted values are described as typical. All specifications apply after a 30 minute warm-up phase with outputs and inputs terminated with 50 Ω to GND. They are valid from 10ºC to 40ºC ambient temperature.

This document relates to user software revision A.01.04.00. Features can be added with future user software revisions.

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Complementary literature:
Product Overview
Pub. No. 5963-9985E
Configuration Guide
Pub. No. 5964-0004E

Other recommended test equipment and tools

- Lightwave communications analyzer HP 83475A
- Digital communications analyzer HP 83480A
- Optical attenuator HP 8156A
- Lightwave multimeter HP 8153A
- HP VEE Visual Engineering Environment HP E2111D

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