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Parallel Cell / Traffic Generator and Analyzer

HP E4829B, HP E4821A

Technical Data



Figure 1: HP E4829B entry system

The HP E4829B parallel cell / traffic generator and analyzer system is made up of several hardware and software modules. A combination of single hardware and software modules are joined together to create an application-specific solution. The following technical data sheet outlines the specifications for the parallel cell / traffic generator and analyzer system, which consists of:

- HP E4821A
- HP E4822A
- HP E4823A
- HP E4824A
- HP E4871A
- HP E4885A
- HP E4886A
- HP E4889A

Generator and analyzer hardware module HP E4821A
The HP E4821A is a C-size VXI hardware module, which includes one complete TX and RX 8/16 bit port. PODs must be added so that they physically interface with the implementation under test (IUT). Modules can be combined to test multiple 8/16 bit ports.

Graphical user interface HP E4871A
The HP E4871A graphical user interface controls the parallel cell / traffic generator and analyzer system from an HP-UX series 700 embedded workstation.

UTOPIA Level 1 / customer interface solution
Two HP E4889A active stimulus / response PODs, together with the software licenses HP E4822A/E4823A, form a solution for 8/16 bit UTOPIA Level 1 / customer interfaces. The PODs are plugged in between the HP E4821A and the IUT.

Product Specifications and Characteristics

UTOPIA Level 2 (MultiPHY) interface solution
An HP E4885A TX POD, an HP E4886A RX POD and an HP E4824A software license together form a solution for the 8/16 bit UTOPIA Level 2 (MultiPHY) interfaces. The PODs interface between the IUT and the HP E4821A.

Cell generation

General
The system allows cells with a word length of 16..128 to be generated (see figure 2). Cells are set up by combining individual segments. A cell structure of up to ten segments can be built and a maximum of sixteen different cell structures can be defined.

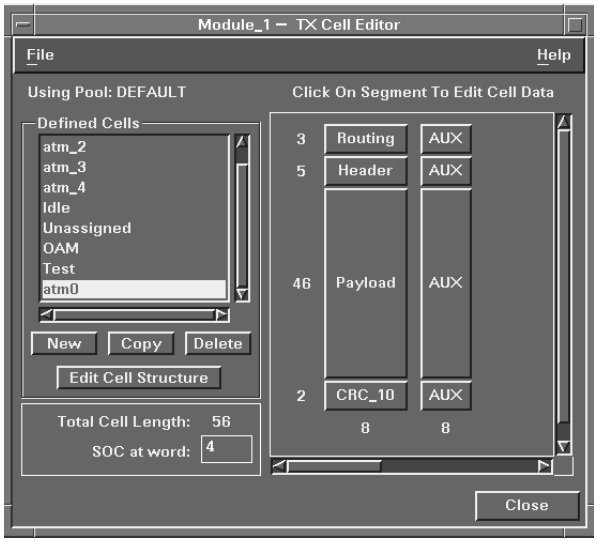


Figure 2: Cell editor, showing enhanced ATM cell with 56 byte

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A segment may consist of memory-based data and/or real-time generated data.

All segments, with the exception of the AUX segment, are valid on the data pins D0..D7/D0..D15. The AUX segment is valid on the auxiliary pins AUX0..AUX7.

The following list shows the available segments and their usage of data memory or algorithmic generators.

Memory segment
- variable length, 1..64 words,
- memory-based data,
- max. ten segments / cell.

PRBS segment
- variable length, 1..64 words,
- PRBS polynomial selectable:
  - 2^9-1 (ITU-T O.153)
  - 2^{15}-1 (ITU-T O.151)
  - 2^{23}-1 (ITU-T O.151),
- max. ten segments / cell.

UNI/NNI ATM-header segments
- fixed 5 bytes / 3 words length,
- memory-based VPI, VCI, GFC, PT, CLP and UDF2 field,
- UDF / HEC data are either memory-based or generated by the HEC generator,
- max. one segment / cell.

CRC-10 segment
- fixed 2 bytes length,
- bit 7..2 of byte 1 is memory-based,
- bit 1..0, of byte 1 and byte 2 from CRC-10 generator is polynomial $G(x)= x^{10}+x^9+x^5+x^4+x+1$,
- computed over a user-defined number of previous segments, but must not include a UNI/NNI ATM-header segment,
- max. one segment / cell,
- must be the last segment of a cell.

TX time-stamp segment
- fixed 4 bytes length,
- data comes from a continuously clocked time-stamp generator with a 32 bit, 20 ns resolution,
- max. one segment / cell.

AUX segment
- valid on auxiliary signals AUX0..AUX7,
- memory-based data,
- max. ten segments / cell.

Cell pools
Cells are stored and recalled from a cell pool, and both cells and cell pools are identified by a custom name. Different users may share or use independent cell pools for different measurements. At run-time, a cell pool will be transferred into a 128 Kword memory. This provides runtime availability of up to 2473 different cells with a size of 53 bytes (8 bit wide interface), or 4854 different cells with a size of 27 words (54 bytes, 16 bit wide interface).

Traffic generation

In order to build up a cell stream, four traffic generators are combined by a priority encoder.

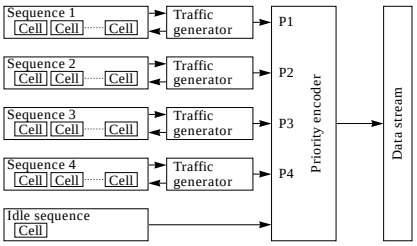


Figure 3: Priority encoder

Each independently defines a cell sequence, a traffic profile and a start (trigger) condition. An additional idle generator can be enabled at the lowest priority; see figure 3.

Sequence
- a sequence is a list of customer-defined cells in any order,
- 0..16384 cells / sequence, with a maximum 16384 cells in total over all five generators.

Traffic profiles
- constant bit rate:
  periodic cells; parameter: T_{cell},
- variable bit rate:
  periodic burst, random cell and random burst;
  parameters: T_{cell}, burst count, T_{pause}, random T_{cell}/T_{pause}, single cell and single burst.

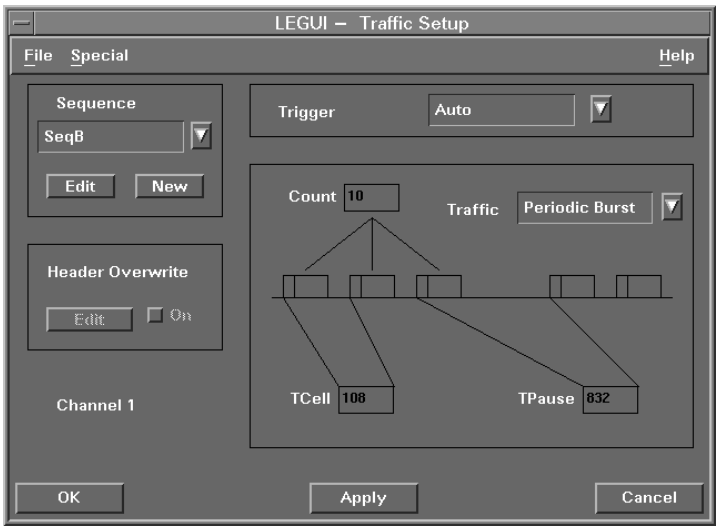


Figure 4: Traffic setup

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T_{cell}
- defines the number of clock cycles between the beginning of two consecutive cells,
- resolution = 1 clock period,
- range: cell length (i.e. back-to-back), or (cell length+6)...262144.

T_{pause}
- defines the number of clock cycles between the beginning of the last cell of a burst and the beginning of the first cell of the consecutive burst,
- resolution = 1 clock period,
- range = cell length..262144.

dvr	PRBS	*dvr*	PRBS
±3	2^3 -1	±1023	2^{11} -1
±7	2^4 -1	±2047	2^{12} -1
±15	2^5 -1	±4095	2^{13} -1
±31	2^6 -1	±8191	2^{14} -1
±63	2^7 -1	±16383	2^{15} -1
±127	2^8 -1	±32767	2^{16} -1
±255	2^9 -1	±65535	2^{17} -1
±511	2^{10} -1		

Figure 5: Deviation ranges

Random T_{cell} / T_{pause}
- T_{cell} and T_{pause} can be randomized, but not simultaneously,
- equal distribution around the mean value $T_{cellmean}$ or $T_{pausemean}$,
- fifteen deviation ranges *(dvr)* defined by a polynomial ±(2^n-1),
- range $T_{cellmean}$: cell length + *dvr*...262144 - *dvr*,
- range $T_{pausemean}$: 64 + *dvr*...262144 - *dvr*, but minimum cell length.

Burst count
- defines the number of cells within one single burst,
- range = 2..65536.

Traffic start (trigger)
- auto, for automatic start after a system run,
- manual, for a manual push-button,
- trigger, selected for a 'high' or 'low' signal either from the connector at the front panel of the module or from the 'trigger in' pin from the POD connector,
- event, detected at the receiver within the same module.

Idle generator
- will fill up the cell stream with idle cells to achieve 100% traffic.

Real-time analysis

General
Cells can be analyzed, provided that the following conditions are met:
- the cell length must be fixed for all received cells,
- range: 16..128 words,
- the SOC signal must be fixed relatively to the end of the cell.

Each cell received is compared with the specified trigger cells and evaluated for CRC / HEC / parity errors and cell types. The different results of these triggers can be combined together to build a term to start an action, such as an acquisition or a count (see figure 6). A simple example is:

IF
HEC error AND
trigger_cell_1

THEN
increment counter 1

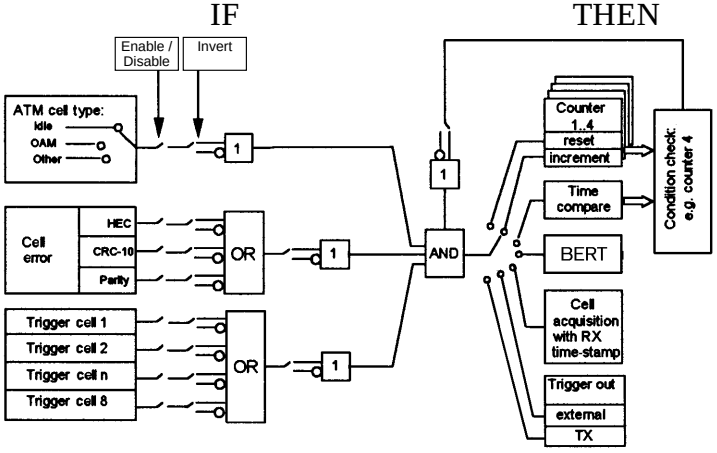


Figure 6: Real-time analysis

IF <*term*>...

Trigger cells
- eight independent trigger cells,
- each single bit of a trigger cell can be masked independently,
- the trigger cells are OR/NOR combined.

Cell errors
- parity, odd, even or none,
- CRC-10 $G(x)= x^{10}+x^9+x^5+x^4+x+1$ must be the last segment of a cell,
- HEC must be in all cells at the same segment position,
- cell error results (error / no-error) are OR/NOR combined.

ATM cell types
- OAM / idle / other are detected from the VPI/VCI and the PT field of an ATM-header,
- the header must be in all cells at the same segment position.

Number of terms
- a maximum of eight *terms* can be defined,
- one *action* per *term* allowed.

THEN <*action*>

Start
- auto; starts the cell analysis on the first received cell,
- on a defined *term*; any previous cell is ignored.

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Cell acquisition
- 128 Kwords of acquisition memory,
- the acquired cell is marked with a 32 bit, 20 ns resolution time-stamp,
- a complete cell or a subset of the cell is acquired, with a minimum of eight bytes / cell.

Count
- four independent counters,
- range: 1..65536,
- increment by one or reset,
- accumulated counting in steps of 10 ms for an infinite count.

Conditions / results feedback
- the counter can be compared with a fixed value, x,
- results: counter =, ≠, <, >,
- a maximum of four results can be fed back during one measurement,
- the results are fed back with a delay of one clock cycle.

Real-time time-stamp processing
- compares the 32 bit time-stamp, inserted at the TX side into the time-stamp segment, with an upper and lower limit,
- results:
  > upper limit
  < lower limit
  between lower and upper limit,
- range: 10 ns..40 s,
- resolution: 20 ns,
- always expects the time-stamp segment to be in the same position, relative to the end of a cell.

Bit error rate
- the bit error rate is measured on the PRBS segment of a cell, typically on the payload of a cell,
- the measurement interval is in multiples of 10 ms,
- measurement results per measurement interval:
  - number of received bits
  - number of errored bits
  - bit error ratio,
- cumulated results:
  - total number of received bits
  - total number of errored bits
  - bit error ratio since last re-synchronization.

Trigger
- generates one signal at the external connector (module or POD),
- generates up to four internal signals, used as events to start a traffic generator within the same module.

Stop
- stops the cell analysis on a defined *term*, or, if selected, on acquisition when the memory is full.

Timing system

Internal clock
- range: 90 KHz..52 MHz,
- resolution: 10 KHz,
- accuracy: typically 1%,
- independent for the TX and the RX PODs.

External clock
- range: 90 KHz..52 MHz,
- the external clock reference must be connected to the clock in pin of the connected POD,
- independent for the TX and the RX PODs,
- for operation with an external clock, the appropriate frequency must be entered.

Physical interfaces

Module to POD connection
A metral connector system with a cable length of 1m (40") connects the generator module HP E4821A to the PODs HP E4885A, HP E4886A and HP E4889A. With an optional cable extension, the length can be increased up to 2 m (80").

Module trigger input / output
The HP E4821A provides two SMD connectors for each trigger in and trigger out.
- the trigger in signal is edge sensitive, selectable for positive / negative transition, compatible with TTL levels and the input is high impedance.
- the trigger out signal is high active for eight clock cycles and levels are TTL compatible for termination with 50 Ohm to ground.

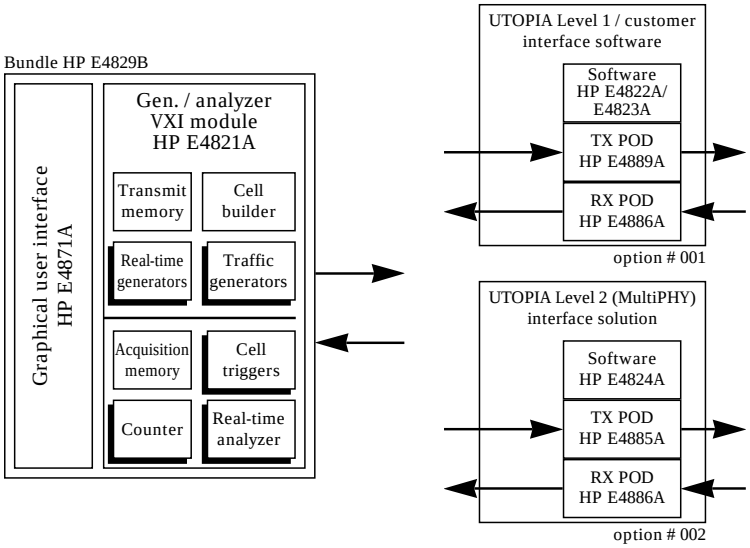


Figure 7: Solutions for UTOPIA Level 1 / customer and Level 2 (MultiPHY) interfaces can be added to the generator and analyzer module, HP E4821A

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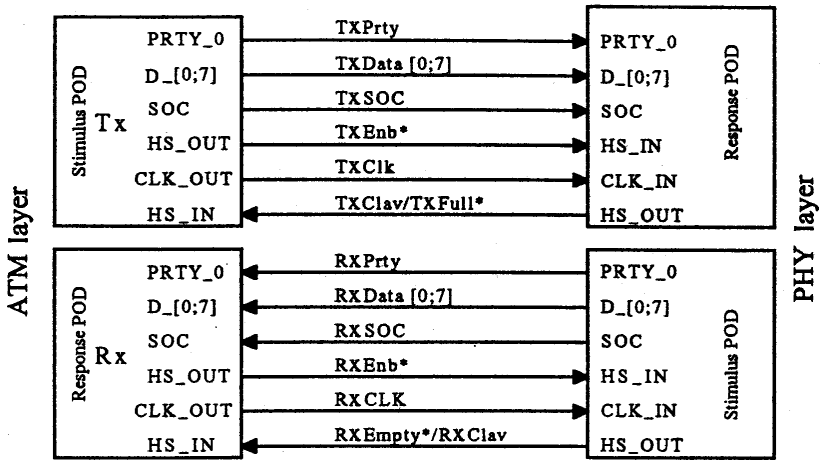


Figure 8: UTOPIA Level 1 interface diagram (HP E4889A PODs)

UTOPIA Level 1, UTOPIA Level 2 and customer interface solutions

The following specifications depend on the selected interface's solution. Within one system, different HP E4821A generator and analyzer modules can be connected to different interface solutions.

UTOPIA Level 1 / customer interface

The HP E4889A POD is used to connect the generator and analyzer module, HP E4821A, to the IUT. The HP E4889A serves as the TX or RX POD.

HP E4889A connection to the IUT

- direct plug-in into the IUT, but only if the appropriate sockets (e.g. 3M 8550-4500 SC/JL 50 pin) are designed into the IUT.
- customized interconnection via the ribbon cables to the IUT. The cable must have a maximum length of 20 cm (8") including PC-board traces.

Data signals

D0..D7/D0..D15

- 128 Kbit memory per TX and RX pin,
- output is at the TX / input is at the RX POD.

Data parity signal

- PRTY over D0..D7/D0..D15,
- real-time generated at the TX POD (output) / real-time verified at the RX POD (input),
- selected: odd, even, none.

Auxiliary signals

AUX 0 .. AUX 7

- 128 Kbits of data / acquisition memory behind each pin,
- output is at the TX / input is at the RX POD.

Handshake / data valid signals

UTOPIA Level 1

- HS OUT / HS IN according to UTOPIA Level 1 Rev. 2.01 for the cell and octet level handshake,
- the POD can either act as the physical layer or the ATM layer device,
- the TxClav and RxClav can be specified from nine bytes / words after the SOC to one byte / word before the end of the cell.

Customer interface

HS OUT

- the output at the TX POD indicates valid data on the D0..D7/D0..D15,
- selected off, and either high or low active,
- inactive at the RX POD.

HS IN

- the input at the RX POD indicates valid data for the D0..D7/D0..D15,
- selected off, and either high or low active,
- inactive at the TX POD.

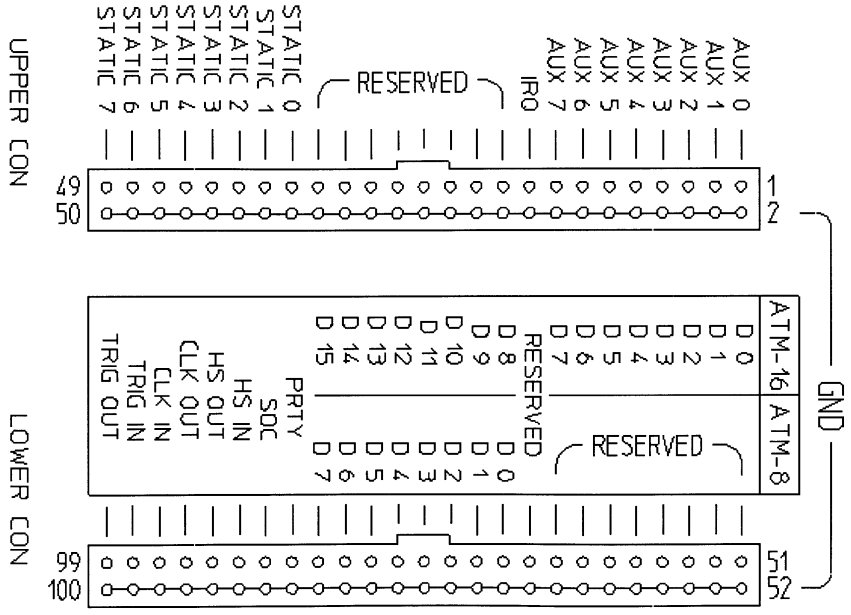


Figure 9: Signal layout at POD connector HP E4889A

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Start of cell signal
SOC, output at the TX POD
- can be placed anywhere from the first to the last byte / word of the cell. If the header segment is used, it cannot occur later than the first byte / word of the header.

SOC, input at the RX POD
- required to indicate the start of the cell for cell analysis,
- must be fixed relatively to the end of the cell for all received cells.

Trigger in / out
Transmitter:
- one trigger in at the POD, TTL level compatible.

Receiver:
- one trigger in and one trigger out at the POD, TTL level compatible.

Clock-to-data delay, custom mode
- the affected signals are: D0..D7/D0..D15, AUX0..AUX7, PRTY, SOC, HS IN, HS OUT,
- range: one period,
- accuracy: typically 1%,
- resolution:
  1/n of a period, depending on the selected range:

Range/MHz	n
52.00 .. 22.50	13
27.50 .. 11.25	26
13.70 .. 5.60	52
6.80 .. 0.09	104

Clock-to-data timing, UTOPIA
- typical values for f > 5 MHz,
- receiver:
  t_s = 4ns, t_H = 1ns,
- transmitter:
  t_d = 15ns.

Levels
All inputs / outputs use ABT technology and are compatible with TTL levels.

UTOPIA Level 2 (MultiPHY) interface

The HP E4885A TX POD and the HP E4886A RX POD are used to connect the HP E4821A generator and analyzer module to the IUT.

HP E4885A/E4886A connection to the IUT
- interconnection to the IUT is via a 12 cm (4.5") ribbon cable with an IDT connector. The cable must have a maximum length of 20 cm (8") including PC-board traces.

Data signals D0..D7/D0..D15
- 128 Kbit memory per TX and RX pin,
- output is at the TX / input is at the RX POD.

Data parity signal PRTY
- real-time generated over D0..D7/D0..D15 at the TX POD (output) / real-time verified at the RX POD (input),
- selected: odd, even, none.

Address signals A[0..4]
- address signals according to UTOPIA Level 2 v.1.0, chapter 4.2 and 4.3 for polling and the selection of the appropriate MultiPHY device.

CLAV0 / CLAV[0..3] signals
- Clav 0, according to UTOPIA Level 2 v.1.0, chapter 4.2 for operation with one TxClav and one RxClav signal.
- Clav[0..3], according to UTOPIA Level 2 v.1.0, chapter 4.3 for direct status indication.
- RxClav when the POD emulates the physical layer or TxClav when the POD emulates the ATM layer device.
- TxClav and RxClav can be specified from six clock cycles before or one clock cycle after the end of the cell.

LENB signal
- Enb* signal according to UTOPIA Level 2 v.1.0,
- RxEnb* when the POD emulates the physical layer or TxEnb* when the POD emulates the ATM layer.

Start of cell signal
SOC, output at the TX POD
- can be placed anywhere from the first to the last byte / word of the cell. If the header segment is used, it cannot occur later than

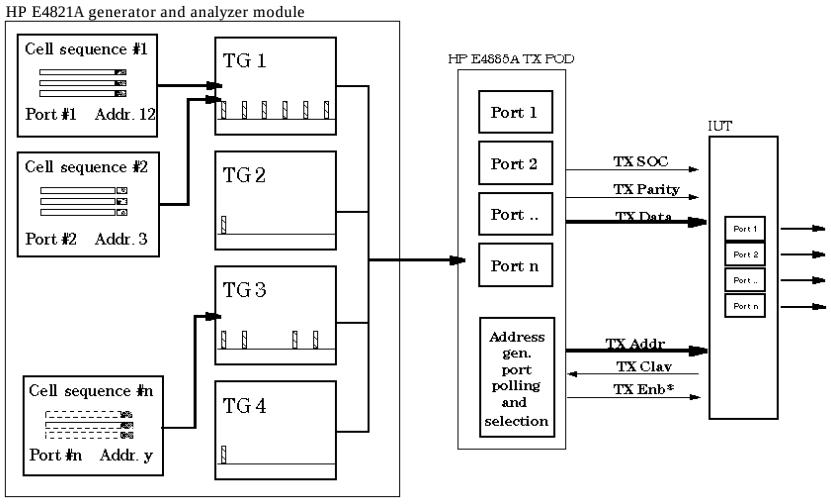


Figure 10: Sending traffic to a MultiPHY device

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the first byte / word of the header.
SOC, input at the RX POD
- required to indicate the start of the cell for cell analysis,
- must be fixed relatively to the end of the cell for all received cells.

Auxiliary signals
AUX 0 .. AUX 7
- 128 Kbits of data / acquisition memory behind each pin,
- output is at the TX / input is at the RX POD.

Trigger in / out
TX POD:
- one trigger in at the POD, TTL level compatible.

RX POD:
- one trigger in and one trigger out at the POD, TTL level compatible.

Timing
Receiver:
- t_s < 4ns, t_H < 1ns,

Transmitter (typical):
- t_d = 0.5T + 4ns, f > 25 MHz
  t_d = 18ns, f < 25 MHz

(T = actual period).

Levels
All inputs / outputs use FCT technology and are compatible with TTL levels.

Polling, port selection and signaling
The system is able to emulate the ATM layer as well as the physical (PHY) layer. Up to 31 PHY ports can be addressed.

When emulating the ATM layer, polling always starts with the lowest port address and is carried out in ascending order during each cell transfer. For PHY port selection, ports are associated with one of four priority classes. Within the same priority class, ports are served in a round robin manner.

When emulating MultiPHY devices, the Clav signaling is generated according to the traffic parameters T_{cell} and T_{pause} .

Maximum bandwidth
The maximum bandwidth of all addressed ports together cannot exceed 400 Mbit/s on an 8 bit and 800 Mbit/s on a 16 bit interface.

Cell sequences / traffic shaping
For each individually addressed port (0..30), one individual sequence of cells is set up. One out of four traffic generators is then applied to the sequence in order to define the traffic profile.

A dedicated single port testing mode allows up to four independent sequences and traffic generators to be linked to one single port.

UTOPIA Level 1 compatibility
The system operates compatibly with the UTOPIA amended Level 1 cell level handshake when either a single port address is specified or the system is set in the single port testing mode.

Configurations
This is a brief overview of the configurations of the parallel cell / traffic generator and analyzer. Please refer to the configuration guide, p/n 5964-1605E, for more details.

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HP E4829B 13-slot entry system
Pre-installed system with one port, including:
- one HP E1401B 13-slot C-size VXI mainframe,
- one HP E1497A V743 embedded controller with 32 MB,
- one HP E4208B embedded disc with pre-installed HP-UX 9.07 (with runtime license for two users) and SICL, SCSI cable and terminator,
- LAN transceiver,
- one HP E4821A hardware module,
- one HP E4871A user software for HP-UX 9.0x,
- UTOPIA Level 1 / customer interface kit and/or
- UTOPIA Level 2 (MultiPHY) interface kit.

In addition, a monitor, keyboard and a mouse are required. For future software updates, a CD-drive is recommended.

Adding additional ports
Up to seven additional ports can be added to the entry system. Each additional port requires:
- one HP E4821A hardware module,
- UTOPIA Level 1 / customer interface kit and/or
- UTOPIA Level 2 (MultiPHY) interface kit.

BSTS configuration
The HP E4821A module can also be plugged into an existing HP E4200B/E4210B broadband series test system (BSTS). Therefore, the parallel cell / traffic generator and analyzer system can be added into a BSTS as an independent test solution. The two applications share a VXI frame and an embedded series 700 workstation, although the hardware, as well as the software, of the BSTS and HP E4821A are run completely independently.

To add the first port to a BSTS system you will need:
- one HP E4871A user software,
- one HP E4821A hardware module,
- UTOPIA Level 1 / customer interface kit and/or
- UTOPIA Level 2 (MultiPHY) interface kit.

Please note:
- the BSTS and the HP E4821A run independently! This means that the functional behavior of the BSTS and the HP E4821A is the same as if they are used in two different frames! Therefore, the HP E4821A is not integrated as a part of the BSTS software or the measurement hardware.
- a maximum of two HP E4821A modules per BSTS frame is supported.



Figure 11: 13-slot entry system



Figure 12: BSTS configuration

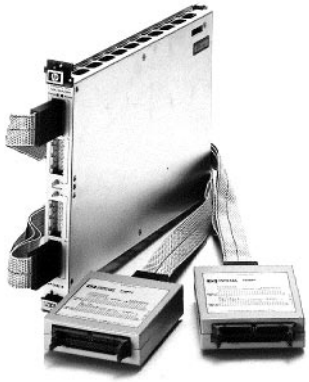


Figure 13: Generator and analyzer module HP E4821A and two PODs, HP E4889A

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HP E4829B entry system characteristics

The HP E4829B includes:
- HP E4821A hardware module,
- HP E4871A user software,
- HP E1401B 13-slot VXI frame,
- HP E1497 #ANC embedded V743 controller,
- HP E4208B embedded disk,
- LAN transceiver,
- operating system HP-UX 9.07,
- SICL, licenses and documentation.

Number of free slots
10

Operating temperature
+10°C .. +40°C

Storage temperature
-20°C .. +60°C

Humidity
80% R.H. @ 40°C

Power requirements
100-240 Vac, +/-10%, 50-60 Hz
100-120 Vac, +/-10%, 400 Hz

Acoustic noise
48 (56) dBA sound pressure at low (high) fan speed

Power consumption
see HP E1401B

Physical dimension
W: 426 mm (16.8”)
H: 310 mm (12.2”)
D: 602 mm (23.7”)

Weight
net: 29kg (63.9lb)
shipping: 50kg (110.2lb)

HP E4821A module characteristics

Slots size
C-1

Device type
register-based

Net weight
1.1 kg

Power requirement
+12V, +5V, - 2V, - 5V, -12V

Warranty
3 years

Operating temperature
+10°C .. +40°C

Storage temperature
-40°C .. +60°C

Humidity
80% R.H. @ 40°C

HP E4889A POD characteristics

Warranty
1 year

Operating temperature
+10°C .. +40°C

Storage temperature
-40°C .. +60°C

Humidity
80% R.H. @ 40°C

Physical dimensions
W: 175 mm (6.9”)
H: 27 mm (1.1”)
D: 126 mm (4.9”)

ISO 9001

All products are produced according to the ISO 9001 quality system.

Related HP literature

For more information:
- parallel cell / traffic generator and analyzer system, configuration guide, p/n 5964-1605E.
- parallel cell / traffic generator and analyzer system, product overview, p/n 5964-1667E.

for latest info:
http://www-europe.hp.com/dvt.

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