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Agilent E4832A ParBERT 675 Mb/s Data Module
Agilent E4838A ParBERT 675 Mb/s Generator Front-End
Agilent E4835A ParBERT 675 Mb/s Analyzer Front-End

Technical Specifications

E4832A 675 Mb/s generator/analyzer module

This module holds any combination of up to two analyzer front-end pairs (E4835A) and four generator front-ends (E4838A).

Clock module/data mode

The generator can operate in clock mode or data mode. Clock mode is achieved when the generator is assigned as a pulse port. Data mode is achieved with assigning it to a data port. In clock mode it is a fixed duty cycle of 50%. In data mode it is NRZ format with variable delay. The analyzer only works as a data port whenever used with variable sampling delay. The sampling delay consists of two elements: the start delay and the fine delay. The fine delay can be varied within ±1 period without stopping.

Data capabilities

PRBS/PRWS and memory-based data are defined by segments. Segments are assigned to a generator, and for stimulating a pattern. On an analyzer, it defines the expected pattern which the incoming data are compared to. The expected pattern can contain mask bits.

The segment length resolution is the resolution to which the length of a pattern segment can be set. The maximum memory per channel of the E4832A can be set in steps of 16 bits up to a length of 2048 Kbit. If the 16-bit segment length resolution is too coarse, memory depth and frequency can be traded.

Sub-frequencies

For applications requiring different frequencies at a fraction of the system clock, the ratio can be divided or multiplied by 2, 4, 8, or 16. This influences the dependency between segment length resolution and maximum memory depth.

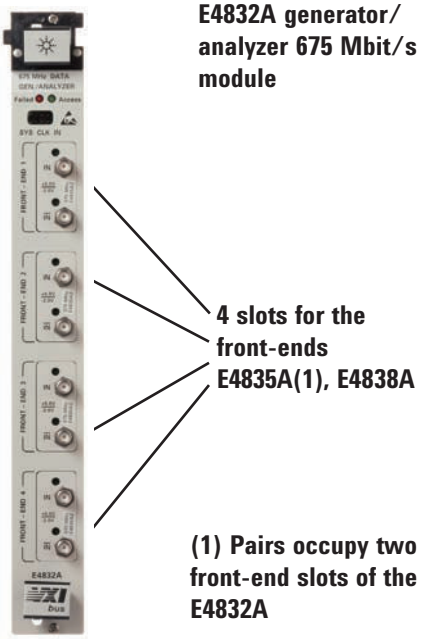


Figure 27. E4832A module

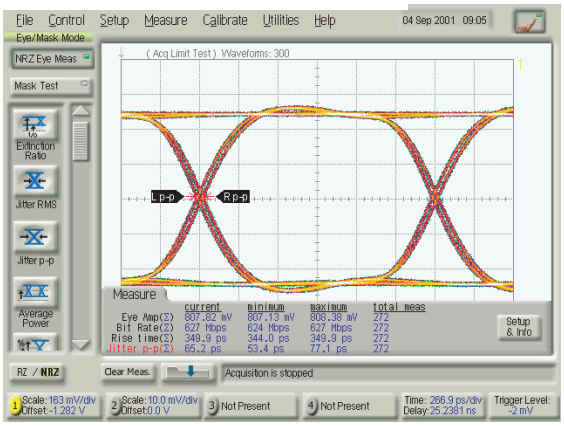


Fig 28. Wave diagram of E4832A generator

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Synchronization

Synchronization is the method of automatically adjusting the proper bit phase for data comparison on the incoming bit stream. The sychronization can be performed on PRBS/PRWS and memory-based data but it is not possible on a mix of PRxs and memory based data.

There are two types of synchronization:

- Bit synchronization
- Auto delay alignment

Bit synchronization is possible to cover a bit alignment for a totally unknown number of cycles. Using memory-based data, the first 48 bits within the expected data segment will work as a detect word which the incoming data are compared to. When the incoming data match with this detect word, analysis will begin.

Auto delay alignment is performed by using the analyzer sampling delay. The sampling delay range is ±50 ns while this is possible.

Using auto delay alignment provides synchronization with an absolute timing relation between a group of analyzer channels. This makes skew measurements are possible.

Table 51. E4832A data generator timing specifications (@ 50% of amplitude, 50 Ω to GND and fastest transition times)

Frequency range	333,334 kHz to 675 MHz
Delay range	0 to 3.0 µs (not limited by period)
Sampling delay resolution	2 ps
Accuracy	±50 ps ±50 ppm relative to the zero-delay placement (1)
Skew	50 ps typ. after deskewing at customer levels
Pulse width	Can be specified as width or % of duty cycle
Range	750 ps to (period -750 ps)
Resolution	2 ps
Accuracy	±200 ps ±0.1%
Duty cycle	1% to 99%, subject to width limits

(1) Valid at 15 to 35 °C room temperature

Table 52. E4832A analyzer timing; all timing parameters are measured at ECL levels terminated with 50 Ω to GND

Sample delay = start delay + fine delay	
Fine delay can be changed without stopping (2)	
Sampling rate (3)	333,334 Kb/s to 675 Mb/s
Sampling delay	(= start delay + fine delay)
range	0 to 3.0 µs (not limited by period)
Fine delay range	±1 period
Accuracy	±50 ps ±50 ppm relative to the zero-delay placement (3)
Resolution	2 ps
Skew	50 ps typ. after deskewing at customer levels

(2) Conditions: frequency > 20.8 MHz and by using the finest segment length resolution.
(3) See tables for front-end deratings

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Table 53. Pattern and sequencing features of E4832A

Patterns:	
Memory based	Up to 2 Mbit
PRBS/PRWS	2^n - 1, n = 7, 9, 10, 11, 15, 23, 31
Mark density	1/8, 1/4, 1/2, 3/4, 7/8 at 2^n - 1, n = 7, 9, 10, 11, 15
Errored PRBS/PRWS	2^n - 1, n = 7, 9, 10, 11, 15
Extended ones or zeros	2^n - 1, n = 7, 9, 10, 11, 15
Clock patterns	Divide or multiply by 1, 2, 4
User patterns	Data editor, file import
Analyzer auto-synchronization (2):	On PRBS or memory-based data manual or automatic by: Bit synchronization (1) with or without automatic phase alignment Automatic delay alignment around start sample delay (range: ±50 ns) BER threshold: 10^{-4} to 10^{-9}

(1) Bit synchronization on data is achieved by detecting a 48 bit unique word at the beginning of the segment. "Don't cares" within the detect word are possible. In this mode no memory-based data can be sent within the same system. If several inputs synchronize, the delay difference between the terminals must be ±5 segment length resolution.

(2) Condition: frequency > 20.8 MHz and by using the finest segment length resolution.

Table 54. Data rate range, segment length resolution, available memory for synchronization and fine delay operation

Data rate range Mb/s	Segment length	Maximum memory resolution depth, bits
20.834 ... 41.666	1 bit	131,008
41.667 ... 83.333	2 bits	262,016
83.334 ... 166.666	4 bits	524,032
166.667 ... 333.333	8 bits	1,048,064
333.334 ... 666.667	16 bits	2,097,152

In general, it is possible to set higher values for the segment length resolution and also at lower frequencies than are indicated in the table. In this case the fine delay function and the auto-synchronization function are unavailable.

Table 55. between the capability of generating PRWS and port width, almost all the combinations are possible except the following:

PRWS	Port width
2^7 - 1	No restriction
2^9 - 1	7
2^{10} - 1	3, 11, 31, 33
2^{11} - 1	23
2^{15} - 1	7, 31
2^{23} - 1	47
2^{31} - 1	No restriction

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Input/output

Addressable technologies
LVDS, (P)ECL, TTL, 3.3 V CMOS

Analyzer input

The analyzer channel can be operated:

- Single-ended normal
- Single-ended compliment
- Differential

For termination there is always 50 Ω connected to a programmable termination voltage. In differential mode there is an additional, selectable 100 Ω differential termination. Independent of the selected termination, there is the choice of whether the anaylsis of the incoming signal is performed on the input or true differential.

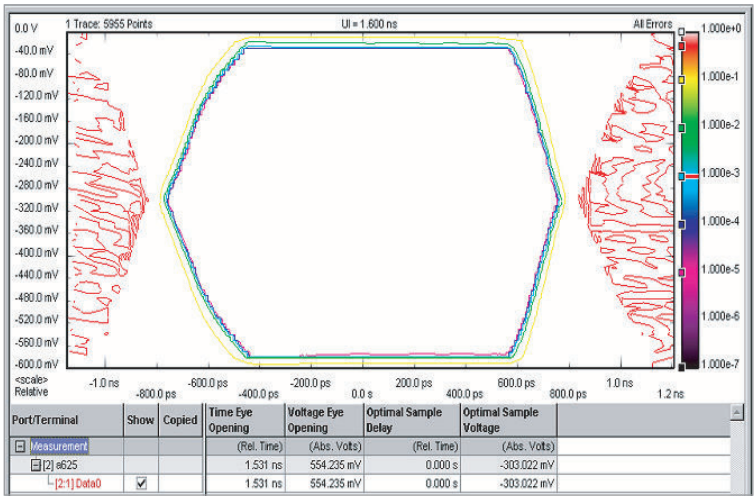


Figure 29. Eye diagram of E4835A analyzer

Table 56. Level parameters for differential generator front-end E4838A 675 Mb/s

Number of channels	1, differential
Impedance	50 Ω typ.
Data formats	RZ, R1, NRZ, DNRZ
Output voltage window	–2.2 to +4.4 V (doubles into open up to max. 5 Vpp)
Amplitude/resolution	0.1 V to 3.50 V / 10 mV
Level accuracy	±3% ± 25 mV typ. after 5 ns settling time
@ LVDS/(P)ECL	±1% ±25 mV typ. after 5 ns settling time
Variable transition time range (10 - 90% of amplitude)	0.5 to 4.5 ns
Accuracy	±5% ±100 ps
@ LVDS/(P)ECL (20 - 80% of amplitude)	0.35 ns typ
Overshoot/ringing	< 7% (< 5% typ).
Jitter Data mode Clock mode	 < 100 ps peak to peak (80 ps typ) 8 ps rms typ.
Channel addition	XOR and analog

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Table 57. Two differential analyzer front-ends E4835A (1), 667 MSa/s

Number of channels	2, differential or single-ended (switchable)
Impedance	50 Ω typ. 100 Ω differential if termination voltage is switched off
Termination voltage (can be switched off)	–2.0 to +3.0 V
Threshold voltage range/ threshold accuracy	–2.00 to +4.50 V/±1% ±20 mV
Threshold resolution	2 mV
Input sensitivity	Differential 50 mV typ Single-ended 100 mV typ
Minimum detectable pulsewidth	400 ps typ. at ECL levels
Input voltage range	Two ranges selectable: 0 to +5 V and -2 to +3 V
Phase margin with ideal input signal with E4838A generator	> 1 UI - 100 ps > 1 UI - 180 ps

(1) Occupy two front-end slots of the E4832A. The E4835A contains two front-ends (E4835AZ) and one common data back end. In this document one front-end is referred to as E4835A.

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