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Agilent 81200

The 81200 Data Generator/Analyzer Platform

Data Sheet

Release 3.5 (Corresponds to SW Release 3.5x)

Push new devices to the limit with comprehensive signal testing

The Agilent 81200 data generator/analyzer platform is the right choice for you if you are an engineer in R&D or manufacturing performing functional and parametric tests on digital subsystems, ICs, or boards. The 81200 allows thorough verification and characterization of digital devices throughout the development cycle, thus reducing risks, costs and time-to-market.

The 81200 is a modular system offering stimulus and analyzer channels in speed classes 200/330/675/2.700Mb/s.

Create virtually any test signal you need

Today's devices require very complex stimuli. With sequencing and looping and up to 8 million vectors of memory per channel, you can create an infinite variety of stimulus signals. Choose from return-to-zero (RZ), non-return-to-zero (NRZ) and return-to-one (R1) formats. Create even more complex signals with Boolean channel addition including return-to-complement.

The internal editor includes memory-based PRBS/PRWS (pseudo-random binary/word sequence) to stimulate traffic.

The 81200 is ideal for performing parallel bit error ratio measurements at up to 2.7Gb/s or for stimulating the digital port of a DAC.



Figure 1: The 81200 data generator/analyzer platform

Simplify your verification and characterization process

Key Features

- Flexible real-time stimulus and response system
- Easy integration into standard VXI environments
- 1Kb/s to 2.7Gb/s
- Up to 8 Mbit memory per channel
- 2-128 RZ channels (doubles for NRZ channels up to 200 Mbit/s)
- Scaleable and upgradeable through modules and front-ends
- 1 ps timing resolution, ± 30 ps edge placement accuracy
- Pattern formats: RZ, R1, NRZ, DNRZ
- PRBS (Pseudo-Random-Bit-Sequence) and PRWS (Pseudo-Random-Word-Sequence) up to 2^{15}-1
- Sequencing with 5 looping levels (nested loops)
- Branching on internal and external events
- Variable delays, levels and transition times can be set independently for each channel
- Semi-automatic deskew eases test setup
- Measurement modes: capture, error capture, error count
- Measurement result displays: state list, waveform viewer, bit-error-rate
- Intuitive, Windows NT® 4.0–based GUI
- Remote Interfaces: LAN, GPIB
- SCPI,with based language, Plug & Play drivers for easy programming in Agilent VEE, C/C++/Visual basic.

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Platform Description

The Agilent 81200 Data Generator/Analyzer Platform is a modular platform which can be tailored to your specific needs, for example, as a pulse generator, single or multi-phase clock generator, a data generator, or as a data generator/analyzer system.

As indicated in the block diagram (Figure 2), each DUT input pin is stimulated by a generator channel with independent data memory, timing and output. The device outputs are sampled by an analyzer channel with individual input threshold, sampling point delay, and memory, for captured and expected data. All data generator and analyzer channels are synchronized by a common system clock and pattern sequence.

Initial set up is easy because the 81200 is supplied ready-to-use. All software and hardware is fully installed. You only need to connect computer peripherals (keyboard, mouse, and monitor) to the main-frame.

Easy Integration into Your Test Environment

The 81200 data generator/analyzer modules can be integrated easily into other VXI-based test platforms, and C-size VXI module can be configured to work with the 81200 system. Plug & Play drivers facilitate easy programming and test system integration.

For details of integrating the 81200 modules into a standard VXI test system, consult the 81200 Data Generator/Analyzer Platform configuration guide, publication number 5965-3417E.

If the integration into a standard VXI test system is not required, please refer to the mainframes described in the next section for configurating a standalone system of the 81200. The advantage of a standalone system is that the system arrives fully installed and ready to go.

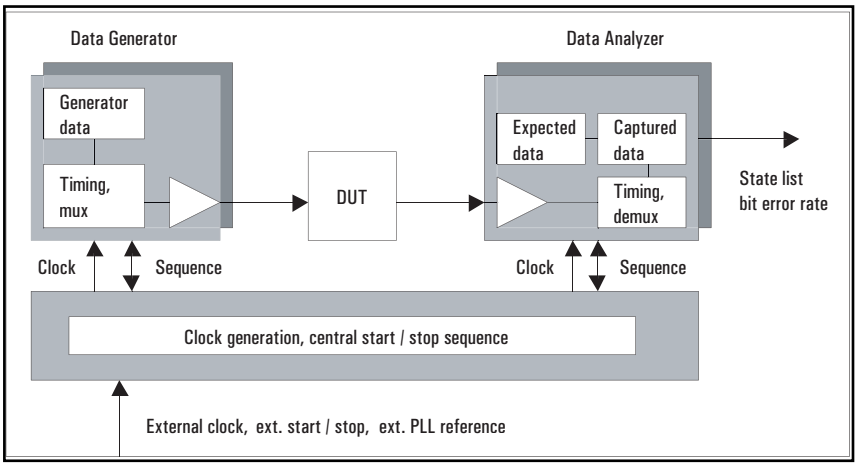


Figure 2: Block Diagram of 81200 functional layout

Comprehensive Characterization

Characterizing digital components is usually a very time-consuming task. To make this task faster and easier with the 81200, consider the wide range of accessories for the Agilent 81200, which include:

- E4839A Test Fixture (see 5968-3580E for more details)
- E4805B Opt 002 8 line trigger input for TTL signals (useful when branching on external events (hardware signals) other then VXI-ECL trigger lines or compare errors)
- E4805B Opt 003 De-skew probe (Comprises Agilent 1144A 880MHz active probe and a BNC (f) to SMA (m) adapter (part number 1250-1200)).
- Agilent general accessories (cable kits, adapters etc). See table 1.

Product Description		Model Number
General Accessories	Cable Kit SMA (m) to SMA (m), matched pair	Agilent 15443A
	Cable Kit: 4*SMA(m) to SMA(m) 1 meter	Agilent 15442A
	Cable Kit: 10*SMA(m) to SCI Connector	Agilent 15441A
	SMA coax. cable, 1 m.	Agilent 8120-4948
	Torque wrench, SMA.	Agilent 8710-1582
	Adapter Kit: 4* SMA(m) I/O Adapter	Agilent 15440A
	Adapter SMA (m)/BNC (f).	Agilent 1250-1200
	Adapter right-angle SMA (m-f).	Agilent 1250-1249
	Adapter right-angle SMA (m-m).	Agilent 1250-1397
	Adapter tee SMA.	Agilent 1250-1698
	Pulse adder/splitter, SMA.	Agilent 11667B
	500 ps transition converter.	Agilent 15433B
	1 ns transition converter.	Agilent 15434B
	2 ns transition converter.	Agilent 15438B
	Cable, GPIB.	Agilent 10833B

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Scaleable and Upgradeable

The 81200 is a modular instrument, which can be tailored to your specific needs. The idea is that you get a system which is configured in such a way that matches your measurement task perfectly.
The front-ends determine the speed and input/output capabilities of your instrument. After you have chosen the front-ends, they are placed in data modules, which are responsible for sequencing, generation and analysis of data patterns. These modules plus at least one clock module, which generates the system frequency of the instrument, are installed in the mainframe (see figure 3). If more channels are needed you can add up to two expander frames to the system, to reach the maximum number of channels (64 channels at 2.7 Gb/s, 128 channels at 675 MHz, or 256 channels at 200/330 Mb/s).

E4849C Mainframe

The mainframe (figure 4) offers eleven to twelve slots for the 81200 modules, depending on the controller option which is chosen. Controller options are a 2-slot VXI PC (E4803A), or an IEEE 1394 PC link to VXI (1 slot) to control the system from an external PC. (E4849C#013) It offers 11 empty slots for e.g 1 clock module and up to 10 data modules. When the 2-slot PC is chosen the system comes installed with the Windows NT® operating system and the E4873A user software. If the controller option, IEEE 1394.PC link (firewire) is chosen, E4849C#013 should be selected. There is an external PC offered, preinstalled with Windows NT and 81200 SW (E4860AS#014) This configuration offers 12 empty slots for 81200 modules. For more modules one or two expansion frames (E4860A#152) can be added to house 22/23 data modules. E4849C#002 Option 002 provides a VXI extender module (E1482B) so that one or two expander frames (E4848B) can be connected, in order for a total of 31 data modules to be housed.



Figure 4: E4949C mainframe

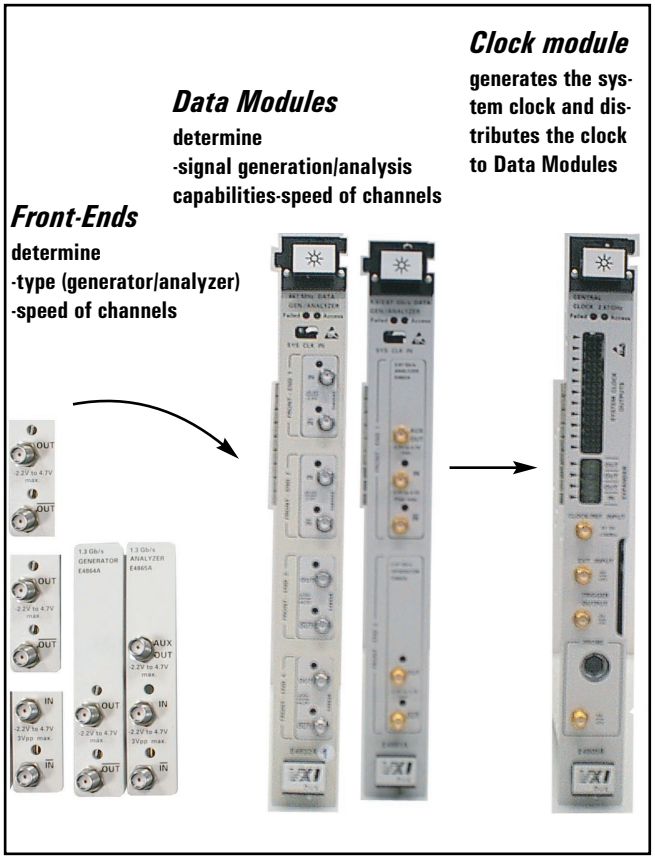


Figure 3: Front-Ends, modules and mainframe.

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Front-End and Module Overview

Each system needs at least one clock module (E4805B) to generate the system clock and, at least one data generator/analyzer module E4841A, E4861A or E4832A.

E4805B Central Clock Module

This module provides clock and sequence data flow control signals to the Data Modules:

- frequency resolution of 1 HZ (instead of four digits)
- synchronizes analyzer channels as well as generator channels
- drives up to 11 E4841A, E4832A and E4861A modules.

E4841A 333Mb/s Data Generator/Analyzer Module

This module provides four slots for any mix of generator or analyzer dual front-ends E4846A or E4847A. With the dual frontends the module can provide 8 independant channels at 5 Mbit memory each.

E4832A 675 MHz Data Generator/Analyzer Module

This module provides four slots for any mix of generator or analyzer front-ends, E4838A,E4835A. This module allows 4 independant channles with PRBS/PRWS measurements up to 2^{15}-1 and has a memory depth of up to 2 Mbit per channel.

E4861A 2.7 Gb/s Data Generator/Analyzer Module

This module provides two slots for any mix of generator and analyzer front-ends E4862A, E4863A. The module provides two independant channels.

Generator Front-ends

E4862A

2.7 Gb/s, data or 2.7GHz clock single channel, differential, 1.8 Vpp.

E4838A

675 MHz, RZ/NRZ, single channel, differential, variable transition times, 3.5 Vpp.

E4846A

200 Mbit/s, NRZ, dual channel, single ended, 3.5 Vpp.

Analyzer Front-ends

E4863A

2.7 GSa/s, single channel, 50 Ω.

E4835A

675 MSa/s, this is a pair of channels, 50 Ω 1 GHz bandwidth. It fills two adjacent slots of the E4832A and provides two independant channels.

E4847A

333 MSa/s, dual channel, 50 Ohm/high-impedance selectable, 350 MHz bandwidth.

For mixed-logic requirements, you can mix slower and faster front-ends to provide an economic way of generatating control signals as well as data.

Table 2 : Module/Front-End Compatibility

Modules	330 Mb/s	675Mb/s	2.7 Gb/s
Front-Ends	E4841A	E4832A	E4861A
E4835A		X	
E4838A		X	
E4846A	X		
E4847A	X		
E4862A			X
E4863A			X

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Technical Specifications

These specifications describe the instrument's warranted performance. Non-warranted values are described as typical. All specifications are valid from 10º C to 40º C ambient temperature after a 30 minute warm up phase, with outputs and inputs at ECL leves terminated with 50 Ω to ground.

Channels and Grouping

Number of Channels: up to 64, 128 or 256 channels depending on the front-end type.

Grouping: connections can be grouped and named according to the requirements of the device-under-test to facilitate setup.

Port Types: individual channels can be assigned as data or pulse ports. Pulse ports are independent of the data sequence. Easy setup of a clock is possible

Pattern and Sequencing

Segment: the memory can be divided into loopable segments.

Segment Types: pattern, pause, PRBS/PRWS*.

Pause Segments: "PAUSE 0" or "PAUSE"1" levels selectable for generator. PAUSE segment for analyzer.

Pattern Formats: NRZ, DNRZ, RZ, and R1 patterns can be selected, as shown in Figure 10.

Powerful Sequencing: a sequence is a succession of segments, as shown in Figure 7. The segment flow is defined by -Loops (finite, infite,nested) and events (branch, goto, trigger). A sequence applies to all channels, but different segment types can be set in different modules.

Note: Generating the segment types PRBS and pattern (user-defined) at the same time requires two different E4841A data generator/analyzer modules. One module generates the PRBS pattern, the other one the user-defined pattern.
To facilitate complete pattern setup there are different editing tools:

Sequence Editor: (defines sequence)
Data Editing: (defines segment content) fill in the pattern, complement, copy, cut, paste, move, insert, append, delete. Binary, octal, hexadecimal, and decimal formats.

Masking: single bits or complete segments can be masked in the expected data memory. This allows specific areas to be ignored in the Compare Data mode.

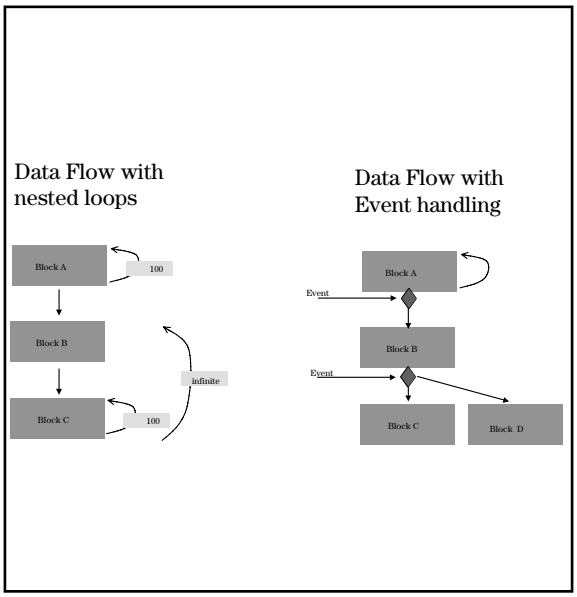


Figure 7: Sequencing capabilities

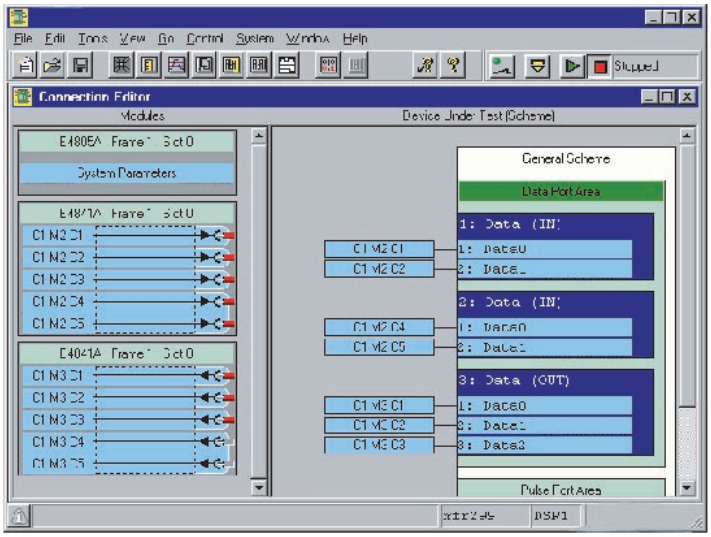


Figure 5: The Connection Window helps you to create a virtual model of your measurement set-up

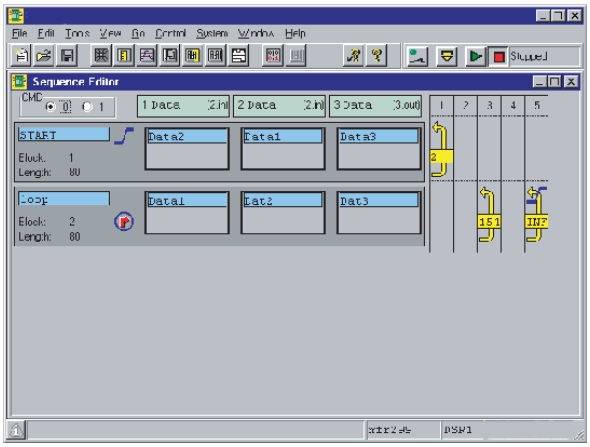


Figure 6: The Sequence Editor lets you set up data segments, different looping levels, and events

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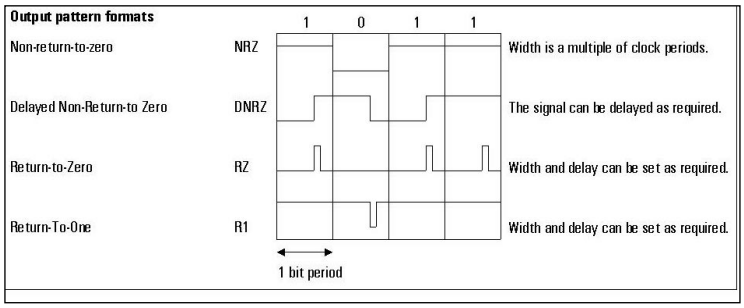


Figure 8: 81200 Pattern Formats

Input/output Specifications

Front-ends: You can choose between three generator front-ends (outputs) and three analyzer front-ends (inputs) of the speed classes 334 MHz, 675 MHz, and 2.7 GHz. For individual specifications see the following pages.

Enable/connect: Each output/input can be switched on and off individually, and the connect/disconnect function allows you to disable/enable respectively, all outputs and inputs at one time.

Connectors: SMA (f) 3.5 mm.

Channel Addition (for the E4832A with E4838A only)
Outputs can be logically combined, as shown in Figure 8. This feature is useful in applications such as:

- clock/data recovery tests that need different pulse widths in a single channel
- return to complement logic.
- With the Analog channel adding a 4 -level- signal is possible, see fig 9b.

Auxiliary Output: The analyzer front-end E4863 provides an auxilary output. A differential signal from the device-under-test can be fed single-endedthrough the analyzer for further usage, e.g. as an input to a jitter analyzer or an oscilloscope. Auxiliary output works in all input modes.

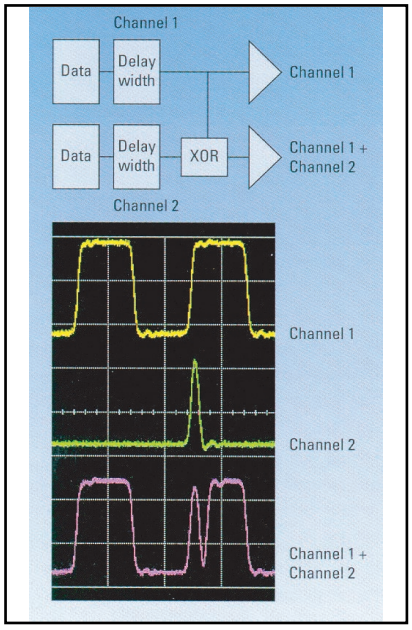


Figure 8a: Channel addition

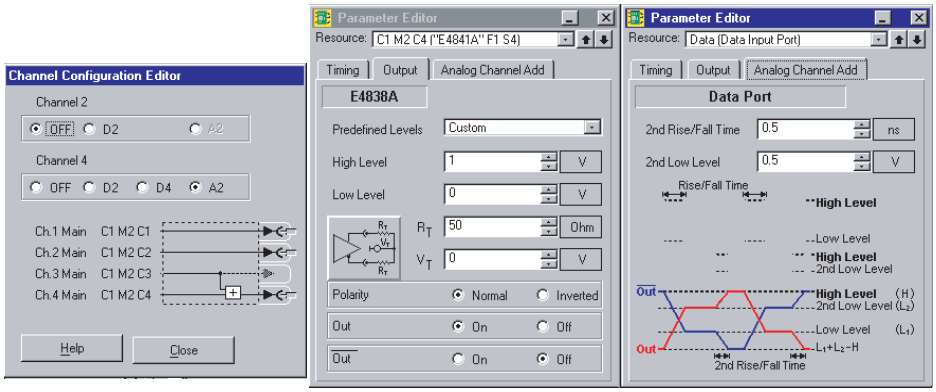


Fig 9a: Analog channel Add setupthe E4838A



Fig 9b : Analog channel Add Agilent E4838A Frontend

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Measurement Modes

The Agilent 81200 Data Generator/ Analyzer Platform provides mea-surement modes when:

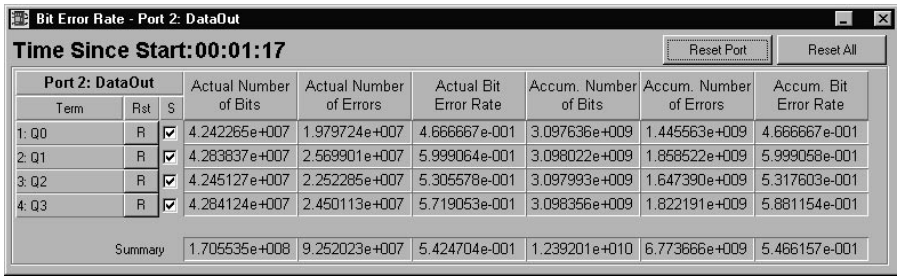
- one or more analyzer front-ends are fitted
- the E4805B provides the clock (or conditions it in the case of an external clock).

The measurement modes are detailed below.

Capture mode: data bits are sampled and stored. Results can be displayed in a state list or viewed using the waveform viewer. Captured data can be edited, filed, exported, or copied to the generator channels for regeneration.

Error Capture Mode: data bits are sampled and compared with an expected pattern in real time. A total of at least 65,504 bytes can be captured before or after an error occurs. Masking is possible for individual bits in pattern segments and whole segments, so that only the bits of interest are captured. The results are stored and can be viewed using the state list or waveform viewer. Errors are highlighted.

Error Count Mode: the same as Error Capture mode, except that the errors are counted instead of being stored. It is possible to watch the result display in real time while the measurement is running and stimulus parameters can be varied. The result is displayed as a bit count (number of bits), an error count (number of errors), or as a bit-error-rate (BER).



Port 2: DataOut			Actual Number of Bits	Actual Number of Errors	Actual Bit Error Rate	Accum. Number of Bits	Accum. Number of Errors	Accum. Bit Error Rate
Term	Rst	S						
1: Q0	R	☑	4.242265e+007	1.979724e+007	4.666667e-001	3.097636e+009	1.445563e+009	4.666667e-001
2: Q1	R	☑	4.283837e+007	2.569901e+007	5.999064e-001	3.098022e+009	1.858522e+009	5.999058e-001
3: Q2	R	☑	4.245127e+007	2.252285e+007	5.305578e-001	3.097993e+009	1.647390e+009	5.317603e-001
4: Q3	R	☑	4.284124e+007	2.450113e+007	5.719053e-001	3.098356e+009	1.822191e+009	5.881154e-001
Summary			1.705535e+008	9.252023e+007	5.424704e-001	1.239201e+010	6.773666e+009	5.466157e-001

Figure 10: The Bit-Error-Rate display shows the actual error rate in real-time.

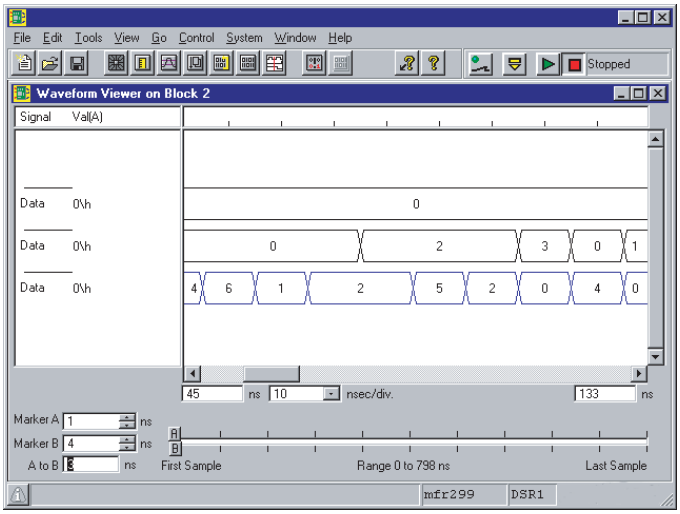


Figure 11: Waveform View

The Waveform Viewer

The waveform viewer can display the Analyzer Data in a graphical way.

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Signal Waveforms

The following waveforms are taken from the different speed classes of the 81200 Family.

The pictures are taken showing once the Generator output on the scope and second the Analyzer Inputs are connected to an ideal-source and with help of the eye opening measurement (ParBERT 81250 measurement software) the performance of the Analyzer is recorded .

ParBERT Settings:

Generator and Analyzer in single ended mode, normal in/out used.

Frequency:
625 Mb/s used for:
E4805A+E4832A + E4838A + E4835A

2.5Gb/s used for:
E4805A+ E4861A + E4862A +E4863A
Data :PRBS 2 ^{15} -1 (stimulus and expected) data
Generator levels:
Low Level -.4V, High levels + .4V

Analyzer/ Eye Opening:
Single ended, terminated to grd.
Compared Bits 10^{6}
BER Threshold 10 $^{-3}$

Trigger Out: clock mode (625 MHz), levels O/1V

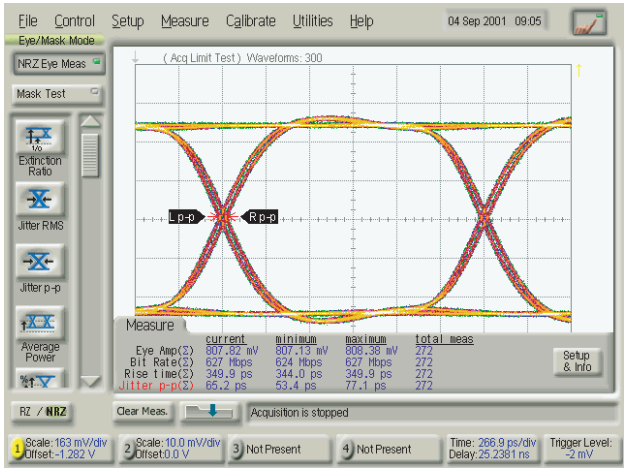
Scope settings:

Agilent 81600 DCA with 83484A 50 GHz module

-connected with 1m SMA cables
-ext trigger from 81200 trigger out
-signal adjusted with Auto scale
-every measurement for 300 events

Ideal source:

transistion time 30ps,
jitter <10ps pp, levels -.5V/



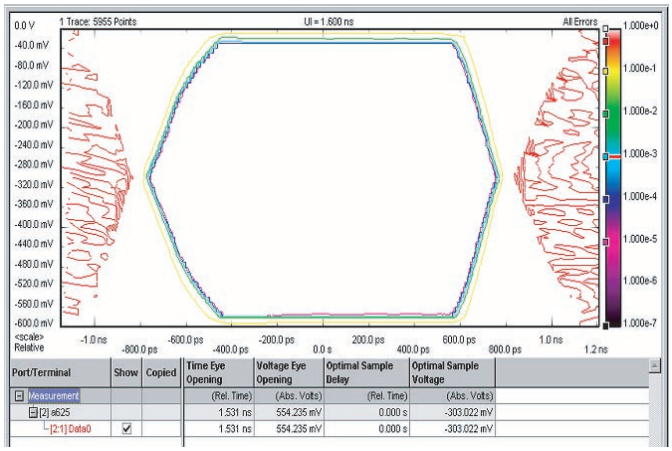
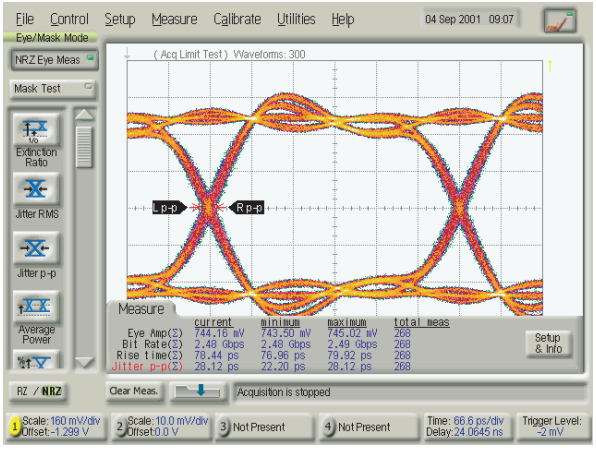


Figure 12 a) b): Signals of E4832A with E4838A Generator + E4835A Analyzer



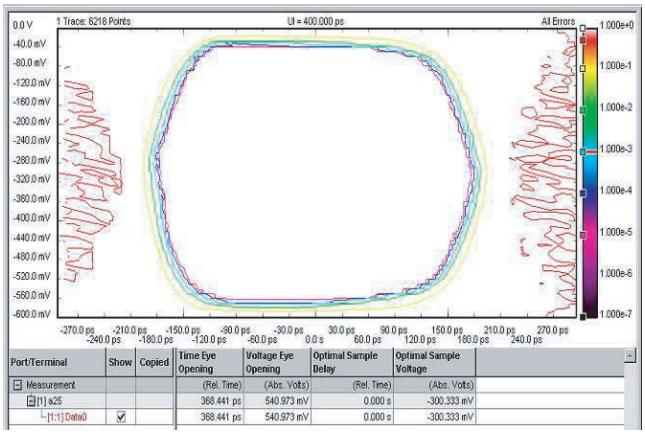


Figure 13a) b): Signal of E4861A with E4862A and E4863A Analyzer

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Technical specifications 2.7Gb/s

E4861A Generator / Analyzer Module

This module holds any combination of up to two analyzer front-end (E4863A and generator front-end E4862A,).

Clock Module/Data Mode

The generator can operate in clock mode or data mode. Clock mode is achieved when the generator is assigned as a Pulse Port.
Data mode is achieved when using it as Data Port. In Clock mode there is a fixed duty cycle of 50%. In data mode there is NRZ format with variable delay. The analyzer works as Data Port always with variable sampling delay. The sampling delay of the analyzer consists of two elements: the start delay and the fine delay. The fine delay can be varied within ± 1 period without stopping.

Data Capabilities

PRBS/PRWS and memory based data are defined by segments. Segments are assigned to a generator for a stimulating pattern, on an analyzer it defines the expected pattern where the incoming data are compared to. The expected pattern can be setup with mask bits.

The segment length resolution is the resolution to which the length of a pattern segment or mask can be set. The maximum memory per channel of the E4861A can be set in steps of 64 bits up to a length of 8192 kbits. If the 64 bit segment length resolution is too coarse, memory depth and frequency can be traded as shown in table 6.

Table 3: E4861A Data Generator Timing Specifications (@ 50 % of amplitude, 50 Ohm to GND

Frequency range*	Clock/Data mode 333.334 MHz/Mb/s to 2.70 GHz
Delay (between channels)	Can be specified as leading edge delay in fraction of bits in each channel
Range	0 to 300 ns (not limited by period)
Resolution	1 ps
Accuracy	± 50 ps ± 50 ppm relative to the zero-delay placement. (From 20°C to 35 °C without autocal) ±30 ps ± 50 ppm typ. relative to the zero-delay placement and temperature change within ± 5 ° C after autocalibration
Skew between modules of same type	50 ps typ. after deskewing at customer levels and unchanged system frequency .
Pulse width	50% of period typ. in clock mode

* See tables for front-end deratings

Table 4: : E4861A Analyzer Timing All timing parameters are measured at ECL and levels, terminated with 50Ω to GND

Sample delay:= start delay + fine delay, fine delay can be change without stopping	
Sampling rate*	Same as generator
Fine delay range	±1 period
Sampling delay range	Same as generator
Accuracy	Same as generator
Resolution	Same as generator
Skew	Same as generator

*See tables for frontend deratings

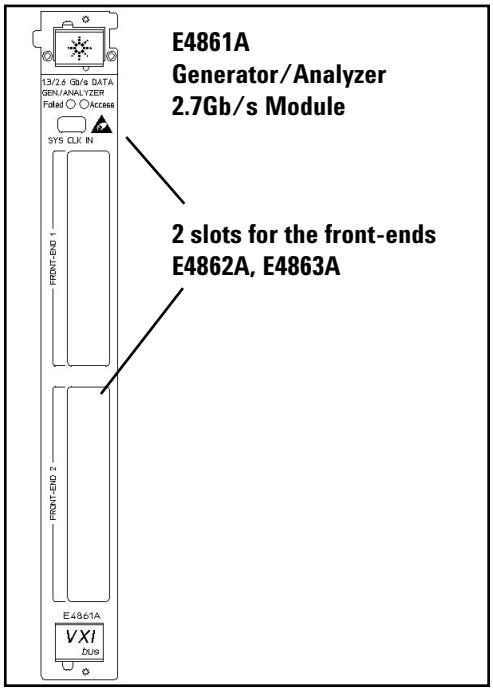


Figure 14: E4861A Module

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Table 5: E4861A Pattern and Sequencing	
Patterns:	
Memory based	up to 8Mbit see table 17
PRBS/PRWS	2^n-1, n=7, 9, 10, 11, 15
Marker Density	1/8, 1/4, 1/2, 3/4, 7/8 at PRBS/PRWS 2^n-1, n=7, 9, 10, 11,15
Errored	2^n-1, n=7, 9, 10, 11, 15
Extended ones or 0	2^n-1, n=7, 9, 10, 11, 15
Clock patterns	Divide or multiplied by 2, 4, 8, 16
User	Data editor, file import

Table 6: Data rate range, segment length resolution, available memory and fine delay operation

Data rate range Mbit/s	Segment length resolution	Maximum memory depth, bits
333.334...666.666	16 bits	2,097,152
666.667...1,333.333	32 bits	4,194,304
1,333.334...2,666.667	64 bits	8,388,608

In general it is possible to set higher values for the segment length resolution and also at lower frequencies than is indicated in the table.

Table 7: Parameters for Analyzer Front-Ends E4863A 2.7 GSa/s	
Number of channels	1 , differential or single ended
Impedance	50 Ohm typ. 100 Ohm differential if termination voltage is switched off
Internal termination voltage (can be switched of)	-2.0 to +3.0 V
Threshold voltage range	-2.0 to + 3.0 V
Threshold resolution	2 mV
Threshold accuracy	± 1% ±20 mV
Input sensitivity (single-ended and differential)	50mV typ
Minimum detectable pulse width	180 ps typ. at ECL levels
Maximum input voltage range	Three ranges selectable: -2V to + 1V -1V to +2V 0V to 3V
Maximum differential voltage	1.8V operating max. 3V
Phase Margin, with ideal input signal **with generator E4862A**	> 1UI - 50 ps > 1UI-75 ps
Auxiliary out	Swing: 400 mV pp typ., AC coupled

Sub-frequencies

For applications requiring different frequencies at a fraction of the system clock, the rate can be divided or multiplied by 1, 2 or 4. This influences the dependency between segment length resolution and maximum memory depth (see table 6).

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Table 8: Parameters for Generator Front-ends E4862A 2.67Gbit/s (E4864A 1.33 GHZ)	
Outputs	1, differential or single ended
Impedance	50 Ohm Typ.
Formats	Clock: Duty cycle 50%±10% typ. Data: NRZ, DNRZ
Output voltage window	-2.00 to + 3.00 V 3.00 V to 4.5(terminated to +3V only)
Maximum external voltage	- 2.2 to +4.7 V
External termination voltage	-2V to +3V
Amplitude / Resolution	low voltage CMOS 0.05 to 1.8 Vpp* / 10 mV
Accuracy HiLevel/Amplitude	±2%±10 mV
Short circuit current	72 mA max
Transition times (20%-80%)	90ps typ@ ECL,LVDS 110ps typ @ Vpp max
Overshooting/ringing	20% + 20mV typ
Jitter, Data mode	<50ps peak-to-peak
Clock mode	<5ps, rms

***does double into open, but outputs may switch off.**

Input/Output

Addressable technologies

LVDS, ECL (terminated with 50 to 0 V/-2 V), PECL (terminated to +3 V Analyzer input requires use of a Bias Tee)

Analyzer Input

The analyzer channel can be operated
-single ended normal
-Single ended complement
-differential
For termination there is always 50 Ohm connected to a programmable termination voltage. In differential mode there is additionally a 100 Ohm differential termination selectable. Independantly of the selected termination, one can select if the anaylsis of the incoming signal shall be performed on the input, inverted input or true differentially. For connecting to PECL it is recommended to use a Bias Tee. The 2.7 Gb/s analyzer offers an auxillary output, where the differential input signal is available as a single ended signal. The bandwidth of the Aux Output is limited to 2GHz.

Generator Output

The Generator output can be used single ended or differential. Enable/Disable relays provide on/off switching. Switched off will provide internal termination. It is recommended either to turn off or externally terminate unused outputs.

The Generator outputs can work into 50 Ohm centre tapped termination or 100 Ohm differential termination. The proper termination scheme can be chosen from the editor to adapt proper level programming.

Protection

Input and Output Relays switch off automatically, when maximum voltages will be exceeded.

Compatibility

The E4861A module will work also with front-ends E4864A and E4865A up to 1.35Gb/s.

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Technical specifications 675 MHz

E4832A 675 MHz Generator/Analyzer Module

This module holds any combination of up to two analyzer front-ends (E4835A) and four generator front-ends (E4838A),

Clock Module/Data Mode

The generator can operate in clock mode or data mode. Clock mode is achieved when the generator is assigned as a Pulse Part.
Data mode is achieved with assigning it and data part. In Clock mode there is a fixed duty cycle of type 50%. In data mode there are NRZ,RZ,R1 formats with variable delay. The analyzer works as data part always with variable sampling delay. The sampling delay consists of two elements: the start delay and the fine delay. The fine delay can be varied within ± 1 period without stopping.

Data Capabilities

PRBS/PRWS and memory based data are defined by segments. Segments are assigned to a generator for a stimulating pattern, on an analyzer it defines the expected pattern where the incoming data are compared to. The expected pattern can be setup with mask bits.

The segment length resolution is the resolution to which the length of a pattern segment can be set. The maximum memory per channel of the E4832A can be set in steps of 16 bits up to a length of 2048 Kbit. If the 16-bit segment length resolution is too coarse, memory depth and frequency can be traded as shown in table 12.

Sub-frequencies:
For applications requiring different frequencies at a fraction of the system clock, the ratio can be divided or multiplied by 2,4,8, or 16. This influences the dependency between segment length resolution and maximum memory depth (see table 12).

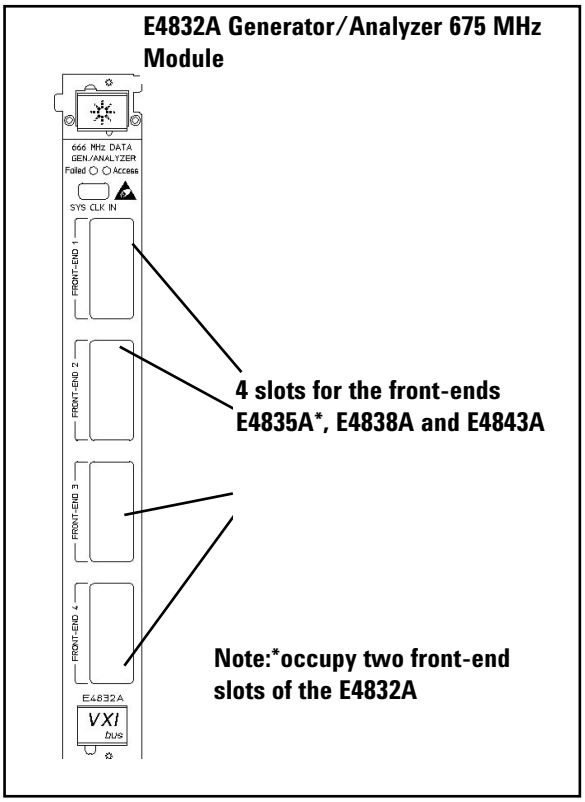


Figure 15: E4832A Module

Table 9: E4832A Data Generator Timing Specifications (@ 50 % of amplitude, 50 Ohm to GND and fastest transition times)	
Frequency range	333.334 kHz to 675 MHz
Delay range	0 to 3.0 µs (not limited by period)
Resolution	2 ps
Accuracy	±50 ps ± 50 ppm relative to the zero-delay Placement *.
Skew	50 ps typ. after deskewing at customer levels
Pulse width	Can be specified as width or % of duty cycle
Range	750ps to [Period-750ps]
Resolution	2 ps
Accuracy	± 200 ps ± 0.1 %.
Duty Cycle	1 % to 99 %, subject to width limits

*Valid at 15...35°C room temperature.

Table 10: E4832A Analyzer Timing All timing parameters are measured at ECL and levels, terminated with 50Ω to GND	
Sample delay:= start delay + fine delay, Fine delay can be changed without stopping**	
Sampling rate*	Same as generator
Fine delay range	±1 period
Sampling delay range	Same as generator
Accuracy	Same as generator
Resolution	Same as generator
Skew	Same as generator

*See tables for frontend deratings

**Conditions: frequency > 20.8 MHz and by using the finest segment length resolution.

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Table 11: Pattern and Sequencing features of E4832A	
Patterns:	
Memory based	up to 2Mbit see table 24
PRBS/PRWS	2^n-1, n=7, 9, 10, 11, 15,
Marker Density	1/8, 1/4, 1/2, 3/4, 7/8 at PRBS/PRWS 2^n-1, n=7, 9, 10, 11,15
Errored	2^n-1, n=7, 9, 10, 11, 15
Extended ones or 0	2^n-1, n=7, 9, 10, 11, 15
Clock patterns	Divide or multiplied by 2, 4, 8, 16
User	Data editor, file import

Table 12: Data rate range, segment length resolution, available memory and fine delay operation

Data rate range Mbit/s	Segment length resolution	Maximum memory depth, bits
20.834...41.666	1 bits	131,008
41.667...83.333	2 bits	262,016
83.334...166.666	4 bits	524,032
166.667...333.333	8 bits	1,048,064
333.334...666.667	16 bits	2,097,152

In general it is possible to set higher values for the segment length resolution and also at lower frequencies than is indicated in the table. In this case the fine delay function and the auto- synchronisation function are unavailable.

Table 13: Level Parameters for Differential Generator Front-end E4838A 667 MHz	
Number of channels	1, differential
Impedance	50 Ohm typ.
Data formats	RZ, R1, NRZ, DNRZ
Output voltage window	-2.2 to +4.4 V (doubles into open up to max. 5 Vpp)
Amplitude / Resolution	0.1V to 3.50 V / 10 mV
Level accuracy	±3 %± 25 mV typ. after 5 ns settling time
@LVDS/(P)ECL	±1 %±25 mV typ. after 5 ns settling time
Variable transition time range (10-90% of amplitude)	0.5 to 4.5 ns
Accuracy @LVDS/(P)ECL (20-80% of amplitude)	±5%±100 ps 0.35 ns typ
Overshoot/ringing	< 7% (< 5% typ).
Jitter Data mode	<100 ps peak to peak ((80ps typ)
Clock mode	8ps rms typ.
Channel addition	XOR and analog

Table 14: Two Differential Analyzer Front-Ends E4835A[1], 667 MSa/s	
Number of channels	2 , differential or single ended (switchable)
Impedance	50 Ohm typ. 100 Ohm differential if termination voltage is switched off
Termination voltage (can be switched off)	-2.0 to + 3.0 V
Threshold voltage range / Threshold accuracy	-2.00 to +4.50 V / ±1%±20mV
Threshold resolution	2 mV
Input sensitivity	Differential 50 mV typ Single-ended 100 mV typ
Minimum detectable pulsewidth	400 ps typ. at ECL levels
Input voltage range	Two ranges selectable: 0 to +5 V and –2 to +3 V
Phase Margin, with ideal input signal **with E4838A Generator**	>1UI- 100ps >1 UI -180 ps

[1] occupy two front-end slots of the E4832A. The E4835A contains two front-ends (E4835AZ) and one common data back end. In this document we refer to one front-end as E4835A.

Input/Output

Addressable technologies

LVDS, (P)ECL, TTL, 3.3 V CMOS

Analyzer Input

The analyzer channel can be operated
-single ended normal
-Single ended complement
-differential

For termination there is always 50 Ohm connected to a programmable termination voltage. In differential mode there is additionally a 100 Ohm differential termination selectable. Independantly of the selected termination, one can select if the anaylsis of the incoming signal shall be performed on the input or inverted input or true differentially.

Generator Output

The Generator output can be used single ended or differential. Enable/Disable realys provide on/off switching. Switched off will provide internal termination. It is recommended either to turn off or externally terminate unused outputs.

The Generator outputs can work into 50 Ohm centre tapped termination or 100 Ohm differential termination. The proper termination scheme can be chosen from the editor to adapt proper level programming.

Compatibility

The E4832A module can also be equipped with E4843A generator front-end.

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Technical specifications 333Mb/s

E4841A 333 Mb/s Generator/Analyzer Module

This module holds any combination of up to four analyzer front-ends (E4847A) and generator front-ends (E4846A). These dual channel front-ends make two channels out of each slot, so eight channels per module. The E4841A is orignally a 667 MHz module, with the use of the dual frontends the maximum data rate is limited to 333 Mb/s. For 675 Mb/s operation the E4832A is recommended.

Segment length resolution:
This is the resolution to which the length of a pattern segment can be set. The maximum memory per channel of the E4841A can be set in steps of 8 bits up to a length of 512 Kbit. If the 8-bit segment length resolution is too coarse, memory depth and frequency can be traded as shown in table 18.

Sub-frequencies:
For applications requiring different frequencies at a fraction of the system clock, the ratio can be divided or multiplied by 2,4,8. This influences the dependency between segment length resolution and maximum memory depth (see table 18).

Using the Analyzer, in error capture mode the memory is half of the value shown. (table 18)

Table 15: E4841A Data Generator Timing Specifications
(@ 50 % of amplitude, 50 Ohm to GND and fastest transition times)

Frequency range*		1.000 kHz to 333.333 MHz
	Delay range	0 to 3.0 s (not limited by period).
		For f < 333.334 kHz" max. delay is 1 period.
	Resolution	2 ps. For f < 170 kHz 0.05% of period
	Accuracy	±50 ps ± 100 ppm relative to the zero delay
		placement. For f < 170 kHz the tolerance increases to +/- 0.1%
	Skew	50 ps typ. after deskewing at customer levels
Pulse width		Can be specified as width or % of duty cycle
	Range*	750ps to [Period-750ps]
	Resolution	2 ps
	Accuracy*	± 200 ps ± 0.1 %
Duty Cycle		1 % to 99 %, subject to width limits

* See tables for front-end deratings

Table 16: E4841A Analyzer Timing All timing parameters are measured at ECL and levels, terminated with 50 Ω to GND

Sampling rate*	Same as generator
Sampling delay range*	Same as generator limited to 1 system period within one front-end.
Accuracy	Same as generator
Resolution	Same as generator
Skew*	Same as generator

*See tables for front-end deratings

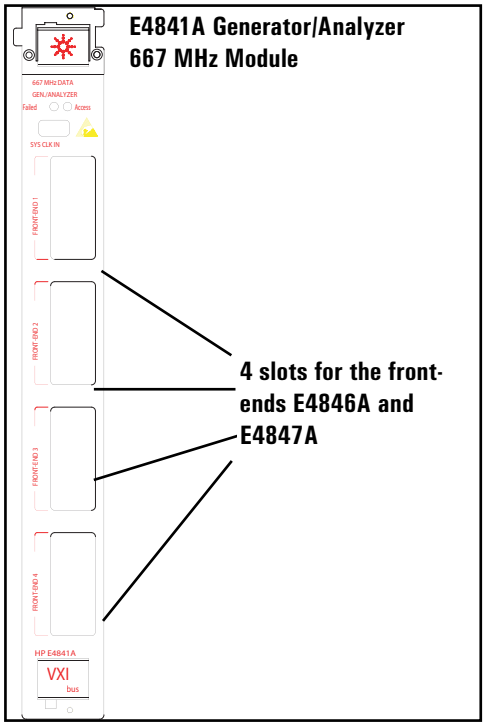


Figure 16

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Table 17: Pattern and Sequencing features of E4841A	
Patterns:	
Memory based	**up to (1Mbit) see table 23**
PRBS/PRWS	2^n-1, n= 7, 9, 10, 11, 15
Clock patterns	Divide or multiplied by 2, 4, 8, (16)
User	Data editor, file import

Table 18: Data rate range, segment length resolution, available memory for synchronisation and fine delay operation

Data rate range Mbit/s	Segment length resolution	Maximum memory depth, bits
20.834...41.666	1 bits	65,504
41.667...83.333	2 bits	131,008
83.334...166.666	4 bits	262,016
166.667...333.333	8 bits	524,032

In general it is possible to set higher values for the segment length resolution at lower frequencie than is indicated in the table

Table 19: Level Parameters for dual Generator Front-End E4846A 200 Mbit/s

	E4846A
Outputs/Source Resistance	2, single-ended 50 Ohm
Maximum Frequency (and Data Formats)	200 Mbit/s (NRZ, DNRZ)
Output Voltage Window	-1.75 to +3.50 V doubles into open)
Addressable Technologies	TTL, ECL (terminated with 50Ω to 0 V/-2 V), PECL (terminated to + 3 V)
Amplitude/Resolution	0.30 to 3.50 Vpp / 10 mV doubles into open)
Accuracy	Levels: ± 5% ± 100 mV
Short Circuit Current	+70 mA max., -35 mA max.
Maximum External Voltage and Termination Voltage Range	-2 to +5 V
Transition Times **20-80% at ECL levels** **10-90% at 2.5 Vpp ampl**	Constant slew rate < 1.2 ns, 700 ps typ. < 2.5 ns, 1.8 ns typ.
Overshoot/Ringing **Droop**	< 5% + 120 mV 2.5 Vpp < 20%, ECL < 10%
Minimum Pulsewidth	ECL: < 1.5 ns, 1 ns typ. 2.5 Vpp: < 4.0 ns, 3 ns typ.

Table 20: Parameters for Analyzer Front-End E4847A 333 MSa/s, dual channel

Analog Bandwidth	**350 MHz typ.**
Number of Channels	**2, independent levels**
Typical Impedance	**50 Ω /10 k Ω parallel < 5 pF**
Termination Voltage	**-2.1 to +3.1 V (50 Ω selected)**
Number of Thresholds	**one per input**
Threshold Voltage Range (into 50 Ω)	**-2.10 to +5.10 V**
Threshold Resolution	**5 mV**
Threshold Accuracy	**±20 mV ± 1%**
Input Sensitivity	**200 mVpp**
Minimum Detectable Pulsewidth	**1 ns typ. at ECL levels**

Input/Output

Addressable technolgies TTL, 3.3V CMOS, (P)ECL

Analyzer Output
-single-ended
-50 Ohm
-High impedence (10K)

The sampling point of the dual channel analyzer input can be individually adjusted within one system period.

Generator output
-single ended outputs
-enable/disable realais

The Delay range of the two channels within one front-end can be sued over the full range. The output can be use into 50 Ohm or open. Into open the voltage range doubles

Compatibilty

The E4841A can be used with E4843A, E4844A, E4837A, front-ends up to 667MHz with up to 1 meg of memory.

I/O Pin Stimulation/Measurement

The E4847A high-impedance analyzer front-end assists measurements on bidirectional ports. In parallel with a generator front-end, the impedance presented to the pin is 50 Ω. A SMA tee connector 15440A (4 Parts) is required.

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Module Descriptions

Each system consists of at least one clock module (E4805B) or clock and data generator module (E4831A), which generates the system clock and at least one 667 MHz generator/ analyzer module (E4832A) or one 2.67 GHz generator/analyzer module (E4861A) which houses the front-ends. The module E4831A is intended for generator only systems.

E4805B Central Clock Module/E4831A Clock and Data Generator Module

The E4805B and E4831A include a PLL (Phase-Lock-Loop) frequency generator to provide a system clock. Depending on the frequency chosen the data module E4841A can be clocked at a ratio of 1,2,4, or 16 times higher or lower than the system clock.

External start/stop: The E4805B can be started, stopped or gated on the selected active input level. With the E4861A there is only start mode.

Ext. Clock/Ext. Reference: This input runs 81200 synchronously with an ext. clock, or when a more accurate reference is needed than the internal oscillator. Usage of a continuous clock is necessary. Burst clock cannot be used as an external clock. Maximum external clock is 2.67 GHz. (Note: no improvement of jitter specifications will be achieved).

Guided deskew: Individual semi-automatic deskew per channel. The deskew probe E4805B #003 allows deskew on the DUT's (Device Under Test) pins with the DUT connected. Deskew range is 20ns.

Interaction with External Environment (Instruments and DUTs) (only with the E4805B 667 MHz Central Clock Module):
The Agilent 81200 can react on user-defined events, which can result simply in a trigger pulse, for example, but also in a change of the pattern sequence, for details see table 14.

Table 21: E4805B Central Clock Specifications

Frequency range{1} **(can be entered as period or frequency)**	1 kHz to 666.66700 MHz. E4861A will run with Clock module in range of 333 MHz to 2.67GHz, E4832A in range of 333 kHz to 667 MHz. {2}
Resolution	1 Hz
Accuracy	±50 ppm with internal PLL reference

{1} May be limited by modules or front- ends
{2} Up to 667 MHz the resolution is 1 Hz
From 667 MHz to 1.3 Gb/s the resolution is 2 Hz.
From 1.3 Gb/s the resolution is 4 Hz

Table 22: External input and ext. clock/ext. ref. Input of E4805B

Zin/Termination voltage	50 Ω /-2.10 V to 3.30 V	
Sensitivity/max levels	400 mVpp /-3 V to + 6 V	
Coupling		
Ext. Input:	dc, -1.40 V to +3.70 V	
Ext. Clock/Ext. Ref:	ac	
Input transitions/slope	< 20 ns. Ext. Input active edge is selectable	
Input frequency/period:		
Ext. Clock	170 kHz – 2.67 GHz	
Ext. Ref	1*, 2*, 5, or 10 MHz	
Required duty cycle	50 ±10 %	
Latency (typical):	to trigger Output	to channel output
Ext. input	16ns ±1 clock**	46ns ±1 clock**
Ext. clock	15ns	45ns
Ext .clock Input multiplier	1,2....255 Add 3ns if an expander frame is used	

*Jitter performance may be degraded

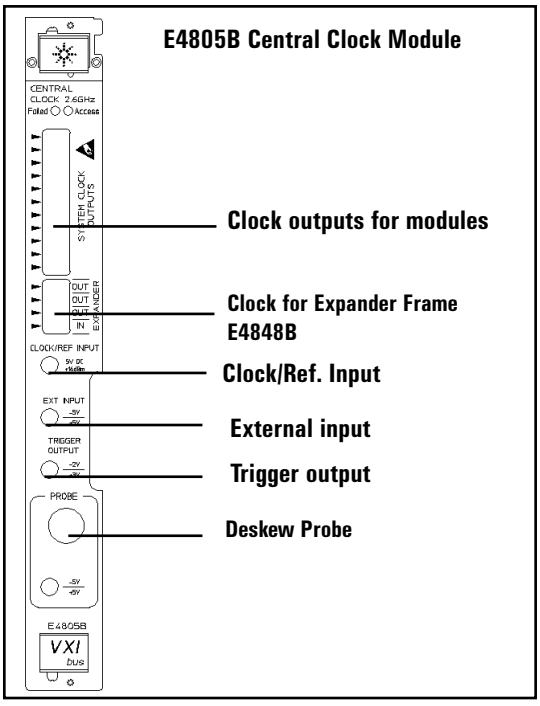


Figure 17:

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Table 23: Trigger output characteristics E4805B	
Trigger output signals	Clock mode or sequence mode (up to 667 MHz). In sequence mode the pulse can be set to mark the start of any segment.
Output impedance	50 Ω
Output level	TTL (frequency < 180 MHz), 1 V to GND, ECL 50 Ω to GND/-2 V, PECL 50 Ω to +3V
Trigger advance	30 ns typ. between trigger output and data output/ sampling point (delay set to zero in both cases)
Maximum input voltage	-2 V to +3.3 V
Jitter (int. reference/int. clock, measured at TRIGGER OUTPUT)	< 10 ps rms (typ. 5ps)

Table 24: : E4805B Sequencing	
Number of Segments	1 to 30 (every segment looped once) 1 to 60 (no segment looped)
Looping levels	Up to 4 nested loops plus one optional infinite loop Loops can be set independently from 1 to 2^{20} repetitions
Start/stop	External input, manual, programmed
Event handling	React on internal and external events. Details see table 13

Table 25: Event handling for E4805B	
Usage on events	**Description**
Stop & Go of data sequences:	Very useful for production tests during interaction with other test equipment
Data segment switching:	Based on the events. Certain portions of the overall sequence can be executed.
Trigger external devices:	External instruments like an oscilloscope can be triggered, e.g. to sample a waveform or an error location.
ATE integration:	The 81200 is started from an ATE platform like an IC test system for complementing missing tester functionalities. The result; pass/fail information is returned back to the ATE platform.
Match loop:	Repetition of a data segment as long as a defined event occurs. Useful for device synchronization, e.g. PLL-based device.
Event trigger sources Events can be defined as any combination of the following sources. A maximum of 10 events can be defined.	
• E4805B option 002 8-line trigger input pod for TTL signals	
• VXI trigger lines T0 and T1	
• Any capture error/or no error detected by one of the analyzer channels	
• Software command control: an event trigger command issued locally or remotely	
Reactions to an event can be set per data segment immediately or deferred and can be any combination of:	
• Data segment jump	
• Launch trigger pulse to the trigger output of the E4805B Central Clock Module	
• VXI trigger lines T0 and T1 can be set to 01, 10 or 11	

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General Characteristics

Mainframes: See table 34.

Save/recall: Pattern segments, settings and complete settings plus segments can be saved and recalled. The number of settings that can be stored is limited only by internal disk space.

Vector import/export: Pattern files can be imported/exported via a 3.5 inch floppy disk, LAN or GP-IB (IEEE 488.2). File format is ASCII using a STIL subset.

Programming interface: GP-IB (IEEE 488.2) and LAN. The interface to applications such as C, Visual Basic, or VEE must be installed. Agilent 81200 Plug & Play drivers for easy programming are available.

Programming language: SCPI 1992.0

Programming times: Vector transfer from memory to hardware depends on the amount of data. Also see table 26.

On-line help: Context-sensitive.

Print-on-demand: Getting started and programming guides can be printed from .pdf files included in the 81200 software.

Self-test: Module and system self-tests can be initiated.

Modules

Module size: VXI C-size, 1 slot.

Module type: Register-based; requires 81200 user software E4873A supplied with the mainframes.

Weight: (including front-ends) Net: 2kg.

Shipping: 2.5 kg.

Warranty: 3 years.

Re-calibration period: 3 years recommended.

Agilent Technologies Quality Standards
The 81200 is produced to the ISO 9001 international quality system standard as part of Agilent Technologies commitment to continually increase customer satisfaction through improved quality control.

Table 26: Programming Times of the 81200

	Programming time
Change of levels	6 ms typ.
Change of delay	16 ms.typ. Not applicable in run mode.
Change of period	60 mstyp. For one E4805B with one E4832A. Not applicable in run mode. Increases with the number of modules but less than proportional.
Stop + start	32 ms typ
Download values: System with 4 channels, 100,000 bit each	< 1.5 s typ
System with 120 channels, 1Mbit each	< 30 s typ
System with 40 channels,	< 10 s typ

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Table 27: General Mainframe Characteristics

	E4849C mainframe	E4848B expander frame
Factory-installed items	E8403A 13-slot VXI C-size frame, One of the Controller options: • #012 VXI 2-slot-PC E9851A with additional 64 MB memory (total 128 MB) with Windows NT 4.0, E4873A Agilent 81200 UserSoftware installed • #013 IEEE 1394 PC link to VXI (E8491B) with installation Licence & CD-ROM of E4873A 81200 User Software	E8403A 13-slot VXI C-size frame, E1482B VXI bus extender module, 1 meter MXI and INTX cable
Number of slots for 81200 modules	11 (for controller option 012) 12 (for controller option 013) (subtract 1 if expander frame is connected)	12
Operating temperature	10 °C to 40 °C	
Storage temperature	-20°C to +60°C	
Humidity	80% rel. humidity at 40 °C	
Power requirements	90-264 Vac, ±10%, 47-66 Hz , 90-264 Vac, ±10%, 300-440 Hz (not recommended, leakage current may exceed safety limits @ > 132 Vac)	
Power available for modules	950 W for 90-110 Vac supplies 1000 W for 110-264 Vac supplies	
Electromagnetic compatibility	EN 55011/CISPR 11 group 1, class A + 21 dB	
Acoustic noise	48 (56) dBA sound pressure at low (high) fan speed	
Safety	IEC 348, UL1244, CSA 22.2 #231, CE-mark	
Physical dimensions	W: 424.5 mm H: 352 mm D: 631 mm	
Weight (Net)	26.8 kg	25.3 kg
Weight (shipping)(max.)	72 kg	67 kg

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Table 28:

	DC Volts	+24V	+12V	+5V	-2V	-5.2V	-12V
Modules (These specifications take already the power specifications of the front-ends into account)							
E4805B Central Clock Module	DC Current	0.15A	0.2A	1.8A	1.4A	3.8A	0.2A
	Dynamic Current	0.015A	0.02A	0.18A	0.14A	0.38A	0.02A
E4861A 2.67 Gb/s Gen./An. Module	DC Current	0.10A	0.50A	5.20A	1.80A	4.00A	0.90A
	Dynamic Current	0.01A	0.05A	0.52A	0.18A	0.40A	0.09A

Note: For the module E4841A and E4832A the power specifications of the chosen front-ends E4846A, E4847A, E4835A or E4838A have to be added to the power specifications of the E4841A and E4832A module to get the overall value of the power specifications

E4841A 667 MHz Gen./An. Module	DC Current		0.03A	2.90A	0.85A	4.20A	0.04A
	Dynamic Current		0.003A	0.290A	0.085A	0.420A	0.004A
E4832A 667 MHz Gen./An. Module	DC Current	0.10A	0.10A	2.60A	0.60A	3.60A	0.10A
	Dynamic Current	0.010A	0.01A	0.26A	0.06A	0.36A	0.01A
Front-Ends							
E4835A Two Differential Analyzer 667 Msa/s	DC Current		0.2A	1.2A	0.2A	0.3A	0.3A
	Dynamic Current		0.02A	0.12A	0.02A	0.03A	0.03A
E4838A Differential Generator 667 MHz, var. Slopes	DC Current		0.45	0.18	0.07	0.38	0.41
	Dynamic Current		0.045	0.018	0.007	0.038	0.041
E4846A 200 Mbit/s Dual Generator	DC Current		0.210A	0.025A	0.050A	0.120A	0.300A
	Dynamic Current		0.021A	0.003A	0.005A	0.0120A	0.030A
E4847A 333 MSa/s Dual Analyzer	DC Current		0.1A	0.9A	0.06A	0.05A	0.06A
	Dynamic Current		0.01A	0.09A	0.006A	0.005A	0.006A

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Table 29: Cooling requirements for the modules E4805B and E4861A with the front-ends installed

Modules	ΔP mm H_2O for 10°C rise	Air Flow Liter/s
E4805B	0.25	3.6
E4861A	0.4	5.2

Table 30: Cooling requirements for the module E4841A with the front-ends installed

Module	ΔP mm H_2O for 15°C rise	Air Flow Liter/s
E4841A	0.3	4.5
E4832A	0.3	4.7

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Related Literature	Pub. Number
Agilent 81200 Data Generator/Analyzer Platform, brochure	5980-0488E
Agilent 81200 Data Generator/Analyzer Platform configuration guide	5965-3417E
Agilent E4839A Test Fixture	5968-3580E
How to transfer Data between Design, Simulation and the Agilent 81200 Data Generator Analyzer	5968-6276E
Flat Panel Display Link Test	5968-8028E
How to Use the Agilent Data Generator/Analyzer Platform Together with VEE for signal Integrity Analysis	5968-3857E
Agilent 81200 Data Generator/Analyzer Platform, Start up Assistance	5980-2640E

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