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- Press the following keys:

[System Utility]
[MORE]
[SERVICE TESTS]
[ADJUSTMTS]
[ADC ADJUSTMNT]
[OFFSET]

Wait for the analyzer to set up the adjustment. The analyzer is ready when the adjustment message appears on the screen.

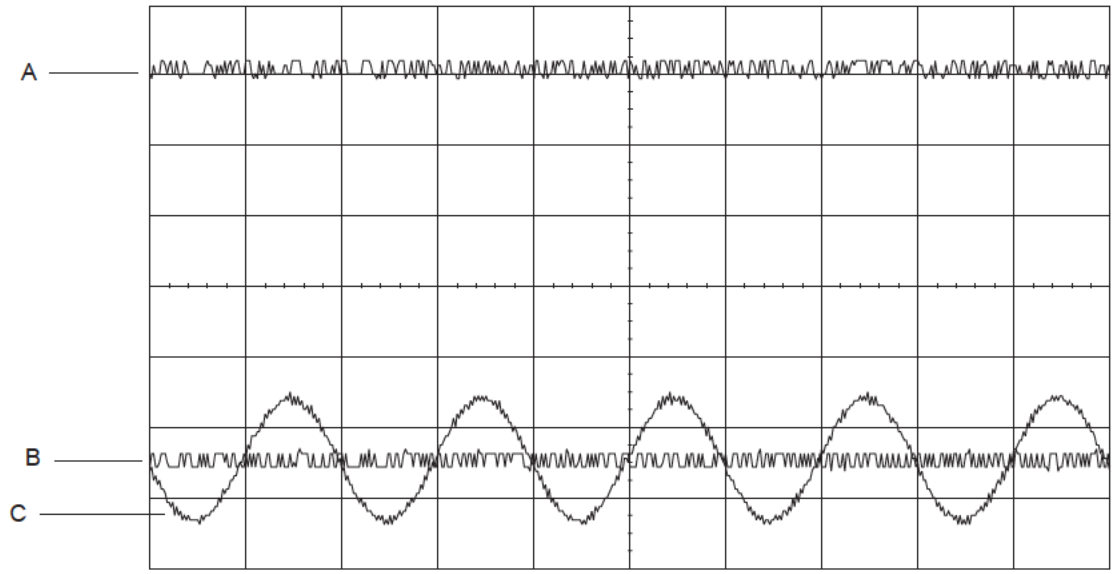
- If the oscilloscope display looks like the following figure, go to step 17.

The following describes the signals shown on the oscilloscope display:

''A'' A straight, horizontal trace in the upper half of the display.

''B'' A "noisy" flat trace at the center of the sine wave trace.

''C'' A clean sine wave in the lower half of the display.



R431 and R405 Correctly Adjusted

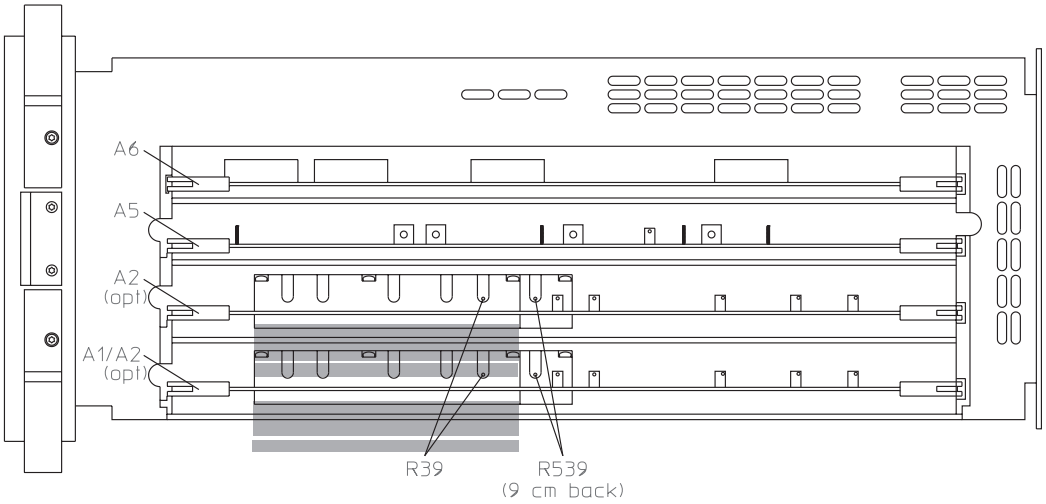
- If trace ''B'' is not flat, adjust A5 R431.
- If trace ''C'' is not centered over trace ''B,'' adjust A5 R405.
- Set the power switch to off (O).
- Disconnect the jumper from A5 TP8 and A5 TP300. Reconnect the cable to A5 P4.

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To adjust the input dc offset

This procedure minimizes the residual dc response of the A1/A2 Input assemblies. The standard two channel analyzer has one A1 Input assembly. The optional four channel analyzer has two A2 Input assemblies: channel 1 and 3 are routed to the A2 Input assembly in the lower slot and channel 2 and 4 are routed to the A2 Input assembly in the upper slot.

Equipment Required: None



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- For the standard two channel analyzer, do the following to adjust input dc offset:
  - **Set the power switch to on (l).**
  - **Press the following keys:**

    [System Utility]
    [MORE]
    [SERVICE TESTS]
    [ADJUSTMTS]
    [CHANNEL 1 ADJUSTMNT]
    [OFFSET]

    Wait for the analyzer to set up the adjustment. The analyzer is ready when the adjustment message appears on the screen.
  - **Adjust A1 R39 for a Y: reading of 90 dBVrms or less.**
  - **Press the following keys:**

    [Rtn]
    [CHANNEL 2 ADJUSTMNT]
    [OFFSET]

    Wait for the analyzer to set up the adjustment. The analyzer is ready when the adjustment message appears on the screen.
  - **Adjust A1 R539 for a Y: reading of 90 dBVrms or less.**

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❑ For the optional four channel analyzer, do the following to adjust input dc offset:

- **Set the power switch to on (|).**
- **Press the following keys:**

  [System Utility]
  [MORE]
  [SERVICE TESTS]
  [ADJUSTMTS]
  [CHANNEL 1 ADJUSTMNT]
  [OFFSET]

  Wait for the analyzer to set up the adjustment. The analyzer is ready when the adjustment message appears on the screen.
- **Adjust A2 R39 in the lower slot for a Y: reading of 90 dBVrms or less.**
- **Press the following keys:**

  [Rtn]
  [CHANNEL 2 ADJUSTMNT]
  [OFFSET]

  Wait for the analyzer to set up the adjustment. The analyzer is ready when the adjustment message appears on the screen.
- **Adjust A2 R39 in the upper slot for a Y: reading of 90 dBVrms or less.**
- **Press the following keys:**

  [Rtn]
  [CHANNEL 3 ADJUSTMNT]
  [OFFSET]

  Wait for the analyzer to set up the adjustment. The analyzer is ready when the adjustment message appears on the screen.
- **Adjust A2 R539 in the lower slot for a Y: reading of 90 dBVrms or less.**
- **Press the following keys:**

  [Rtn]
  [CHANNEL 4 ADJUSTMNT]
  [OFFSET]

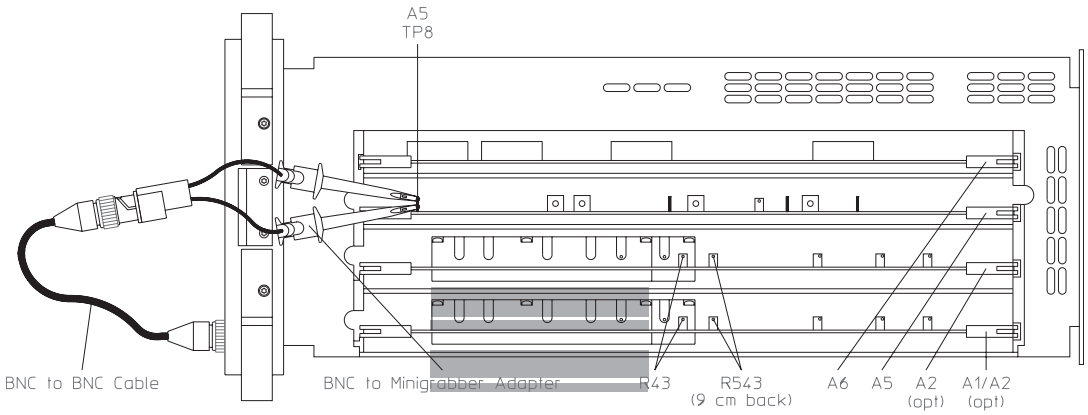
  Wait for the analyzer to set up the adjustment. The analyzer is ready when the adjustment message appears on the screen.
- **Adjust A2 R539 in the upper slot for a Y: reading of 90 dBVrms or less.**

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To adjust common mode rejection

This procedure optimizes the common mode rejection of the A1/A2 Input assemblies. The standard two channel analyzer has one A1 Input assembly. The optional four channel analyzer has two A2 Input assemblies: channel 1 and 3 are routed to the A2 Input assembly in the lower slot and channel 2 and 4 are routed to the A2 Input assembly in the upper slot.

Equipment Required: BNC-to-BNC Cable
BNC(f)-to-Minigrabber Adapter



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❑ For the standard two channel analyzer, do the following to adjust common mode rejection:

- **Set the power switch to off (O).**
- **Connect the BNC(f)-to-minigrabber adapter to the BNC cable. Connect both minigrabber clips (signal and ground) to A5 TP8 and the BNC connector to the analyzer's CH 1 connector.**
- **Set the power switch to on (I).**
- **Press the following keys:**

  [System Utility]
  [MORE]
  [SERVICE TESTS]
  [ADJUSTMTS]
  [CHANNEL 1 ADJUSTMNT]
  [CMRR]

  Wait for the analyzer to set up the adjustment. The analyzer is ready when the adjustment message appears on the screen.
- **While monitoring the Y: value, adjust A1 R43 for a minimum marker value.**
- **Disconnect the BNC cable from the analyzer's CH 1 connector and connect to the CH 2 connector.**
- **Press the the following keys:**

  [Rtn]
  [CHANNEL 2 ADJUSTMNT]
  [CMRR]

  Wait for the analyzer to set up the adjustment. The analyzer is ready when the adjustment message appears on the screen.
- **While monitoring the Y: value, adjust A1 R543 for a minimum marker value.**

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- For the optional four channel analyzer, do the following to adjust common mode rejection:
  - **Set the power switch to off (O).**
  - **Connect the BNC(f)-to-minigrabber adapter to the BNC cable. Connect both minigrabber clips (signal and ground) to A5 TP8 and the BNC connector to the analyzer's CH 1 connector.**
  - **Set the power switch to on (I).**
  - **Press the following keys:**

    [System Utility]
    [MORE]
    [SERVICE TESTS]
    [ADJUSTMTS]
    [CHANNEL 1 ADJUSTMNT]
    [CMRR]

    Wait for the analyzer to set up the adjustment. The analyzer is ready when the adjustment message appears on the screen.
  - **While monitoring the Y: value, adjust A2 R43 in the lower slot for a minimum marker value.**
  - **Disconnect the BNC cable from the analyzer's CH 1 connector and connect to the CH 2 connector.**
  - **Press the the following keys:**

    [Rtn]
    [CHANNEL 2 ADJUSTMNT]
    [CMRR]

    Wait for the analyzer to set up the adjustment. The analyzer is ready when the adjustment message appears on the screen.
  - **While monitoring the Y: value, adjust A2 R43 in the upper slot for a minimum marker value.**
  - **Disconnect the BNC cable from the analyzer's CH 2 connector and connect to the CH 3 connector.**
  - **Press the the following keys:**

    [Rtn]
    [CHANNEL 3 ADJUSTMNT]
    [CMRR]

    Wait for the analyzer to set up the adjustment. The analyzer is ready when the adjustment message appears on the screen.

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- **While monitoring the Y: value, adjust A2 R543 in the lower slot for a minimum marker value.**
- **Disconnect the BNC cable from the analyzer's CH 3 connector and connect to the CH 4 connector.**
- **Press the the following keys:**

  [Rtn]
  [CHANNEL 4 ADJUSTMNT]
  [CMRR]

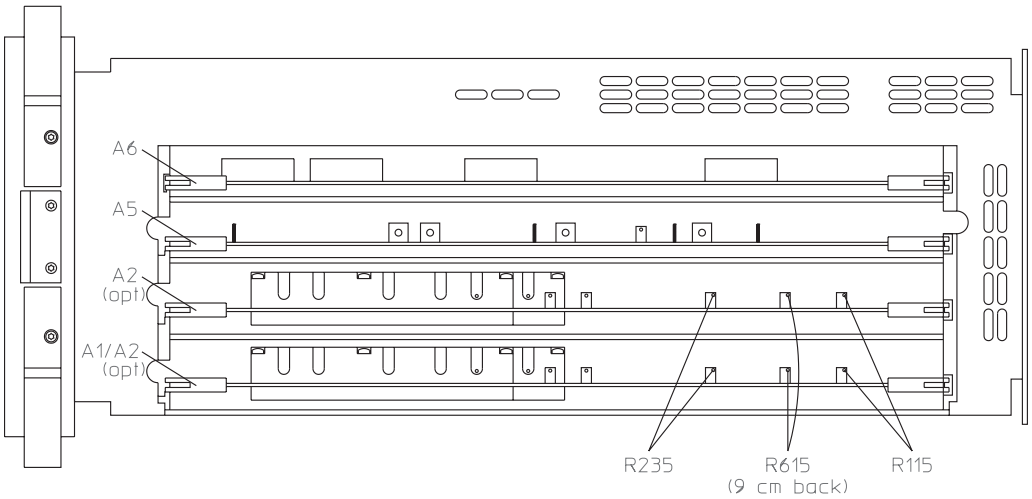
  Wait for the analyzer to set up the adjustment. The analyzer is ready when the adjustment message appears on the screen.
- **While monitoring the Y: value, adjust A2 R543 in the upper slot for a minimum marker value.**
- **Set the power switch to off (O) and disconnect the minigrabber clips from A5 TP8.**

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To adjust filter flatness

This procedure adjusts the anti-alias filter on the A1/A2 Input assemblies. The standard two channel analyzer has one A1 Input assembly. The optional four channel analyzer has two A2 Input assemblies: channel 1 and 3 are routed to the A2 Input assembly in the lower slot and channel 2 and 4 are routed to the A2 Input assembly in the upper slot.

Equipment Required: None



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❑ For the standard two channel analyzer, do the following to adjust filter flatness:

- **Set the power switch to on (|).**
- **Press the following keys:**

  [System Utility]
  [MORE]
  [SERVICE TESTS]
  [ADJUSTMTS]
  [CHANNEL 1 ADJUSTMNT]
  [50 kHz]

  Wait for the analyzer to set up the adjustment. The analyzer is ready when the adjustment message appears on the screen.
- **While monitoring the Yr: value, adjust A1 R115 for a marker value of 0 0.1 dB.**
- **Press the [100 kHz FLATNESS] softkey.**

  Wait for the analyzer to set up the adjustment. The analyzer is ready when the adjustment message appears on the screen.
- **While monitoring the Yr: value, adjust A1 R235 for a marker value of 0 0.1 dB.**
- **Press the following keys:**

  [Rtn]
  [CHANNEL 2 ADJUSTMNT]
  [50 kHz FLATNESS]

  Wait for the analyzer to set up the adjustment. The analyzer is ready when the adjustment message appears on the screen.
- **While monitoring the Yr: value, adjust A1 R615 for a marker value of 0 0.1 dB.**

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❑ For the optional four channel analyzer, do the following to adjust filter flatness:

- **Set the power switch to on (|).**
- **Press the following keys:**

  [System Utility]
  [MORE]
  [SERVICE TESTS]
  [ADJUSTMTS]
  [CHANNEL 1 ADJUSTMNT]
  [25 kHz]

  Wait for the analyzer to set up the adjustment. The analyzer is ready when the adjustment message appears on the screen.
- **While monitoring the Yr: value, adjust A2 R115 in the lower slot for a marker value of 0 ±0.1 dB.**
- **Press the [50 kHz FLATNESS] softkey.**

  Wait for the analyzer to set up the adjustment. The analyzer is ready when the adjustment message appears on the screen.
- **While monitoring the Yr: value, adjust A2 R235 in the lower slot for a marker value of 0 ±0.1 dB.**
- **Press the following keys:**

  [Rtn]
  [CHANNEL 2 ADJUSTMNT]
  [25 kHz FLATNESS]

  Wait for the analyzer to set up the adjustment. The analyzer is ready when the adjustment message appears on the screen.
- **While monitoring the Yr: value, adjust A2 R115 in the upper slot for a marker value of 0 ±0.1 dB.**
- **Press the [50 kHz FLATNESS] softkey.**

  Wait for the analyzer to set up the adjustment. The analyzer is ready when the adjustment message appears on the screen.
- **While monitoring the Yr: value, adjust A2 R235 in the upper slot for a marker value of 0 ±0.1 dB.**

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- **Press the following keys:**

  [Rtn]
  [CHANNEL 3 ADJUSTMNT]
  [25 kHz FLATNESS]

  Wait for the analyzer to set up the adjustment. The analyzer is ready when the adjustment message appears on the screen.
- **While monitoring the Yr: value, adjust A2 R615 in the lower slot for a marker value of 0 0.1 dB.**
- **Press the following keys:**

  [Rtn]
  [CHANNEL 4 ADJUSTMNT]
  [25 kHz FLATNESS]

  Wait for the analyzer to set up the adjustment. The analyzer is ready when the adjustment message appears on the screen.
- **While monitoring the Yr: value, adjust A2 R615 in the upper slot for a marker value of 0 0.1 dB.**

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To adjust the display voltage

This procedure adjusts the A102 DC-DC Converter assembly's display voltage to match the voltage required by the A101 Display assembly. This adjustment is only required when the DC-DC Converter assembly or the Display assembly is replaced.

Equipment Required: Multimeter

Warning

The display voltage is +210 Vdc 10 Vdc nominal. Use caution when performing this adjustment to avoid personal injury.

- **Set the power switch to off (O).**
- **Record the V(ALL ON): voltage.**

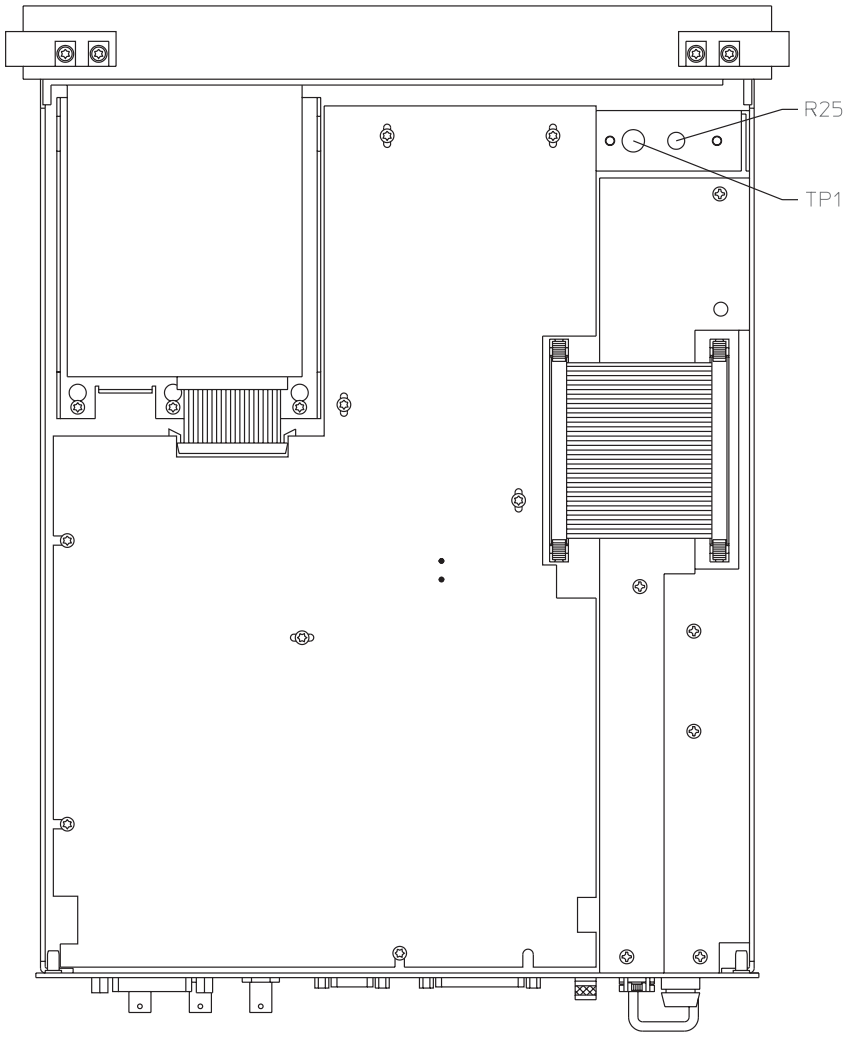
The V(ALL ON): voltage is printed on a sticker on the component side of the Display assembly. The V(ALL ON): voltage is normally between +200 Vdc and +220 Vdc.

Caution

Do not adjust the display voltage above +230 Vdc. The Display assembly can be damaged if the voltage is adjusted above +230 Vdc.

- **Turn A102 R25 clockwise to its stop.**
- **Set the multimeter to a range greater than 220 Vdc and connnect to A102 TP1 using a shielded test clip.**
- **Set the power switch to on (l).**
- **Using a non-metalic flat-edge adjustment tool, adjust A102 R25 for the voltage recorded in step 2.**
- **Set the power switch to off.**

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6

Replacing Assemblies

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Replacing Assemblies

This chapter tells you what to do before and after you replace an assembly and shows you how to disassemble the analyzer.

Warning

Disconnect the power cord from the rear panel before disassembly or assembly of the Agilent 35670A.

Even with power removed, there can be sufficient stored energy in some circuits to cause personal injury. These voltages will discharge to a relatively safe level approximately five seconds after the power cord is disconnected.

Caution

Do not connect or disconnect cables from circuit assemblies with the line power turned on (|).

To protect circuits from static discharge, remove or replace assemblies only at static-protected work stations.

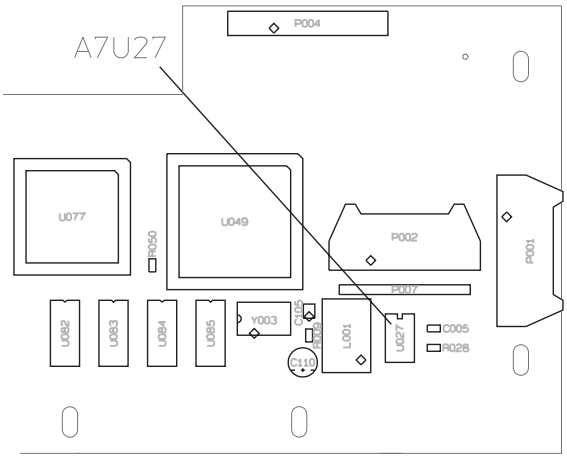
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What to do before replacing the CPU assembly

The analyzer's serial number and firmware options are stored in EEPROM (U27) on the A7 CPU assembly. Before replacing the CPU assembly, remove A7 U27 from the faulty assembly and insert into the new assembly.

Caution

All firmware options will be lost if A7 U27 is not removed from the faulty assembly and inserted into the new assembly.



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What to do after replacing an assembly

- **Reinstall all assemblies and cables that were removed during troubleshooting.**
- **Do the required adjustments listed in the following table.**
- **Do the self test, page 4-31.**
- **Do the required performance tests listed in the following table.**

Assembly Replaced	Required Adjustment	Required Performance Test
A1 Input	ADC gain, offset and reference, page 5-7 Input dc offset, page 5-10 Common mode rejection, page 5-13 Filter flatness, page 5-17	DC offset Noise Spurious signals Amplitude accuracy Flatness Amplitude linearity A-weight filter Channel match ICP supply
A2 Input	ADC gain, offset and reference, page 5-7 Input dc offset, page 5-10 Common mode rejection, page 5-13 Filter flatness, page 5-17	DC offset Noise Spurious signals Amplitude accuracy Flatness Amplitude linearity A-weight filter Channel match ICP supply
A5 Analog	Source, page 5-6 ADC, page 5-7 Input dc offset, page 5-10	DC offset Noise Spurious signals Amplitude accuracy Flatness Amplitude linearity Channel match Single channel phase accuracy External trigger Source amplitude accuracy Source flatness Source distortion
A6 Digital		Source amplitude accuracy Source dc offset Source flatness

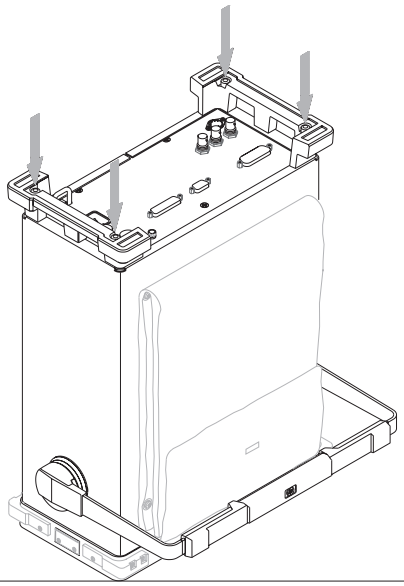
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Assembly Replaced	Required Adjustment	Required Performance Test
A7 CPU	Frequency reference, page 5-5	Frequency accuracy
A8 Memory		
A9 NVRAM		
A10 Rear Panel		Tach function (option 1D0 only) External trigger
A11 Keyboard Controller		
A12 BNC		
A13 Primary Keypad		
A14 Secondary Keypad		
A22 BNC		
A90 Fan		
A98 Power Supply		
A99 Motherboard		
A100 Disk Drive		
A101 Display	Display voltage, page 5-21	
A102 DC-DC Converter	Display voltage, page 5-21	

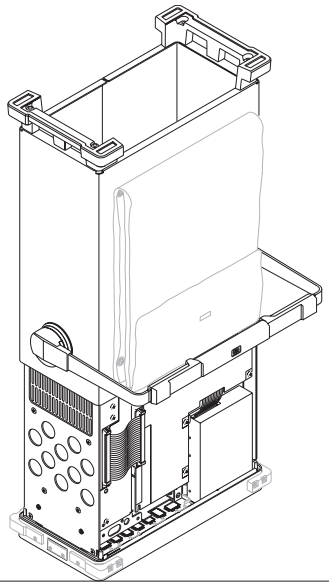
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To remove cover

1 Place the analyzer on its front panel. Using a 4 mm hex driver, loosen the four corner screws.



2 Slide the cover straight up.

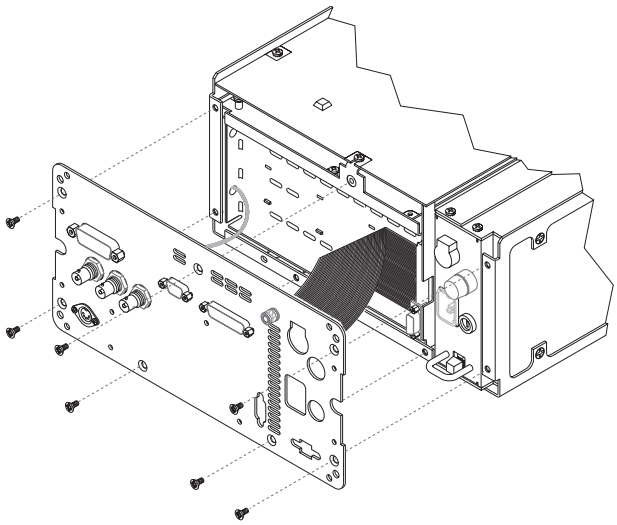


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To remove rear panel

1 Remove cover (see ‘’To remove cover’’).

2 Using a T-15 torx driver, remove the seven screws from the rear panel. Pull the rear panel straight off.



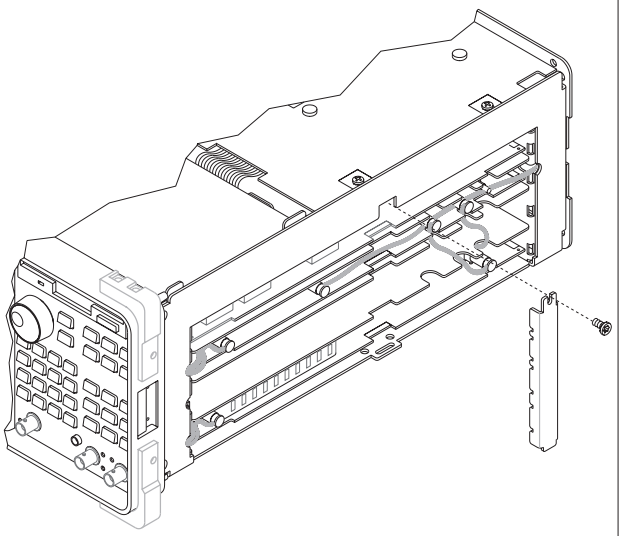
3 Disconnect the ribbon cable and the coaxial cable from the A10 Rear Panel assembly.

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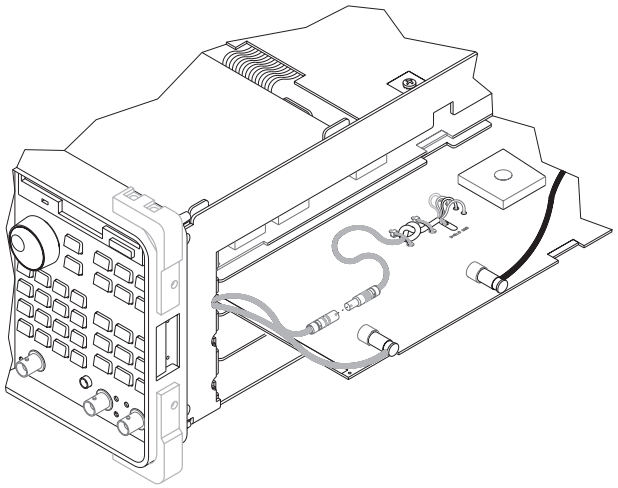
To remove front panel

1 Remove cover (see ''To remove cover'').

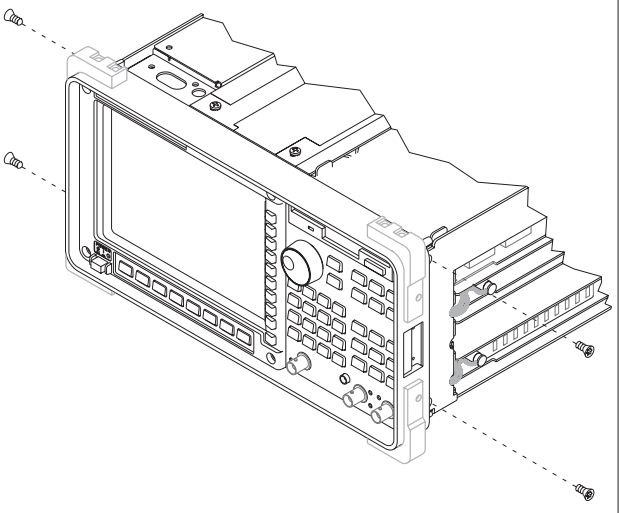
2 Remove assembly retainer bracket.



3 Slide A5 Analog assembly part way out and disconnect gray mic cable.



4 Using a T-15 torx driver, remove the two screws on each side of the front panel.



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5 Pull the top of the front panel out of the frame.

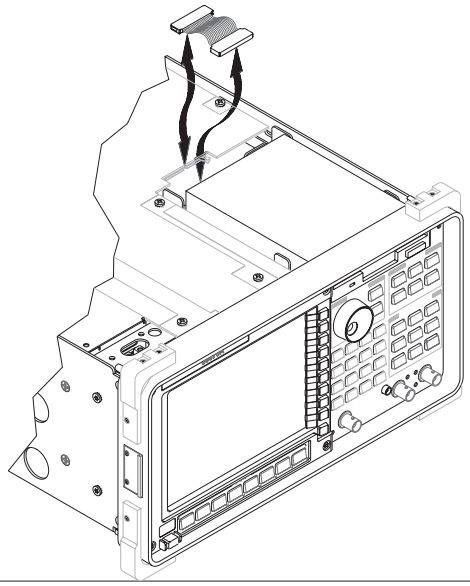
6 Disconnect the ribbon cables from the front panel. Disconnect the coaxial cables connected to the A12/A22 BNC assembly.

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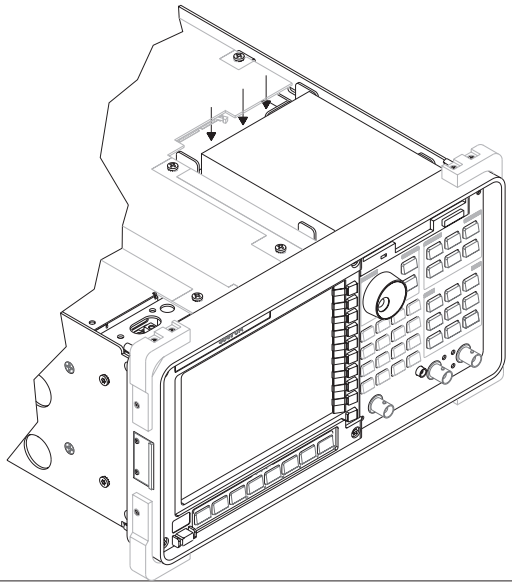
To remove disk drive

1 Remove cover (see ‘’To remove cover’’).

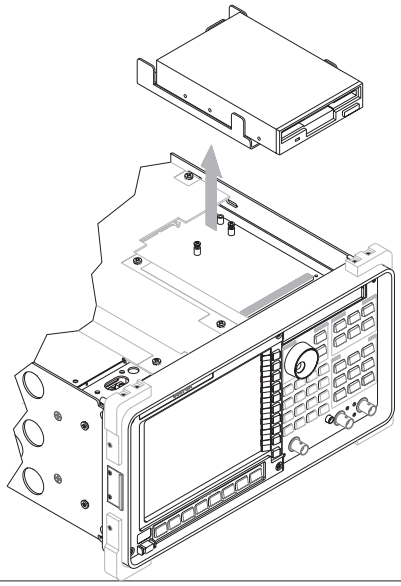
2 Disconnect the disk drive cable.



3 Using a T-10 torx driver, loosen the three screws at the back of the disk drive bracket.



4 Slide the disk drive back and lift up.

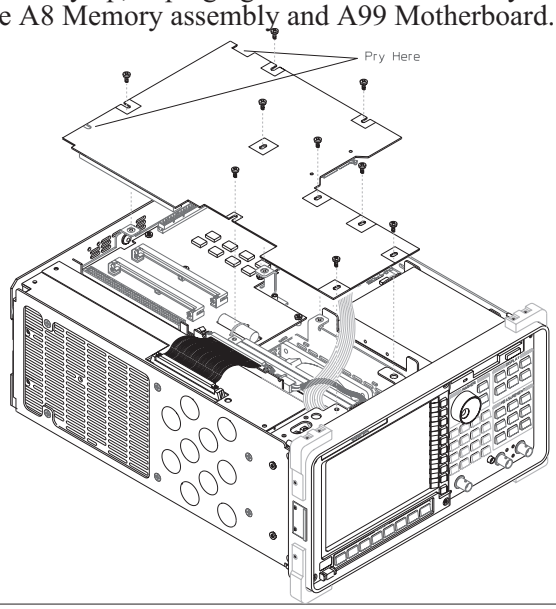


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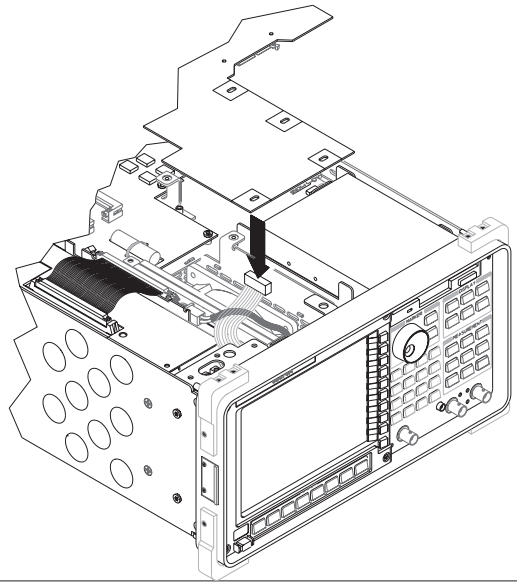
To remove CPU

1 Remove cover (see ‘’To remove cover’’).

2 Using a T-10 torx driver, remove the nine screws from the A7 CPU assembly. Lift the assembly up, unpluging the A7 CPU assembly from the A8 Memory assembly and A99 Motherboard.



3 Disconnect the ribbon cables from the A7 CPU assembly.



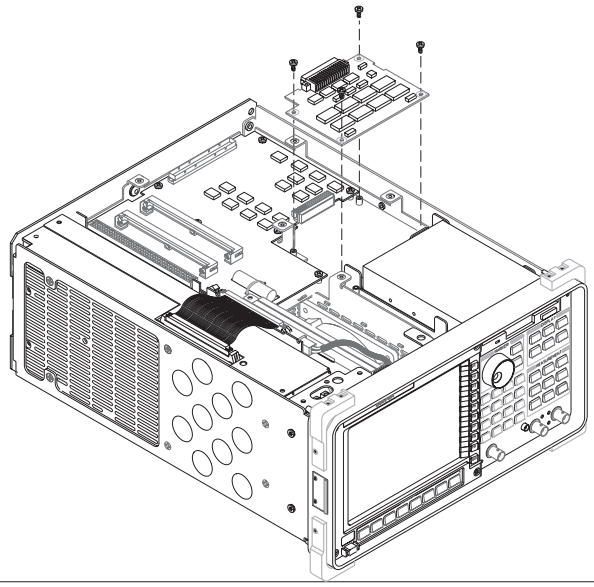
4 The analyzer’s serial number and firmware options are stored in EEPROM (U27) on the A7 CPU assembly. Before replacing the CPU assembly, remove A7 U27 from the faulty assembly and insert into the new assembly. See ‘’What to do before replacing the CPU assembly’’ on page 6-3.

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To remove NVRAM

1 Remove A7 CPU assembly (see ‘’To remove CPU’’).

2 Using a T-10 torx driver, remove the four screws from the A9 NVRAM assembly.

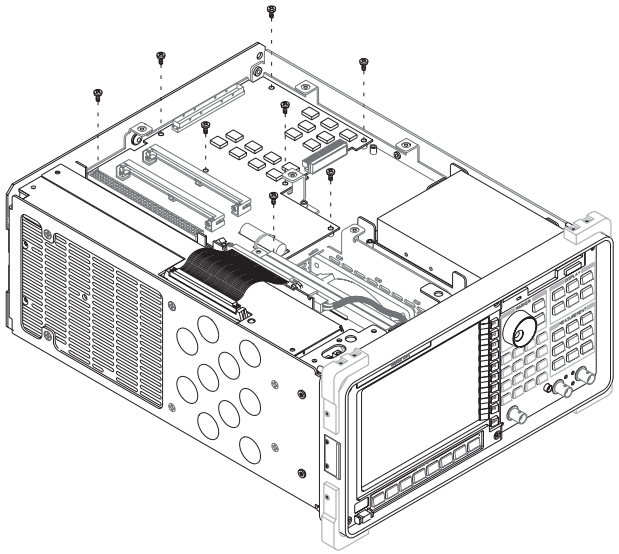


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To remove memory

1 Remove A7 CPU assembly (see ‘’To remove CPU’’). Remove optional A9 NVRAM assembly (see ‘’To remove NVRAM’’).

2 Using a T-10 torx driver, remove the eight screws from the A8 Memory assembly.

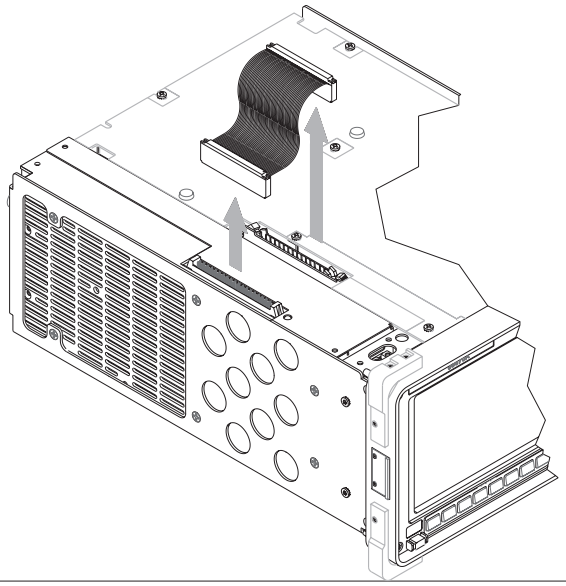


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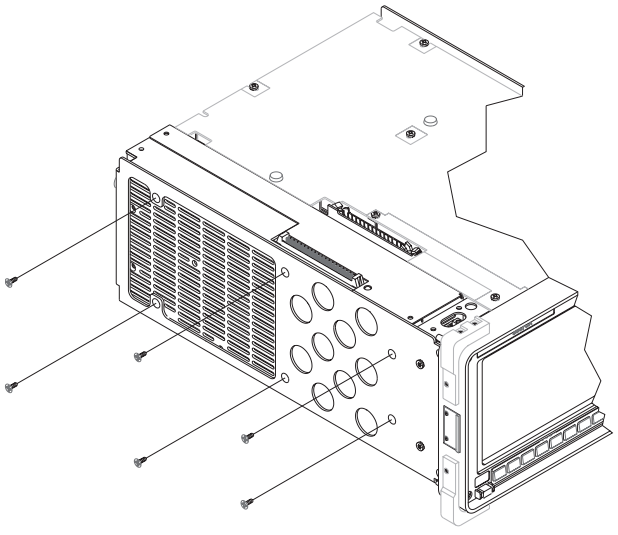
To remove power supply

1 Remove rear panel (see ‘’To remove rear panel’’).

2 Disconnect the ribbon cable from the A98 Power Supply assembly.



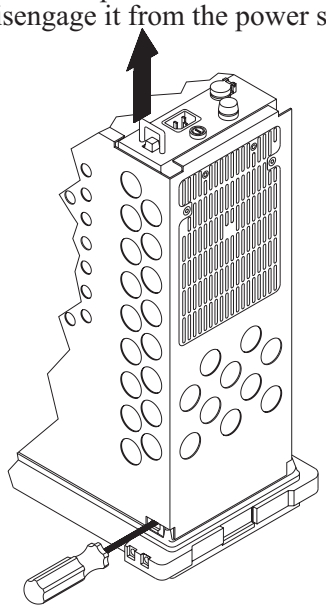
3 Using a T-15 torx driver, remove the six screws from the A98 Power Supply assembly.



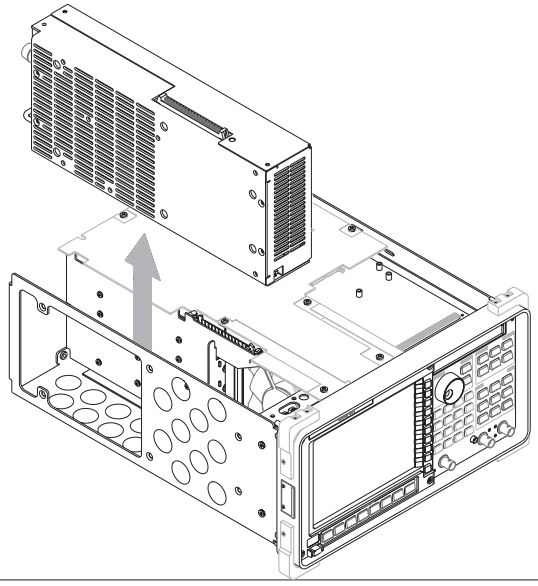
4 Set the front panel power switch in the off (O) position (switch in the out position).

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5 Using a straight-edge screw driver, hold the power switch rod in position and lift the A98 Power Supply to disengage it from the power switch rod.



6 Lift the A98 Power Supply assembly straight up.

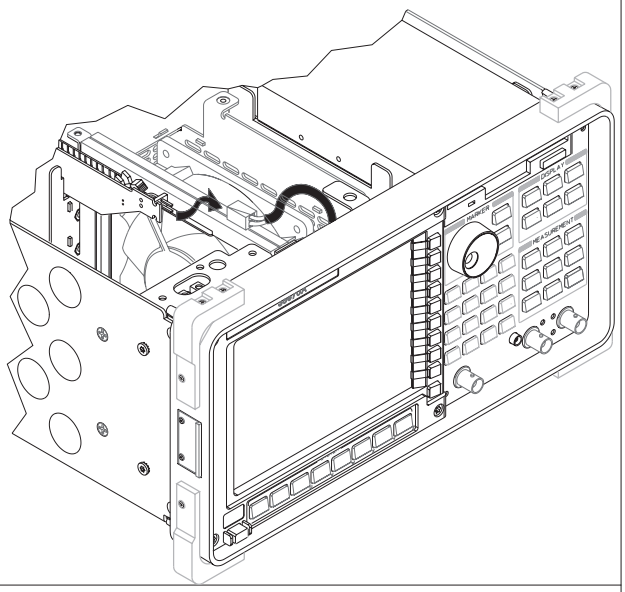


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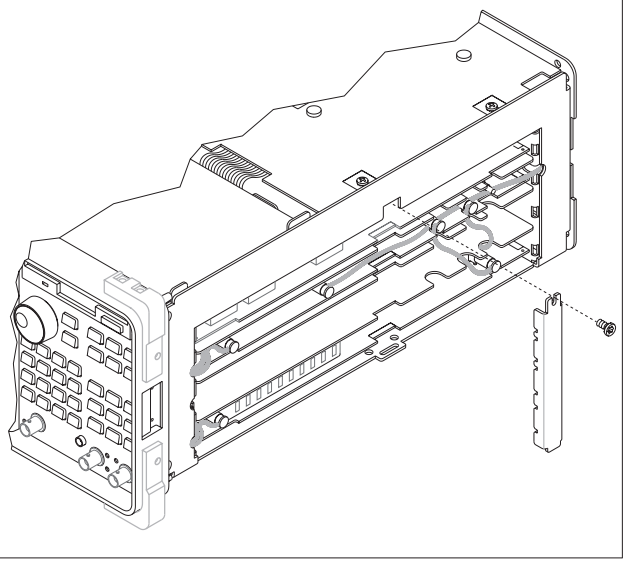
To remove motherboard

1 Remove A98 Power Supply assembly (see ''To remove power supply''). Remove A7 CPU assembly (see ''To remove CPU'').

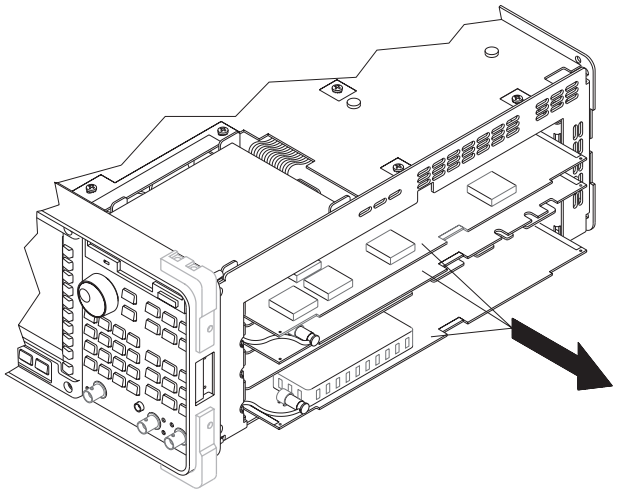
2 Disconnect the fan cable from the A99 Motherboard.



3 Remove assembly retainer bracket.

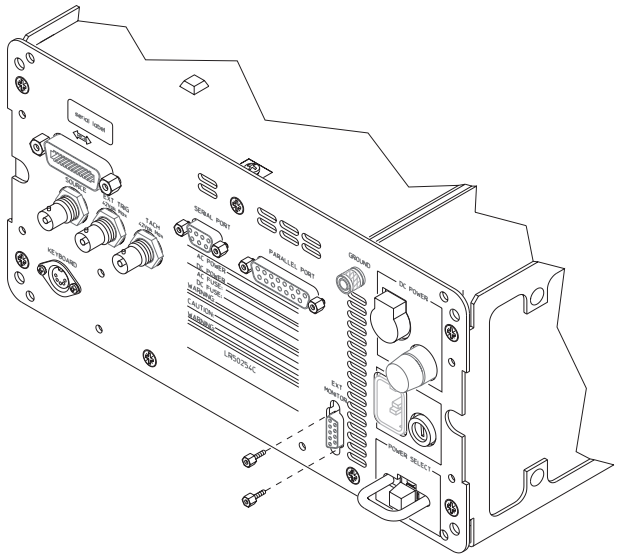


4 Unplug all assemblies from the A99 Motherboard.)

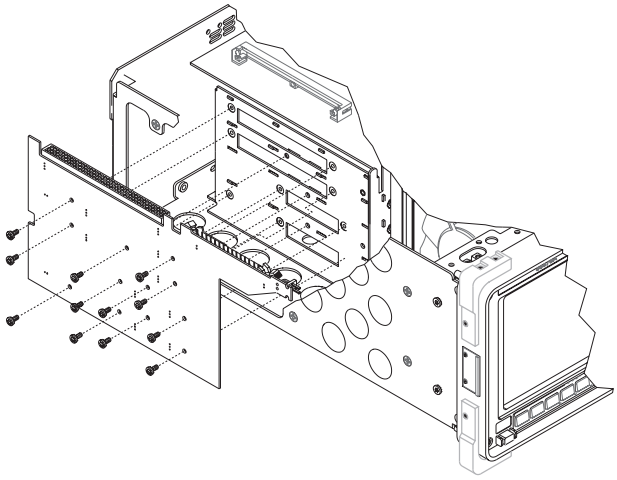


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5 Using a 5 mm open-ended wrench, remove the two screws from the EXT MONITOR connector.



6 Using T-10 torx driver, remove the twelve screws in A99 Motherboard.

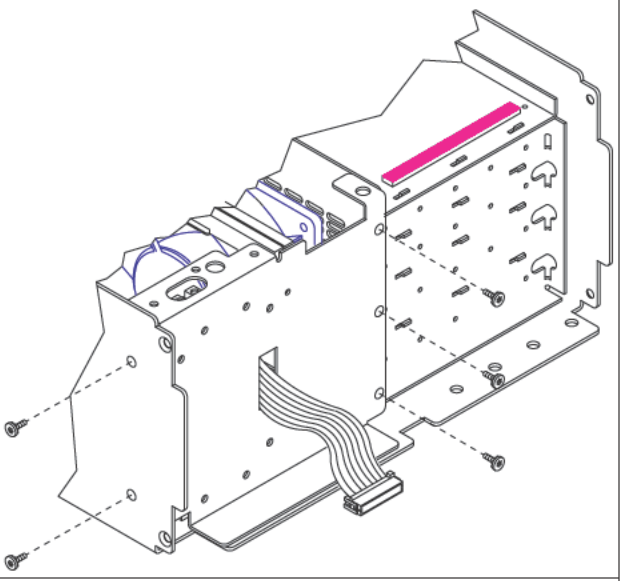


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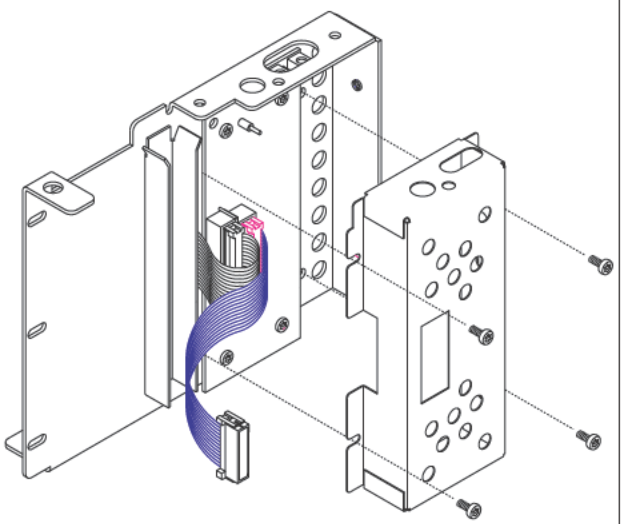
To remove dc-dc converter

1 Remove front panel (see ''To remove front panel''). Remove A7 CPU assembly (see ''To remove CPU'').

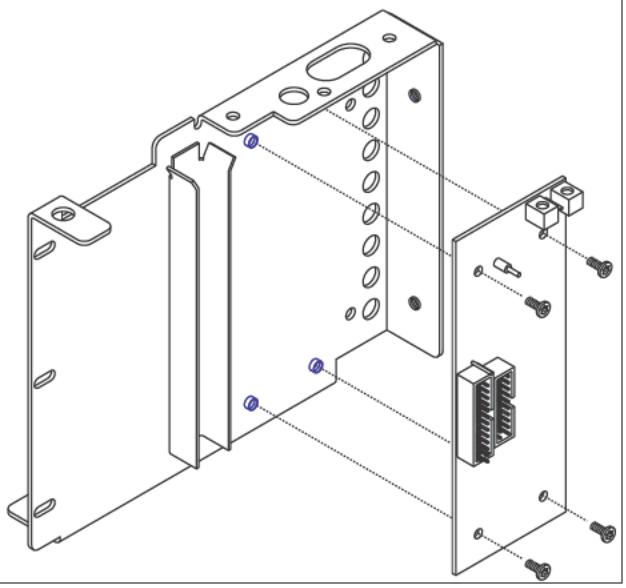
2 Using a T-10 torx driver, remove the five screws from the front wall.



3 Using a T-10 torx driver, remove the four screws from the shield. Unplug ribbon cables.



4 Using a T-10 torx driver, remove the four screws from the A102 DC-DC Converter assembly.



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7

Replaceable Parts

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Replaceable Parts

This chapter contains information for ordering replacement parts for the Agilent 35670A Dynamic Signal Analyzer.

Ordering Information

Replacement parts are listed in the following ten tables:

- Assemblies
- Cables
- Instrument Covers and Handles
- Assembly Covers and Brackets
- Front Panel Parts
- Rear Panel Parts
- Chassis Parts
- Card Nest Parts
- Screws, Washers, and Nuts
- Miscellaneous Parts

To order a part listed in one of the tables, quote the Agilent Technologies part number (HP Part Number), the check digit (CD), indicate the quantity required, and address the order to the nearest Agilent Technologies sales and service office (see the inside back cover of this guide). The check digit verifies that an order has been transmitted correctly, ensuring accurate and timely processing of the order. The first time a part is listed in the table, the quantity column (Qty) lists the total quantity of the part used in the analyzer. For definitions of the abbreviations and the corresponding name and address of the manufacturers' codes shown in the tables, see ''Code Numbers.''

Caution

Many of the parts listed in this chapter are static sensitive. Use the appropriate precautions when removing, handling, and installing all parts to avoid unnecessary damage.

Non-Listed Parts

To order a part that is NOT listed in the replaceable parts tables, indicate the instrument model number, instrument serial number, description and function of the part, and the quantity of the part required. Address the order to the nearest Agilent Technologies sales and service office (see the inside back cover of this guide).

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Direct Mail Order System

Within the U.S.A., Agilent Technologies can supply parts through a direct mail order system. Advantages of the Direct Mail Order System are:

- Direct ordering and shipment from the Agilent Parts Center.
- No maximum or minimum on any mail order. There is a minimum order for parts ordered through a local Agilent sales and service office when the orders require billing and invoicing.
- Transportation charges are prepaid. A small handling charge is added to each order.
- No invoicing. A check or money order must accompany each order.
- Mail order forms and specific ordering information are available through your local Agilent Technologies sales and service office. See the inside back cover of this guide for a list of Agilent Technologies sales and service office locations and addresses.

Code Numbers

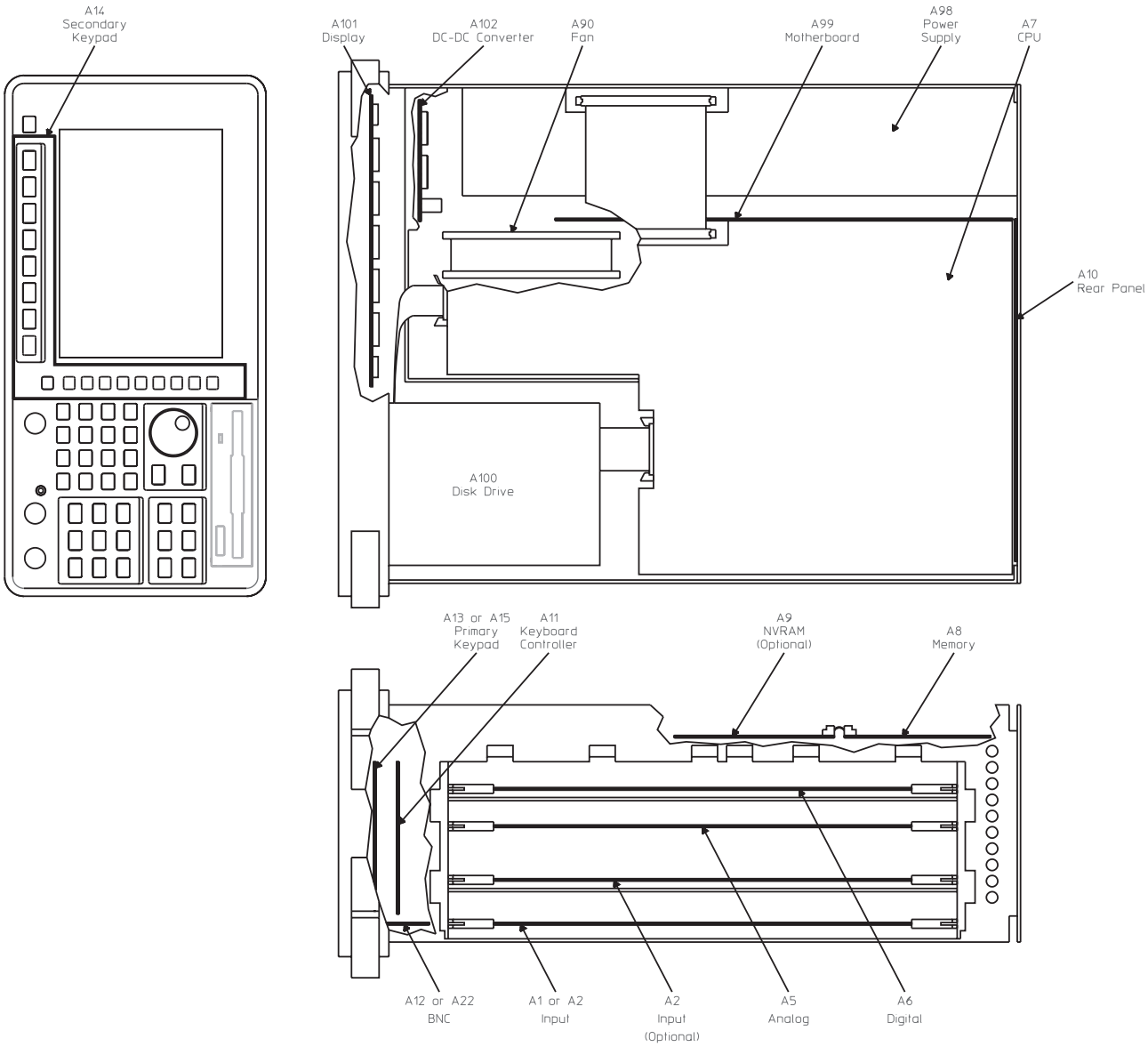
The following table provides the name and address for the manufacturers' code numbers (Mfr Code) listed in the replaceable parts tables.

Mfr No.	Mfr Name	Address
00268	LEMO USA, Inc.	Santa Rosa, CA 95406 U.S.A.
00779	Amp Inc.	Harrisburg, PA 17105 U.S.A.
00955	Koszegi Industries Inc.	South Bend, IN 46624 U.S.A.
05791	Lyn-Tron Inc	Burbank, CA 91505 U.S.A.
09353	C & K Components Inc	Newton, MA 02158 U.S.A.
10421	Epson America Inc.	Dallas, TX 75284 U.S.A.
11919	Computer Products Inc.	Chicago, IL 60693 U.S.A.
12690	Fuji Polymer Industries Co. Inc.	Nagoya-Shi Japan
24931	Specialty Connector Co	Franklin, IN 46131 U.S.A.
28480	Agilent Technologies Company	Palo Alto, CA 94304 U.S.A.
30817	Instrument Specialties Co. Inc.	Placentia, CA 92670 U.S.A.
34785	Dek Inc.	St Charles, IL 60174 U.S.A.
56501	Thomas & Betts Corp	Bridgewater, NJ 08807 U.S.A
57003	Chomerics Shielding Technology	Carson, CA 90745 U.S.A.
71400	Cooper Industries Inc	St Louis, MO 63178 U.S.A.
73734	Federal Screw Products Co.	Chicago, IL 60618 U.S.A.
75915	Littelfuse Inc.	Des Plaines, IL 60016 U.S.A.
76381	3M Co.	Seattle, WA 98124 U.S.A.

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Assemblies

After replacing an assembly, see ‘’What to do after replacing an assembly’’ in chapter 6 for required adjustments and performance tests.
The reference designator for the screws that fasten the A90 Fan assembly is MP600. The reference designator for the screws that fasten the A98 Power Supply assembly is MP603. The reference designator for the screws that fasten all other assemblies is MP601.



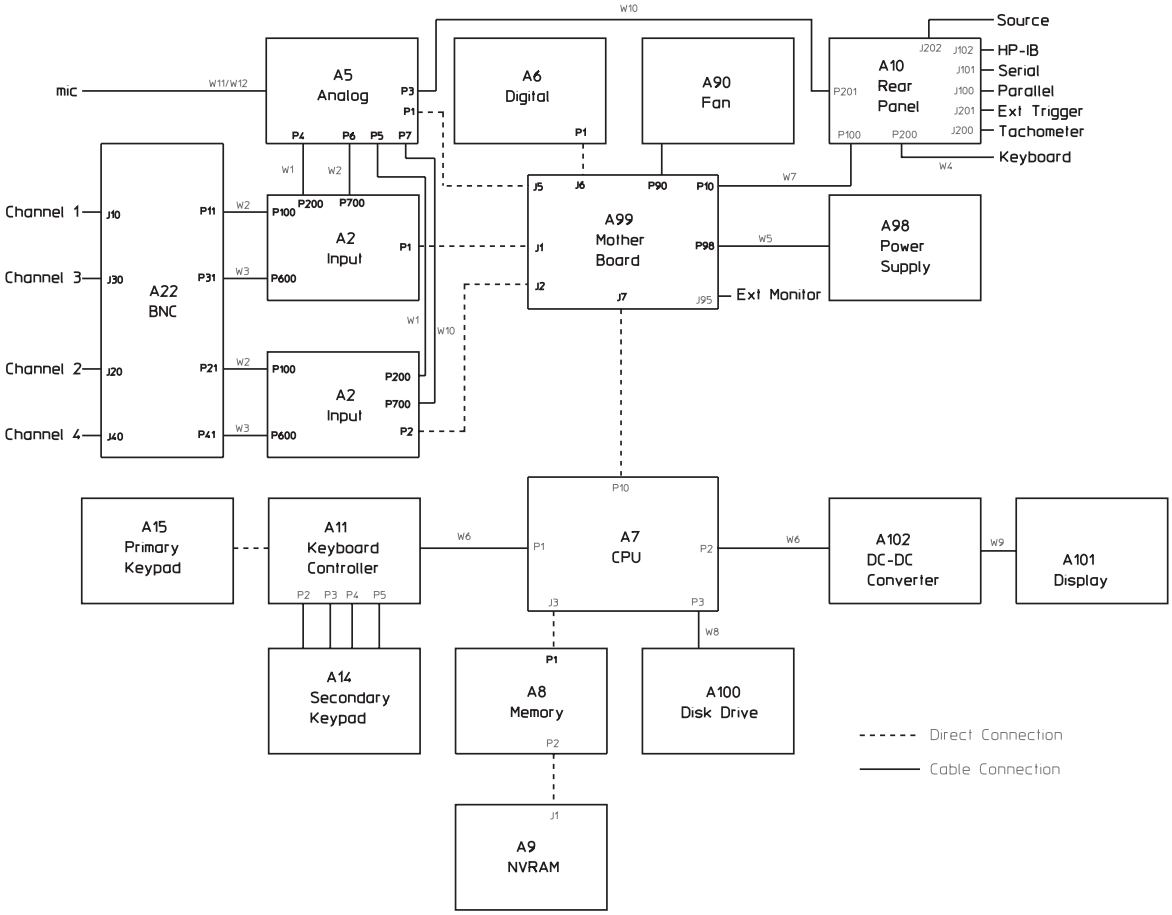
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Ref Des	Agilent Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
A1	35670 69501	9	1	INPUT ASSEMBLY 2 CHANNEL	28480	35670 69501
A2	35670 69502	0	2	INPUT ASSEMBLY 4 CHANNEL	28480	35670 69502
A5	35670 69505	3	1	ANALOG ASSEMBLY	28480	35670 69505
A6	35670 69506	4	1	DIGITAL ASSEMBLY	28480	35670 69506
A7	35670 69507	5	1	CPU ASSEMBLY †	28480	35670 69507
A8	35670 66508	6	1	MEMORY ASSEMBLY	28480	35670 66508
A9	35670 66509	7	1	NVRAM ASSEMBLY	28480	35670 66509
A10	35670 66510	4	1	REAR PANEL ASSEMBLY	28480	35670 66510
A11	35670 66511	5	1	KEYBOARD CONTROLLER	28480	35670 66511
A12	35670 66512	6	1	BNC ASSEMBLY 2 CHANNEL	28480	35670 66512
A13	35670 66513	7	1	PRIMARY KEYPAD ASSEMBLY 2 CHANNEL	28480	35670 66513
A14	35670 64300	6	1	SECONDARY KEYPAD ASSEMBLY	28480	35670 64300
A15	35670 66515	9	1	PRIMARY KEYPAD ASSEMBLY 4 CHANNEL	28480	35670 66515
A22	35670 66522	8	1	BNC ASSEMBLY 4 CHANNEL	28480	35670 66522
A90	03585 68501	6	1	FAN ASSEMBLY	28480	03585 68501
A98	0950 2357	9	1	POWER SUPPLY ASSEMBLY	11919	NFS177 7630
A99	35670 66599	9	1	MOTHERBOARD	28480	35670 66599
A100	0950 2141	9	1	DISK DRIVE ASSEMBLY	10421	SMD 340
A101	2090 0340	9	1	DISPLAY ASSEMBLY	28480	2090 0340
A102	0950 2335	3	1	DC DC CONVERTER ASSEMBLY	28480	0950 2335

† The analyzer's serial number and firmware options are stored in EEPROM (U27) on the A7 CPU assembly. Before replacing the CPU assembly, remove A7 U27 from the faulty assembly and insert into the new assembly. See ''What to do before replacing the CPU assembly'' on page 6 3.

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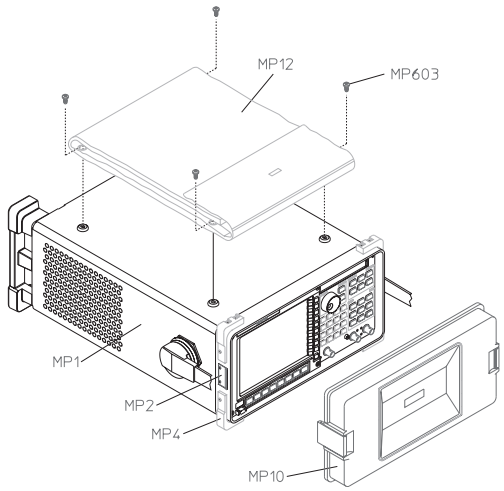
Cables



Ref Des	Agilent Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
W1	03585 61603	5	2	CBL ASM CXL FSMB/FSMB 100MM OR	28480	03585 61603
W2	03585 61604	6	3	CBL ASM CXL FSMB/FSMB 177MM YL	28480	03585 61604
W3	03586 61678	5	2	CBL ASM CXL FSMB/FSMB 205MM GY	28480	03586 61678
W4	35665 61601	7	1	CBL ASM CDIN/FHSG 80MM MULT	28480	35665 61601
W5	8120 6243	9	1	CBL POWER 60POS RIBBON 75MM LG	28480	8120 6243
W6	8120 6236	0	2	CBL KEYBOARD 16POS RIBBON	28480	8120 6236
W7	8120 6242	8	1	CBL REAR PANEL 60POS RIBBON	28480	8120 6242
W8	8120 6241	7	1	CBL DISC DRIVE 34POS RIBBON	28480	8120 6241
W9	8120 6240	6	1	CBL DISPLAY 20POS RIBBON	28480	8120 6240
W10	03586 61677	4	2	CBL ASM CXL FSMB/FSMB 265MM BL	28480	03586 61677
W11	35670 61620	7	1	CBL FRT PNL ADAPTER 4 CON LEMO	28480	35670 61620
W12	35670 61621	8	1	CBL ADAPTER PLUG 4 COND W/LEMO	28480	35670 61621

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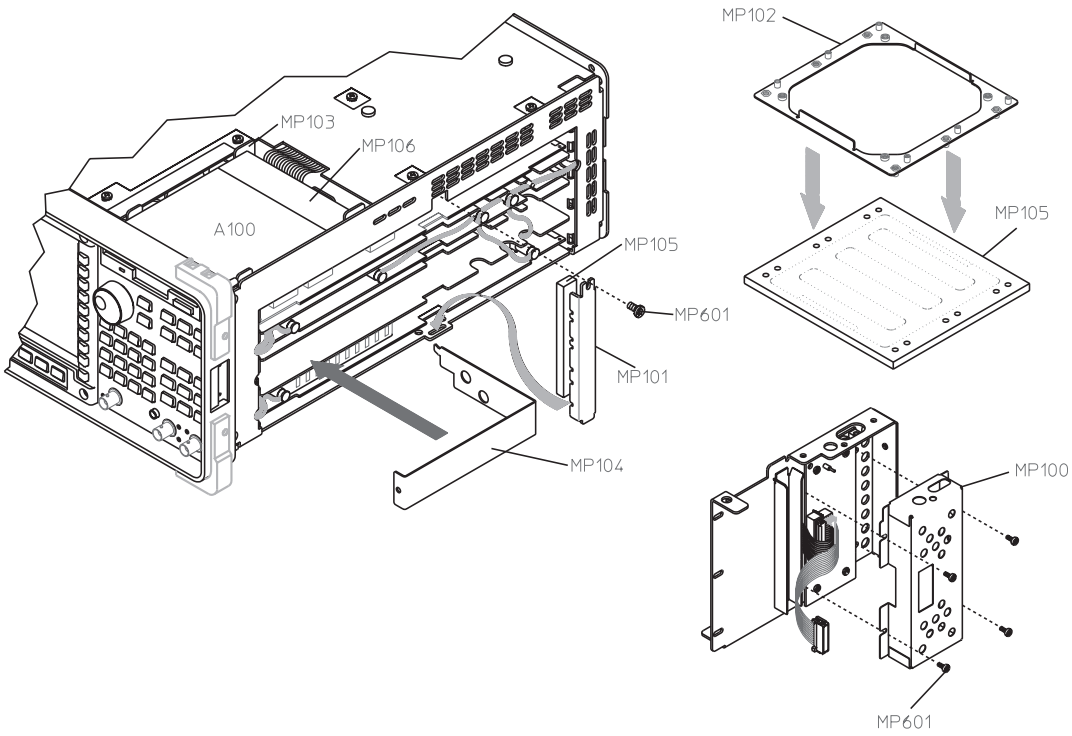
Instrument Covers and Handles



Ref Des	Agilent Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
MP1	35670 64101	5	1	SHTF ASSY COVER ALV	28480	35670 64101
MP2	5021 5483	4	2	COVER LATCHES	28480	5021 5483
MP4	5062 4806	9	1	MOLD BUMPER SET 4PC FF CORNRS	28480	5062 4806
MP10	35670 64102	6	1	IMPACT COVER 35670A	28480	35670 64102
MP12	1540 0292	9	1	PKG CASE ACCESSORY	00955	1051 B 2
MP13	1530 0272	4	1	VIEWING HOOD	28480	1530 0272
MP15	8160 0689	9	2	STMP RFI GASKET.228LNG BECUZN	30817	0097 954 15

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Assembly Covers and Brackets

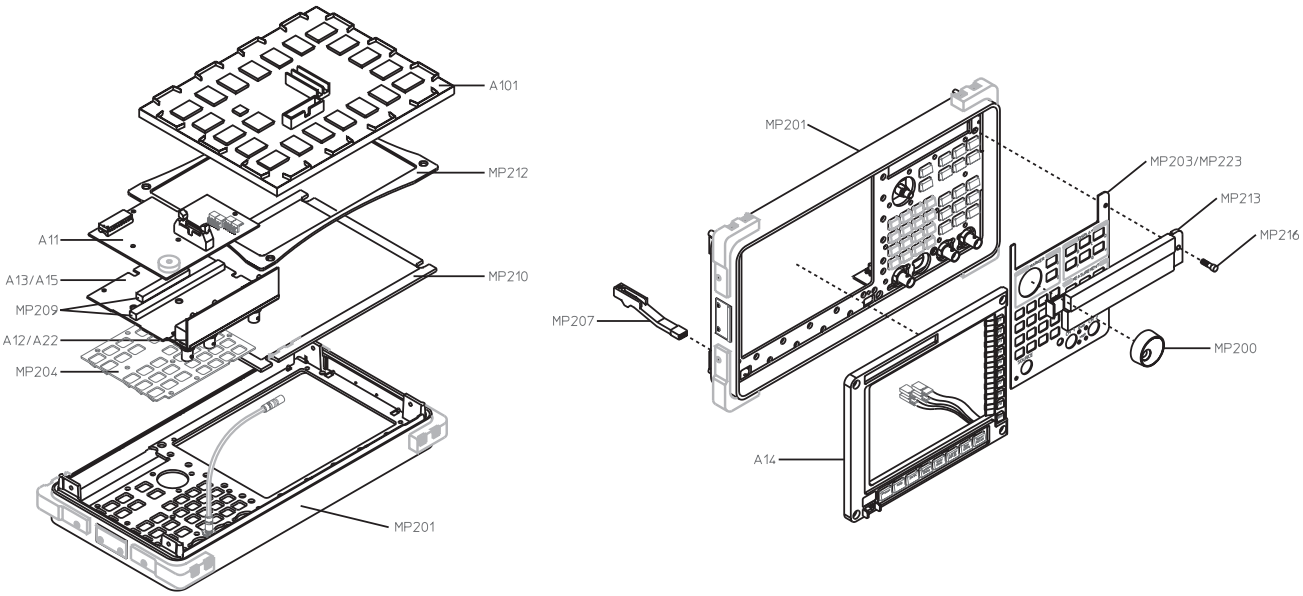


Ref Des	Agilent Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
MP100	35670 00605	0	1	SHTF SHIELD DISP PWR SUPPLY	28480	35670 00605
MP101	35670 01203	6	1	SHTF BRKT,PCB RETAINER	28480	35670 01203
MP102	35670 01204	7	1	SHTF BRACKET FAN AL	28480	35670 01204
MP103	35670 01205	8	1	SHTF DISC BRKT	28480	35670 01205
MP104	35670 04102	0	1	SHTF SLOT PLUG	28480	35670 04102
MP105	35670 44701	9	2	GSKT FAN MOUNT W/SLUGS	28480	35670 44701
MP106	4040 2321	2	1	DUST COVER DISC DRIVE	28480	4040 2321

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Front Panel Parts

The reference designator for the screws that fasten the bezel (MP208) to the front frame (MP201) is MP604. The reference designator for the nuts that fasten the A101 Display assembly to the front frame is MP611. The reference designator for the screws that fasten the front frame to the chassis is MP603.

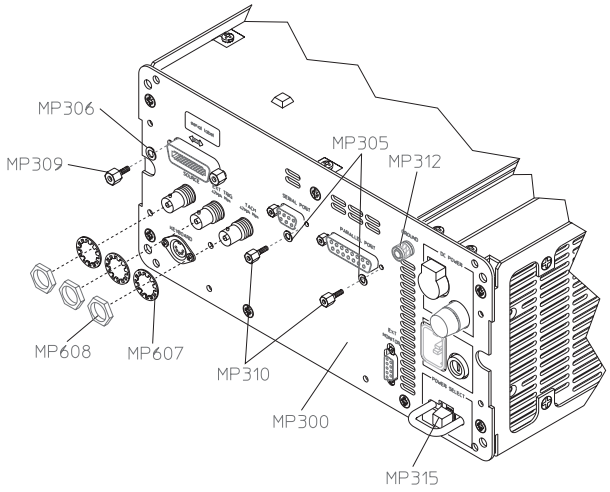


Ref Des	Agilent Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
MP200	0370 3069	2	1	MOLD KNB 1.12DRD RPG .25ID	28480	0370 3069
MP201	35670 22001	6	1	CSTG FRT FRAME MACH&PAINTED	28480	35670 22001
MP203	35670 34305	8	1	PNL OVRLY DRESS 2CHAN PLCR	28480	35670 34305
MP204	35670 41901	5	1	KYPD HARDKEY HINGED	28480	35670 41901
MP207	35670 43701	7	1	MOLD PUSHROD PWR WHT	28480	35670 43701
MP209	1252 4960	5	2	CONNECTOR MULTICONTACT	12690	05 10108
MP210	35670 29301	3	1	LNZ FLTR RFI/OPTICAL	28480	35670 29301
MP212	35670 44703	1	1	DISPLAY GASKET	28480	35670 44703
MP213	35670 44101	3	1	MOLD COVER DISC DRIVE PCMT SLS	28480	35670 44101
MP214	8160 0423	9	3	RFI ROUND STRIP MNL/SIL RBR .125 IN OD	57003	01 0501 1891
MP215	8160 0467	1	1	RFI STRIP FINGERS BE CU BRIGHT DIP	30817	97 555 A X
MP216	0515 0482	5	1	SCREW SKT HD CAP M3 X 0.5 8MM LG	28480	0515 0482
MP223	35670 34302	5	1	PNL OVRLY DRESS 4CHAN PLCR	28480	35670 34302

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Rear Panel Parts

The reference designator for the screws that fasten the KEYBOARD connector and A10 Rear Panel assembly to the rear panel is MP601. The reference designator for the screws that fasten the rear panel to the chassis is MP603.



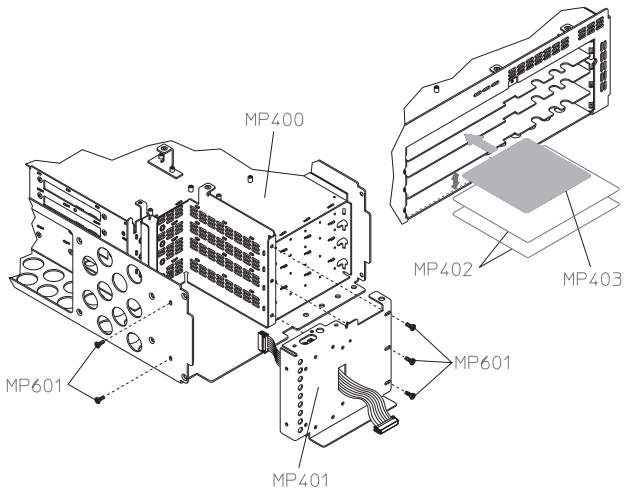
Caution

The POWER SELECT switch must be in the DC position (out position) when the key cap (MP315) is removed. If the switch is not in the DC position when the key cap is removed, the switch may be damaged.

Ref Des	Agilent Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
MP300	35670 00201	2	1	SHTF REAR PANEL W/SILKSCREEN	28480	35670 00201
MP305	2190 0913	9	6	WASHER LK HLCL NO. 4 .115 IN ID	28480	2190 0913
MP306	2190 0586	2	2	WASHER LK HLCL 4.0 MM 4.1 MM ID	28480	2190 0586
MP309	0380 0643	3	2	STANDOFF HEX .255 IN LG 6 32 THD	28480	0380 0643
MP310	0380 1832	4	4	STDF HXMF MIXED 4.8MMLG STLZN	00779	747404 3
MP312	1510 0038	8	1	BINDING POST ASSY SGL THD STUD	28480	1510 0038
MP314	2950 0072	3	1	NUT HEX DBL CHAM 1/4 32 THD .062 IN THK	28480	2950 0072
MP315	5041 0564	4	1	KEYCAP	28480	5041 0564

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Chassis Parts



Ref Des	Agilent Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
MP400	35670 00101	1	1	SHTF CHASSIS ASSY	28480	35670 00101
MP401	35670 00102	2	1	SHTF WALL ASSY FRONT	28480	35670 00102
MP402	35670 04103	1	2	INPUT BD INSULATOR	28480	35670 04103
MP403	35650 00601	2	1	SHTF CVR SHLD MUFL	28480	35650 00601
MP404	35670 64302	8	1	LBL CABLE 2CH CBL ROUTINE	28480	35670 64302
MP405	35670 64304	0	2	LBL CABLE 4CH CBL ROUTINE	28480	35670 64304

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Screws, Washers, and Nuts

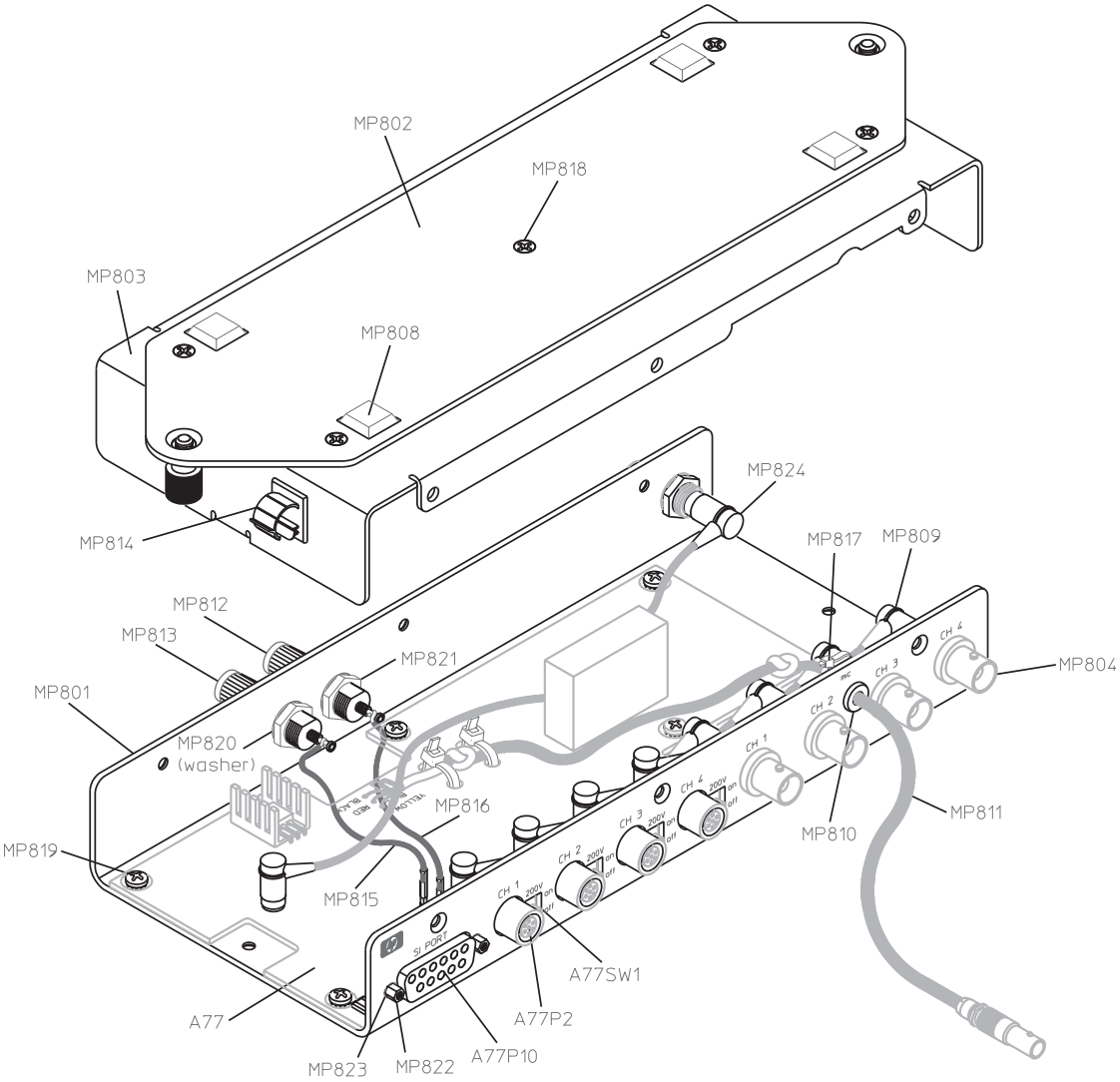
Ref Des	Agilent Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
MP600	0515 0374	4	16	SCREW MACHINE ASSEMPLY M3 X 0.5 10MM LG	28480	0515 0374
MP601	0515 0430	3	66	SCREW MACHINE ASSEMPLY M3 X 0.5 6MM LG	28480	0515 0430
MP602	0515 1940	2	4	SCR MCH M2.5 6MMLG PHTX SST *	28480	0515 1940
MP603	0515 2043	8	21	SCR MCH M4.0 8MMLG FHTX SST *	28480	0515 2043
MP604	0515 1622	7	4	SCR CAP M4.0 8MMLG SKHX SSTBL	28480	0515 1622
MP607	2190 0099	2	3	WASHER LK INTL T 7/16 IN .472 IN ID	28480	2190 0099
MP608	2950 0035	8	3	NUT HEX DBL CHAM 15/32 32 THD	28480	2950 0035
MP611	0535 0031	2	4	NUT HEX W/LKWR M3 X 0.5 2.4MM THK	28480	0535 0031
MP613	2190 0060	7	1	WASHER LK INTL T 1/4 IN .256 IN ID	28480	2190 0060
MP619	1252 0699	9	2	SCR JCK 4 40 .25LG THRD STLZN	05791	ST 9411 36

Miscellaneous Parts

Ref Des	Agilent Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
MP702	1400 1122	0	1	CLAMP CABLE .187 DIA .735 WD NYL	34785	021 0188
MP703	1400 1229	8	1	CLAMP CABLE .375 DIA 1 WD NYL	34785	021 0375
MP704	0403 0285	9	4	BUMPER FOOT ADH MTG 12.7 MM WD	76381	SJ 5018 GRAY
MP705	1400 0249	0	1	CABLE TIE .062 .625 DIA .091 WD NYL	56501	TY 23M 8
MP707	0403 0179	0	18	BUMPER FOOT ADH MTG	76381	SJ 5012 BLACK
A8B200	1420 0336	8	1	BATTERY	55002	T06/46
A10F200	2110 0665	0	1	FUSE 1A 125V NTD .28X.096	75915	R251001T1
A98 F1	2110 0342	0	1	FUSE 8A 250V NTD 1.25X.25 UL	71400	ABC 8
A98 F2	2110 0920	0	1	FUSE 30A 32VDC NORMAL BLOW 3AG	75915	311 030

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Option UK4 Parts



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Ref Des	Agilent Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
A77	35670 66577	3	1	MICROPHONE PC ASSEMBLY	28480	35670 66577
A77P2	1252 5280	4	4	CONN LEMO 7 CNT FEMALE RT PC	00268	EPG.1B.307.HLN
A77P10	1252 1481	9	1	CON RECT D SUB 15CKT 15PN THL	00779	748876 1
A77SW1	3101 3124	4	4	SW SL .02A 20VA1D	09353	1101 M2S4AV2 BE
MP801	35670 00121	5	1	SHTF BTTM OUTBOX W/SILKSCREEN	28480	35670 00121
MP802	35670 01206	9	1	SHTF BRKT MNTG OUTBOX	28480	35670 01206
MP803	35670 00120	4	1	SHTF LID OUTBOX PAINTED	28480	35670 00120
MP804	1250 1558	7	5	ADAPTER COAX STR F BNC F RCA PHONO	24931	29JJ126 3
M0808	0403 0285	9	4	BUMPER FOOT ADH MTG 12.7 MM WD	76381	SJ 5018 GRAY
MP809	8120 4891	9	4	CBL RCA 153MM BK	28480	8120 4891
MP810	0400 0009	9	1	GROMMET RND .125 IN ID .25 IN GRV OD	28480	0400 0009
MP811	35670 61621	8	1	CBL ADAPTER PLUG 4 COND W/LEMO	28480	35670 61621
MP812	1510 0091	3	1	BINDING POST SGL SGL TUR JGK RED	28480	1510 0091
MP813	1510 0107	2	1	BINDING POST SGL SGL TUR JGK CBK	28480	1510 0107
MP814	1400 1122	0	1	CLAMP CABLE .187 DIA .735 WD NYL	34785	021 0188
MP815	8120 3828	0	1	LJPR 22GA BLK 100MM Dx8	28480	8120 3828
MP816	8120 3860	0	1	LJPR 22GA RED 100MM Dx8	28480	8120 3860
MP817	1400 0249	0	3	CABLE TIE .062 .625 DIA .091 WD NYL	56501	TY 23M 8
MP818	0515 1946	8	13	SCR MCH M3.0 6MMLG FHTX SST	28480	0515 1946
MP819	0515 0430	3	7	SCR MCH ASSEMPLY M3 X 0.5 6MM LG	28480	0515 0430
MP820	2190 0016	3	2	WASHER LK INTL T 3/8 IN .377 IN ID	28480	2190 0016
MP821	2950 0001	8	2	NUT HEX DBL CHAM 3/8 32 THD .094 IN THK	73734	9002 NP
MP822	1252 0699	9	2	SCR JCK 4 40 .25LG THRD STLZN	05791	ST 9411 36
MP823	2190 0583	9	2	WASHER LK HLCL 2.5 MM 2.6 MM ID	28480	2190 0583
MP824	8120 2587	6	1	CABLE ASSY COAX 50 OHM 1.5KV 8.5 IN LG	28480	8120 2587
	35670 90014	4	1	MICROPHONE & POWER OP NOTE	28480	35670 90051
	8120 1839	9	1	CABLE ASSY COAX 50 OHM 24 IN LG JGK	28480	8120 1839
	8120 6237	1	4	CBL ASM CXL BNC	28480	8120 6237

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8

Circuit Descriptions

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Circuit Descriptions

This chapter contains the overall instrument description and individual assembly descriptions for the Agilent 35670A Dynamic Signal Analyzer. The overall instrument description lists the assemblies in the analyzer and describes the analyzer's overall block diagrams. The assembly descriptions give additional information for each assembly. For signal connections and descriptions, see chapter 9, ''Voltages and Signals.''

Overall Instrument Description

The Agilent 35670A Dynamic Signal Analyzer is an FFT spectrum/network analyzer with a frequency range that extends from 0.19531 Hz to 102.4 kHz in single channel mode and from 0.097656 Hz to 51.2 kHz in two channel mode. The optional four channel analyzer has a frequency range that extends from 0.097656 Hz to 51.2 kHz in two channel mode and from 0.048828 Hz to 25.6 kHz in four channel mode. The analyzer has a built-in signal source providing random noise, burst random noise, periodic chirp, burst chirp, pink noise, and fixed sine. Measurements can be saved to an internal 3.5-inch flexible disk drive, an external HP SS-80 disk drive, or to internal non-volatile memory. Plots and prints of the measurements can be made directly to printers and plotters with GPIB, parallel, or serial interfaces. The analyzer also supports the Instrument Basic programming language (IBASIC).

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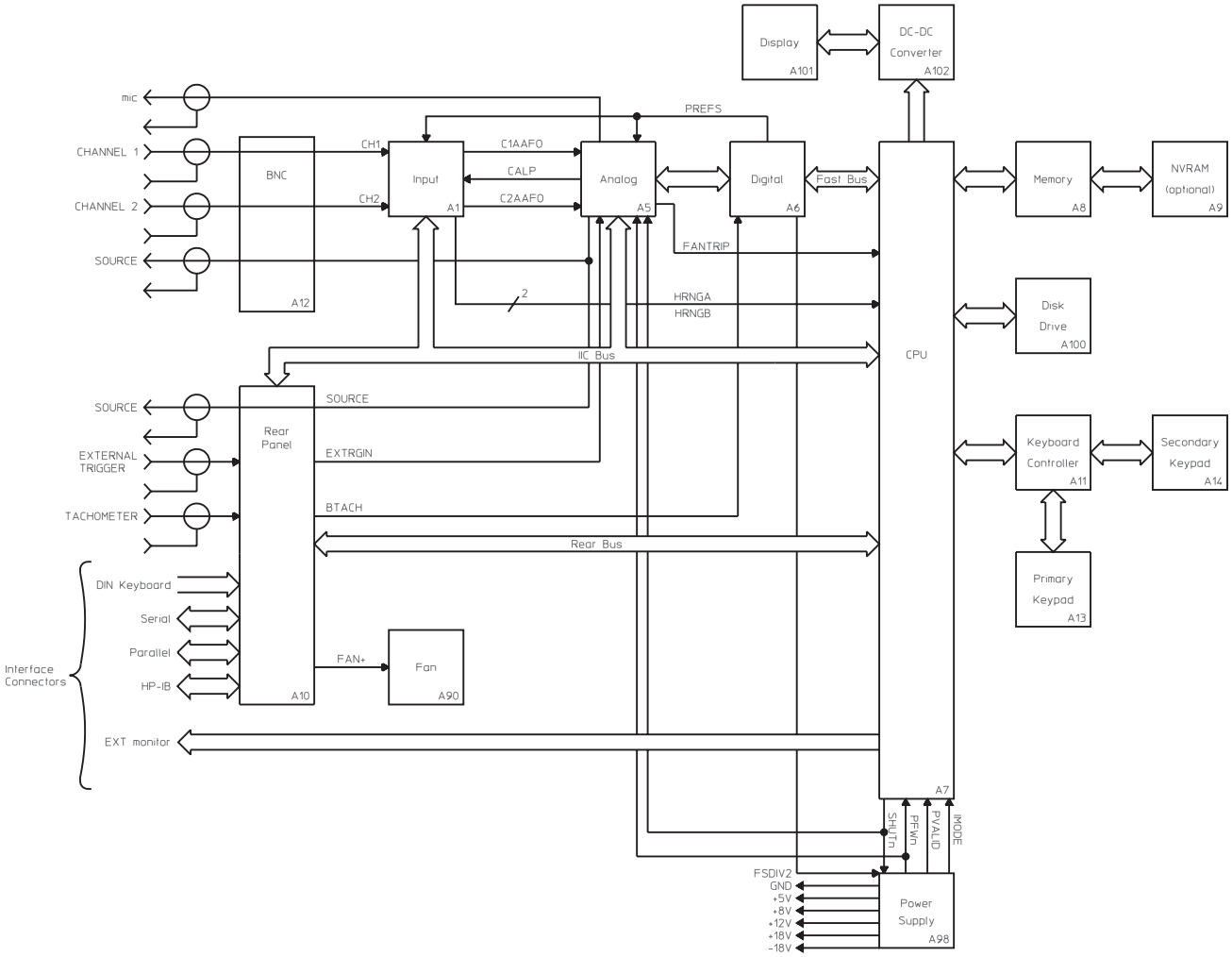
Overall Block Diagram

The following figures show the overall block diagrams for both the two channel and the four channel analyzer. Each block in the diagrams represents a functional block in the analyzer. The assembly that performs the function is listed in the block.

BNC	Contains the BNC connectors for both input channels and the source. For the four channel analyzer, the BNC assembly contains the BNC connectors for all four input channels. Both BNC assemblies filter the input channels HIGH (BNC center conductor) and LOW (BNC shell) input signals to reduce noise at the inputs.
Input	Buffers, attenuates, amplifies, and filters the input signals. The input assembly also provides common mode and differential overload detection, and half-range detection. The two channel analyzer contains one A1 Input assembly and the four channel analyzer contains two A2 Input assemblies.
Analog	Converts the input signals from the Input assembly (or assemblies) to digital data. The Analog assembly also converts the digital data from the Digital assembly's digital source to the analog source signal. For the two channel analyzer, the analog source signal is routed to the Rear Panel assembly and to the BNC assembly. For the four channel analyzer, the analog source signal is routed only to the Rear Panel assembly.
Digital	Prepares the digital data from the Analog assembly for the CPU assembly. This assembly also generates the digital source data for the Analog assembly.
CPU	Controls the analyzer. The following is a partial list of the operations it performs: • Configures the assemblies • Controls the Disk Drive assembly • Controls the Display assembly • Initiates the power-up sequence and calibration routine • Processes digital data from the Digital assembly • Computes the Fast Fourier Transform (FFT) • Monitors for a keystroke • Monitors the assemblies for overloads or other error conditions • Runs the self tests
DC-DC Converter	Generates the driver supply voltages for the Display assembly.
Display	Offers a view of the processed data. See the description of the Display Controller for the "A7 CPU" later in this chapter for further details.
Memory	Contains RAM, NVRAM, ROM, and the battery-backed real time clock for the CPU assembly.
NVRAM	Provides the CPU assembly with additional NVRAM. This assembly is optional.
Disk Drive	Stores and retrieves information on 3.5-inch flexible disks.
Keyboard Controller	Tells the CPU assembly which key was pressed.
Primary Keypad	Consists of hardkeys and an RPG.

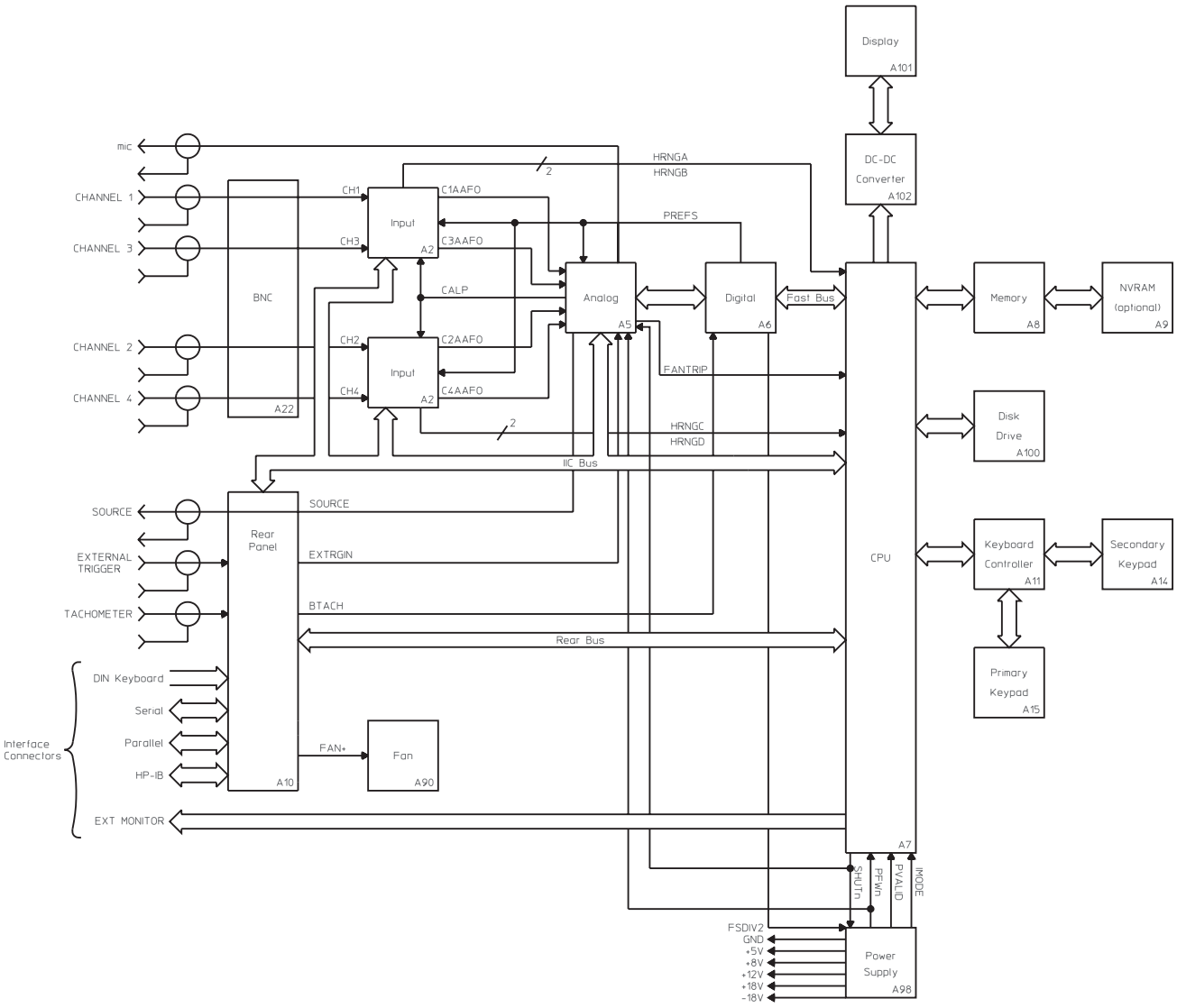
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Secondary Keypad	Consists of hardkeys and softkeys.
Power Supply	Supplies the dc voltages shown in the block diagram. See “Power Supply Voltage Distribution” in chapter 9 for additional information.
Rear Panel	Provides the interface for devices connected to its GPIB connector, parallel connector, serial connector, and DIN keyboard connector. The Rear Panel assembly also provides the fan control, external trigger connector, source connector, and tachometer connector and counter.



Two Channel Overall Block Diagram

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Four Channel Overall Block Diagram

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A1 Input

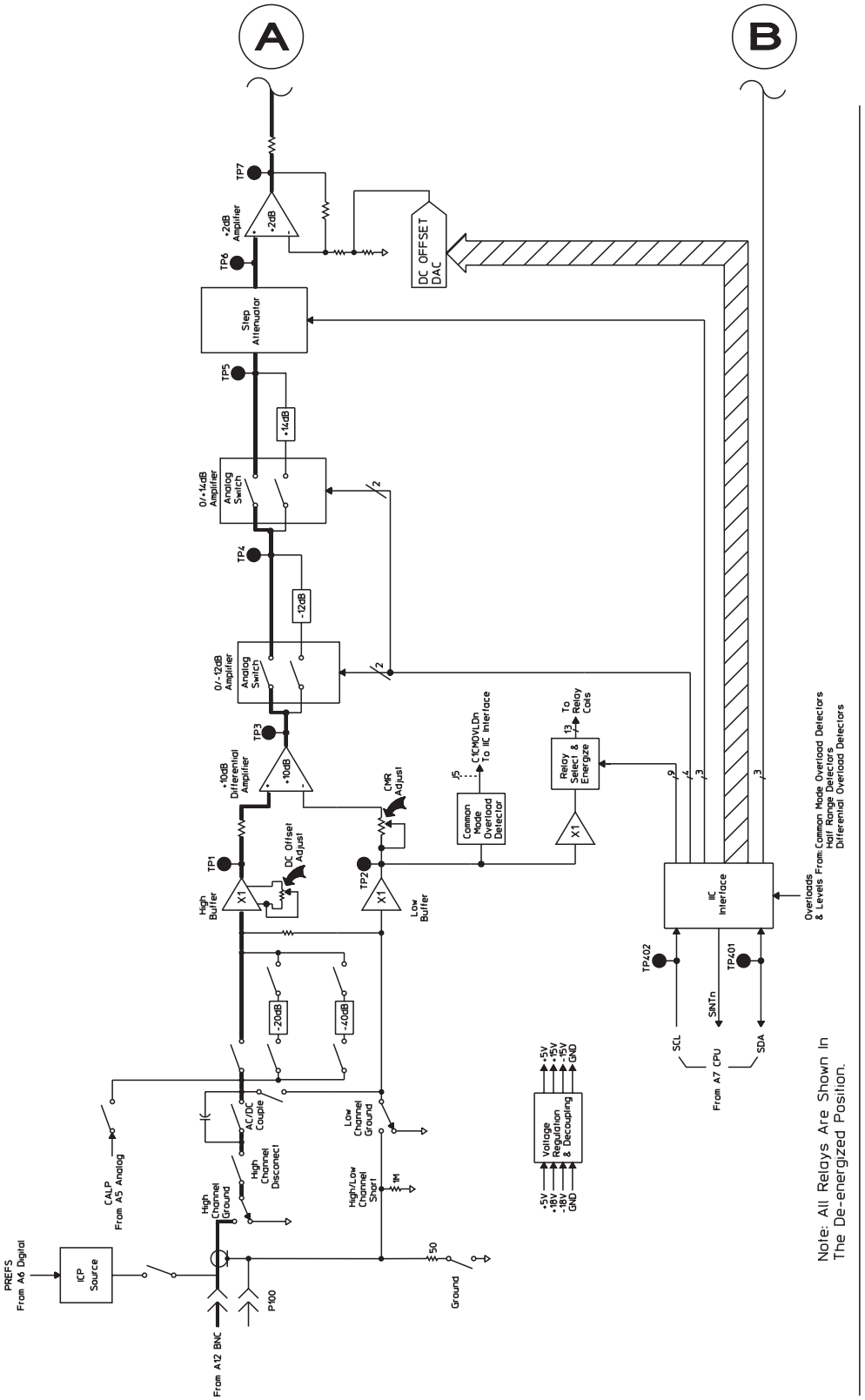
The A1 Input assembly is the input assembly for the two channel analyzer. The A1 Input assembly conditions the channel 1 and channel 2 input signals before they are sent to the analog-to-digital converter on the A5 Analog assembly. The A1 Input assembly sets the voltage ranges, conditions the input signals, and filters out alias components. Signal conditioning is done with relays, high and low buffers, and a series of amplifiers and attenuators. In addition, autozero DACs compensate for any dc offset added to the signals by the circuits on this assembly. This assembly also monitors the input signals for common mode or differential overloads and for half-range conditions. Unless stated otherwise, the following description applies to the block diagrams for both channel 1 and channel 2.

ICP Source	Supplies power to transducers such as accelerometers when enabled. The ICP Source is a 4.25 (1.5 mA floating current source. The power for the current source is obtained by switching the (15 V supplies at the sample frequency (262 kHz), isolating through a 1:1 transformer, rectifying and filtering. When disabled, the source is disconnected by a relay and the switching power supply is disabled.
Input Relays	Select one of the 0 dB, 20 dB, or 40 dB pads and configure the input. The relays are controlled by Relay Select & Energize.
Relay Select & Energize	Selects and energizes the input relays. Relay Select & Energize is controlled by the IIC Interface.
High Buffer	Buffers the HIGH input signal (BNC center conductor). The High Buffer contains a bootstrap circuit that prevents harmonic distortion and large common mode signals from saturating the buffer.
Low Buffer	Buffers the LOW input signal (BNC shell). The operation of the Low Buffer is identical to the High Buffer.
+10 dB Differential Amplifier	Begins the gain and attenuation stages. This amplifier subtracts the HIGH and LOW input signals from the high and low buffers. The common mode rejection adjustment, adjusts the +10 dB Differential Amplifier to reject common mode signals.
0 /–12 dB Amplifier	Can attenuate the signal by 12 dB.
0 /+14 dB Amplifier	Can amplify the signal by 14 dB.
Step Attenuator	Can attenuate the input signal from 0 dB to –14 dB, in 2 dB steps.
+2 dB Amplifier	Adds a gain of 2 dB and allows the DC Offset DAC to vary the dc offset of the input signal. The purpose of the amplifiers and attenuators up to this point is to ensure that the input signal does not overdrive the anti-alias filter or analog-to-digital converter.

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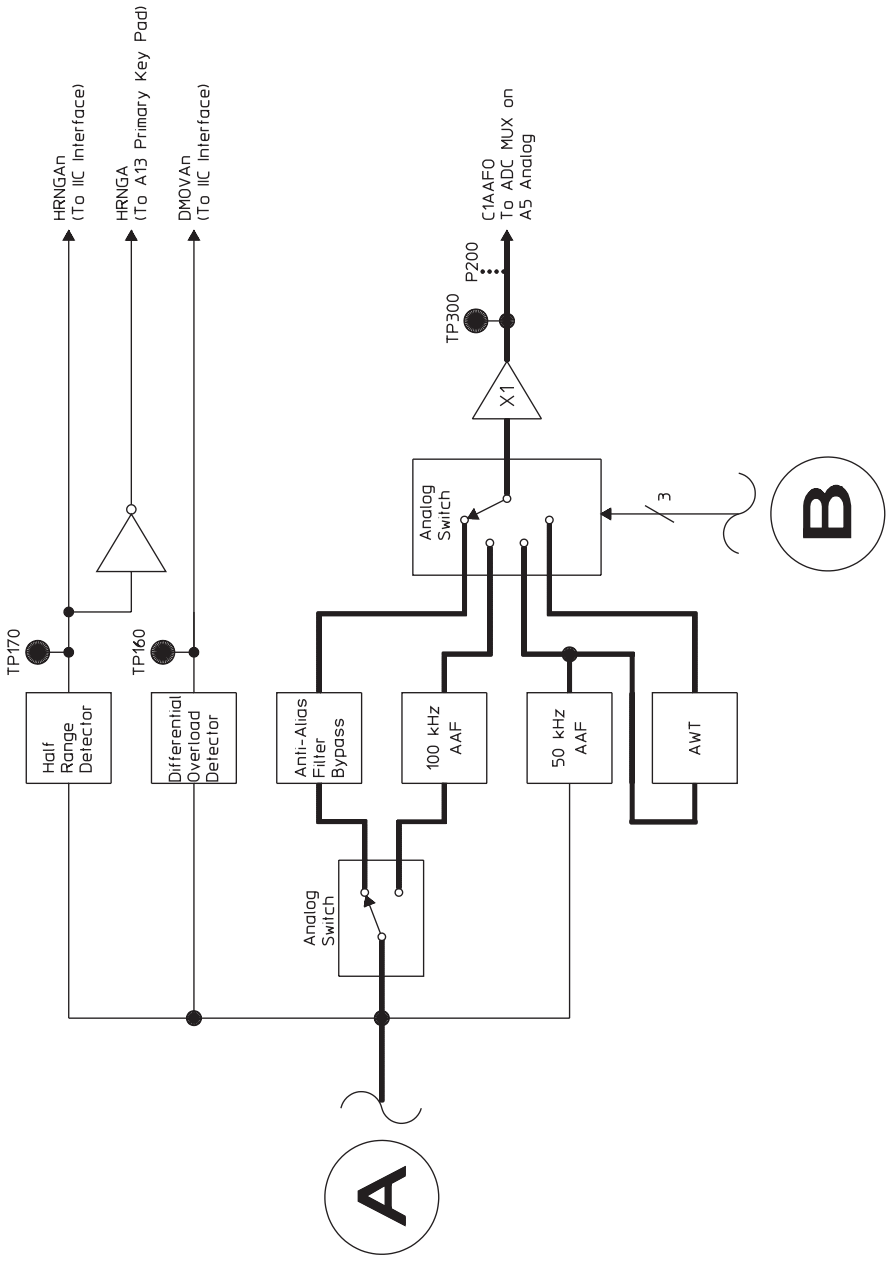
DC Offset DAC	Compensates for any dc offset added to the input signal due to circuitry in the signal path. The required dc offset is calculated during the analyzer's calibration routine and is added to the input signal in 0.345 mV increments by varying the dc offset at the inverting input of the +2 dB Amplifier (see "Calibration Routine Description" in chapter 10).
Anti-Alias Filter Bypass	Bypasses all filters.
100 kHz Anti-Alias Filter	Provides alias protection up to 100 kHz for single channel measurements. Only the channel 1 input path has a 100 kHz Anti-Alias Filter.
50 kHz Anti-Alias Filter	Provides alias protection up to 50 kHz for two channel measurements.
A-Weight Filter	Provides additional filtering in the 50 kHz anti-alias filter path for acoustic measurements.
Analog Switch	Selects one of four possible signals in the channel 1 input path to send to the ADC — the signal from the Anti-Alias Filter Bypass, 100 kHz Anti-Alias Filter, 50 kHz Anti-Alias Filter, or A-Weight Filter. In the channel 2 input path, the Analog Switch selects one of three possible signals to send to the ADC — the signal from the Anti-Alias Filter Bypass, 50 kHz Anti-Alias Filter, or A-Weight Filter.
Half Range and Differential Overload Detectors	Sense the signal at the anti-alias filters. When a detector detects a half-range or overload condition, a digital low is sent to the IIC Interface by the detector. The half-range detector also sends a control signal to the A13 Primary Keypad assembly when a half-range condition occurs.
IIC (Inter-IC) Interface	Contains 32 ports and connects the A1 Input assembly to the serial IIC bus. The A7 CPU assembly uses the IIC bus to configure the input circuits. When a common mode or differential overload occurs, the IIC Interface forces SINTn low to interrupt the CPU assembly. The CPU assembly then reads the IIC Interface to determine the type of interrupt and the channel it occurred on. During up/down autoranging, the A7 CPU queries the A1 Input assembly for half range status. For a description of the IIC bus, see the description of the IIC Controller for the "A7 CPU" later in this chapter.

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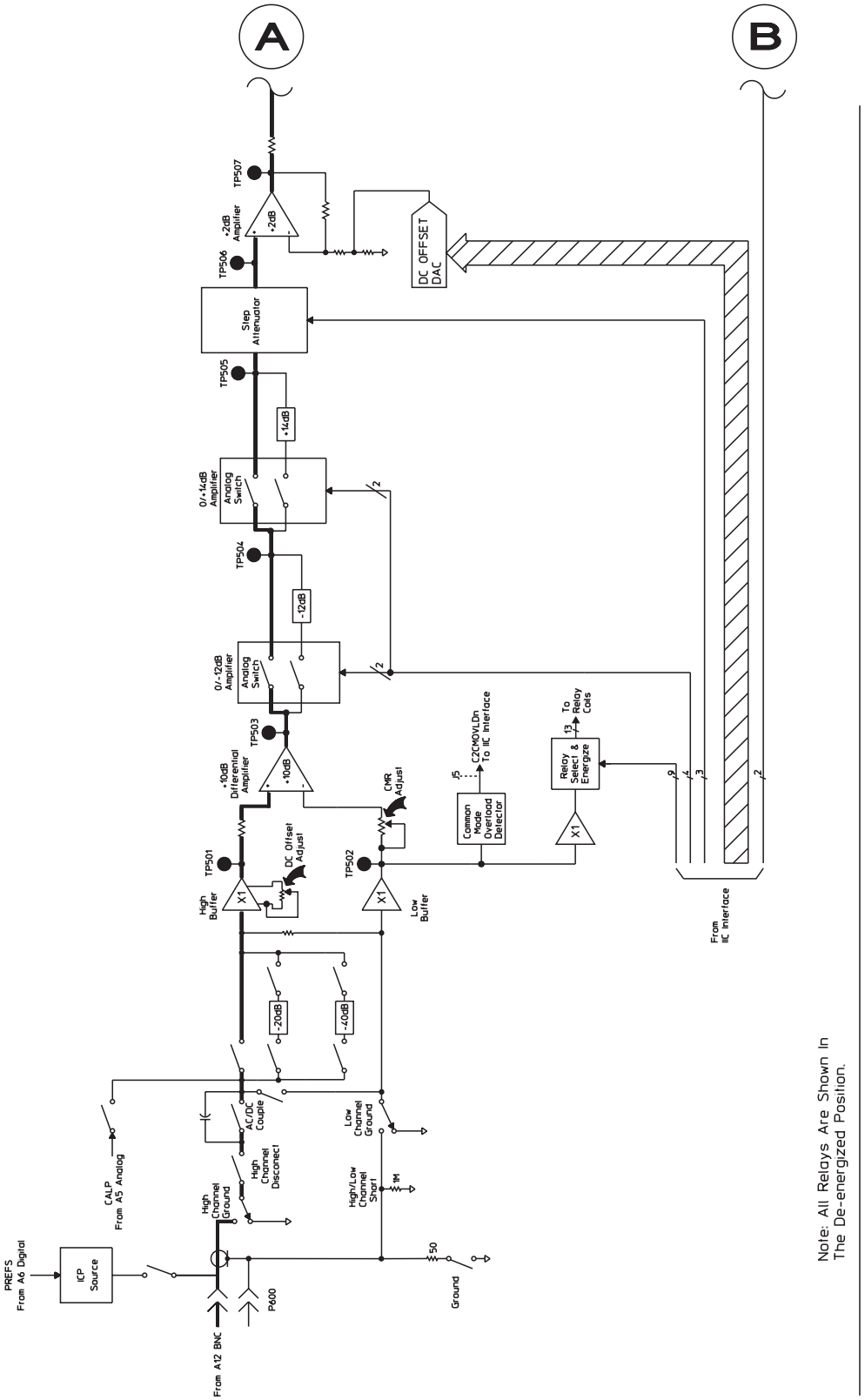
A1 Input Block Diagram: Channel 1

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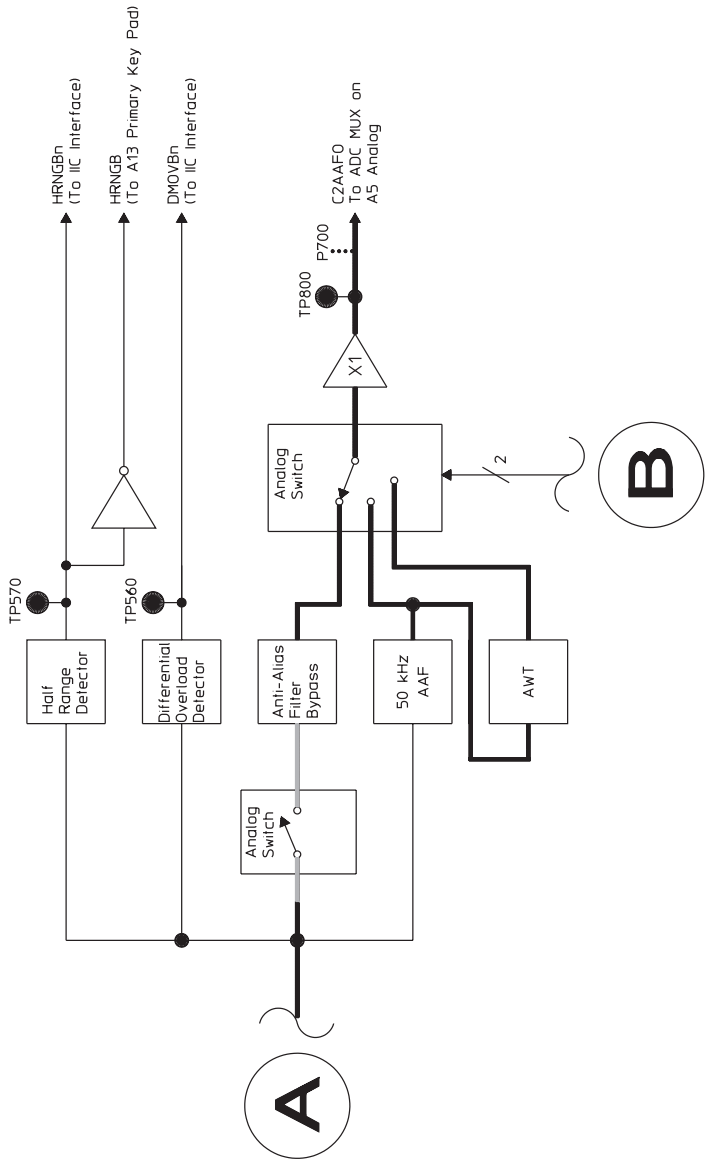
A1 Input Block Diagram: Channel 1 (continued)

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A1 Input Block Diagram: Channel 2

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A1 Input Block Diagram: Channel 2 (continued)

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A2 Input

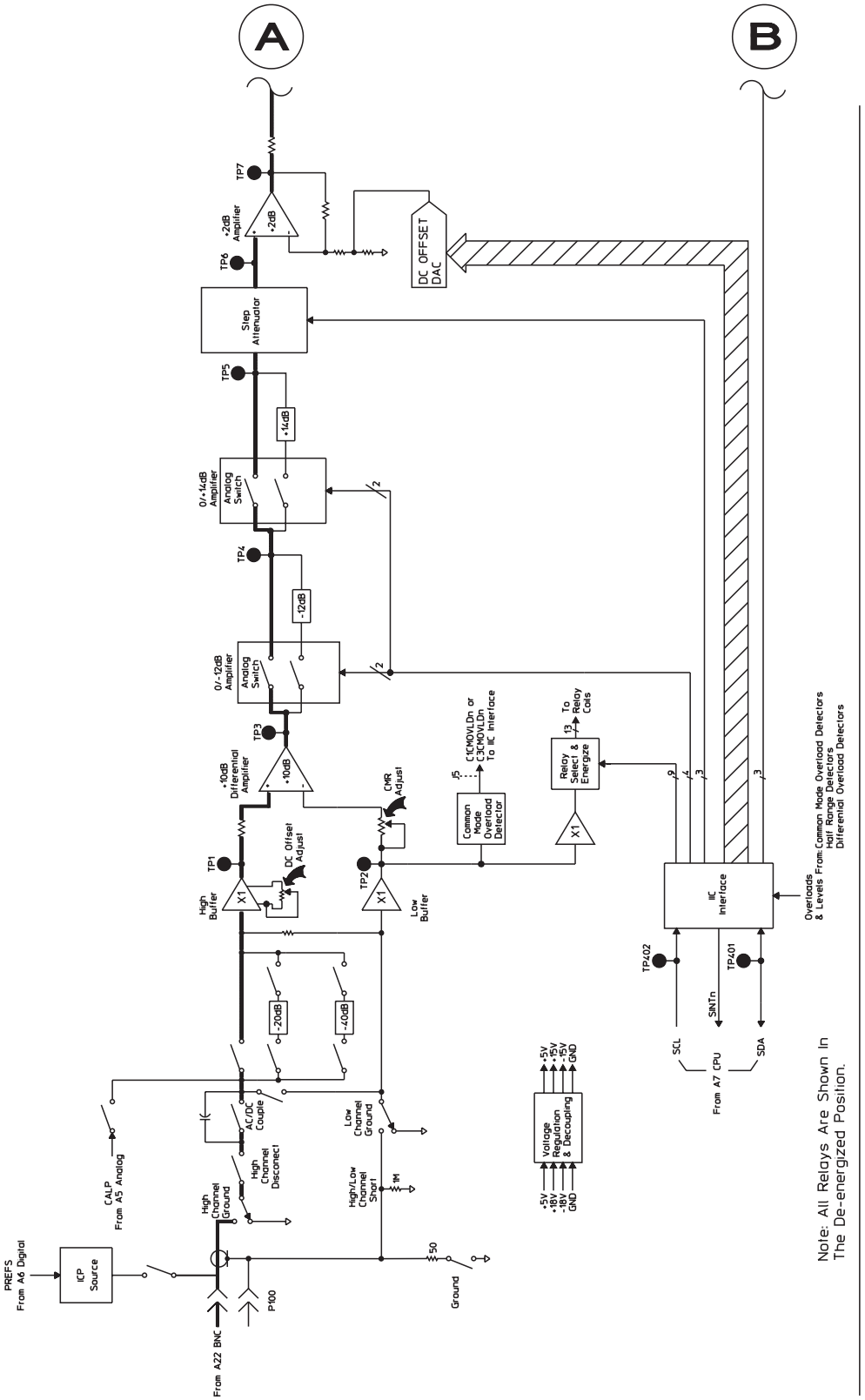
The A2 Input assembly is the input assembly for the four channel analyzer. The four channel analyzer contains two A2 Input assemblies. The A2 Input assembly connected to J1 on the Motherboard conditions the channel 1 and channel 3 input signals before they are sent to the analog-to-digital converter on the A5 Analog assembly. The A2 Input assembly connected to J2 on the Motherboard conditions the channel 2 and channel 4 input signals before they are sent to the analog-to-digital converter on the A5 Analog assembly. The Input assembly sets the voltage ranges, conditions the input signals, and filters out alias components. Signal conditioning is done with relays, high and low buffers, and a series of amplifiers and attenuators. In addition, autozero DACs compensate for any dc offset added to the signals by the circuits on this assembly. The assembly also monitors the input signals for common mode or differential overloads and for half-range conditions. Unless stated otherwise, the following description applies to the block diagrams for all four channels.

ICP Source	Supplies power to transducers such as accelerometers when enabled. The ICP Source is a 4.25 (1.5 mA floating current source. The power for the current source is obtained by switching the (15 V supplies at the sample frequency (262 kHz), isolating through a 1:1 transformer, rectifying and filtering. When disabled, the source is disconnected by a relay and the switching power supply is disabled.
Input Relays	Select one of the 0 dB, 20 dB, or 40 dB pads and configure the input. The relays are controlled by Relay Select & Energize.
Relay Select & Energize	Selects and energizes the input relays. Relay Select & Energize is controlled by the IIC Interface.
High Buffer	Buffers the HIGH input signal (BNC center conductor). The High Buffer contains a bootstrap circuit that prevents harmonic distortion and large common mode signals from saturating the buffer.
Low Buffer	Buffers the LOW input signal (BNC shell). The operation of the Low Buffer is identical to the High Buffer.
+10 dB Differential Amplifier	Begins the gain and attenuation stages. This amplifier subtracts the HIGH and LOW input signals from the high and low buffers. The common mode rejection adjustment, adjusts the +10 dB Differential Amplifier to reject common mode signals.
0 /–12 dB Amplifier	Can attenuate the signal by 12 dB.
0 /+14 dB Amplifier	Can amplify the signal by 14 dB.
Step Attenuator	Can attenuate the input signal from 0 dB to –14 dB, in 2 dB steps.
+2 dB Amplifier	Adds a gain of 2 dB and allows the DC Offset DAC to vary the dc offset of the input signal. The purpose of the amplifiers and attenuators up to this point is to ensure that the input signal does not overdrive the anti-alias filter or analog-to-digital converter.

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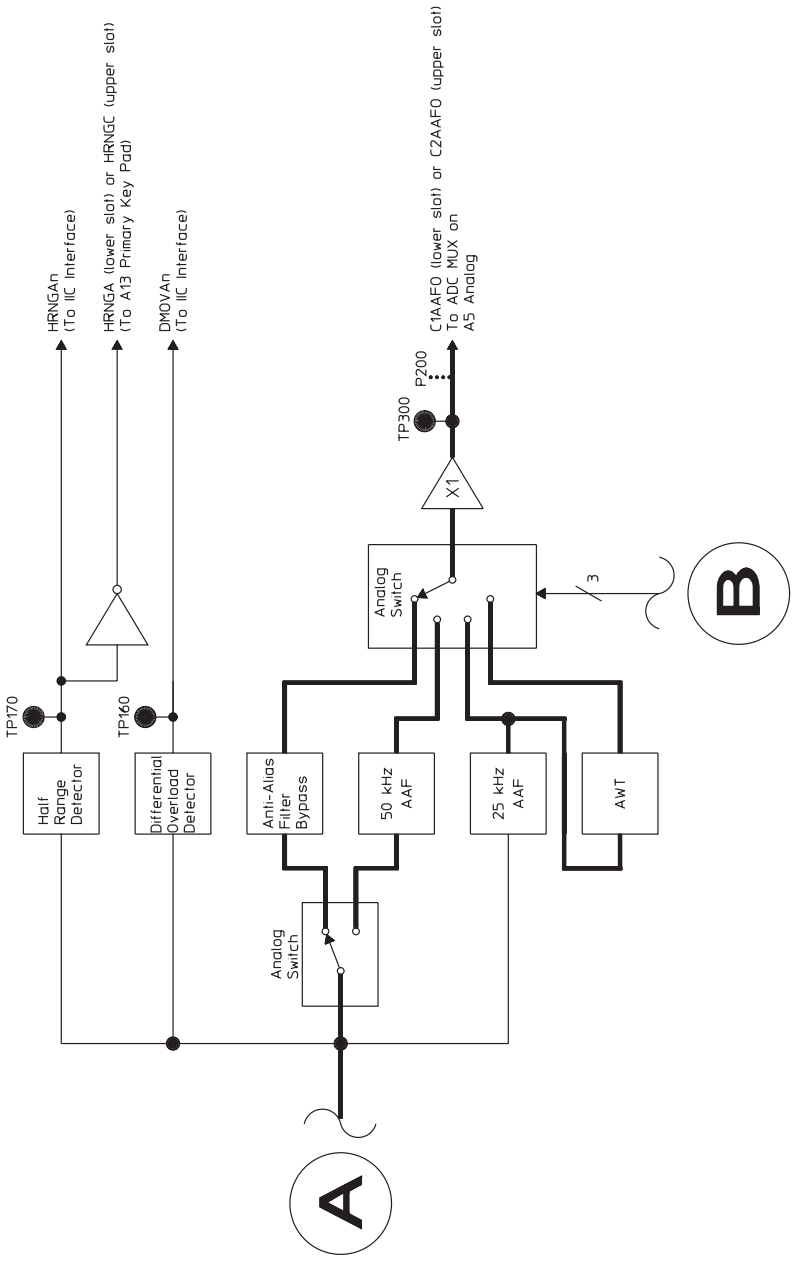
DC Offset DAC	Compensates for any dc offset added to the input signal due to circuitry in the signal path. The required dc offset is calculated during the analyzer's calibration routine and is added to the input signal in 0.3.45 mV increments by varying the dc offset at the inverting input of the +2 dB Amplifier (see "Calibration Routine Description" in chapter 10).
Anti-Alias Filter Bypass	Bypasses all filters.
50 kHz Anti-Alias Filter	Provides alias protection up to 50 kHz for two channel measurements.
25 kHz Anti-Alias Filter	Provides alias protection up to 25 kHz for four channel measurements.
A-Weight Filter	Provides additional filtering in the 25 kHz anti-alias filter path for acoustic measurements.
Analog Switch	Selects one of four possible signals in the channel 1 or channel 2 input path to send to the ADC — the signal through the Anti-Alias Filter Bypass, 50 kHz Anti-Alias Filter, 25 kHz Anti-Alias Filter, or A-Weight Filter. In the channel 3 or 4 input path, the Analog Switch selects one of three possible signals to send to the ADC — the Anti-Alias Filter Bypass, 25 kHz Anti-Alias Filter, or the A-Weight Filter.
Half Range and Differential Overload Detectors	Sense the signal at the anti-alias filters. When a detector detects a half-range or overload condition, a digital low is sent to the IIC Interface by the detector. The half-range detector also sends a control signal to the A13 Primary Keypad assembly that lights an LED when a half-range condition occurs.
IIC (Inter-IC) Interface	Contains 32 ports and connects the A2 Input assembly to the serial IIC bus. The A7 CPU assembly uses the IIC bus to configure the input circuits. When a common mode or differential overload occurs, the IIC Interface forces SINTn low to interrupt the CPU assembly. The CPU assembly then reads the IIC Interface to determine the type of interrupt and the channel it occurred on. During up/down autoranging, the A7 CPU queries the A1 Input assembly for half range status. For a description of the IIC bus, see the description of the IIC Controller for the "A7 CPU" later in this chapter.

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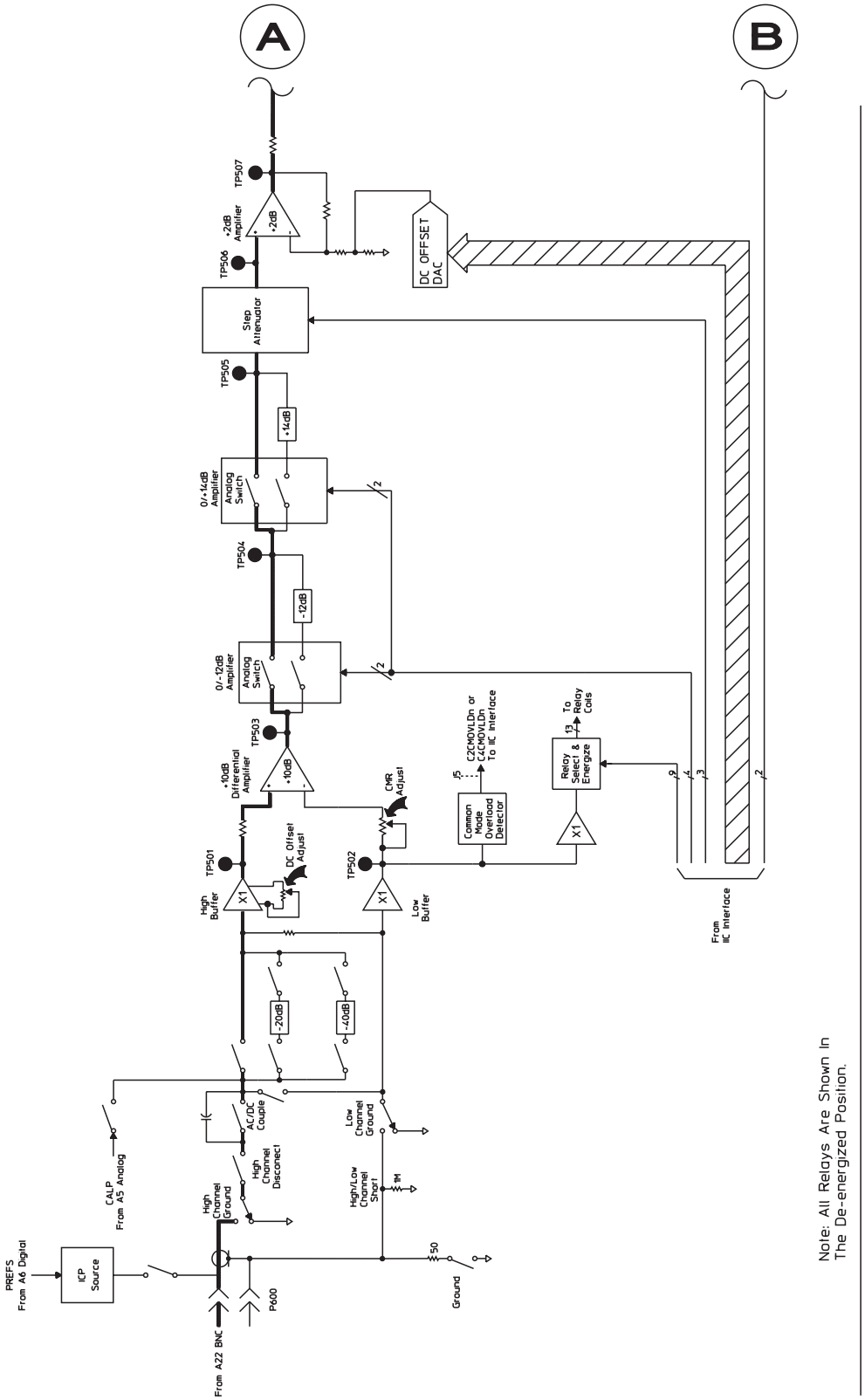
A2 Input Block Diagram: Channel 1 or Channel 2

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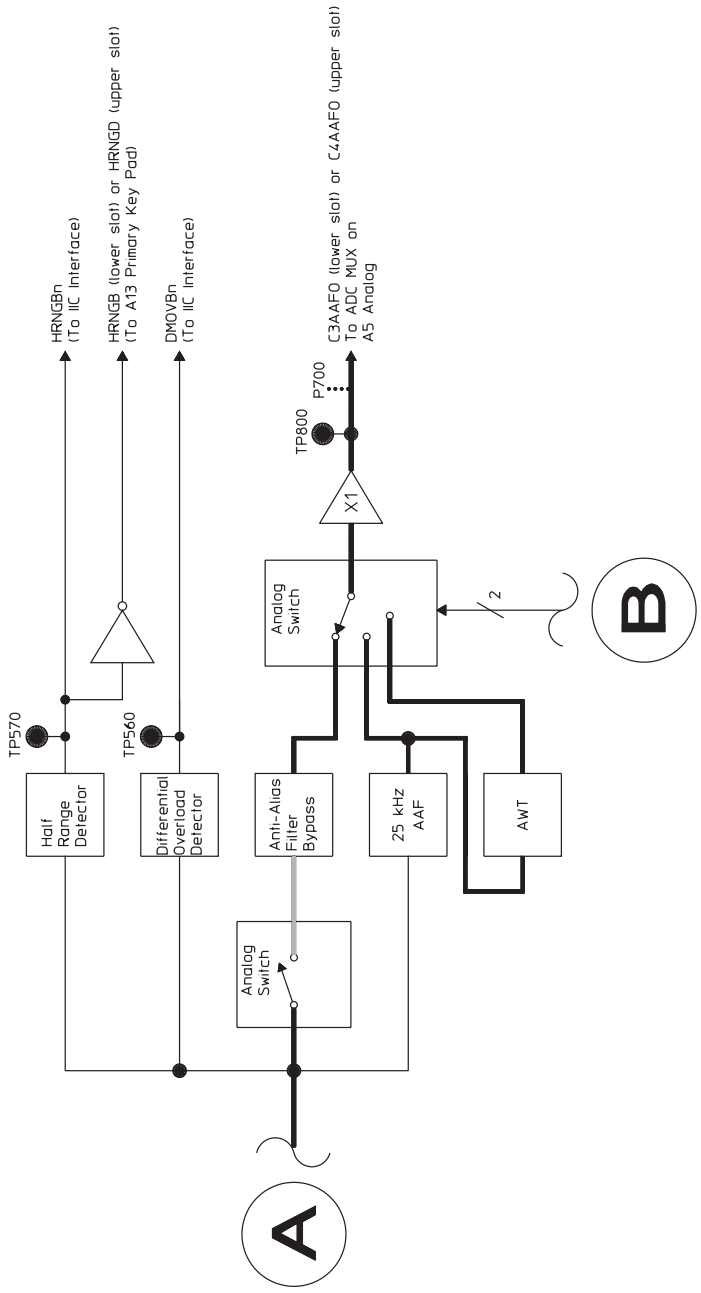
A2 Input Block Diagram: Channel 1 or Channel 2 (continued)

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A2 Input Block Diagram: Channel 3 or Channel 4

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A2 Input Block Diagram: Channel 3 or Channel 4 (continued)

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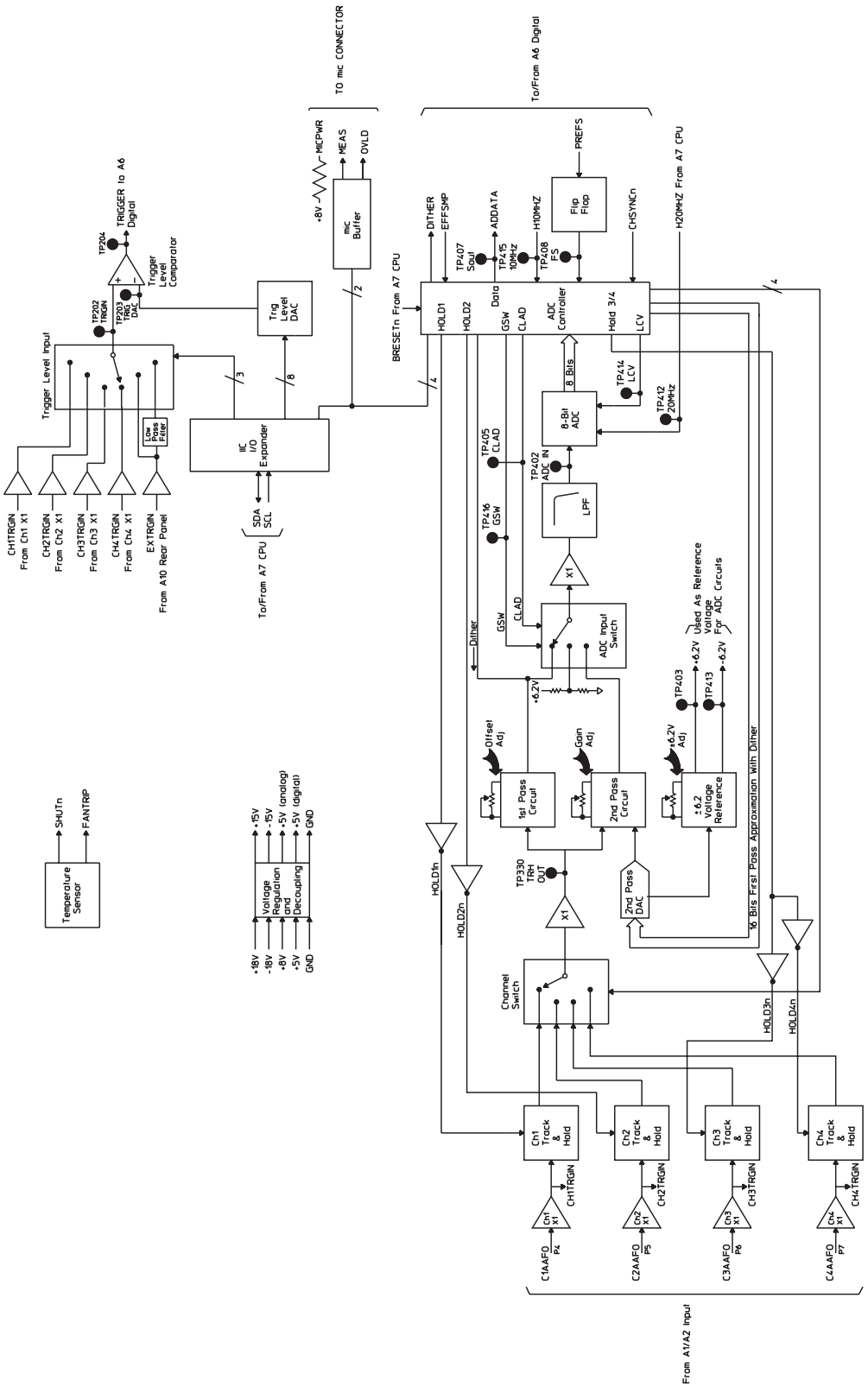
A5 Analog

The A5 Analog assembly converts the analog input from the A1 Input assembly or A2 Input assemblies to 16-bit serial, digital data. The Analog assembly also converts digital data from the A6 Digital assembly to the analog source output.

The input conversion process passes the analog inputs from all active channels through an 8-bit ADC (analog-to-digital converter) twice adding dither (noise) to improve linearity and the accuracy of low-level signals. All active inputs are sampled simultaneously and held until all have been converted. For the first-pass conversion, the input is scaled then converted to 8-bit serial, digital data. Dither is added to the first-pass data and the sum is converted to an analog voltage. The analog voltage is subtracted from the input and the difference is scaled then converted to 8-bit, serial data in the second pass. The first-pass and second-pass values are added to get the final 16-bit data word. A third conversion clears the 8-bit ADC.

Channel 1 Track & Hold	Holds a voltage sample of the channel 1 input signal for the period of time required by the ADC circuits to digitize the voltage.
Channel 2 Track & Hold	Holds a voltage sample of the channel 2 input signal for the period of time required by the ADC circuits to digitize the voltage.
Channel 3 Track & Hold	Holds a voltage sample of the channel 3 input signal for the period of time required by the ADC circuits to digitize the voltage.
Channel 4 Track & Hold	Holds a voltage sample of the channel 4 input signal for the period of time required by the ADC circuits to digitize the voltage.
Channel Switch	For the two channel analyzer, the Channel Switch multiplexes the channel 1 and channel 2 input signals during two channel measurements . During single channel measurements, the channel 1 and channel 2 signals are not multiplexed. Instead, the Channel Switch is fixed to the output of the Channel 1 Track & Hold. For the four channel analyzer, the Channel Switch multiplexes the channel 1 and channel 2 input signals during two channel measurements. During four channel measurements, the Channel Switch multiplexes the channel 1, 2, 3, and 4 input signals. The output of the Channel Switch is converted to a 16-bit digital word by passing the signal through an 8-bit ADC twice.
1st Pass Circuit	Divides the Channel Switch output by four and level shifts it to the 8-bit ADC input range of 0 to –0.5 V.
ADC Controller	Adds dither (noise) to the first pass signal to increase the accuracy and reduce the non-linearity of the Analog-to-Digital conversion. After the first pass signal is filtered and converted to an 8-bit word, the ADC Controller adds the dither and outputs a 16-bit word to the 2nd Pass DAC. After the second pass signal is filtered and converted to an 8-bit word, the ADC Controller adds the second pass word to the first pass word to obtain a 16-bit data word. The ADC Controller then sends the converted data as ADDATA to the A6 Digital assembly. The ADC Controller also detects an ADC overload when the signal to the analog-to-digital converter is too high. The overload information is sent as ADCOL and ADCUL to the A6 Digital assembly.

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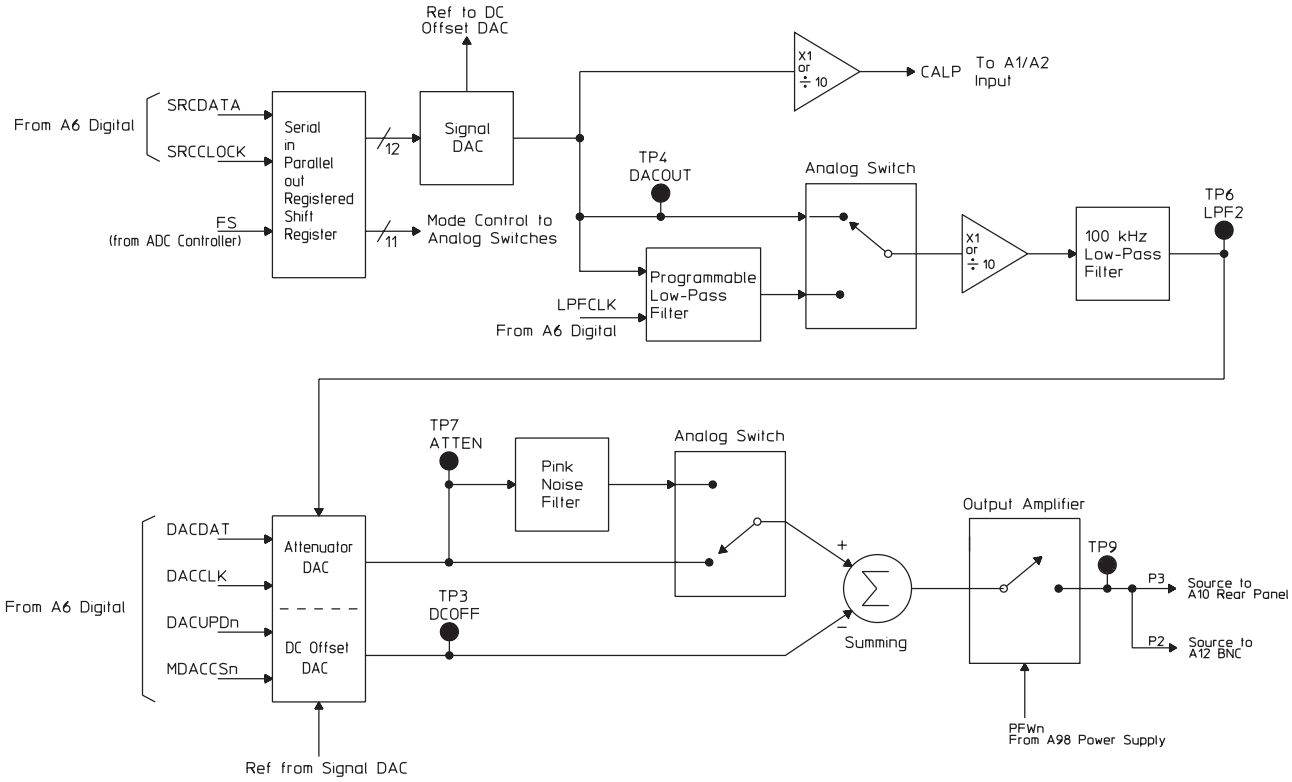


A5 Analog Block Diagram: ADC and Trigger

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ADC Input Switch	Connects the first pass signal to the low pass filter on the first pass. On the second pass, the ADC Input Switch connects the second pass signal to the low pass filter. After the second pass, the ADC Input Switch connects a 0.34 Vdc signal to the low pass filter to reset the 8-Bit ADC.
Low Pass Filter	Reduces noise and prevents high frequency signals from overdriving the 8-bit ADC.
8-Bit ADC	Converts the signal to an 8-bit word.
2nd Pass DAC	Converts the first pass word plus dither to a voltage that is sent to the 2nd Pass Circuit.
2nd Pass Circuit	Compares the output of the 2nd Pass DAC (converted first pass signal plus dither) to the original input signal (which is still held by the Track & Hold) and produces a difference voltage. This difference voltage is the second pass signal.
±*6.2 Voltage Reference*	Reduces the error due to temperature variations. This voltage reference is used by the 1st Pass Circuit, 2nd Pass Circuit, ADC Input Switch, 8-bit ADC, and Track & Hold. Since the 8-bit ADC's gain is derived from this voltage reference, the adjustment for this voltage reference is also the gain adjustment for the 8-bit ADC.
Trigger-Level Input	Connects the appropriate signal to the Trigger-Level Comparator.
Temperature Sensor	Senses the analyzer's internal temperature. If the internal temperature exceeds a set point, this circuit sets FANTRIP high which turns the fan back on if the fan was turned off by the user. If the temperature becomes excessive, this circuit sets SHUTn low which forces all A98 Power Supply assembly output voltages to zero.
Trigger-Level Comparator	Compares the signal level with the value from the Trigger Level DAC.
Trigger Level DAC	Provides the trigger level. The A7 CPU assembly sets the trigger level via the IIC bus using the value set with the [TRIGGER SETUP] and [LEVEL] softkeys.
Mic Buffer	Buffers control signals for the optional sound intensity probe. When a measurement is being made, the MEAS line goes high to turn on the probe's green LED. If an overload occurs during the measurement, the OVLD line goes high to turn on the probe's yellow LED.
IIC Interface	Provides the interface between the A7 CPU assembly and the A5 Analog assembly.
Serial In Parallel Out Shift Register	Provides the mode control to the Analog Switches and the digital source data to the DAC.
Signal DAC	Converts the digital source data to an analog signal. During calibration, the analog signal from the DAC is buffered or attenuated by 10. The calibration signal (CALP) is then routed to each input channel.
Programmable Low-Pass Filter	Filters the analog signal from the Signal DAC when selected. Filter bandwidth is set by LPFCLK from the A6 Digital assembly; it can be set from 51.2 kHz to 1.56 Hz in binary steps. Random noise and burst random noise signals below 51.2 kHz are filtered. Arbitrary signals below 51.2 kHz can be filtered using the front panel keys.
100 kHz Low-Pass Filter	Provides image rejection, reduces noise, and prevents high frequency signals from overdriving the Attenuator DAC. It also compensates for sinx/x rolloff at the 262.144 kHz sample rate.
Attenuator DAC/DC Offset DAC	Attenuates the signal and generates a dc offset.
Pink Noise Filter	Shapes the noise for a flat response in octave mode.
Summing	Combines the signal with the dc offset.
Output Amplifier	Amplifies and buffers the signal. A relay disconnects the signal from the SOURCE connector 10 ms before the A98 Power Supply assembly's output voltages fall out of regulation.

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A5 Analog Block Diagram: Analog Source and Calibrator

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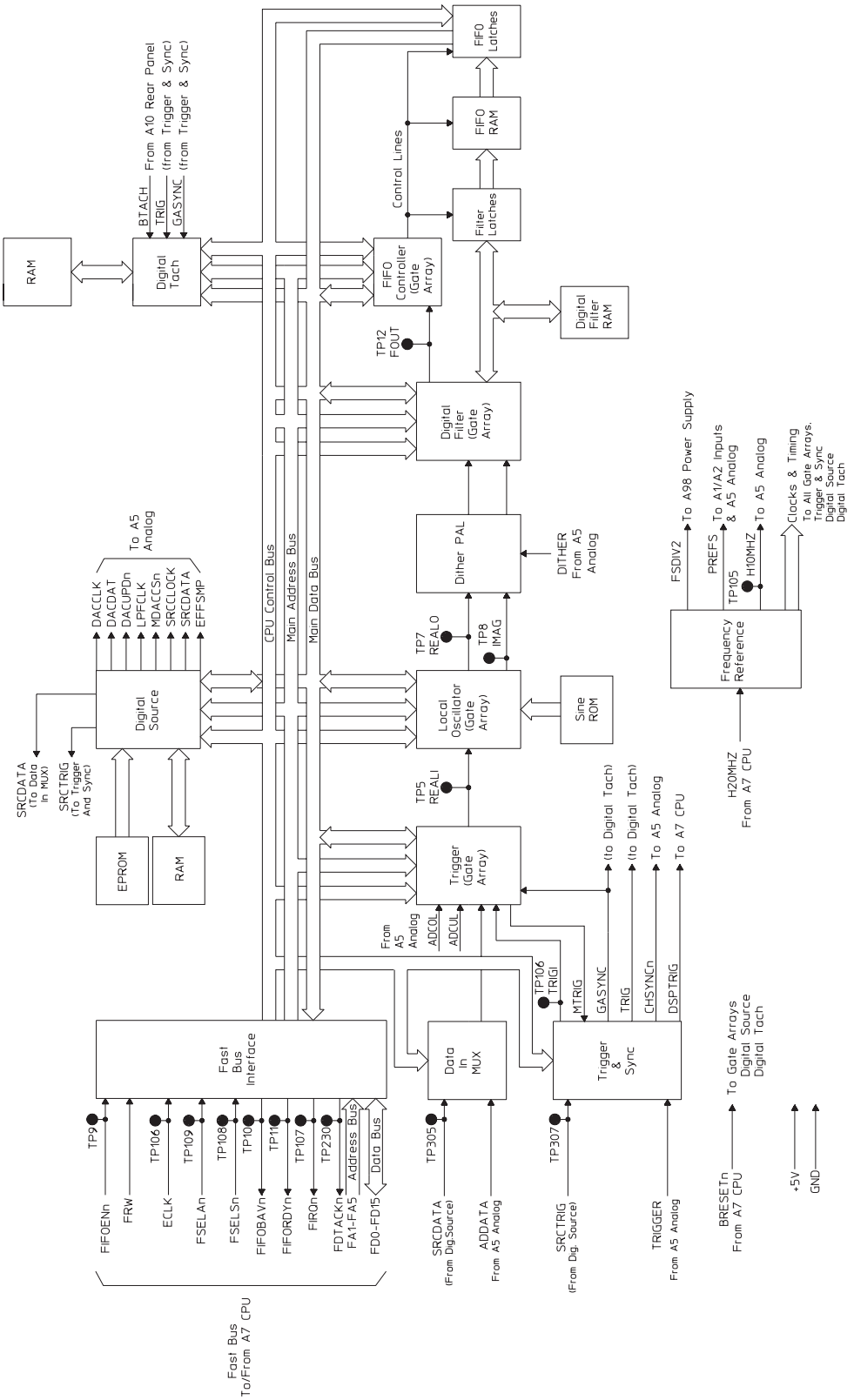
A6 Digital

The A6 Digital assembly prepares the digital input data for the A7 CPU assembly. The Digital assembly also generates the digital source data for the A5 Analog assembly. The Digital assembly receives the input signals as 16-bit serial, digital data from the Analog assembly. The Digital assembly uses digital signal processing to prepare the data for the CPU assembly. The CPU assembly configures the Digital assembly via the fast bus. This includes setting up the source, calibrator, and all gate arrays. See “A99 Motherboard” in chapter 9 for a description of the fast bus signals. This assembly provides the following:

- Trigger
- Local Oscillator
- Digital Filter and RAM
- FIFO Controller and RAM
- Digital Source
- Digital Tachometer
- ADC timing and synchronization signals

Data in MUX	Selects ADDATA from the A5 Analog assembly for most modes of operation. For time capture and some self-tests, the Data in Mux selects SRCDATA from the Digital Source.
Trigger & Sync	Pulls TRIGI low to inform the Trigger circuit that the selected trigger occurred. Synchronizes the ADC (on the A5 Analog assembly), Digital Source, Digital Tach, and Trigger Gate Array.
Trigger Gate Array	Synchronizes data transfer by telling the FIFO Controller when to collect the time record in FIFO RAM. This circuit also controls pre- and post-trigger.
Local Oscillator	Frequency shifts the data to allow start frequencies other than 0 hertz. To frequency shift the data, the Local Oscillator digitally mixes or heterodynes the data down into the range of the FFT span selected. This makes the data complex and the sample is now represented by two serial, digital signals — REALO and IMAG. During baseband measurements (where the start frequency is 0 hertz), the data is only scaled through the Local Oscillator.
Dither PAL	Adds span-dependent dither (noise) to the digital data.
Digital Filter	Filters the digital data before placing the samples in the Filter Latches for the FIFO. As the Digital Filter operates, it may discard some samples to effectively reduce the sample rate. This allows frequency spans narrower than full span (due to the properties of the FFT, the sample rate must be varied to vary the frequency span). During full span measurements, no samples are discarded and data is just passed through.
Digital Filter RAM	Stores intermediate values for the Digital Filter during the filtering process.
Filter Latches	Temporarily hold a data point as it is passed from the Digital Filter to the FIFO RAM.

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A6 Digital Block Diagram

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FIFO Controller	Gathers the data from the Filter Latches when the selected trigger occurs and places the data into FIFO RAM. After a time record is collected, this circuit controls data flow from FIFO RAM to the CPU.
FIFO RAM	Stores data from the Digital Filter. When the FIFO RAM has a complete time record, the FIFO Controller pulls FIFOBAVn low to inform the A7 CPU assembly that a block of data is ready for transfer.
FIFO Latches	Hold a data sample until the Fast Bus Interface is ready to transfer the sample.
Digital Source and RAM	The A7 CPU assembly loads the Digital Source RAM by putting the data needed by the Digital Source into main memory (on the A8 Memory assembly). The CPU assembly then performs a memory-to-memory DMA transfer from main memory to Digital Source RAM via the fast bus. This data represents any source type except random, pink, or fixed sine which are generated internally by the Digital Source. Any source type, except fixed sine, will be frequency-translated and bandwidth-limited to correspond to the instrument frequency range.
Digital Tachometer and RAM	Counts and stores the buffered tachometer pulses (BTACH) from the A10 Rear Panel assembly. At the start of a measurement, GASYNC sets the Digital Tachometer's counter to zero. The counter starts counting and the tachometer signal latches the counter outputs. The latched tachometer times are stored in RAM and read over the Fast Bus Interface by the A7 CPU assembly as needed.
Frequency Reference	Provides all clocks and timing for the gate arrays, Trigger & Sync, Digital Source, and Digital Tach. In addition, the Frequency Reference generates PREFS and H10MHZ to synchronize data transfers from the ADC on the A5 Analog assembly, and FSDIV2 for the A98 Power Supply assembly.
Fast Bus Interface	Connects the A6 Digital assembly to the fast bus. The fast bus transfers time records from FIFO RAM to the A7 CPU assembly for processing. The fast bus is also used by the CPU assembly to read tachometer data, to send time capture data or source data to the Digital Source, and to configure the Trigger, Local Oscillator, Digital Filter, FIFO Controller, Digital Source and Digital Tachometer.

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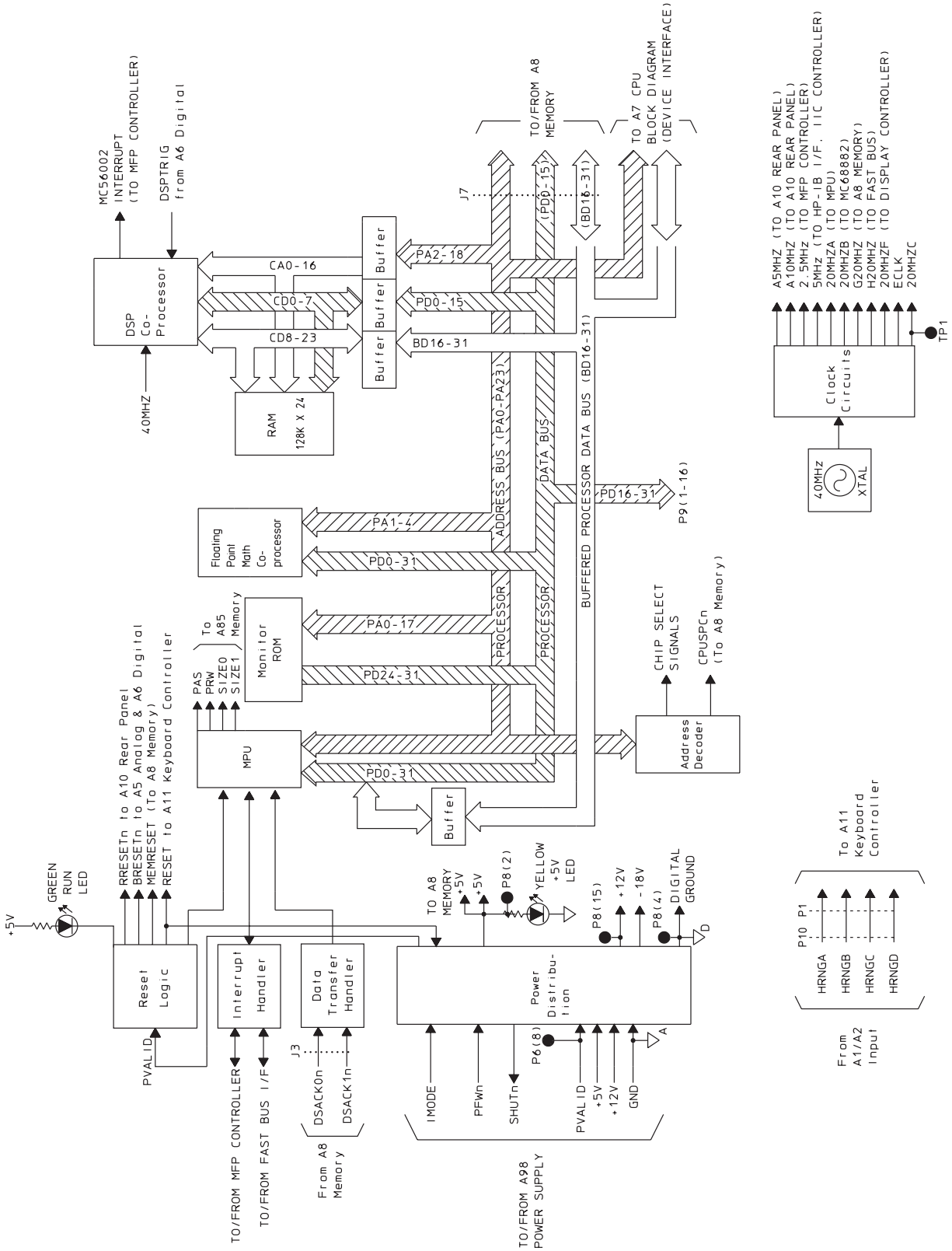
A7 CPU

The A7 CPU assembly controls the entire analyzer. It performs multiple tasks, such as:

- Initiating the power-up sequence and calibration routines
- Capturing front panel keystrokes
- Configuring the measurement hardware
- Processing input data from the A6 Digital assembly
- Controlling the A101 Display assembly
- Monitoring the hardware for faults or overloads
- Running the self tests
- Handling all data transfers for the fast bus, rear bus, and A100 Disk Drive assembly

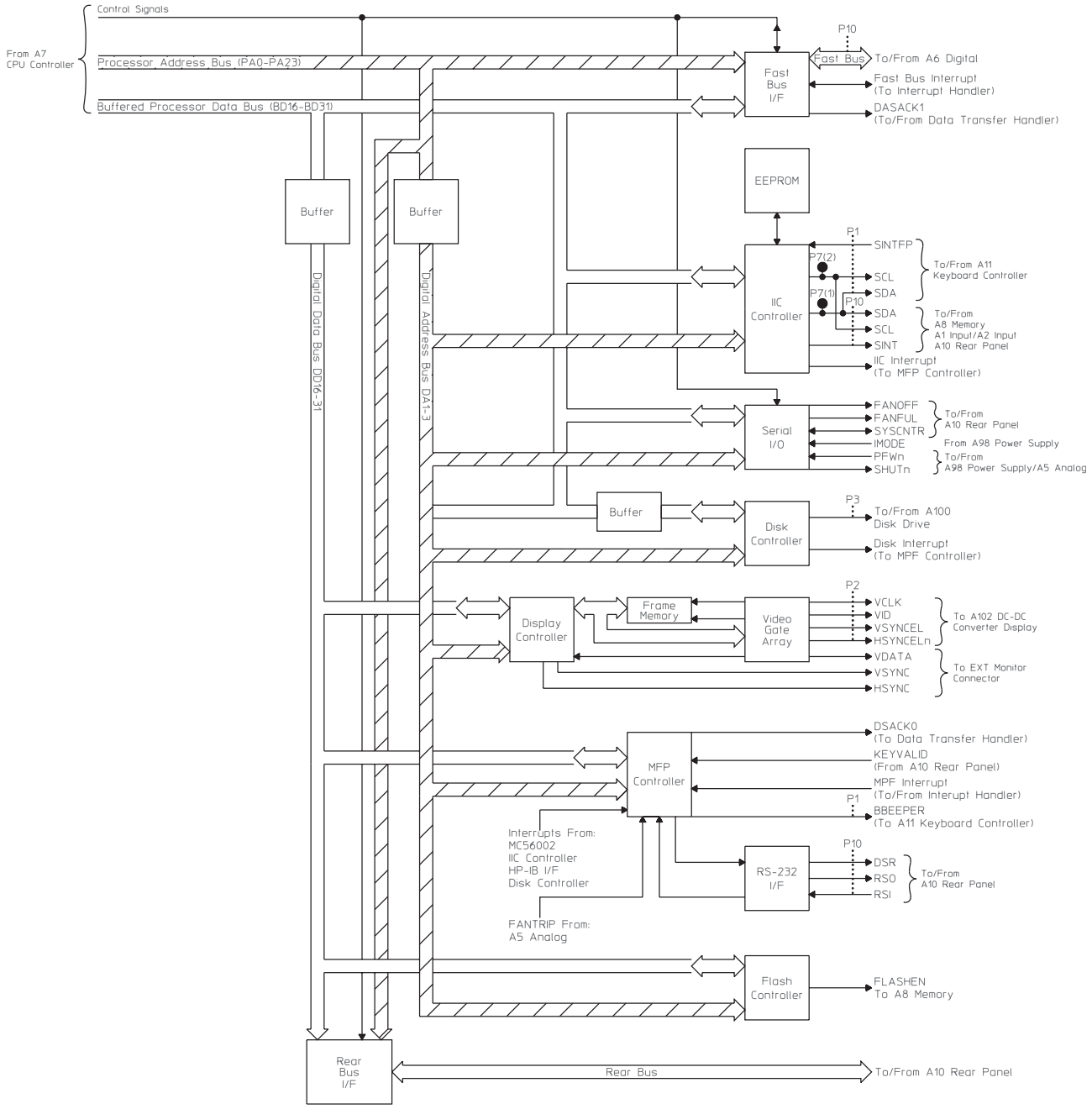
MPU (Microprocessor)	Controls the processor address bus and the buffered processor data bus. At power-up, this circuit initializes the analyzer from the information stored in the Monitor ROM. This circuit also processes interrupts from the Interrupt Handler and synchronizes data transfers on the processor data bus with the Data Transfer Handler. The MPU also has access to battery-backed-up SRAM on the A8 Memory assembly. This allows the CPU assembly to store and update information such as the analyzer's address, default disk, and peripheral addresses.
Monitor ROM	Stores the information used by the MPU to initialize the analyzer.
DSP and Floating Point Math Co-processor	Relieve the MPU of math intensive-tasks by supplying the computational power needed for accurate, high-speed signal processing operations — for example, windowing and Fast Fourier Transform (FFT) for the analyzer's narrow-band zoom mode. The DSP Co-processor is a high speed (40 MHz) math co-processor that performs complex mathematical operations. The Floating Point Math Co-processor performs floating point mathematical operations. The DSP Co-processor and Floating Point Math Co-processor work as slave co-processors to the MPU and the DSP Co-processor has its own RAM. This arrangement leaves the MPU free to perform other functions while the DSP Co-processor and Floating Point Math Co-processor perform math-intensive operations.
Interrupt Handler	Processes interrupts for the MPU. The Interrupt Handler sets the interrupt priority level and returns an interrupt acknowledge to the circuit that generated the interrupt. If the MFP controller causes an interrupt, the MPU reads a status byte from the MFP controller to determine the circuit that caused the interrupt.
Data Transfer Handler	Synchronizes data transfers in the analyzer with the MPU. When a data transfer occurs, the Data Transfer Handler notifies the MPU when the transfer is complete.
Clock Circuits	Provide the clocks for the CPU assembly and the A8 Memory assembly.

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A7 CPU Block Diagram

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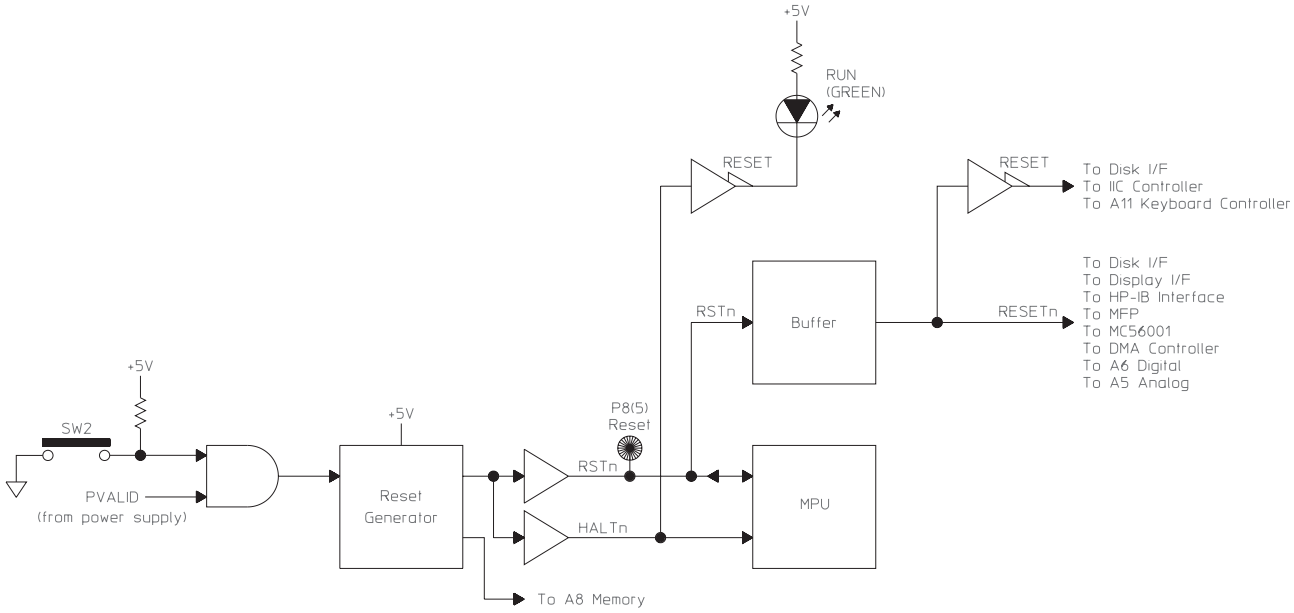
A7 CPU Block Diagram: Interface

Reset Logic

Puts the analyzer into a known state. A reset occurs at power-up and power-down (PVALID from the A98 Power Supply assembly goes high), when the reset switch S2 (located on the CPU assembly) is pressed, or when a RESET instruction is executed.

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PVALID from the power supply goes high when +5 volts reaches a valid level. The Reset Generator produces a 128 ms reset pulse when PVALID goes high and S2 is open, or when S2 is closed then opened and PVALID is high. At the end of the reset pulse, RSTn goes high, which terminates the reset and allows all circuits to begin operation.



Reset Logic

Fast Bus Interface

Connects the CPU assembly to the fast bus. All data transfers between the A6 Digital assembly and the CPU assembly occur over the fast bus. The fast-bus address lines (FA0 through FA5) and data lines (FD0 through FD15) are simply extensions of the processor address and data busses. This allows fast transfers between the two assemblies. See ''A99 Motherboard'' in chapter 9 for a description of the fast bus signals.

MFP (Multiple-Function Peripheral) Controller

Handles interrupts and handshaking during data transfers for the IIC Controller, Disk Controller, Display Controller, and RS-232 Interface.

Interrupts from these circuits are sent to the MFP Controller. When the MFP Controller receives an interrupt, it interrupts the prioritized Interrupt Handler, which in turn interrupts the MPU. The MPU then reads a status byte from the MFP Controller to determine the cause of the interrupt. The MFP Controller also tells the Data Transfer Handler if any data transfers occurred for these circuits.

IIC (Inter-IC) Controller

Manages the IIC bus. It allows direct communication between the CPU assembly and the following assemblies via the IIC bus:

- A1 or A2 Input
- A5 Analog
- A8 Memory (calendar/clock chip)
- A10 Rear Panel (tachometer control)
- A11 Keyboard Controller

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All of these assemblies appear as slaves to the IIC Controller. The IIC Controller has access to EEPROM, which allows the CPU assembly to store information such as the analyzer's serial number. If the CPU assembly is replaced, the EEPROM integrated circuit (U27) on the faulty assembly must be removed and inserted into the new assembly (see ''What to do before replacing the CPU assembly'' in chapter 6). The IIC Controller also has access to a battery backed real-time clock on the A8 Memory assembly.

The IIC bus consists of the following four signal lines:

- SCL (serial clock)
- SDA (serial data)
- SINTn (serial interrupt)
- SINTFPn (serial interrupt for A11 Keyboard Controller assembly)

Pull-up resistors connect these signals to logic high (all four lines are open collector or open drain). See ''A8 Memory,'' ''A11 Keyboard Controller,'' and ''A99 Motherboard'' in chapter 9 for descriptions of the IIC signals.

Disk Controller Allows the analyzer to store or retrieve data from the internal 3.5-inch flexible A100 Disk Drive assembly. It provides all the control signals necessary to operate the Disk Drive assembly. The Disk Controller performs the following functions:

- Turns on the disk drive motor
- Selects the disk drive head
- Turns on the disk drive LED
- Selects a track on the flexible disk
- Writes or reads serial data to or from the flexible disk

The Disk Controller puts data on the flexible disk in a bit stream that consists of data and clock bits. When data is read from the disk, this circuit separates the data bits from the clock bits, converts the serial data bits to an 8-bit parallel word, and puts the data word on the processor data bus. The operation is reversed when data is written to the disk.

Display Controller Takes parallel data from the processor data bus and places the data in Frame Memory.

Frame Memory Consists of four 256K ⎫4-bit RAM chips. One bit in Frame Memory corresponds to one pixel on the display. The data in Frame Memory is then sent to the Video Gate Array.

Video Gate Array Continuously updates the display with the contents of Frame Memory. The Video Gate Array also supplies the horizontal and vertical sync signals for the display.

RS-232 Interface Allows the analyzer to communicate with other devices such as terminals, plotters, or printers via Instrument Basic. See *Using Instrument Basic with the Agilent 35670A* for additional information.

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A8 Memory

The A8 Memory assembly provides the A7 CPU assembly with ROM, dynamic RAM (DRAM), static RAM (SRAM), and a real-time clock.

Memory Controller

Provides the interface between the A7 CPU assembly and the Memory assembly for data transfer.

FLASH ROM, DRAM, and SRAM

Stores data in 32-bit words. To access a memory location, the A7 CPU assembly puts the address of the desired 32-bit word on the processor address bus. The following user-accessible states are stored in SRAM. These states are unchanged by power-up or preset.

[**Local/Gpib**]
[SYSTEM CONTOLLR]
[ADDRESSBL ONLY]
[ANALYZER ADDRESS]
[PLOTTER ADDRESS]
[PRINTER ADDRESS]
[DISK ADDRESS]
[DISK UNIT]

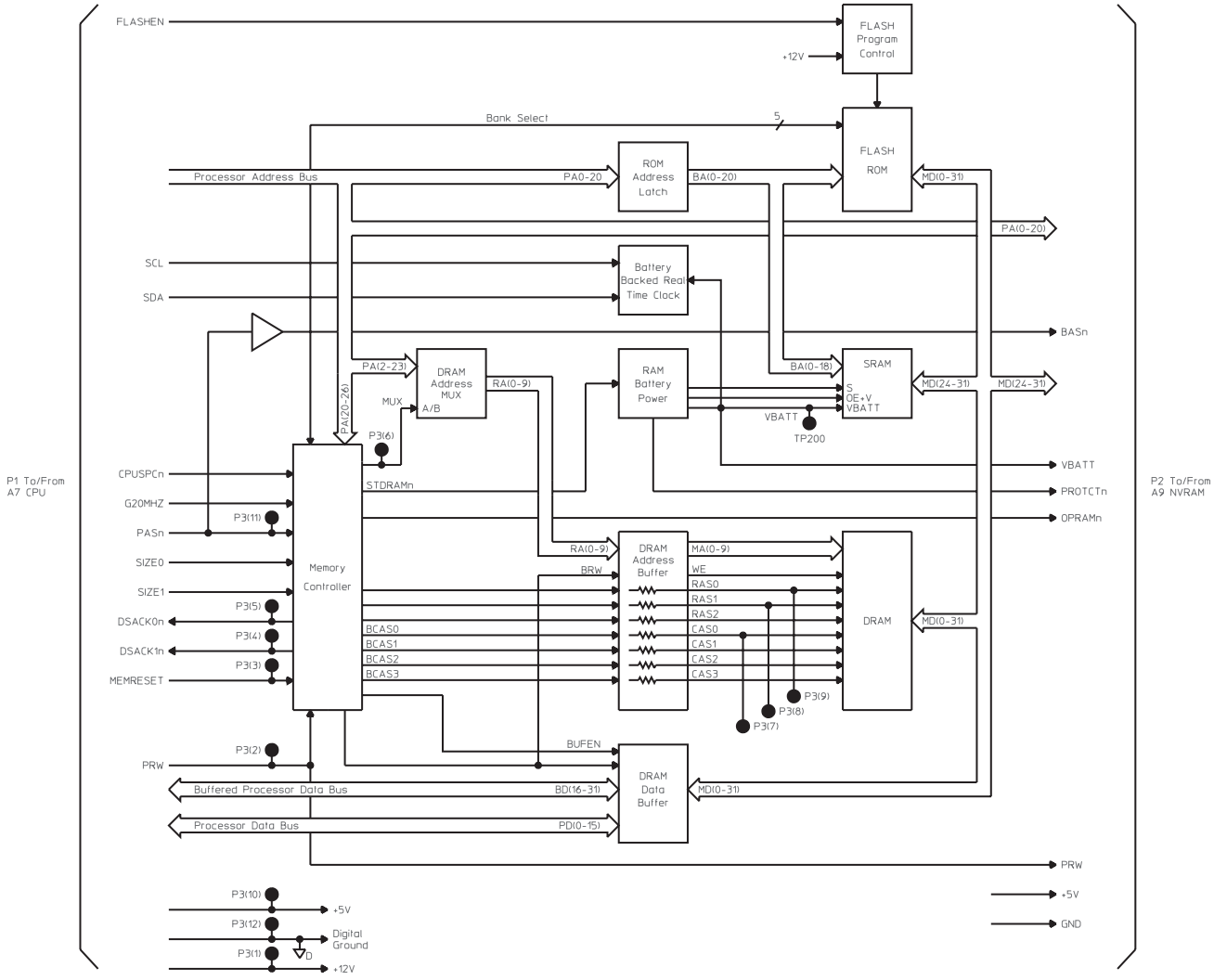
[**System Utility**]
[CLOCK SETUP]
[TIME HHMM]
[DATE MMDDYY]
[TIMESTAMP SETUP]
[KEYBOARD SETUP]

[**Plot/Print**]
[PLOT/PRNT DEVICE]
[PLOT/PRNT DESTINATN]
[SETUP]
[PLOT LINE SETUP]
[MORE SETUP]
[PLOT PEN SPEED]
[P1 P2 SETUP]
[TIME STMP ON OFF]
[PAGE EJCT ON OFF]
[SERIAL SETUP]

[**Disk Utility**]
[FORMAT DISK]
[DISK TYPE LIF DOS]
[DEFAULT DISK]
[NON-VOL RAM DISK]
[VOLATILE RAM DISK]
[INTERNAL DISK]
[EXTERNAL DISK]

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ROM Address Latch,DRAM Address MUX and Buffer	Buffer the processor address bus.
DRAM Data Buffer	Buffers the data on the Processor Data Bus and the Buffered Processor Data Bus.
FLASH Program Control	Allows the FLASH ROM to be reprogrammed.
RAM Battery Power	Provides battery backup for SRAM and the Battery Backed Real Time Clock.
Battery Backed Real Time Clock	Keeps track of the current time and date.



A8 Memory Block Diagram

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A9 NVRAM

The optional A9 NVRAM assembly provides the A7 CPU assembly with additional nonvolatile RAM.

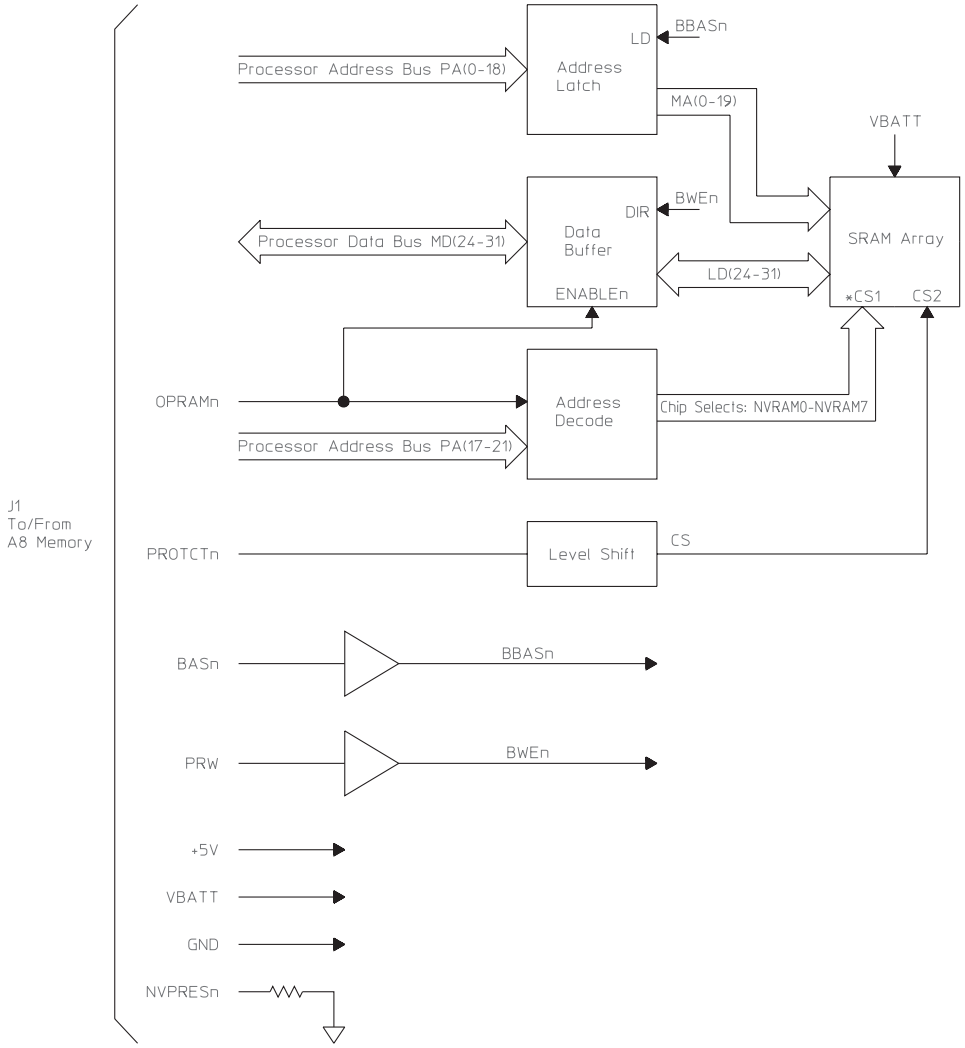
Address Latch — Holds the address from the processor address bus. This circuit latches the address when an address strobe occurs (BBASn goes low).

Data Buffer — Buffers the processor data bus.

Address Decode — Enables one of the eight battery-backed static RAM chips in the SRAM Array.

Level Shift — Disables the SRAM Array during power-up and power down, when the A7 CPU assembly's processor is externally reset, and when +5 volts on the A8 Memory assembly is too low.

SRAM Array — Contains eight battery-backed static RAM chips.



A9 NVRAM Block Diagram

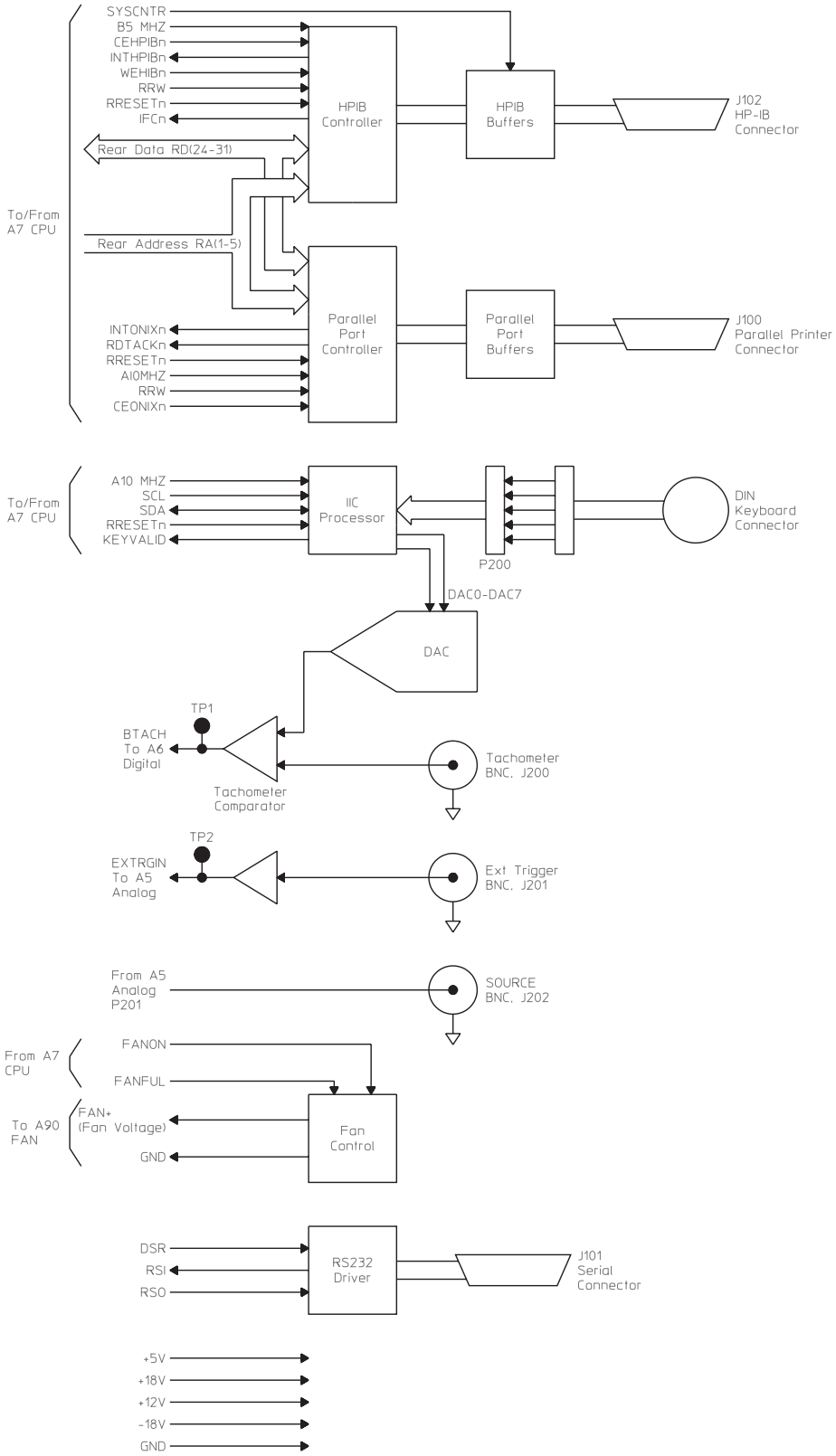
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A10 Rear Panel

The A10 Rear Panel assembly contains the BNC connectors for the external trigger input, tachometer input, and source output. The Rear Panel assembly also contains DIN, GPIB, serial, and parallel interface connectors. In addition, the Rear Panel assembly provides the fan control for the A90 Fan assembly.

GPIB Controller and *Buffers*	Allow the analyzer to communicate with devices such as plotters, printers, or a host computer via an GPIB cable. These circuits handle all GPIB functions for the analyzer.
Parallel Port Controller and Buffers	Allow the analyzer to send data to printers with Centronics interfaces.
IIC Processor	Provides the interface from the DIN keyboard connector to the A7 CPU assembly. The IIC Interface also decodes the control lines for the DAC.
DAC	Sets the tachometer trigger level. The A7 CPU assembly sends the control signals to the Rear Panel assembly over the IIC bus. The IIC Processor decodes the control signals.
Tachometer Comparator	Compares the input signal from the Tachometer BNC connector with the trigger level set by the DAC. The output of the comparator changes TTL levels when the input signal crosses the trigger level.
External Trigger Buffer	Buffers the external trigger signal.
Fan Control	Provides the A90 Fan assembly with a voltage that controls the fan speed. A temperature sensor provides a control signal that changes with the analyzer's internal temperature. When the temperature increases, Fan Control increases the fan speed. When the temperature decreases, Fan Control decreases the fan speed. Control lines from the A7 CPU assembly can also set the fan speed to high or turn the fan off.
Serial Driver	Drives the serial data lines to and from devices connected to the Serial Port. The serial port is only available using Instrument Basic.

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A10 Rear Panel Block Diagram

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A11 Keyboard Controller

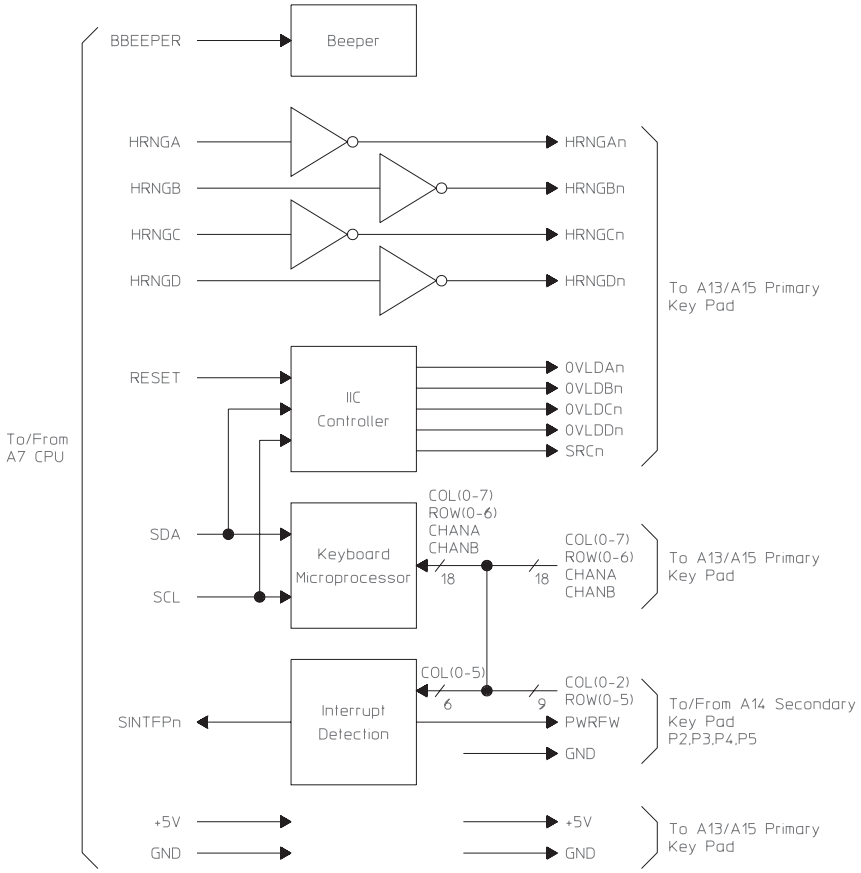
The A11 Keyboard Controller assembly together with the A13 Primary and A14 Secondary Keypad assemblies make up the front panel keyboard. This assembly provides the interface between the A7 CPU assembly and the keypads.

Beeper Generates a tone when instructed by the A7 CPU assembly. The beeper can be turned off by pressing [**System Utility**] [BEEPER ON **OFF**].

IIC Controller Decodes data from the IIC bus providing the A13 Primary Keypad assembly with control lines that turn overload and source LEDs on and off.

Keyboard Microprocessor Interrupts the A7 CPU assembly when a key is pressed or the RPG is turned. The CPU assembly then addresses the Keyboard Microprocessor and reads an 8-bit frame of data from the IIC bus to determine which key was pressed (for information about the IIC bus, see the description of the IIC Controller in the ''A7 CPU'' earlier in this chapter).

Interrupt Detection Informs the A7 CPU assembly every time a key is pressed or the RPG is turned.



A11 Keyboard Controller Block Diagram

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A12 BNC

The A12 BNC assembly connects the BNC connectors on the two channel analyzer's front panel to their respective assembly. The Source BNC is connected to the A5 Analog assembly and the Channel 1 and Channel 2 BNCs are connected to the A1 Input assembly. In addition, this assembly provides RFI filtering for the Channel 1 and Channel 2 HIGH and LOW inputs.

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A13 Primary Keypad

The A13 Primary Keypad assembly contains the marker, display, numeric, and measurement keys for the two channel analyzer. The Primary Keypad assembly also contains the RPG and the LEDs that indicate a half range or overload condition on a channel. See ‘’A11 Keyboard Controller’’ for additional information.

A14 Secondary Keypad

The A14 Secondary Keypad assembly contains the system keys and the softkeys. See ‘’A11 Keyboard Controller’’ for additional information.

A15 Primary Keypad

The A15 Primary Keypad assembly contains the marker, display, numeric, and measurement keys for the four channel analyzer. The Primary Keypad assembly also contains the RPG and the LEDs that indicate a half range or overload condition on a channel. See ‘’A11 Keyboard Controller’’ for additional information.

A22 BNC

The A22 BNC assembly connects the BNC connectors on the four channel analyzer’s front panel to their respective assembly. The Channel 1 and Channel 3 BNCs are connected to the A2 Input assembly connected to A99 J1. The Channel 2 and Channel 4 BNCs are connected to the A2 Input assembly connected to A99 J2. In addition, this assembly provides RFI filtering for the HIGH and LOW inputs.

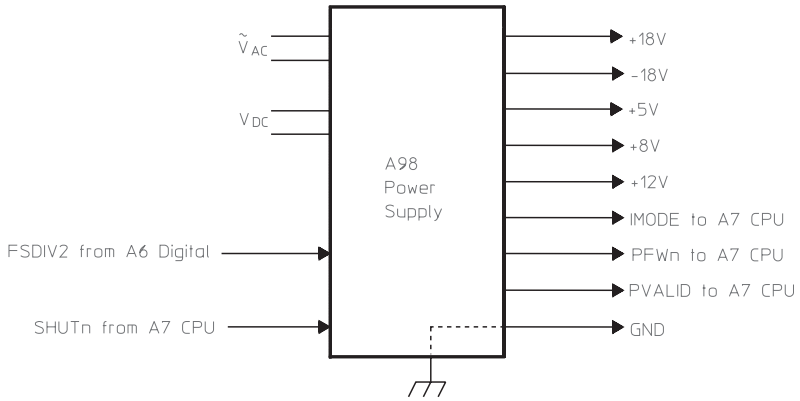
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A90 Fan

The A90 Fan assembly cools the analyzer. The A10 Rear Panel assembly controls the speed of the Fan assembly. As the temperature increases, the Rear Panel assembly increases the fan speed. As the temperature decreases, the Rear Panel assembly decreases the fan speed. The fan can also be turned off or set to full speed by pressing [**System Utility**] [FAN SETUP] [FAN OFF] or [FULL SPEED].

A98 Power Supply

The A98 Power Supply assembly is a switching power supply that provides the voltages for all the assemblies in the analyzer. The Power Supply can operate on ac line power or on a dc battery pack. See ''Power Supply Voltage Distribution'' in chapter 9 for a list of the voltages and the assemblies that use each voltage.



A98 Power Supply Block Diagram

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A99 Motherboard

The A99 Motherboard assembly provides a common point of contact for voltage and signal distribution. The Motherboard also buffers the external monitor signals and routes the buffered signals to the EXT MONITOR connector. See ''A99 Motherboard'' in chapter 9 for a list of all signals that are distributed via the Motherboard assembly.

A100 Disk Drive

The internal A100 Disk Drive assembly stores and retrieves information from 3.5-inch flexible disks. This assembly is controlled by the A7 CPU assembly. See the description of the Disk Controller in ''A7 CPU'' (earlier in this chapter) for additional information.

A101 Display

The A101 Display assembly shows processed data sent by the A7 CPU assembly. See the description of the Display Controller for the ''A7 CPU'' (earlier in this chapter) for further details.

A102 DC-DC Converter

The A102 DC-DC Converter assembly generates the driver supply voltages for the A101 Display assembly and routes the display data from the A7 CPU assembly to the Display assembly.

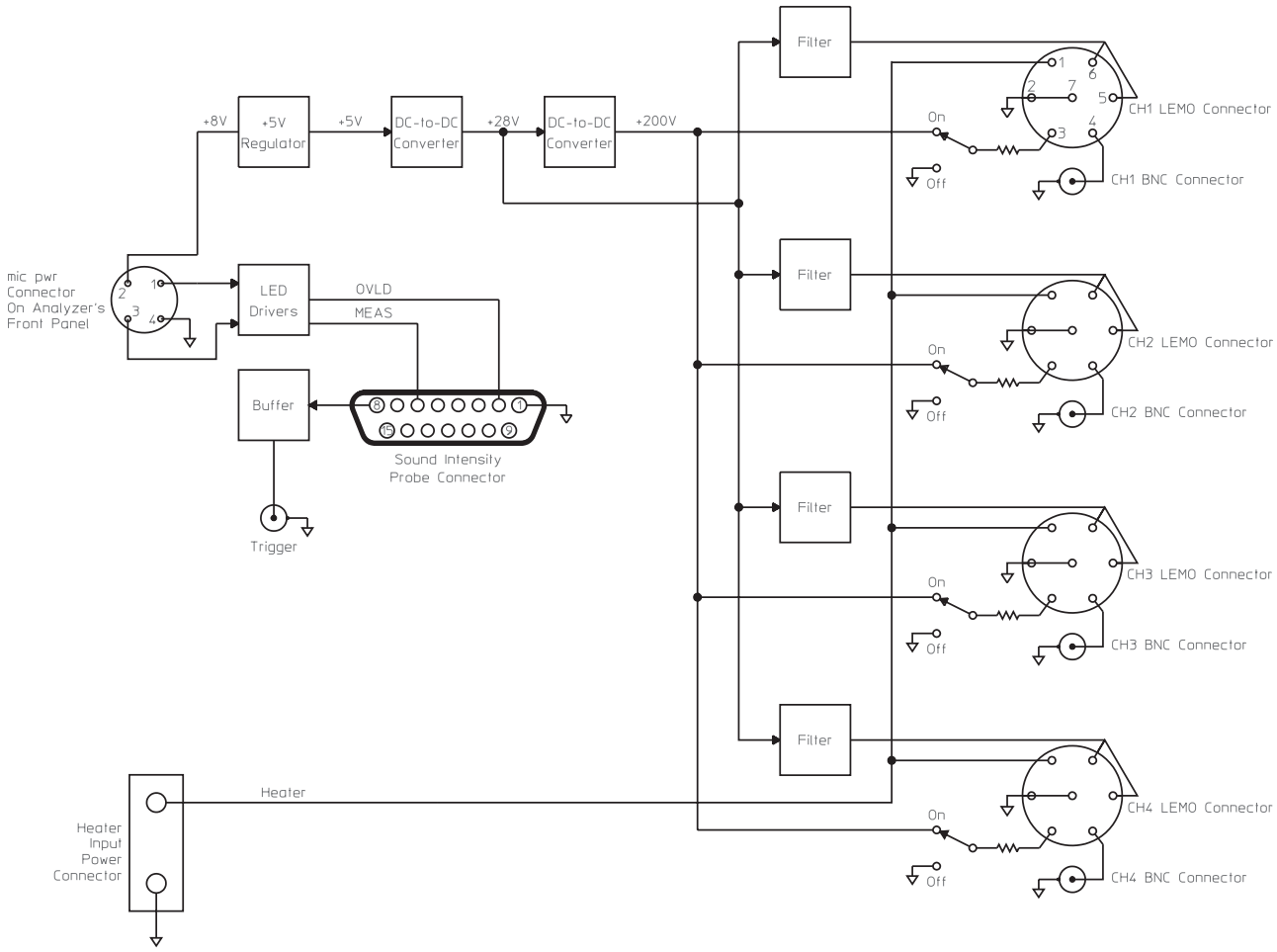
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Option UK4 Microphone Adapter and Power Supply

The optional Microphone Adapter and Power Supply provides four LEMO connectors with power for microphones. The input signal from each LEMO connector is routed to a BNC connector. BNC cables then connect the input signals to the analyzer's input channels.

+5 V Regulator	Regulates +8 V to +5 V.
DC-to-DC Converter	Converts +5 V to +28 V. The second DC-to-DC Converter converts +28 V to +200 V.
Filter	Filters +28 V providing the microphone preamplifier voltage to pins 5 and 6 of each LEMO connector.
On Off	Connects a 200 V polarization voltage or ground to pin 3 of each LEMO connector.
Heater Input Power	Allows an externally supplied heater voltage to be connected to pin 1 of each LEMO connector.
LED Drivers	Provides control lines for the overload and measurement LEDs on the HP 35230A Sound Intensity Probe.
Buffer	Buffers the trigger signal from the HP 35230A Sound Intensity Probe. A BNC cable connects the trigger signal to the analyzer's rear panel.
Sound Intensity Probe Connector	Provides the interface to the HP 35230A Sound Intensity Probe.

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Option UK4 Microphone Adapter and Power Supply Block Diagram

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9

Voltages and Signals

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Voltages and Signals

This chapter shows where the signals and voltages are used in the analyzer and describes each signal. The signals are described in groups as shown in the following table.

Section Title	Describes signals routed ...
A1 Input	through SMB cables from A1 Input to A5 Analog
A2 Input	through SMB cables from A2 Input to A5 Analog
A8 Memory	between A8 Memory and A7 CPU
A9 NVRAM	between A9 NVRAM and A8 Memory
A10 Rear Panel	between A10 Rear Panel and external connectors
A11 Keyboard Controller	between A11 Keyboard Controller and A7 CPU
A12 BNC	through A12 BNC
A13 Primary Keypad	between A13 Primary Keypad and A11 Keyboard Controller
A14 Secondary Keypad	between A14 Secondary Keypad and A11 Keyboard Controller
A22 BNC	through A22 BNC
A99 Motherboard	through A99 Motherboard
A100 Disk Drive	between A100 Disk Drive and A7 CPU
A101 Display	between A101 Display and A7 CPU
A102 DC-DC Converter	between A102 DC-DC Converter and A101 Display

Note

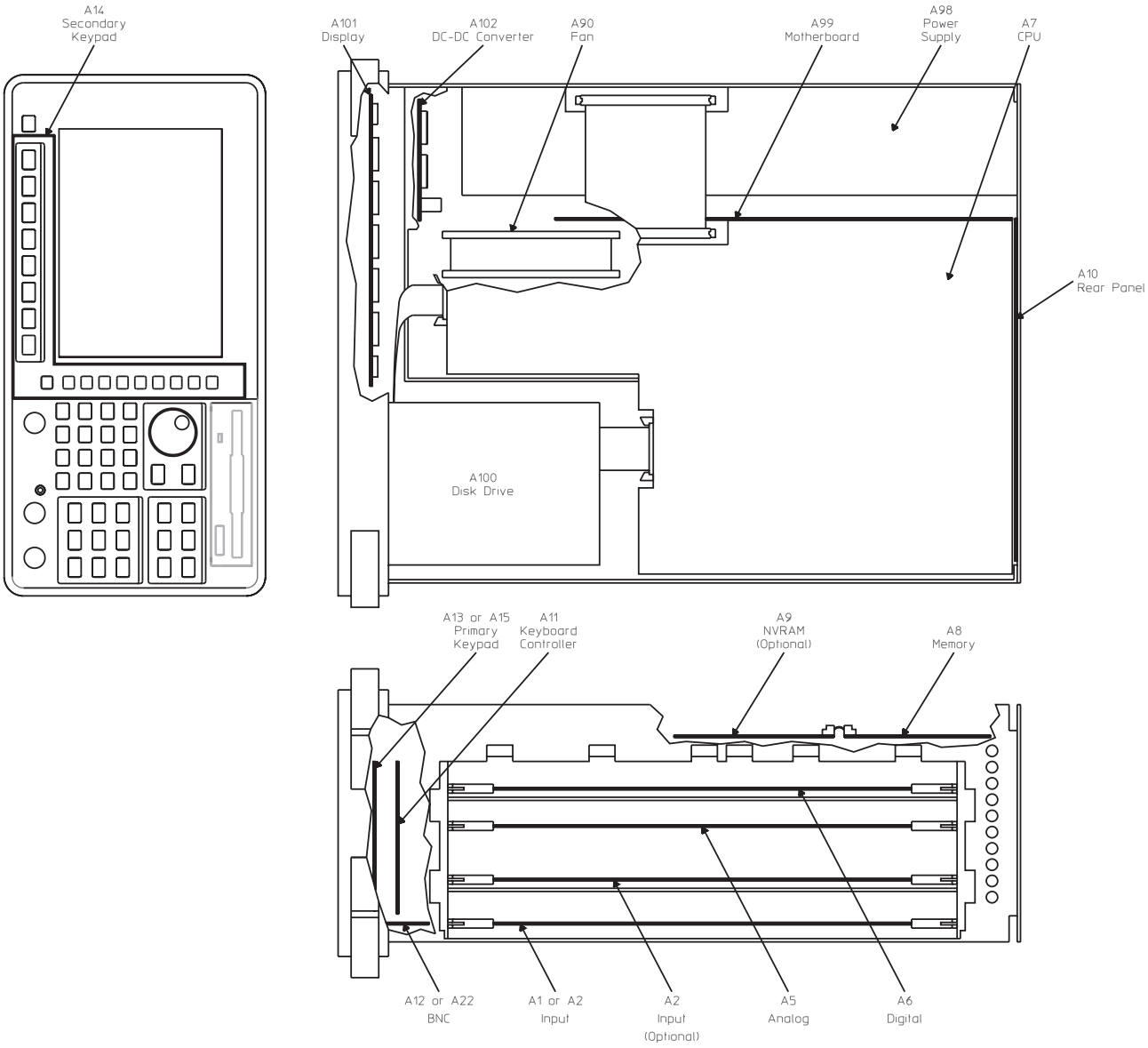
Signals with a mnemonic that end with a lower case ‘’n’’ are active low.

Signal levels listed as low or high are TTL levels unless stated otherwise.

Measurements given in dBm are terminated in 50 ohms unless stated otherwise.

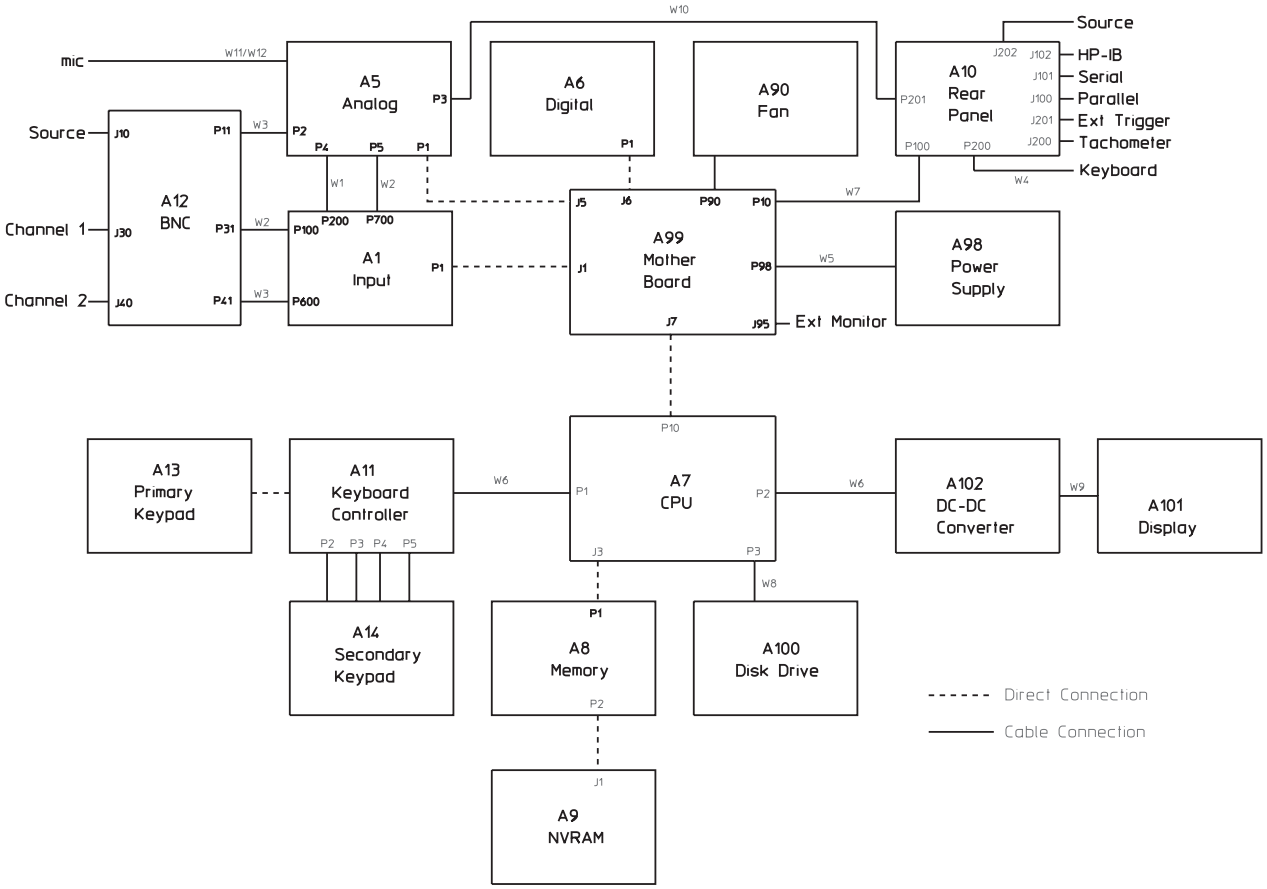
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Assembly Locations and Connections



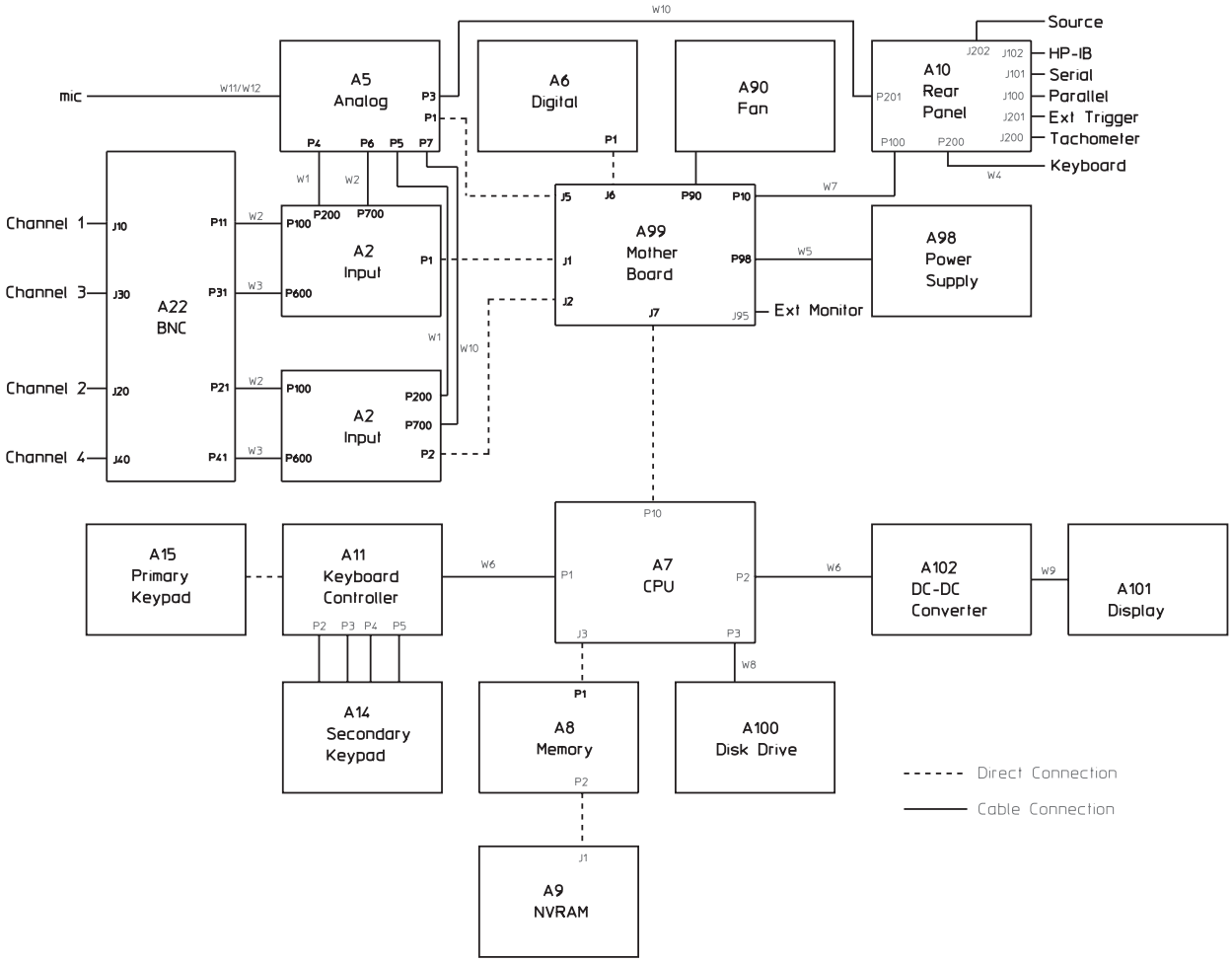
Assembly Locations

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Assembly Connections for Two Channel Analyzer

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Assembly Connections for Four Channel Analyzer

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Power Supply Voltage Distribution

The following table shows the power supply voltages used by each assembly in the analyzer. In addition, the table also shows the path taken by these voltages. Some assemblies use the power supply voltages as supplied by the Power Supply assembly. However, most assemblies contain voltage regulation and voltage decoupling circuits to provide additional regulation and decoupling for their own use.

From	Path	To	Voltages					
			+18 V	18 V	+12 V	+8 V	+5 V	Gnd
Pwr Supply	W5	A99	•	•	•	•	•	•
	W5/A99	A1/A2	•	•		•		•
	W5/A99	A5	•	•		•	•	•
	W5/A99	A6					•	•
	W5/A99/W7	A10	•	•	•		•	•
	W5/A99	A90					•	•
	W5/A99	A7		•	•		•	•
	W5/A99/A7	A8			•		•	•
	W5/A99/A7/A8	A9					•	•
	W5/A99/A7/W6	A11					•	•
	W5/A99/A7/W6/A11	A13					•	•
	W5/A99/A7/W6/A11	A14						•
	W5/A99/A7/W8	A100					•	•
	W5/A99/A7/W6	A101			•		•	•
	W5/A99/A7/W6	A102			•		•	•

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A1 Input

Analyzers with only two channels contain one A1 Input assembly. The A1 Input assembly conditions both input signals. After the signals are conditioned by the Input assembly they are routed through SMB cables to the A5 Analog assembly. The signal from A1 P200 to A5 P4 is C1AAFO (Channel 1 Anti-Alias Filter Out). The signal from A1 P700 to A5 P5 is C2AAFO (Channel 2 Anti-Alias Filter Out). The amplitude of C1AAFO or C2AAFO is 1 Vrms with the analyzer set to the 1 dBVrms range and a 1.122 Vrms signal connected to the channel's input connector.

A2 Input

Analyzers with the four channel option contain two A2 Input assemblies. The A2 Input assemblies condition all four input signals. After the signals are conditioned by the Input assemblies they are routed through SMB cables to the A5 Analog assembly. For the Input assembly connected to A99 J1, the signal from A2 P200 to A5 P4 is C1AAFO (Channel 1 Anti-Alias Filter Out) and the signal from A2 P700 to A5 P6 is C3AAFO (Channel 3 Anti-Alias Filter Out). For the Input assembly connected to A99 J2, the signal from A2 P200 to A5 P5 is C2AAFO (Channel 2 Anti-Alias Filter Out) and the signal from A2 P700 to A5 P7 is C4AAFO (Channel 4 Anti-Alias Filter Out). The amplitude of C1AAFO, C2AAFO, C3AAFO, or C4AAFO is 1 Vrms with the analyzer set to the 1 dBVrms range and a 1.122 Vrms signal connected to the channel's input connector.

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A8 Memory

The following table lists signals routed between the A8 Memory assembly and the A7 CPU assembly. This table shows several things — if the assembly generates or uses the signal or voltage, and if a signal is bidirectional. A description of each signal follows the table.

Signal Name	A7 J3 Pin(s)	A8 P1 Pin(s)	A7 J3	A8 P1
BD16	25C	C8	⇔	⇔
BD17	25B	B8	⇔	⇔
BD18	26C	C7	⇔	⇔
BD19	26B	B7	⇔	⇔
BD20	26A	A7	⇔	⇔
BD21	27C	C6	⇔	⇔
BD22	27B	B6	⇔	⇔
BD23	27A	A6	⇔	⇔
BD24	28C	C5	⇔	⇔
BD25	28B	B5	⇔	⇔
BD26	28A	A5	⇔	⇔
BD27	29C	C4	⇔	⇔
BD28	29B	B4	⇔	⇔
BD29	29A	A4	⇔	⇔
BD30	30C	C3	⇔	⇔
BD31	30B	B3	⇔	⇔
CPUSPCn	17A	A16	S	•
DSACK0n	3A	A30	•	S
DSACK1n	4A	A29	•	S
FLASHEN	19A	A14	S	•
G20MHZ	32C	C1	S	•
MEMRESET	20A	A13	S	•
PA0	1C	C32	S	•
PA1	1B	B32	S	•
PA2	2C	C31	S	•
PA3	2B	B31	S	•
PA4	3C	C30	S	•
PA5	3B	B30	S	•
PA6	4C	C29	S	•

S This assembly is the source of the signal.

• This assembly uses the signal.

⇔ This signal is bidirectional.

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Signal Name	A7 J3 Pin(s)	A8 P1 Pin(s)	A7 J3	A8 P1
PA7	4Bjio	B29	S	•
PA8	5C	C28	S	•
PA9	5B	B28	S	•
PA10	6C	C27	S	•
PA11	6B	B27	S	•
PA12	8C	C25	S	•
PA13	8B	B25	S	•
PA14	9C	C24	S	•
PA15	9B	B24	S	•
PA16	10C	C23	S	•
PA17	10B	B23	S	•
PA18	11C	C22	S	•
PA19	11B	B22	S	•
PA20	12C	C21	S	•
PA21	12B	B21	S	•
PA22	13C	C20	S	•
PA23	13B	B20	S	•
PA24	11A	A22	S	•
PA25	18A	A15	S	•
PA26	31B	B2	S	•
PASn	16A	A17	S	•
PD0	16C	C17	⇔	⇔
PD1	16B	B17	⇔	⇔
PD2		C16	⇔	⇔
PD3	17B	B16	⇔	⇔
PD4	18C	C15	⇔	⇔
PD5	18B	B15	⇔	⇔
PD6	19C	C14	⇔	⇔
PD7	19B	B14	⇔	⇔
PD8	20C	C13	⇔	⇔
PD9	20B	B13	⇔	⇔
PD10	21C	C12	⇔	⇔
PD11	21B	B12	⇔	⇔
PD12	22C	C11	⇔	⇔
PD13	22B	B11	⇔	⇔
PD14	23C	C10	⇔	⇔
PD15	23B	B10	⇔	⇔
PRW	9A	A24	S	•
SCL	22A	A11	S	•
SDA	23A	A10	⇔	⇔
SIZE0	12A	A21	S	•
SIZE1	13A	A20	S	•
+5	5A, 6A, 10A, 15A, 15B, 15C	A18, B18, C18, A23, A27, A28	•	•
+12	31A, 32A	A1, A2	•	•

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Gnd	1A, 2A, 7A, 7B, 7C, 8A, 14A, 14B, 14C, 21A, 24A, 24B, 24C, 25A, 30A, 31C	C2, A3, A8, A9, B9, C9, A12, A19, B19, C19, A25, A26, B26, C26, A31, A32	•	•
Not Used	32B	B1		

S This assembly is the source of the signal.

• This assembly uses the signal

⇔ This signal is bidirectional.

This assembly *does not* use this signal.

BD16 —31 Buffered Data Bus — This is the buffered processor data bus from the A7 CPU assembly. This bus is further buffered on the A8 Memory assembly.

CPUSPCn CPU Space — This line goes low when the CPU space transfer occurs. When this line is low the A8 Memory assembly does not respond.

DSACK0n — DSACK1n Data Strobe Acknowledge — During a write cycle, DSACK0n goes low after the A8 Memory assembly places valid data on the data bus. During a read cycle, DSACK0n goes low after the Memory assembly reads the data. When DSACK0n goes low and DSACK1n is low, 32 bits of data are valid on PD0-15 and BD16-31. When DSACK0n goes low and DSACK1n is high, 8 bits of data are valid on BD24-31.

FLASHEN Flash Enable — This line is high only when the FLASH memory on the A8 Memory assembly is being programmed. This line enables +12 V to the FLASH memory programming pin.

G20MHZ 20 MHz Clock — This is a 50% duty cycle, 20 MHz clock. This clock provides the timing for the A8 Memory assembly.

MEMRESET Memory Reset — A high on this line resets the digital logic on the A8 Memory assembly. This line pulses high during power-up and power-down, and when the A7 CPU assembly's microprocessor executes the RESET instruction or is externally reset.

PA0 — PA26 Processor Address Bus — This is the processor address bus from the A7 CPU assembly. This bus is buffered on the A8 Memory assembly. PA0 and PA1 also operate with SIZE0 and SIZE1 to specify the alignment of the operand.

PASn Processor Address Strobe — A low on this line starts a memory access cycle. This line pulses low when a valid address is on the processor address bus (PA1 — PA23).

PD0 — 15 Processor Data Bus — This is the processor data bus from the A7 CPU assembly.

PRW Processor Read/Write — This line is high when the current memory cycle is a read and low when the current memory cycle is a write.

SCL Serial Clock — This is the serial clock for the IIC bus. The IIC controller on the A7 CPU assembly generates this clock to synchronize the transfer of data on the IIC bus.

SDA Serial Data — This is the IIC bus bidirectional data line. This line transmits real-time clock data between the A7 CPU assembly and the A8 Memory assembly in 8-bit frames. The IIC controller on the CPU assembly controls data transfers on the IIC bus.

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SIZE0 — SIZE1	Data Size — These lines determine the size of the operand. When SIZE0 is high and SIZE1 is low, the operand size is 8 bits. When SIZE0 is low and SIZE1 is high, the operand size is 16 bits. When both SIZE0 and SIZE1 are high, the operand size is 24 bits. When both SIZE0 and SIZE1 are low, the operand size is 32 bits.

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A9 NVRAM

The following table lists signals routed between the optional A9 NVRAM assembly and the A8 Memory assembly. This table shows several things — if the assembly generates or uses the signal or voltage, and if a signal is bidirectional. A description of each signal follows the table.

Signal Name	Pin(s)	A8 P2	A9 J1
BASn	A6	•	•
MD24	B4	⇔	⇔
MD25	C4	⇔	⇔
MD26	B3	⇔	⇔
MD27	C3	⇔	⇔
MD28	B2	⇔	⇔
MD29	C2	⇔	⇔
MD30	B1	⇔	⇔
MD31	C1	⇔	⇔
NVPRESn	A16		S
OPRAMn	A2	S	•
PA0	C6	S	•
PA1	B6	S	•
PA2	C7	S	•
PA3	B7	S	•
PA4	C8	S	•
PA5	B8	S	•
PA6	C9	S	•
PA7	B9	S	•
PA8	C10	S	•
PA9	B10	S	•
PA10	C12	S	•
PA11	B12	S	•
PA12	C13	S	•
PA13	B13	S	•
PA14	C14	S	•
PA15	B14	S	•
PA16	C15	S	•
PA17	B15	S	•

S This assembly is the source of the signal.

• This assembly uses the signal.

⇔ This signal is bidirectional.

This assembly *does not* use this signal.

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Signal Name	Pin(s)	A8 P2	A9 J1
PROTCTn	A9	S	•
PA18	C16	S	•
PA19	A4	S	•
PA20	A12	S	•
PA21	B16	S	•
PRW	A3	•	•
VBATT	A13, A14, A15	S	•
+5	A10, A11, B11, C11	•	•
Gnd	A1, A5, B5, C5, A7, A8	•	•

S This assembly is the source of the signal.
• This assembly uses the signal.
⇔ This signal is bidirectional.
This assembly *does not* use this signal.

BASn — Buffered Address Strobe — This line pulses low when a valid address is on the processor address bus (PA0 — PA21).

MD24 — MD31 — Memory Data Bus — This is the buffered processor data bus from the A7 CPU assembly. This bus is further buffered on the A8 Memory assembly.

NVPRESn — NRAM Present — A low on this line indicates that the A9 NVRAM assembly is connected to the A8 Memory assembly. This line is checked only during manual troubleshooting procedures.

OPRAMn — Optional RAM — A low on this line enables the battery-backed static RAM on the A9 NVRAM assembly.

PA0 — PA21 — Processor Address Bus — This is the processor address bus from the A7 CPU assembly. This bus is buffered on the A8 Memory assembly.

PROTCTn — Protect — A low on this line disables the battery-backed static RAM on the A9 NVRAM assembly. This line pulses low during power-up and power-down, when the A7 CPU assembly's microprocessor is externally reset, and when +5 volts on the A8 Memory assembly is too low.

PRW — Processor Read/Write — This line is high when the current memory cycle is a read and low when the current memory cycle is a write.

VBATT — Battery Voltage — This line provides the power to the battery-backed static RAM on the A9 NVRAM assembly. When the analyzer is on, the +5 volts on the A8 Memory assembly provides the power for this line. When the analyzer is off, the battery on the Memory assembly provides the power for this line. Since power is applied to the static RAM even when the analyzer is off, the static RAM is non-volatile.

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A10 Rear Panel

This section describes the signals at the A10 Rear Panel assembly's interface connectors and input connectors. The signals are described in the following order:
GPIB
Serial Port
Parallel Port
DIN Keyboard
Source Output
Tachometer Input
External Trigger Input

GPIB

The following table lists signals at the GPIB connector (A10 J102). A general description of each signal follows the table. For a detailed description of how the analyzer interprets the GPIB lines, see the *Agilent 35670A GPIB Command Reference*.

Signal Name	Pin
ATN	11
DAVn	6
DIO1	1
DIO2	2
DIO3	3
DIO4	4
DIO5	13
DIO6	14
DIO7	15
DIO8	16
EOIn	5
IFCn	9
NDACn	8
NRFDn	7
RENn	17
SRQn	10
Shield	12
GND	18 24

ATN — Attention — This line is controlled by the controller in charge. When this line is low, the DIO lines contain interface commands. When this line is high, the DIO lines contain data.

DAVn — Data Valid — This line goes low when valid data is on the bus and NRFDn is high. This line is controlled by the GPIB controller.

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DIO1 — DIO8 — Data Input/Output — These are inverted data lines that conform to IEEE specification IEEE-488. When ATN is low, these lines contain interface commands. When ATN is high, these lines contain data.

EOIn — End or Identify — If ATN is high, a low on this line marks the end of a message block. If ATN is low, a low on this line requests a parallel poll.

IFCn — Interface Clear — This line goes low to halt all current operations on the bus, unaddress all other devices, and disable serial poll. The system controller becomes the controller in charge. This line is only used during the analyzer's developement.

NDACn — Not Data Accepted — This line goes high when the DIO lines have been latched by the acceptor.

NRFDn — Not Ready for Data — This line goes high when the acceptor is ready to accept data.

RENn — Remote Enable — This line is low when the GPIB has control and high during local operation.

SRQn — Service Request — This line is low when a device on the GPIB needs service.

Serial Port

The following table lists signals at the Serial Port connector (A10 J101). The Serial Port is a 9-pin EIA-574 port that is only available using Instrument Basic. A description of each signal follows the table.

Signal Name	Pin
DSR	6
DTR	1
RTS	4
RxD	3
TxD	2
Logic Gnd	7
Not Used	5, 8 9

DSR — Data Set Ready — Some devices check this line for a high to verify that the analyzer is connected and ready. The user can set this line high or set this line to go high only when the analyzer is ready for data transfer.

DTR — Data Terminal Ready — This line is tied high. Some devices check this line for a high to verify that the analyzer is connected and ready.

RTS — Request To Send — This line is tied high. Some devices require this line to be high before transferring data.

RxD — Receive Data — This is the serial EIA-574 receive data line. This line transmits data from peripheral devices one byte at a time.

TxD — Transmit Data — This is the serial EIA-574 transmit data line. This line transmits data to peripheral devices one byte at a time.

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Parallel Port

The Parallel Port is a 25-pin, Centronics port. The Parallel Port can interface with printers or plotters. The following table lists signals at the Parallel Port connector (A10 J100). A description of each signal follows the table.

Signal Name	Pin
ACKn	10
BUSY	11
FAULTn	15
IPn	16
PA0	2
PA1	3
PA2	4
PA3	5
PA4	6
PA5	7
PA6	8
PA7	9
PE	12
SELECT	13
STROBEn	1
Logic Gnd	18
Not Used	14, 17, 19 25

ACKn — Acknowledge — The printer pulses this line low after it accepts a byte of data and is ready for more data.

BUSY — Busy — The printer sets this line high when it cannot receive data due to data entry, a full buffer, or error status.

FAULTn — Fault — The printer sets this line low if it reaches an error state.

IPn — Input Prime — This line pulses low to reset the printer and clear the print buffer.

PA0 - PA7 — Printer Data Bus —This is the 8-bit parallel data bus. These lines transmit a byte of data to the printer.

PE — Paper Error — The printer sets this line high when it is out of paper.

SELECT — Selected — The printer sets this line high to indicate that it has been selected.

STROBEn — Strobe — This line pulses low when a byte of data is ready. A low pulse on this line clocks the data into the printer.

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DIN Keyboard

The following table lists signals at the DIN keyboard connector (A10 P200). A description of each signal follows the table.

Signal Name	Pin
KEYCLK	1
KEYDAT	3
+5 V	4
Logic Gnd	2
Not Used	5

KEYCLK — Key Board Clock — This clock synchronizes the transfer of keyboard data from the external keyboard to the A10 Rear Panel assembly.

KEYDAT — Key Board Data — This is 8-bit serial data from an external keyboard to the A10 Rear Panel assembly .

Source Output

The source output is routed from P3 on the A5 Analog assembly through an SMB cable to P201 on the A10 Rear Panel assembly. The A10 Rear Panel assembly then routes the source signal to the Source BNC connector. In two channel analyzers, the source output is also routed from P2 on the A5 Analog assembly through an SMB cable to P11 on the A12 BNC assembly. The A12 BNC assembly then routes the source signal to the Source BNC connector on the front panel. The source signal can be random noise, burst random noise, periodic chirp, burst chirp, pink noise, or fixed sine. The signal's amplitude range is ±5 Vpk.

Tachometer Input

The A10 Rear Panel assembly converts the signal connected to the Tachometer BNC connector to a TTL representation of the tachometer input (BTACH).

External Trigger Input

The A10 Rear Panel assembly buffers the signal connected to the External Trigger BNC connector. The maximum trigger input level is ±25 Vpk. The minimum trigger pulse width is 600 ns and the maximum trigger pulse rate is 800 kHz.

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A11 Keyboard Controller

The following table lists signals routed between the A11 Keyboard Controller assembly and the A7 CPU assembly. This table shows several things — if the assembly generates or uses the signal or voltage, and if a signal is bidirectional. A description of each signal follows the table.

Signal Name	Pin(s)	A7 P1	A11
BBEEPER	3	S	•
HRNGA	11		•
HRNGB	9		•
HRNGC	2		•
HRNGD	1		•
RESET	5	S	•
SCL	15	S	•
SDA	13	⇔	⇔
SINTFPn	7	•	S
+5 V	10	•	•
Gnd	6, 8, 12, 14, 16	•	•
Not Used	4		

S This assembly is the source of the signal.
• This assembly uses the signal.
⇔ This signal is bidirectional.
This assembly *does not* use this signal.

BBEEPER — Buffered Beeper — This line controls the frequency of the front panel beeper tone.

HRNGA — Half Range A — In both the two channel and four channel analyzer, a high on this line turns on the channel 1 half range LED. This line goes high when the A1 or A2 Input assembly detects that the amplitude of the channel 1 input signal reached half the set range.

HRNGB — Half Range B — In a two channel analyzer, a high on this line turns on the channel 2 half range LED. In a four channel analyzer, a high on this line turns on the channel 3 half range LED. This line goes high when the A1 Input assembly detects that the amplitude of the channel 2 input signal reached half the set range or when the A2 Input assembly detects that the amplitude of the channel 3 input signal reached half the set range.

HRNGC — Half Range C — In a four channel analyzer, a high on this line turns on the channel 2 half range LED. This line goes high when the A2 Input assembly detects that the amplitude of the channel 2 input signal reached half the set range. This line is only used in four channel analyzers.

HRNGD — Half Range D — In a four channel analyzer, a high on this line turns on the channel 4 half range LED. This line goes high when the A2 Input assembly detects that the amplitude of the channel 4 input signal reached half the set range. This line is only used in four channel analyzers.

RESET — System Reset — A high on this line resets the digital logic on the A11 Keyboard Controller assembly. This line pulses high during power-up and power-down, and when the A7 CPU assembly's microprocessor executes the RESET instruction or is externally reset.

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SCL	Serial Clock — This is the serial clock for the keyboard IIC bus. The IIC controller on the A7 CPU assembly generates this clock to synchronize the transfer of data from the A11 Keyboard Controller assembly.
SDA	Serial Data — This is the keyboard IIC bus. When a key is pressed or the RPG is turned, SINTFPn interrupts the A7 CPU assembly and this line transmits data to the A7 CPU assembly in 8-bit frames.
SINTFPn	Serial Interrupt from the Front Panel — A high-to-low transition on this line interrupts the A7 CPU assembly. This line goes low when a key is pressed or when the RPG is turned.

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A12 BNC

The A12 BNC assembly is only used in two channel analyzers. The A12 BNC assembly routes the signals connected to the Channel 1 BNC connector and Channel 2 BNC connector to the A1 Input assembly. The A12 BNC assembly also routes the source signal from the A5 Analog assembly to the Source BNC connector. The signal connected to Channel 1 should be between 0.19531 Hz to 102.4 kHz in single channel mode and between 0.097656 Hz to 51.2 kHz in two channel mode. The signal connected to Channel 2 should be between 0.097656 to 51.2 kHz. For both channels, the signal's amplitude range must be between +27 dBVrms and –51 dBVrms for full scale measurements. The source output signal can be random noise, burst random noise, periodic chirp, burst chirp, pink noise, or fixed sine. The amplitude range of the source output is ±5 Vpk.

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A13 Primary Keypad

The following table lists signals routed between the A11 Keyboard Controller assembly and the A13 Primary Keypad assembly. This table shows several things — if the assembly generates or uses the signal. A description of each signal follows the table.

Signal Name	A11 Location	A11	A13
CHANA	U1 pin 21	•	S
CHANB	U1 pin 6	•	S
COL0	U1 pin 5	•	S
COL1	U1 pin 4	•	S
COL2	U1 pin 3	•	S
COL3	U1 pin 2	•	S
COL4	U1 pin 1	•	S
COL5	U1 pin 27	•	S
COL6	U1 pin 26	•	S
COL7	U1 pin 25	•	S
HRNGAn	U3 pin 2	S	•
HRNGBn	U3 pin 4	S	•
HRNGCn	U3 pin 6?	S	•
HRNGDn	U3 pin 8?	S	•
OVLDAn	U2 pin 4	S	•
OVLDBn	U2 pin 5	S	•
OVLDCn	U2 pin 6	S	•
OVLDDn	U2 pin 7	S	•
ROW0	U1 pin 13	•	S
ROW1	U1 pin 14	•	S
ROW2	U1 pin 15	•	S
ROW3	U1 pin 16	•	S
ROW4	U1 pin 17	•	S
ROW5	U1 pin 22	•	S
ROW6	U1 pin 23	•	S
SRCn	U2 pin 9	S	•
+5 V	U1 pin 19	•	•
Gnd	U1 pin 12	•	•

S This assembly is the source of the signal.
• This assembly uses the signal.

CHANA — CHANB

These lines indicate the RPG's direction and offset.

COL0 - COL7

Column 0 - Column 7 — A high-to-low transition on one column line indicates that a key in that column was pressed. After the A11 Keyboard Controller assembly's microprocessor determines the keypad row location and the key number, the microprocessor sets columns 0 to 5 low which forces SINTFPn low. A high-to-low transition on SINTFPn informs the A7 CPU assembly that a key was pressed.

HRNGAn

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	Half Range A — In both the two channel and four channel analyzer, a low on this line turns on the channel 1 half range LED. This line goes low when the A1 or A2 Input assembly detects that the amplitude of the channel 1 input signal reached half the set range. This line is HRNGA inverted by the A11 Keyboard Controller assembly.
HRNGBn	Half Range B — In a two channel analyzer, a low on this line turns on the channel 2 half range LED. In a four channel analyzer, a low on this line turns on the channel 3 half range LED. This line goes low when the A1 Input assembly detects that the amplitude of the channel 2 input signal reached half the set range or when the A2 Input assembly detects that the amplitude of the channel 3 input signal reached half the set range. This line is HRNGB inverted by the A11 Keyboard Controller assembly.
HRNGCn	Half Range C — In a four channel analyzer, a low on this line turns on the channel 2 half range LED. This line goes low when the A2 Input assembly detects that the amplitude of the channel 2 input signal reached half the set range. This line is HRNGC inverted by the A11 Keyboard Controller assembly. This line is only used in four channel analyzers.
HRNGDn	Half Range D — In a four channel analyzer, a low on this line turns on the channel 4 half range LED. This line goes low when the A2 Input assembly detects that the amplitude of the channel 4 input signal reached half the set range. This line is HRNGD inverted by the A11 Keyboard Controller assembly. This line is only used in four channel analyzers.
OVLDAn	Overload A — In a four channel analyzer, a low on this line turns on the channel 1 overload LED. This line goes low when the A2 Input assembly detects that the amplitude of the channel 1 input signal exceeded the set range. This line is only used in four channel analyzers.
OVLDBn	Overload B — In four channel analyzers, a low on this line turns on the channel 2 overload LED. This line goes low when the A2 input assembly detects that the amplitude of the channel 2 input signal exceeded the set range. This line is only used in four channel analyzers.
OVLDCn	Overload C — In a two channel analyzer, a low on this line turns on the channel 1 overload LED. In a four channel analyzer, a low on this line turns on the channel 3 overload LED. This line goes low when the A1 Input assembly detects that the amplitude of the channel 1 input signal exceeded the set range or when the A2 Input assembly detects that the amplitude of the channel 3 input signal exceeded the set range.
OVLDDn	Overload D — In a two channel analyzer, a low on this line turns on the channel 2 overload LED. In a four channel analyzer, a low on this line turns on the channel 4 overload LED. This line goes low when the A1 Input assembly detects that the amplitude of the channel 2 input signal exceeded the set range or when the A2 Input assembly detects that the amplitude of the channel 4 input signal exceeded the set range.
ROW0 - ROW6	Row 0 - Row 7 — When the row lines are set high, the row line that remains low indicates that a key in that row was pressed.
SRCn	Source On — A low on this line turns on the source LED. This line goes low when the Source is turned on.

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A14 Secondary Keypad

The following table lists signals routed between the A11 Keyboard Controller assembly and the A14 Secondary Keypad assembly. This table shows several things — if the assembly generates or uses the signal. A description of each signal follows the table.

Signal Name	A11 Connection	A11	A14
COL0	P2 Pin 3	•	S
COL1	P2 Pin 2	•	S
COL2	P2 Pin 1	•	S
ROW0	P3 Pin 3	•	S
ROW1	P3 Pin 2	•	S
ROW2	P3 Pin 1	•	S
ROW3	P4 Pin 3	•	S
ROW4	P4 Pin 2	•	S
ROW5	P4 Pin 1	•	S
PWRFW	P5 Pin 3	S	•
GND	P5 Pin 1	•	•

S This assembly is the source of the signal.
• This assembly uses the signal.

COL0 - COL2 — Column 0 - Column 2 — A high-to-low transition on one column line indicates that a key in that column was pressed. After the A11 Keyboard Controller assembly's microprocessor determines the keypad row location and the key number, the microprocessor sets the column lines low which forces SINTFPn low. A high-to-low transition on SINTFPn informs the A7 CPU assembly that a key was pressed.

ROW0 - ROW5 — Row 0 - Row 5 — A low on one row line indicates that a key in that row was pressed.

PWRFW — Power Fail Warning — A high on this line turns on the power-on LED.

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A22 BNC

The A22 BNC assembly is only used in four-channel analyzers. The A22 BNC assembly routes the signals connected to the Channel 1 BNC connector and Channel 3 BNC connector to the A2 Input assembly connected to J1 on the Motherboard. The A22 BNC assembly also routes the signals connected to the Channel 2 BNC connector and Channel 4 BNC connector to the A2 Input assembly connected to J2 on the Motherboard. The signal connected to Channel 1 and Channel 2 should be between 0.097656 Hz to 51.2 kHz in two-channel mode and between 0.048828 Hz to 25.6 kHz in four-channel mode. The signal connected to Channel 3 and Channel 4 should be between 0.048828 Hz to 25.6 kHz. For all channels, the signal's amplitude range must be between +27 dBVrms and –51 dBVrms for full-scale measurements.

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A99 Motherboard

The following table lists all signals routed through the Motherboard. The table uses bold face type to show which assembly can generate the signal. A description of each signal follows the ''Motherboard Voltages'' table.

Signal Name	Assembly Using Signal								
	A1/A2	A2	A5	A6	A7	A10	A90	A98	Ext Mon
	Motherboard Connector								
	J1	J2	J5	J6	J7	P10	P90	P98	P95
	Connector Pin Number								
A10MHZ					**150**	59			
ADCOLn			**17B**	17A					
ADCULn			**17C**	17B					
ADDATA			**20C**	20A					
B5MHZ					**148**	60			
BRESETn			12A	12B	**112**				
BTACH				32A		**10**			
CALP	C1	C1	**1A**						
CEHPIBn					**138**	25			
CEONIXn					**139**	31			
CHSYNCn			18C	**18A**					
DACCLK			9C	**9B**					
DACDAT			10C	**10A**					
DACUPDn			8C	**8B**					
DITHER			**11A**	11A					
DSPTRIG				**25A**	125				
DSR					**46**	11			
ECLK				22C	**72**				
EFFSMP			19C	**18B**					
EXTRGIN			32B			**8**			
FA1				13B	**64**				
FA2				13C	**114**				
FA3				14B	**65**				
FA4				14C	**115**				
FA5				15B	**66**				
FAN+						**43**	2		
FANFUL					**93**	46			
FANOFF					**143**	45			
FANTRIP			9A		61				
FD0				**25B**	**76**				

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Signal Name	Assembly Using Signal								
	A1/A2	A2	A5	A6	A7	A10	A90	A98	Ext Mon
	Motherboard Connector								
	J1	J2	J5	J6	J7	P10	P90	P98	P95
	Connector Pin Number								
FD1				**25C**	**126**				
FD2				**26B**	**77**				
FD3				**26C**	**127**				
FD4				**27B**	**78**				
FD5				**27C**	**128**				
FD6				**28B**	**79**				
FD7				**28C**	**129**				
FD8				**29B**	**80**				
FD9				**29C**	**130**				
FD10				**30B**	**81**				
FD11				**30C**	**131**				
FD12				**31B**	**82**				
FD13				**31C**	**132**				
FD14				**32B**	**83**				
FD15				**32C**	**133**				
FDTACKn				**19B**	69				
FIFOBAVn				**18C**	68				
FIFOENn				23B	**123**				
FIFORDYn				**24B**	75				
FIRQn				**20C**	70				
FRW				19C	**119**				
FSDIV2				**6C**				30	
FSELAn				24C	**74**				
FSELSn				23C	**124**				
H10MHZ			22C	**22B**					
H20MHZ			21C	21B	**121**				
HRNGA	**A10**				107				
HRNGB	**B10**				57				
HRNGC		**A10**			108				
HRNGD		**B10**			58				
HSYNC					56				8
IFCn					84	**14**			
IMODE					102			**28**	
INTHPIBn					88	**26**			
INTONIXn					89	**32**			
KEYVALID					135	**17**			
LPFCLK			10B	**10B**					

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Signal Name	Assembly Using Signal								
	A1/A2	A2	A5	A6	A7	A10	A90	A98	Ext Mon
	Motherboard Connector								
	J1	J2	J5	J6	J7	P10	P90	P98	P95
	Connector Pin Number								
MDACCSn			8B	**8A**					
PFWn			16A		101			**29**	
PREFS	B16	B16	23C	**23A**					
PVALID					52			**59**	
RA1					**140**	**35**			
RA2					**91**	**38**			
RA3					**141**	**37**			
RA4					**92**	**40**			
RA5					**142**	**39**			
RD24					**94**	**48**			
RD25					**144**	**49**			
RD26					**95**	**50**			
RD27					**145**	**51**			
RD28					**96**	**54**			
RD29					**146**	**53**			
RD30					**97**	**56**			
RD31					**99**	**55**			
RDTACKn					137	**23**			
RRESETn					**134**	12			
RRW					**90**	36			
RSI					86	**20**			
RSO					**136**	19			
SCL	B15	B15	11C		**60**	2			
SDA	**A15**	**A15**	**11B**		**111**	1			
SHUTn			4C		**51**			58	
SINTn	**C15**	**C15**			62				
SPARE1			7C	7B					
SPARE2			9B	9A					
SPARE3				6B	53				
SPARE4	A1	A1	1C						
SRCCLOCK			7B	**7A**					
SRCDATA			6C	**6A**					
SYSCNTR					**85**	18			
TRIGGER			**12C**	12A					
VDATA					**73**				3, 4, 5
VSYNC					**106**				9
WEHPIBn					**87**	24			

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The following table lists all voltages routed through the Motherboard (see ‘’Power Supply Voltage Distribution’’ earlier in this chapter for a complete list of assemblies using each voltage).

Voltage	Assembly Using Voltage								
	A1/A2	A2	A5	A6	A7	A10	A90	A98	EXT MON
	Motherboard Connector								
	J1	J2	J5	J6	J7	P10	P90	P98	P95
	Connector Pin Number								
+18 V	A3 – C3	A3 – C3	3A – 3C			5 – 6		18 – 19 48 – 49	
–18 V	A5 – C5	A5 – C5	5A – 5C		103	3 – 4		25 – 26 55 – 56	
+12 V					4 – 5 54 – 55 104–105	21 – 22		15 – 17 45 – 47	
+8 V	A7 – C7	A7 – C7	14A–14C					27 57	
+5 V			16B–16C	1A – 4C	1 – 3 12 – 20 47 – 50 63 98 100 113	27 – 30		1 – 8 31 – 38	
GND	B1 A2 C2 A4 C4 A6 – C6 A8 – C8 A9 C9 A11 C11 A12–C12B 13–C13C14 A16 C16	B1 A2 C2 A4 C4 A6 – C6 A8 – C8 A9 C9 A11 C11 A12 C12 C13 A14 C14 A16 C16	1B 2A – 2C 4A – 4B 6A – 6B 7A 8A 12B 13A–13 15A–15 17A 18A–18B 19A–19B20 A–20B21A –21B22A–2 2B23A–23 B25A < @1 50 > 25C26A–26 B27A–27C 28A–28C29 A–29C30A 31A	5A – 5C 7C 9C 10C 11B–11C12 C 13A 15A 17C 19A 20B 21A 21C 22A 24A 26A 27A 28A 29A 30A	7 – 11 21 – 45 59 71 109 118 120 122 147 149	7 9 13 15 – 16 33 – 34 44 47 52 57 – 58	1	9 – 14 20 – 24 39 – 44 50 – 54 60	1 2 6

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A10MHZ	10 MHz Clock — This is a 50% duty cycle, 10 MHz clock. This clock provides the timing for the IIC processor on the A10 Rear Panel assembly.
ADCOLn	ADC Overload — This line goes low when the input to the A5 Analog assembly's ADC exceeds its positive limit.
ADCULn	ADC Underload — This line goes low when the input to the A5 Analog assembly's ADC exceeds its negative limit.
ADDATA	Analog to Digital Data — This line is the digital representation of the input signal from the A5 Analog assembly's ADC controller. The ADC controller sends this digital representation to the A6 Digital assembly once per sample (3.8147 ms).
B5MHZ	5 MHz Clock — This is a 50% duty cycle, 5 MHz clock. This clock provides the timing for the GPIB controller on the A10 Rear Panel assembly.
BRESETn	Buffered Reset — A low on this line resets the digital logic on the A5 Analog and A6 Digital assembly. This line pulses low during power-up and power-down, and when the A7 CPU assembly's microprocessor executes the RESET instruction or is externally reset.
BTACH	Buffered Tachometer — This line is a TTL representation of the A10 Rear Panel assembly's tachometer input.
CALP	Calibration Signal — This line is the calibration signal from the A5 Analog assembly. During calibration routines, this signal calibrates the input circuit on the A1 or A2 Input assembly. See "Calibration Routine Description" in chapter 10, ''Internal Test Descriptions,'' for further details.
CEHPIBn	GPIB Controller Chip Enable — This line is low whenever the GPIB controller is accessed for read or write operations.
CEONIXn	Chip Enable for the Parallel Port Controller — A low on this line enables the parallel port controller on the A10 Rear Panel assembly.
CHSYNCn	Channel Synchronize — A low on this line synchronizes the A5 Analog assembly's ADC controller with the A6 Digital assembly.
DACCLK	Source Attenuation DAC Clock — This clock provides the timing for data transfer to the A5 Analog assembly's source attenuator and dc offset DAC. This clock is generated by the A6 Digital assembly's digital source.
DACDAT	Source Attenuation DAC Data — This line provides the control for the A5 Analog assembly's attenuator DAC and dc offset DAC. This serial data line is generated by the A6 Digital assembly's digital source.
DACUPDn	Source Attenuation DAC Latch — This is a control line from the A6 Digital assembly's digital source. A low on this line latches DACDAT after it is clocked into the A5 Analog assembly's attenuator DAC and dc offset DAC.
DITHER	Dither — This line provides digital noise to the A6 Digital assembly's digital filter. The noise bandwidth is set by EFFSMP.
DSPTRIG	DSP Trigger — This is a trigger line for the DSP processor on the A7 CPU assembly. The DSP processor uses this line during gated measurements.
DSR	Data Set Ready — Some devices connected to the serial port check this line for a high to verify that the analyzer is connected and ready. The user can set this line high or set this line to go high only when the analyzer is ready for data transfer.
ECLK	E Clock — The gate arrays on the A6 Digital assembly use this clock for read and write timing.
EFFSMP	Effective Sample Rate — This line sets the update rate for DITHER. The update rate is frequency and span dependent, and controls the dither bandwidth.

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EXTRGIN	External Trigger In — This is a buffered version of the A10 Rear Panel assembly's external trigger input.
FA1 — FA5	Fast Bus Address Lines — These lines are a buffered form of the A7 CPU assembly's microprocessor address bus. The CPU assembly uses these lines to address different circuits on the A6 Digital assembly.
FAN+	Fan Voltage — This voltage can vary from approximately +12 V to 0 V. This variable voltage turns the fan on and off and controls the speed of the A90 Fan assembly.
FANFUL	Fan Full — A high on this line causes FAN+ to go to its positive limit. When FAN+ is at its positive limit, the A90 Fan assembly is on and turning at its highest speed.
FANOFF	Fan Off — A high on this line causes FAN+ go to its negative limit. When FAN+ is at its negative limit, the A90 Fan assembly is off.
FANTRIP	Fan Trip — A high on this line causes FANOFF to go low which allows the fan to turn on and cool the analyzer. This line goes high when the fan is turned off and the internal temperature exceeds a set point.
FD0 — FD15	Fast Bus Data Lines — These bidirectional data lines are a buffered version of the A7 CPU assembly's buffered microprocessor data bus. These lines allow communication between the CPU assembly and A6 Digital assembly.
FDTACKn	Fast Bus Data Transfer Acknowledge — A low on this line terminates asynchronous bus cycles.
FIFOBAVn	First In First Out Block Available — This line goes low after the FIFO gate array on the A6 Digital assembly collects a complete block of data.
FIFOENn	First In First Out Enable — This line pulses low in response to a low on FIFOBAVn. This line enables the transfer of one data word from the A6 Digital assembly's FIFO gate array to the A7 CPU assembly over the fast bus.
FIFORDYn	First In First Out Ready — This line goes low when a data word is ready to be transferred from the A6 Digital assembly over the fast bus.
FIRQn	Fast Bus Interrupt Request — A low on this line interrupts the A7 CPU assembly.
FRW	Fast Bus Read/Write — This line is high during a read cycle and low during a write cycle. This line is a buffered version of the read/write line (PRW).
FSDIV2	Sample Clock Divided By 2 — This is a 50% duty cycle, 131.072 kHz clock generated by the A6 Digital assembly to synchronize the A98 Power Supply assembly. The Power Supply assembly phase locks its switching frequency to this clock.

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FSELAn	Fast Bus Asynchronous Select — This line is low when an asynchronous fast bus cycle is in operation.
FSELSn	Fast Bus Synchronous Select — This line is low when a synchronous fast bus cycle is in operation. The A6 Digital assembly uses this signal to enable I/O to its gate arrays and to the A5 Analog assembly's source attenuator DAC and dc offset DAC.
H10MHZ	10 MHz Clock — This is a 50% duty cycle, 9.961472 MHz clock. This clock is H20MHZ divided by 2.
H20MHZ	20 MHz Clock — This is a 50% duty cycle, 19.922944 MHz clock. This clock provides the timing for the analyzer.
HRNGA	Half Range A — In both the two channel and four channel analyzer, a high on this line turns on the channel 1 half range LED. This line goes high when the A1 or A2 Input assembly detects that the amplitude of the channel 1 input signal reached half the set range.
HRNGB	Half Range B — In a two channel analyzer, a high on this line turns on the channel 2 half range LED. In a four channel analyzer, a high on this line turns on the channel 3 half range LED. This line goes high when the A1 Input assembly detects that the amplitude of the channel 2 input signal reached half the set range or when the A2 Input assembly detects that the amplitude of the channel 3 input signal reached half the set range.
HRNGC	Half Range C — In a four channel analyzer, a high on this line turns on the channel 2 half range LED. This line goes high when the A2 Input assembly detects that the amplitude of the channel 2 input signal reached half the set range. This line is only used in four channel analyzers.
HRNGD	Half Range D — In a four channel analyzer, a high on this line turns on the channel 4 half range LED. This line goes high when the A2 Input assembly detects that the amplitude of the channel 4 input signal reached half the set range. This line is only used in four channel analyzers.
HSYNC	Horizontal Synchronization — A high on this line causes the external monitor to do a horizontal retrace. The Motherboard buffers this signal and routes it to the EXT MONITOR connector.
IFCn	Interface Clear — This line is only used during the analyzer's development.
IMODE	Input Mode — This line indicates the A98 Power Supply assembly's input power mode. When this line is high, the Power Supply assembly is operating on ac power. When this line is low, the Power Supply assembly is operation on dc power.
INTHPIBn	GPIB Controller Interrupt — A low on this line interrupts the A7 CPU assembly. This line is controlled by the A10 Rear Panel assembly's GPIB controller.
INTONIXn	Parallel Port Interrupt — A low on this line interrupts the A7 CPU assembly. This line is controlled by the A10 Rear Panel assembly's parallel port controller.
KEYVALID	Key Valid — A high on this line interrupts the A7 CPU assembly. This line goes high when a key is pressed on an external keyboard.

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LPFCLK	Low Pass Filter Clock — This is a control line from the A6 Digital assembly's digital source. This line controls the cut-off frequency of the A5 Analog assembly's programmable low pass filter.
MDACCSn	Source Attenuation DAC Chip Select — This is a control line from the A6 Digital assembly's digital source. A low on this line enables the Attenuator DAC and DC offset DAC on the A5 Analog assembly.
PFWn	Power Fail Warning — This line goes low 10 ms before the A98 Power Supply assembly's output voltages fall out of regulation. A low on this line tells the A7 CPU assembly to prepare for power down and opens a relay which disconnects the source output on the A5 Analog assembly. This line goes low in response to SHUTn going low or when the supply voltage is disconnected or is too low.
PREFS	Pre-Sample Clock — This is a 262.144 kHz clock. This clock is at the same frequency as the system sample rate, but it is inverted and advanced in time by 100 ns.
PVALID	Power Valid — This line is high when the +5 V supply from the A98 Power Supply assembly is stabilized.
RA1 - RA5	Rear Bus Address Lines — These lines are a buffered form of the A7 CPU assembly's microprocessor address bus. The CPU assembly uses these lines to address different circuits on the A10 Rear Panel assembly.
RD24 - RD31	Rear Bus Data Lines — These bidirectional data lines are an extension of the A7 CPU assembly's digital data bus. These lines allow communication between the CPU assembly and A10 Rear Panel assembly.
RDTACKn	Rear Bus Data Transfer Acknowledge — A low on this line terminates asynchronous bus cycles.
RRESETn	Rear Reset — A low on this line resets the digital logic on the A10 Rear Panel assembly. This line pulses low during power-up and power-down and when the A7 CPU assembly's microprocessor executes the RESET instruction or is externally reset.
RRW	Rear Bus Read/Write — This line is high during a read cycle and low during a write cycle. This line is an extension of the processor read/write line (PRW).
RSI	RS-232 Input — This is the serial RS-232-C receive data line. This line transmits data to the A7 CPU assembly from peripheral devices one byte at a time.
RSO	RS-232 Output — This is the serial RS-232-C transmit data line. This line transmits data from the A7 CPU assembly to peripheral devices one byte at a time.
SCL	Serial Clock — This is the serial clock for the IIC bus. The IIC controller on the A7 CPU assembly generates this clock to synchronize the transfer of data on the IIC bus.
SDA	Serial Data — This is the IIC bus bidirectional data line. This line transmits data to or from the A7 CPU assembly in 8-bit frames. The IIC controller on the CPU assembly controls data transfers on the IIC bus.
SHUTn	Power Supply Shut Down — A connection to ground on this line forces all Power Supply output voltages to zero. This line is normally an open circuit, but becomes a connection to ground if the analyzer's internal temperature becomes excessive or if the power supply is operating on dc power and no measurement has been made within 30 minutes.
SINTn	Serial Interrupt — This is the IIC bus interrupt line. A low on this line interrupts the A7 CPU assembly.

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SRCCLOCK	Source Clock — This clock provides the timing for data transfer to the A5 Analog assembly's serial-in parallel-out shift register. This clock is generated by the A6 Digital assembly's digital source.
SRCDATA	Source Data — This is the data line for the A5 Analog assembly's serial-in parallel-out shift register. This serial data line is generated by the A6 Digital assembly's digital source.
SYSCNTR	System Control — A high on this line enables the A10 Rear Panel assembly's GPIB buffers. This line is high when the analyzer is under GPIB control.
TRIGGER	Trigger — This line changes state when the selected trigger (channel 1, channel 2, channel 3, channel 4, or external trigger) equals or exceeds the trigger level. An active edge on this line causes the A6 Digital assembly to trigger the analyzer.
VDATA	Video Data — This is the serial data line for the external monitor. The Motherboard buffers this line and routes three lines to the EXT MONITOR connector. Pin 3 is the data line for the color red, pin 4 is the data line for the color green, and pin 5 is the data line for the color blue.
VSYNC	Vertical Synchronization — A high on this line causes the external monitor to do a vertical retrace. The Motherboard buffers this signal and routes it to the EXT MONITOR connector.
WEHPIBn	GPIB Write Enable — A low on this line enables write operations to the A10 Rear Panel assembly's GPIB controller.

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A100 Disk Drive

The following table lists signals routed between the A100 Disk Drive assembly and the A7 CPU assembly. This table shows several things — if the assembly generates or uses the signal or voltage, and if a signal is bidirectional. A description of each signal follows the table.

Signal Name	Pin(s)	A7 P3	A100
DIR	17	S	•
DISKINn	22	•	S
DRIVESELn	21, 29	S	•
DSKCHGn	1	•	S
HDSEL	3	S	•
HIDENSn	33	•	S
INDEXn	27	•	S
MTRn	19, 31	S	•
ReDATAn	5	•	S
SELO	25	S	•
SEL1	23	S	•
STEPn	15	S	•
TOOn	9	•	S
WDATA	13	S	•
WGATE	11	S	•
WRIPROTn	7	•	S
+5 V	24, 26, 28	•	•
Gnd	2 20 (even)	•	•
Not Used	30, 32, 34		

S This assembly is the source of the signal.
• This assembly uses the signal.
This assembly does not use this signal.

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DIR	Direction — This line sets the direction for the disk head. A high on this line sets the direction away from the spindle. A low on this line sets the direction toward the spindle.
DISKINn	Disk In — This line goes low when a flexible disk is inserted in the A100 Disk Drive assembly.
DRIVESELn	Drive Select — A low on this line selects the A100 Disk Drive assembly.
DSKCHGn	Disk Change — This line goes low when a flexible disk is removed from the A100 Disk Drive assembly. This line remains low until a flexible disk is installed and STEPn goes low.
HDSEL	Head Select — A low on this line selects the lower disk drive head. A high on this line selects the upper disk drive head.
HIDENSn	High Density Select — This line goes low when a high density flexible disk is inserted in the A100 Disk Drive assembly.
INDEXn	Index — This line pulses low with each revolution of the flexible disk.
MTRn	Motor On — A low on this line turns on the disk drive motor.
ReDATAn	Read Data — This line pulses low for each bit detected on the flexible disk.
SEL0 - SEL1	Drive Select — When SEL0 and SEL1 are low, the A100 Disk Drive assembly is enabled.
STEPn	Step — A low on this line moves the disk drive head. When STEPn and DIR are low, the head moves toward the disk spindle. When STEPn is low and DIR is high, the head moves away from the disk spindle.
T00n	Track 00 — This line is low when the head is positioned over track 0 on the flexible disk.
WDATA	Write Data — When WGATE is low, a low pulse on this line writes a bit to the disk.
WGATE	Write Gate — When this line is low, information may be written to the A100 Disk Drive assembly under control of the WDATA line.
WRIPROTn	Write Protect — This line is low when a write-protected disk is installed in the A100 Disk Drive assembly.

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A101 Display

The following table lists signals routed between the A102 DC-DC Converter assembly and the A101 Display assembly. This table shows several things — if the assembly generates or uses the signal or voltage, and if a signal is bidirectional. A description of each signal follows the table.

Signal Name	Pin(s)	A102	A101
HSYNCELn	11	•	•
PSENBLn	18	•	S
VCLK	15	•	•
VID	13	•	•
VSYNCEL	9	•	•
+215 V	4	S	•
-175 V	1	S	•
+40 V	5	S	•
+20 V	17	S	•
+12 V	6	•	•
+5 V	7	•	•
Gnd	2, 3, 12, 14, 16	•	•
Not Used	19, 20		

S This assembly is the source of the signal.
• This assembly uses the signal.
This assembly does not use this signal.

HSYNCELn — Horizontal Synchronization — A low on this line causes a horizontal retrace on the A101 Display assembly. Between each HSYNCELn pulse, 560 pixels are sent to the Display assembly.

PSENBLn — Power Supply Enable — A low on this line enables the A102 DC-DC Converter assembly's power supply. The power supply generates the driver supply voltages. The driver supply voltages are +20 V, +40 V, +215 V, and –175 V.

VCLK — Video Clock — This 20 MHz clock provides the timing reference for HSYNCELn, VID, and VSYNCEL. The rising edge of this clock determines setup and hold times.

VID — Video Data — This is the serial data line for the A101 Display assembly. This line transmits video data to the Display assembly. The video data is transmitted at the VCLK rate between horizontal and vertical retraces (during the time HSYNCELn is high and VSYNCEL is low). Only the first 400 lines of data are displayed after a VSYNCEL pulse.

VSYNCEL — Vertical Synchronization — A high on this line causes a vertical retrace on the A101 Display assembly.

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A102 DC-DC Converter

The following table lists signals routed between the A7 CPU assembly and the A102 DC-DC Converter assembly. This table shows several things — if the assembly generates or uses the signal or voltage, and if a signal is bidirectional. A description of each signal follows the table.

Signal Name	Pin(s)	A7 P2	A102
HSYNCELn	11	S	•
VCLK	13	S	•
VID	15	S	•
VSYNCEL	9	S	•
+12 V	1, 2	•	•
+5 V	3, 4	•	•
Gnd	7, 8, 10, 12, 14, 16	•	•
Not Used	5, 6		

S This assembly is the source of the signal.
• This assembly uses the signal.
This assembly does not use this signal.

HSYNCELn — Horizontal Synchronization — A low on this line causes a horizontal retrace on the A101 Display assembly. Between each HSYNCELn pulse, 560 pixels are sent to the Display assembly.

VCLK — Video Clock — This 20 MHz clock provides the timing reference for HSYNCELn, VID, and VSYNCEL. The rising edge of this clock determines setup and hold times.

VID — Video Data — This is the serial data line for the A101 Display assembly. This line transmits video data to the Display assembly. The video data is transmitted at the VCLK rate between horizontal and vertical retraces (during the time HSYNCELn is high and VSYNCEL is low). Only the first 400 lines of data are displayed after a VSYNCEL pulse.

VSYNCEL — Vertical Synchronization — A high on this line causes a vertical retrace on the A101 Display assembly.

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10

Internal Test Descriptions

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Internal Test Descriptions

This chapter describes the power-on test, calibration routine, fault log messages, and self tests. This chapter also contains a list of the GPIB commands for each self test.

Power-on Test Description

The power-on test is run when the analyzer is powered up. The calibration routine is run immediately following the power-on test. The power-on test exercises the A7 CPU assembly and A8 Memory assembly. This test is divided into low-level and high-level subtests.

Low-level Subtests

The low-level power-on subtests exercise the core of the A7 CPU assembly and A8 Memory assembly. If an error occurs during the low-level subtests, the test stops and displays an error code on the A7 CPU assembly's power-on test LEDs.

High-level Subtests

The high-level power-on subtests exercise the fast bus and the multi-function peripheral on the A7 CPU assembly. The high-level subtests are also self tests (see ''Self-Test Descriptions''). If an error occurs during the high-level subtests, an error message is entered in the test log.

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Power-on Test Messages

The ‘’Power-on Test Messages’’ table provides additional information for interpreting the power-on test LEDs. Using the ‘’Binary to Hexadecimal’’ table, translate the power-on test LEDs to their equivalent hexadecimal code (see ‘’To troubleshoot power-up failures’’ on page 4-15 for details on decoding the power-on test LEDs to their binary code). The ‘’Power-on Test Messages’’ table describes the power-on subtests in the order they are run. The table also shows the relationship between a failing power-on subtest and the assemblies or sub-blocks.

False error codes can be caused by shorts on the buses, reset line, or interrupt line. If an error code is caused by the last bus connected, it is probably the source of the failure.

Binary to Hexadecimal

Binary 1 = LED on 0 = LED off	Hexadecimal
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7
1000	8
1001	9
1010	A
1011	B
1100	C
1101	D
1110	E
1111	F

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Power-on Test Messages

Hexadecimal Code	Message	Assembly/Sub-block								
		A98 Power Supply	A7 MPU & Address Decoder	A7 MPU Buses, Coprocessor, DSP, MFP	A7 Monitor ROM	A7 Display Controller	A8 Memory	Fast Bus or IIC Bus	A11 Keyboard Controller	
Undefined	Initial power-on	X	X	X						
FF*	CPU flashes LEDs	0	X	X	X					
04	LED DSACK failure	0	X	X	X					
13	CPU failure	0	X	X	X					
01	Coprocessor DSACK failure	0	0	X	X					
17	Coprocessor failure	0	0	X	X					
18	Boot ROM checksum failure	0	0	0	X					
06	Display DSACK failure	0	0	0	0	X				
10	Display failure	0	0	0	0	X				
1B	Main RAM too small	0	0	0	0	0	X			
02	Main RAM DSACK	0	0	0	0	0	X			
14	Main RAM bit failure	0	0	0	0	0	X			
16	Main RAM refresh failure	0	0	0	0	0	X			
1C	Program ROM checksum error	0	0	0	0	0	X			
00	Clear ~4s	0	X	X	0	0				
A1	Starting DSP test	0	0	X	0	0	0			
A2	Fast bus test	0	0	0	0	0	0	X		
A0	MFP test failure	0	0	X	0	0				
AE	Front panel test	0	0	X	0	0	0	0	X	

0 Assembly or sub block is used but is probably not the cause of the failure message.
X Assembly or sub block is probably the cause of the failure message.
(blank) Assembly or sub block is not used in the test.
FF* If the area of failure is unclear, all LEDs flash continuously.

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Calibration Routine Description

The calibration routine consists of a dc-offset calibration and a frequency calibration. The calibration routine occurs immediately following the power-on tests and periodically afterwards to compensate for any drift. The calibration routine sets the input relays to disconnect the internal circuitry from the BNC center conductor and shell, and connect the source (via CALP) to the input channels. Measurements are then taken using several input paths to produce correction curves for all input ranges.

If calibration fails, the calibration routine is repeated up to two more times. Each time calibration fails, a calibration failure message is added to the fault log. If calibration fails all three times, a calibration failure message is displayed on the screen.

If you abort a self test before the self test is finished, the analyzer may fail its calibration routine. To prevent this from happening, press [**Preset**] [DO PRESET] or cycle power after you abort a self test.

To manually start the calibration routine, press the [**System Utility**] [CALIBRATN] [SINGLE CAL].

To prevent the calibration routine from occurring, set the power switch to on (|), then as soon as Booting System appears on the display, press and hold in the [**Preset**] key until Autorange in progress appears. This not only prevents the calibration routine from occurring but also bypasses the auto start file if one exists.

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DC-Offset Tables and Frequency Correction Curves

The dc-offset calibration builds 5 dc-offset tables — one for each anti-alias filter and one for each channel when the anti-alias filters are bypassed. The values in the dc-offset tables are sent to the channel dc-offset DACs to compensate for dc offsets introduced by analog input circuits. Forty values are entered in each table — a value for each range setting from –51 dB to +27 dB, in 2 dB increments. For each range, the table value is derived by changing the offset values of the dc offset DAC until the best possible offset compensation is found. In all instrument modes, the analyzer corrects for dc offsets by setting each channel's dc-offset DAC to the value from the table that matches the current anti-alias filter and range setting.

The frequency calibration generates correction curves in the frequency domain to compensate for unflatness in the analog input circuits. A precise signal is connected from the source to the input channels via the calibration path (CALP). Correction curves are then produced for each range setting by taking the difference between the source output and the measured response. In FFT analysis, correlation analysis, and swept sine instrument modes, the analyzer multiplies the measured result with the value from the frequency correction curve that matches the current range and span setting. In this way, errors introduced by circuits in the analyzer are removed before the measurement is displayed.

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Calibration Error Messages

The dc-offset tables and frequency correction curves produced by the calibration routine are compared with a set of maximum allowable error curves. The Quick Confidence self test runs the calibration routine and places error messages in the Test Log if any measurement exceeds the maximum allowable error. To run the Quick Confidence self test press the following keys:

[**System Utility**]
  [SELF TEST]
  [QUICK CONF TEST]

The following lists the possible error messages:

Quick Confidence failure information:
Channel X 0 dB freq
Channel X 20 dB freq
Channel X 40 dB freq
Channel X step attenuator
Channel X –12 dB pad
Channel X +14 dB pad
Quick Confidence FAIL

Where X = 1, 2, 3, or 4 and freq = 100k, 50k, or 25k

Viewing the Calibration Correction Curves

The calibration correction curves can be viewed for any input range or frequency span. However, there is no frequency correction if the anti-alias filter is bypassed or if the A-weight filter is on. When there is no frequency correction, the calibration curve is a flat 0 dB line.

You can save the calibration trace to a data register only when in FFT analysis or correlation analysis instrument mode. However, these data registers can be displayed in any instrument mode.

The following key sequence shows how to view the calibration correction curves for channel 1 and 2 at a 1 Vrms range setting, full span. Other curves can be displayed by changing the input range and frequency span.

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[**Inst Mode**]
[2 CHANNEL]
[**Input**]
[CHANNEL 1 RANGE]
1
[dBVrms]
[CHANNEL 2 RANGE]
1
[dBVrms]
[**Disp Format**]
[UPPER/LOWER]
[**System Utility**]
[CALBRATIN]
[SAVE CH1 CAL TRACE]
[INTO D1]
[SAVE CH2 CAL TRACE]
[INTO D2]
[**Meas Data**]
[MORE]
[DATA REGISTER]
[D2]
[**Active Trace**]
[D1]
[**Scale**]
[Y PER DIV (DECADES)]
1
[ENTER]
[CENTER REFERENCE]
0
[ENTER]
[**Active Trace**]
[Y PER DIV (DECADES)]
1
[ENTER]
[CENTER REFERENCE]
0
[ENTER]

Note

Display A shows the message D1 CAL CHAN 1 and display B shows the message D2 CAL CHAN 2.

The calibration correction curves should be contained within ±5 dB. The ±5 dB limit applies to all ranges at full span.

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Fault Log Messages

0	Unknown Fault	This error message occurs when the fault could not be determined.
1	I2C: Timeout	This error message occurs if the A7 CPU assembly's IIC controller takes too long to tell the MPU that it is ready for a new command.
2	I2C: No Device Acknowledge	This error message occurs if the A7 CPU assembly's IIC controller does not sense the acknowledge part of the formal handshake used to transmit data over the IIC bus.
3	Calibration failure	This error message occurs if the calibration routine generates correction vectors that exceed the maximum allowable error vectors or if the calibration routine is bypassed because of a hardware failure.
4	ROM Checksum error	This error message occurs if the power-on test detects a ROM checksum error.
5	BOOTROM Checksum Error	This error message occurs if the power-on test detects a BOOTROM checksum error.
6	DSP Failure	This error message occurs if the power-on digital signal processor test fails.
7	Main RAM Error	This error message occurs if the power-on RAM test fails.
8	Math Coprocessor Failure	This error message occurs if the power-on math coprocessor test fails.
9	LED Error	This error message occurs if the power-on LED test fails.
10	Display Failure	This error message occurs if the power-on display test fails.
11	CPU Failure	This error message occurs if the power-on CPU test fails.
12	Floppy Controller Timeout	This error message occurs if the A7 CPU assembly's disk drive controller did not respond within 10 ms of receiving a command.
13	Internal Disk Trk0 Failure	This error message occurs if the A100 Disk Drive assembly did not locate track 0 (as indicated by a low on T00n) when instructed by the A7 CPU assembly to move to track 0.
14	NVRAM or Battery Backup Failure	This error message occurs if the A7 CPU assembly's IIC Controller determined that the A8 Memory assembly's non-volatile RAM or RAM battery power failed.

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Self-Test Descriptions

Thirty-seven self tests are available that can be run in groups or individually. The following table lists the group of self tests that are run when you select [FUNCTIONL TESTS], [ALL]. This group does not include any of the self tests that require a formatted flexible disk. The table lists the assemblies used by each self test and shows the assembly that would most likely cause the failure. To run these self tests in the order shown, press the following keys:

[**System Utility**]
  [SELF TEST]
  [FUNCTIONL TESTS]
  [ALL]

To run a single self test, press the softkey shown in the table instead of [ALL]. To determine the key path for the self-test softkeys, see “Self-Test Menu Map and GPIB Commands” starting on page 10-18.

Certain instrument malfunctions cause multiple self-test failures. Therefore, to determine the most likely cause when more than one self test fails, look in the ‘’Functional Tests All Self-Test Group’’ table for assemblies common to all failing self tests.

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Functional Tests All Self-Test Group

Softkey	Self Test Name	Assembly									
		CPU	Memory	Digital	BNC	Input	Input	Analog	Rear Panel	Keyboard Contrr	Disk Driv
		A7	A8	A6	A12/ A22	A1	A2	A5	A10	A11	A100
[INTERRUPT]	Interrupt	X	0								
[MULTI FCTN PERIPHERL]†	Multi Fctn Peripheral	X	0								
[FRONT PANEL]†	Front Panel	X	0							X	
[GPIB FUNC TEST]	GPIB	X	0								
[DISK CONTROLLR]	Disk Controller	X	0								
[DISK FIFO]	Disk FIFO	X	0								
[IIC BUS]	IIC Bus	X	0	X		X	X	X	X	X	
[FAST BUS]†	Fast Bus	X	0	X							
[TRIGGER]	Trigger Gate Array	0	0	X							
[LO]	LO Gate Array	0	0	X							
[DIGITAL FILTER]	Digital Filter Gate Array	0	0	X							
[FIFO]	FIFO	0	0	X							
[BASEBAND]	Baseband	0	0	X		X	X	X			
[ZOOM]	Zoom	0	0	X		X	X	X			
[DGTL SRCE THRU DSP]	Source through DSP	0	0	X							
[SOURCE LO]	Source LO	0	0	X							
[SOURCE TO CPU]	Source to CPU	0	0	X							
[WITHOUT LO]	Source without LO	0	0	X		X	X	X			
[WITH LO]	Source with LO	0	0	X		X	X	X			
[ADC GATE ARRAY]	ADC Gate Array	0	0	0				X			
[OFFSET]	Input Offset	0	0	0		X	X	X			
[DISTORTN]	Input Distortion	0	0	0		X	X	X			
[INPUT TRIGGER]	Input Trigger	0	0	0		X	X	X			
[INPUT A-WEIGHT]	Input A-Wt Filter	0	0	0		X	X	X			
[AAF BYPASS]	Input AAF/Bypass	0	0	0		X	X	X			
[INPUT ICP]	Input ICP Source	0	0	0		X	X	X			
[TACHOMETR]$! C5,5,0,255,255,255	Tachometer	0	0	X	0				X		
[QUICK CONF TEST]	Quick Confidence	0	0	0		X	X	X			

X This assembly or sub-block is the most likely cause of the failure message. 0 This assembly or sub-block is used by the self test but is not the most likely cause of the failure message. No symbol means that the assembly is not used by the self test.

† High level power on tests
The power supply and display are used in every test.

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Self Tests that Perform a Measurement

The following self tests perform measurements:

Self Test	Front Panel Softkey
Baseband	[BASEBAND]
Zoom	[ZOOM]
Source thru DSP	[DGTL SRCE THRU DSP]
ADC gate array	[ADC GATE ARRAY]
Source to CPU	[SOURCE TO CPU]
Source with LO	[WITH LO]
Source Without LO	[WITHOUT LO]
Input Offset	[OFFSET]
Input Distortion	[DISTORTN]
Input Trigger	[INPUT TRIGGER]
Input A-Wt Filter	[INPUT A-WEIGHT]
Input AAF/Bypass	[AAF BYPASS]
Input ICP Source	[INPUT ICP]

The measurements that these self tests perform are averaged measurements, with only one trace per average. Some hardware setup modes used in these self tests are not used by normal measurements and can not be accessed from the front panel.

The measurements bypass any standard corrections and do not perform calibration data corrections. Therefore, all self-test measurements using analog data have limits larger than the standard calibration tolerances.

Once the hardware is set up, data is taken and time records are processed according to the needs of the specific test. Some tests monitor overloads, others require spectrum data, and others require time record data. After the data is collected, it is compared to an internal reference specification to determine if the self test passed or failed. The pass or fail information along with any additional information is placed in the Test Log.

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Individual Self-Test Descriptions

[AAF BYPASS] This test verifies that the anti-alias filters and the bypass circuits on the A1 Input assembly or A2 Input assemblies are operating correctly. In this test, the A5 Analog assembly's source outputs a signal that is connected to the input channels via the calibration path (CALP). For the A1 Input assembly's channel 1, power spectrum measurements are made with the signal routed through the 100 kHz anti-alias filter, the 50 kHz anti-alias filter, and the bypass circuit. For the A1 Input assembly's channel 2, power spectrum measurements are made with the signal routed through the 50 kHz anti-alias filter and the bypass circuit. For the A2 Input assembly's channel 1 or 2, power spectrum measurements are made with the signal routed through the 50 kHz anti-alias filter, the 25 kHz anti-alias filter, and the bypass circuit. For the A2 Input assembly's channel 3 or 4, power spectrum measurements are made with the signal routed through the 25 kHz anti-alias filter and the bypass circuit.

[ADC GATE ARRAY] This test verifies that the A5 Analog assembly's ADC gate array is functioning correctly. This test consists of 7 tests — positive overflow, negative overflow, positive limit, negative limit, 1st pass, 2nd pass, and zero. The positive and negative overflow tests set up the ADC test mode to cause positive and negative overflows, then check the A6 Digital assembly's digital filter for interrupt flags. The positive and negative limit tests check the ADC's positive and negative limits. The 1st and 2nd pass tests connect the calibration signal from the A5 Analog assembly to the A1 Input assembly or A2 Input assemblies. The 1st pass test sets the 2nd pass result to zero and checks the signal into the ADC for the proper value and the A6 Digital assembly's gate array for interrupts or overloads. The 2nd pass test sets the 1st pass result to zero and checks the signal into the ADC for the proper value and the A6 Digital assembly's gate array for interrupts or overloads. The zero test checks for minimal output while the gate array outputs zero data.

[BASEBAND] This test verifies that the A6 Digital assembly's gate arrays are operating correctly. The trigger gate array provides dc input data. The signal is then measured at 0 Hz for 63.58 Vpk ±0.635V and from 4 Hz to 1.6 kHz for 0 Vpk ±0.06358V.

[DGTL SRCE THRU DSP] This test verifies that the A6 Digital assembly's gate arrays and digital source are operating correctly. In this test, the digital source outputs a periodic chirp to the gate arrays. The resultant spectrum is then checked from 384 Hz to 51.2 kHz.

[DIGITAL FILTER] This test verifies that the digital filter's gate array on the A6 Digital assembly is operating correctly. The A7 CPU assembly's microprocessor configures the digital filter's gate array over the fast bus. The microprocessor then reads the control lines to check circuits internal to the gate array and verify correct configuration. This test also writes to and reads from the gate array's RAM, checking for stuck bits. The Trigger Gate Array test [TRIGGER] and the LO Gate Array test [LO] must pass for this test to pass. No data paths on the A6 Digital assembly are checked.

[DISK CONTROLLR] This test verifies that the disk controller on the A7 CPU assembly is operating correctly. In this test, the microprocessor sends a series of writes to and reads from the disk controller.

[DISK FIFO] This test verifies that the disk controller's FIFO on the A7 CPU assembly is operating correctly. In this test, the CPU assembly's microprocessor writes 2048 pseudo-random bytes to the disk FIFO. The microprocessor then reads the disk FIFO.

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[DISTORTN] This test checks for noise and distortion in the input circuits of the A1 Input assembly or A2 Input assemblies. In this test, the A5 Analog assembly's source outputs a signal that is connected to the input channels via the calibration path (CALP). For each channel in the A1 Input assembly, the signal is measured at 16.640 kHz for 5 Vpk ±0.5 Vpk and from 24.96 kHz to 51.2 kHz for 0 Vpk ±0.01V. For each channel in the A2 Input assemblies, the signal is measured at 8.320 kHz for 5 Vpk ±0.5 Vpk and from 12.48 kHz to 25.6 kHz for 0 Vpk ±0.01V.

[FAST BUS] This test verifies that the fast bus is operating correctly. In this test, the microprocessor on the A7 CPU assembly writes data to the trigger gate array and digital tach on the A6 Digital assembly over the fast bus. The microprocessor then reads the data.

[FIFO] This test verifies that the FIFO gate array on the A6 Digital assembly is operating correctly. In this test, the A7 CPU assembly's microprocessor configures the FIFO gate array. The microprocessor then reads the control lines to check circuits internal to the gate array and verify correct configuration. The Trigger Gate Array [TRIGGER], Digital Filter Gate Array [FILTER], and LO Gate Array [LO] tests must pass for this test to pass. No data paths on the Digital assembly are checked.

[FRONT PANEL] This test verifies that the IIC controller on the A11 Keyboard Controller assembly is operating correctly. In this test, the microprocessor on the A7 CPU assembly reads the IIC controller on the Keyboard Controller assembly and verifies that no front-panel keys are held down.

[GPIB CONNECTOR] This test was not implemented.

[GPIB FUNC TEST] This test verifies that the GPIB interface on the A10 Rear Panel assembly is operating correctly. In this test, the A7 CPU assembly's microprocessor sets the GPIB interface to a listen only state, then tests for a listen only state.

[IIC BUS] This test verifies that the A7 CPU assembly can write to and read from all assemblies with IIC interfaces. This test also checks the A7 CPU assembly's EEROM. The following assemblies have IIC interfaces:

A1 Input
A2 Input
A5 Analog
A6 Digital
A8 Memory
A10 Rear Panel
A11 Keyboard Controller

[INPUT A-WEIGHT] This test verifies that the A-weight filters on the A1 Input assembly or A2 Input assemblies are operating correctly. In this test, the A5 Analog assembly's source outputs a chirp signal that is connected to the input channels via the calibration path (CALP). For each channel, the power spectrum is measured at three frequencies with and without the A-weight filter in the input path.

[INPUT ICP] This test verifies that the ICP sources on the A1 Input assembly or A2 Input assemblies are operating correctly. In this test, the ICP sources are turned on, then measured for 25 ±10 Vdc. During this test, the front panel input BNC connectors must not be connected to anything.

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[INPUT TRIGGER] This test checks the trigger-level circuits on the A5 Analog assembly for both positive and negative slope triggering. In this test, the A5 Analog assembly's source outputs a 512 Hz, 5 Vpk signal that is connected to the input channels via the calibration path (CALP).

[INTERRUPT] This test verifies that the interrupt circuits on the A7 CPU assembly are operating correctly. In this test, the microprocessor writes to the multi-function peripheral interrupt registers and reads the registers for verification. This test does not actually set up an interrupt but does test the multi-function peripheral in greater depth than the [MULTI FCTN PERIPHERL] test.

[LO] This test verifies that the local oscillator gate array on the A6 Digital assembly is operating correctly. In this test, the A7 CPU assembly's microprocessor configures the local oscillator gate array. The microprocessor then reads the control lines to check circuits internal to the gate array and verify correct configuration. The microprocessor then checks the phase of its internal oscillator. The Trigger Gate Array [TRIGGER] test must pass for this test to pass. No data paths on the A6 Digital assembly are checked.

[LONG CONF TEST] This test performs most of the self tests. The tests are performed in the following order:

[INTERRUPT]
[MULTI FCTN PERIPHERL]
[FRONT PANEL]
[GPIB FUNC TEST]
[DISK CONTROLLR]
[DISK FIFO]
[IIC BUS]
[FAST BUS]
[TRIGGER]
[LO]
[DIGITAL FILTER]
[FIFO]
[BASEBAND]
[ZOOM]
[DGTL SRCE THRU DSP]
[SOURCE LO]
[SOURCE TO CPU]
[WITHOUT LO]
[WITH LO]
[ADC GATE ARRAY]
[OFFSET]
[DISTORTN]
[INPUT TRIGGER]
[INPUT A-WEIGHT]
[AAF BYPASS]
[QUICK CONF TEST]

[MULTI FCTN PERIPHERL] This test verifies that the multi-function peripheral on the A7 CPU assembly is operating correctly. In this test, the microprocessor writes to the multi-function peripheral, then reads the registers checking for errors. Further testing of the multi-function peripheral is done by the [INTERRUPT] test.

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[OFFSET] This test verifies that the analyzer can correct for dc offsets generated by the input circuits on the A1 Input assembly or A2 Input assemblies. In this test, the input circuits are connected to ground. For the A1 Input assembly's channel 1, time record measurements are taken with the signal routed through the 100 kHz anti-alias filter and through the 50 kHz anti-alias filter with the dc offset DAC set to 127, then to –127. For the A1 Input assembly's channel 2, time record measurements are taken with the signal routed through the 50 kHz anti-alias filter with the dc offset DAC set to 127, then to –127. For the A2 Input assembly's channel 1 or 2, time record measurements are taken with the signal routed through the 50 kHz anti-alias filter and through the 25 kHz anti-alias filter with the dc offset DAC set to 127, then to –127. For the A2 Input assembly's channel 3 or 4, time record measurements are taken with the signal routed through the 25 kHz anti-alias filter with the dc offset DAC set to 127, then to –127.

[QUICK CONF TEST] This test calibrates the analyzer and checks the calibration limits. Any calibration errors are entered in the Test Log. See "Calibration Routine Description" earlier in this chapter for a description of the calibration routine.

[RANDOM SEEK] This test verifies that the A100 Disk Drive assembly's head can move to a random sector on the flexible disk. In this test, the disk controller on the A7 CPU assembly instructs the disk-drive head to move to a random record. This test requires a formatted flexible disk.

[READ] This test verifies that the A100 Disk Drive assembly can read a flexible disk. In this test, the A7 CPU assembly's disk controller instructs the Disk Drive assembly to read the current record on the flexible disk. While the current record is being read, the disk controller monitors the RDDATAn signal to verify the read operation. The current record is set by the [SEEK RECORD] test. This test requires a formatted flexible disk.

[READ/WRITE] This test verifies that the A100 Disk Drive assembly can read and write to a flexible disk. In this test, the A7 CPU assembly's disk controller instructs the Disk Drive assembly to read the current record on the flexible disk. While the current record is being read, the disk controller monitors the RDDATAn signal to verify the read operation. The disk controller then instructs the Disk Drive assembly to write to the current record. While the current record is being written to, the disk controller monitors the WDATAn signal to verify the write operation. The current record is set by the [SEEK SECTOR] test. This test requires a formatted flexible disk that is not write protected.

[READ/WRITE ALL] This test verifies that the A100 Disk Drive assembly can read and write to all records of a flexible disk. In this test, the A7 CPU assembly's disk controller instructs the Disk Drive assembly to read every available record on the flexible disk (excluding privileged tracks). While the flexible disk is being read, the disk controller monitors the RDDATAn signal to verify the read operation. The disk controller then instructs the Disk Drive assembly to write to every available record on the flexible disk (excluding privileged tracks). While the flexible disk is being written to, the disk controller monitors the WDATAn signal to verify the write operation. This test stops on the first error. The execution time for this test depends upon the size of the disk. For example, if there are no errors, this test takes approximately one hour for a double-sided, low-density disk. This test requires a formatted flexible disk that is not write protected.

[RESTORE] This test verifies that the A100 Disk Drive assembly's head can move away from track 0, then back to track 0. In this test, the A7 CPU assembly's disk controller instructs the disk-drive head to move away from track 0, then back to track 0. The disk controller monitors the T00n signal to verify the move operation. This test requires a formatted flexible disk.

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[SERIAL PORT] This test verifies that the RS-232 interface on the A7 CPU assembly is capable of sending and receiving data. In this test, the user connects the transmit data line to the recieve data line. Data is sent out on the transmit data line and read back on the receive data line.

[SEEK RECORD] This test verifies that the A100 Disk Drive assembly's head can move to a user specified record on the flexible disk. In this test, the disk controller on the A7 CPU assembly instructs the disk-drive head to move to a user specified record. The user specified record number must be in the range of valid record numbers. The default record number is 0. This test requires a formatted flexible disk.

[SOURCE LO] This test verifies that the local oscillator (LO) gate array on the A6 Digital assembly is operating correctly. In this test, the A7 CPU assembly's microprocessor configures the LO gate array and reads its control lines to check circuits internal to the gate array and verify correct configuration. No data paths on the Digital assembly are checked.

[SOURCE TO CPU] This test verifies that the core of the digital source on the A6 Digital assembly is operating correctly. In this test, the A7 CPU assembly's microprocessor configures the digital source to output a 12.8 kHz chirp. The microprocessor then reads the final chirp value in the digital-source RAM. This test does not use the time record to verify the chirp.

[TACHOMETR] This test verifies that the tachometer circuits on the A10 Rear Panel assembly and A6 Digital assembly are operating correctly. In this test, a BNC cable must be connected from the source connector to the tachometer connector. The tachometer pulses are counted for 200 milliseconds with the source turned off. The count should be zero. Next the source is set to 100 Hz, 3.53 Vrms and the tachometer pulses are counted for another 200 milliseconds. This time the count should be 20 ±1.

[TRIGGER] This test verifies that the trigger gate array on the A6 Digital assembly is operating correctly. In this test, the A7 CPU assembly's microprocessor configures the trigger gate array. The microprocessor then reads the control lines to check circuits internal to the gate array and verify correct configuration. This test also verifies functions internal to the gate array such as internal trigger level, trigger interrupts, overload interrupts, and post trigger delay.

[WITH LO] This test verifies the capability of the A5 Analog assembly's analog source to output a flat zoomed periodic chirp signal. In this test, the A6 Digital assembly's local oscillator is used with the analog source to produce a zoomed periodic chirp signal. The signal is connected to the input channels via the calibration path (CALP). The flatness of the signal is measured from 13.6 kHz to 26.4 kHz.

[WITHOUT LO] This test verifies the capability of the A5 Analog assembly's analog source to output a flat baseband chirp signal. In this test, the Analog assembly's analog source outputs a baseband chirp signal (starting at 0 Hz) that is connected to the A1 Input assembly or A2 Input assemblies via the calibration path (CALP). The flatness of the signal is measured from 384 Hz to 51.2 kHz.

[ZOOM] This test checks most of the DSP chain, including the LO gate array. In this test, the Digital assembly's trigger gate array outputs a dc value to the DSP chain.

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Self-Test Menu Map and GPIB Commands

The analyzer's self tests can be run from the front panel or by a controller via GPIB. To run a test from the front panel, press [**System Utility**] followed by the appropriate softkey in the table. To run a test via GPIB, send the equivalent GPIB command (to abort a test, send TEST:ABOR).

To view the analyzer's fault log via GPIB, send DISP:CONT FTAB. To clear the fault log send SYST:FLOG:CLE. To return to the top line of the test log and delete the line from the test log, send TEST:LOG:DATA:LINE?

The following table shows the softkeys and GPIB commands for each self test.

Self Test	GPIB Command
[SELF TEST]	–
[QUICK CONF TEST]	*TST?
[LONG CONF TEST]	TEST:LONG
[FUNCTIONL TESTS]	–
[DISPLAY PATTERN]	TEST:DISP:PATT ON | OFF
[I/O]	–
[FRONT PANEL]	TEST:IO:FPAN; *WAI
[GPIB]	–
[GPIB FUNC TEST]	TEST:IO:GPIB; *WAI
[GPIB CONNECTOR]	–
[INTERNAL DISK]	–
[DISK CONTROLLR]	TEST:IO:DISK:CONT; *WAI
[DISK FIFO]	TEST:IO:DISK:FIFO; *WAI
[RESTORE]	TEST:IO:DISK:REST; *WAI
[RANDOM SEEK]	TEST:IO:DISK:RAND; *WAI
[SEEK RECORD]	TEST:IO:DISK:SEEK n; *WAI †
[READ]	TEST:IO:DISK:READ; *WAI
[READ/WRITE]	TEST:IO:DISK:WRIT; *WAI
[READ/WRITE ALL]	TEST:IO:DISK:RWR; *WAI
[ALL]	TEST:IO:DISK:ALL; *WAI
[IIC BUS]	TEST:IO:IIC; *WAI
[FAST BUS]	TEST:IO:FBUS; *WAI
[SERIAL PORT]	TEST:IO:SER; *WAI
[ALL]	TEST:IO:ALL; *WAI

† where n 0 to [(tracks per side x sides x sectors per track) 1]

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Self Test	GPIB Command
[SELF TEST]	–
[FUNCTIONL TESTS]	–
[DIGITAL PROCESSOR]	–
[TRIGGER]	TEST:DSP:TRIG; *WAI
[LO]	TEST:DSP:LO; *WAI
[DIGITAL FILTER]	TEST:DSP:FILT; *WAI
[FIFO]	TEST:DSP:FIFO; *WAI
[BASEBAND]	TEST:DSP:BAS; *WAI
[ZOOM]	TEST:DSP:ZOOM; *WAI
[DGTL SRCE THRU DSP]	TEST:DSP:SOUR; *WAI
[ALL]	TEST:DSP:ALL; *WAI
[SOURCE]	–
[SOURCE LO]	TEST:SOUR:LO; *WAI
[SOURCE TO CPU]	TEST:SOUR:CPU; *WAI
[WITHOUT LO]	TEST:SOUR:BAS; *WAI
[WITH LO]	TEST:SOUR:ZOOM; *WAI
[ALL]	TEST:SOUR:ALL; *WAI
[INPUTS]	–
[OFFSET]	TEST:INP:OFFS; *WAI
[DISTORTN]	TEST:INP:DIST; *WAI
[INPUT TRIGGER]	TEST:INP:TRIG; *WAI
[INPUT A-WEIGHT]	TEST:INP:AWE; *WAI
[AAF BYPASS]	TEST:INP:AAF; *WAI
[INPUT ICP]	TEST:INP:ICP; *WAI
[ALL]	TEST:INP:ALL; *WAI
[TACHOMETR]	TEST:TACH; *WAI
[ADC GATE ARRAY]	TEST:ADC:GARR; *WAI
[OTHER]	–
[INTERRUPT]	TEST:PROC:INT; *WAI
[MULT FCTN PERIPHERL]	TEST:PROC:MFP; *WAI
[ALL]	TEST:PROC:ALL; *WAI
[ALL]	TEST:ALL; *WAI
[LOOP MODE ON/OFF]	TEST:LOOP:MODE ON | OFF
[TEST LOG]	DISP:CONT TTAB
[CLEAR TEST LOG]	TEST:LOG:CLE
[NEXT PAGE]	–
[PREVIOUS PAGE]	–

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11

Backdating

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Backdating

This chapter provides information necessary to modify this manual for instruments that differ from those currently being produced. The information in this chapter documents earlier instrument configurations and associated servicing procedures.

With the information provided in this chapter, this manual can be corrected so that it applies to any earlier version or configuration of the instrument.

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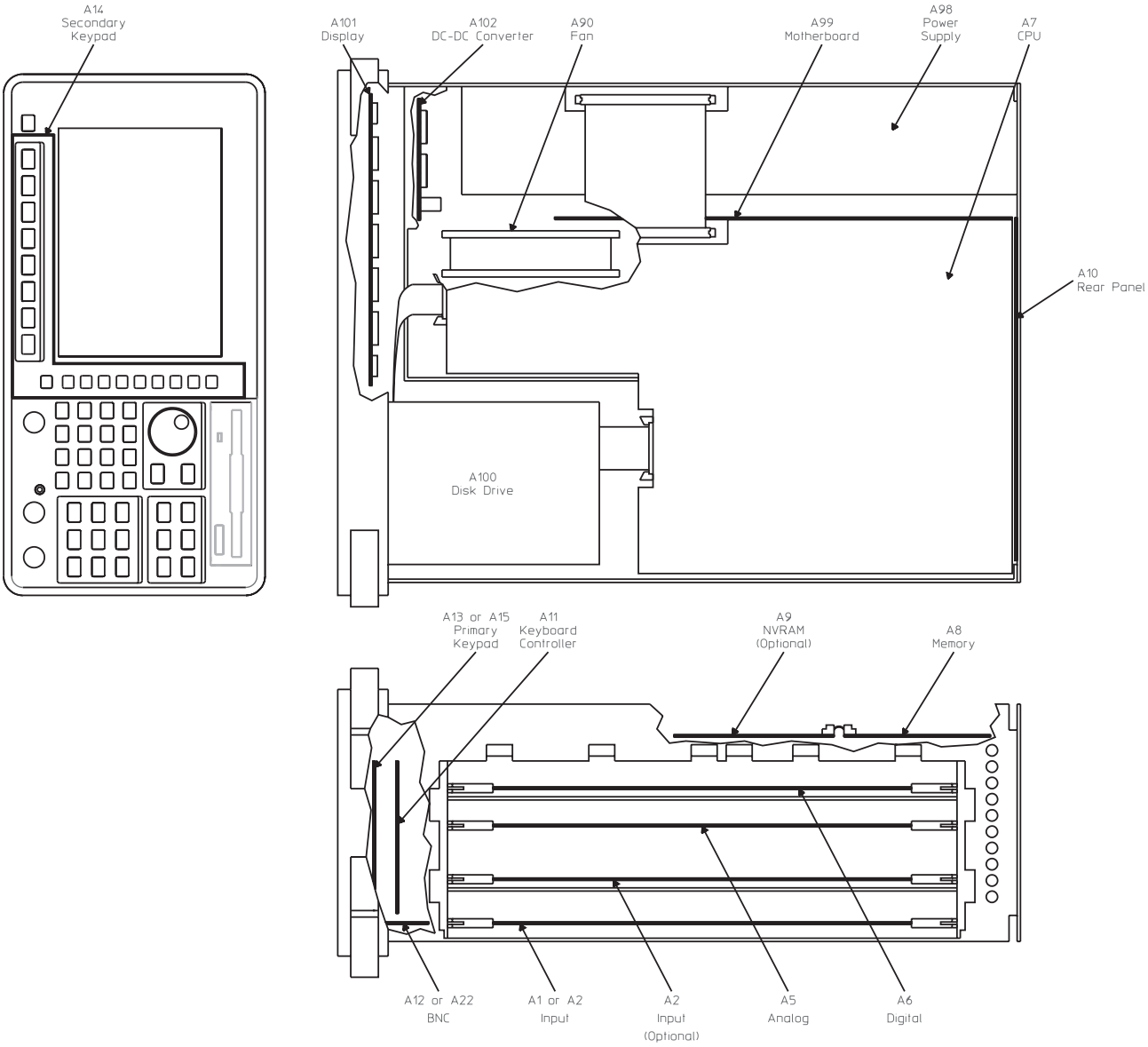
Quick Reference

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Quick Reference

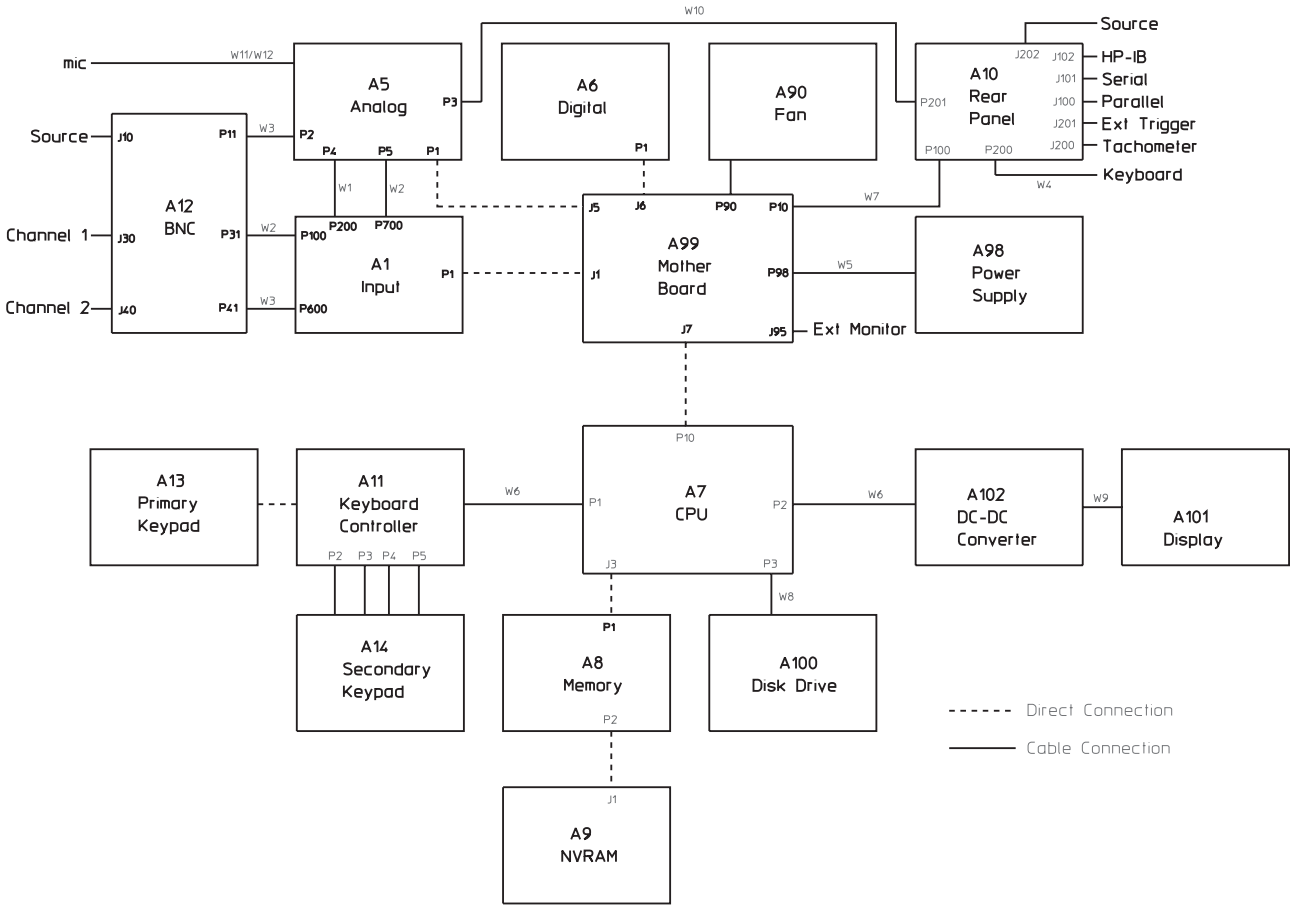
This chapter shows assembly locations, cable connections, and all the block diagrams for the Agilent 35670A Dynamic Signal Analyzer. All block diagrams, except the overall block diagrams, show the connector numbers for signals routed through RF cables. The block diagrams do not show connector numbers for signals routed through the analyzer's Motherboard assembly.

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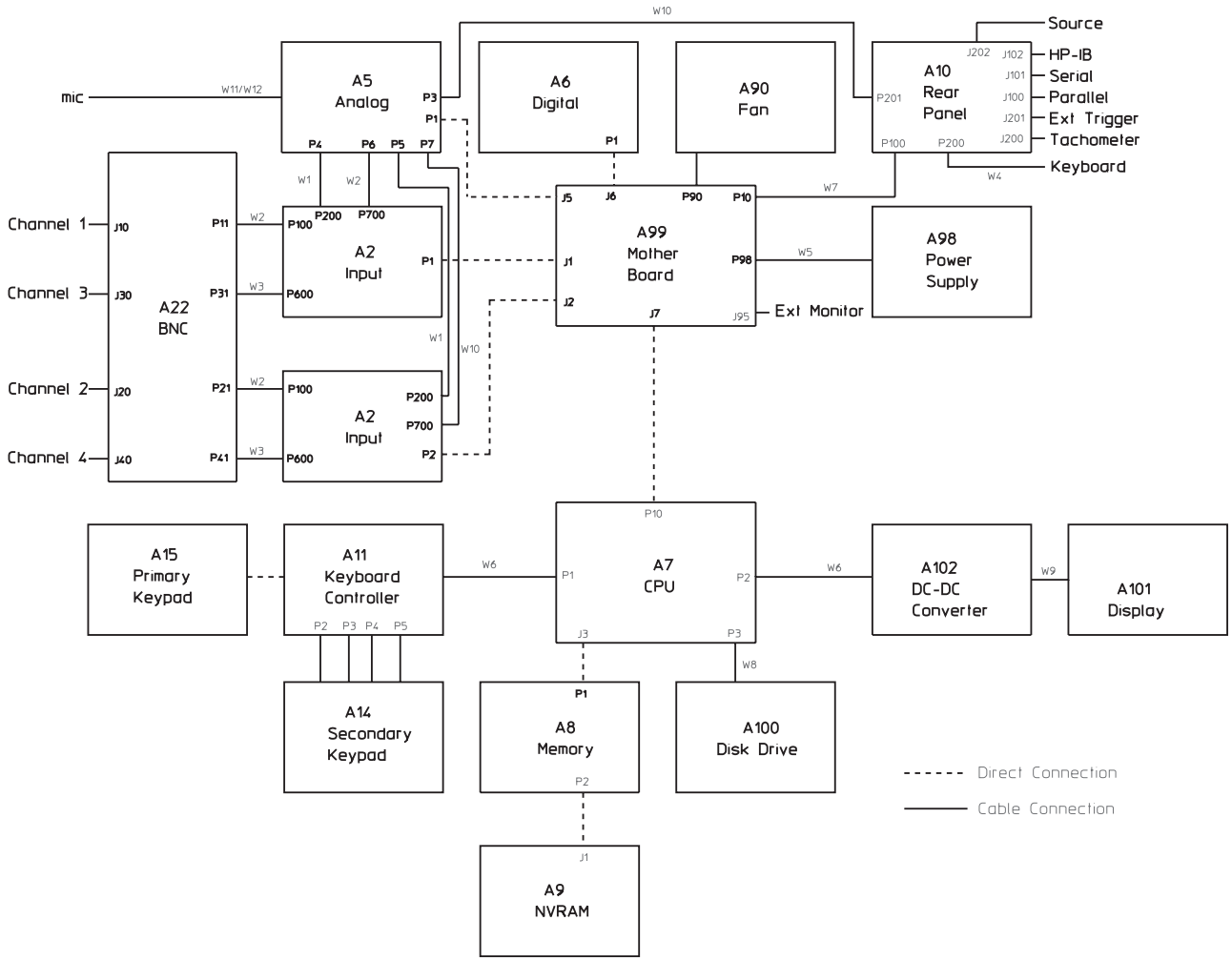
Assembly Locations

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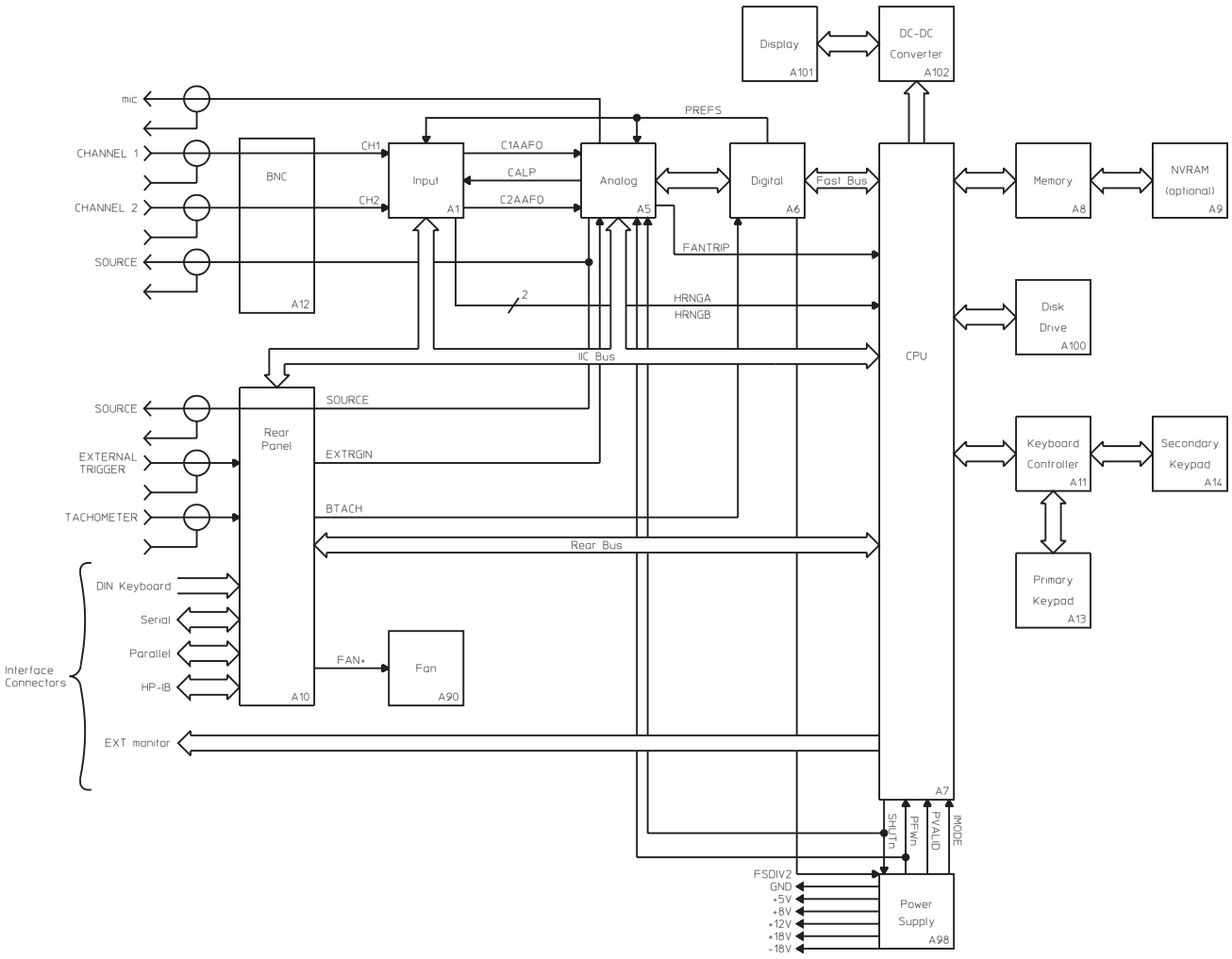
Assembly Connections for Two Channel Analyzer

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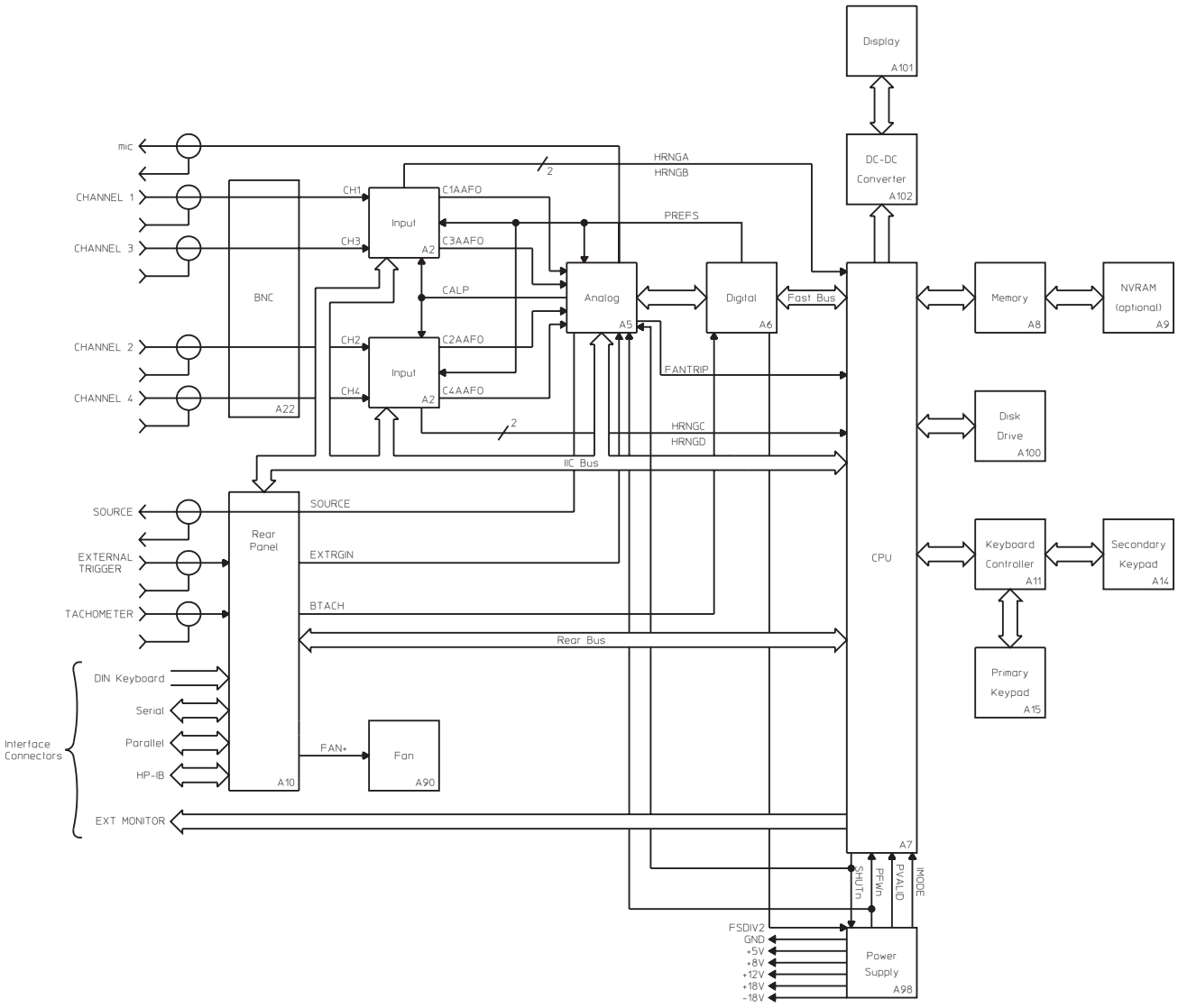
Assembly Connections for Four Channel Analyzer

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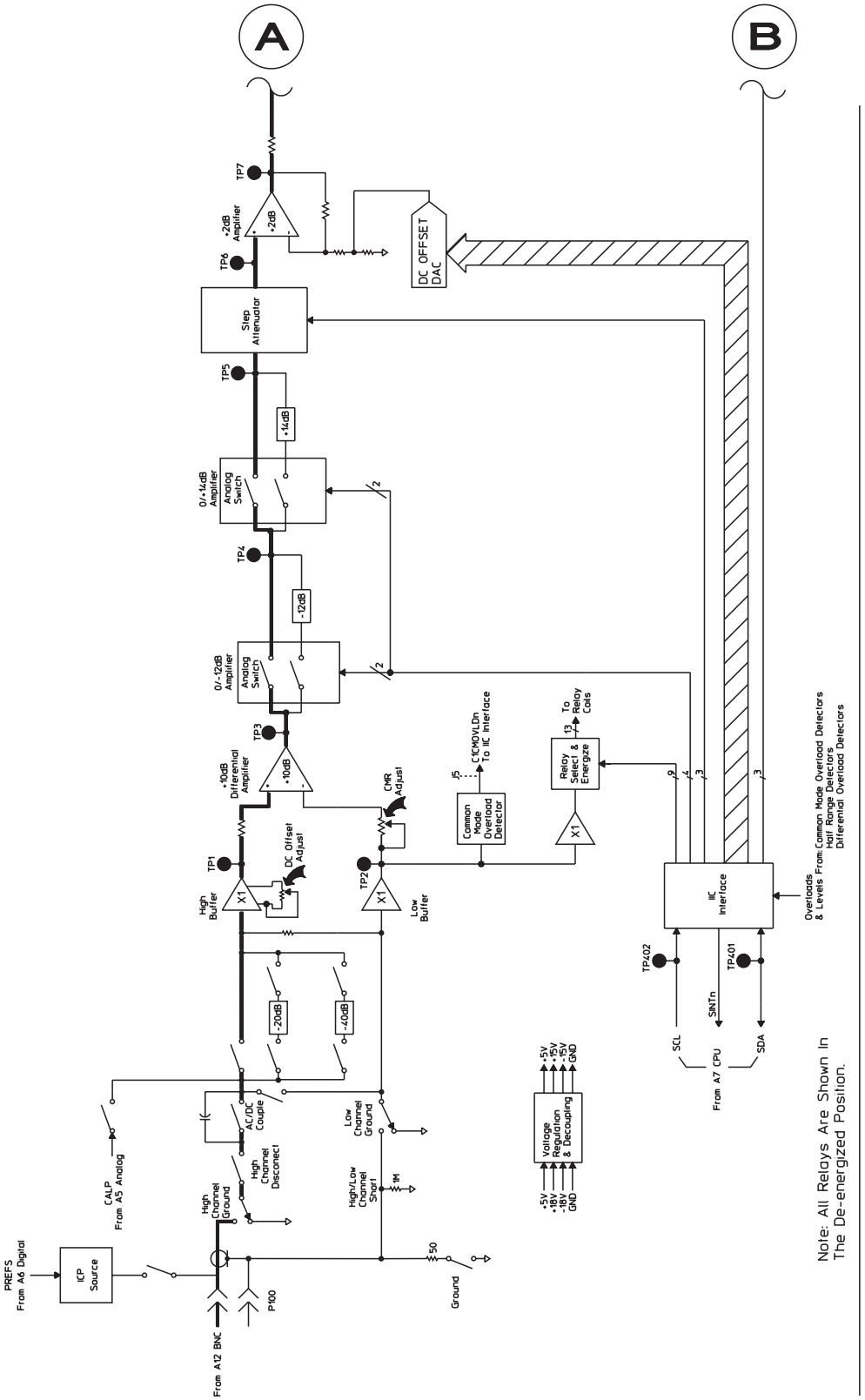
Two Channel Overall Block Diagram

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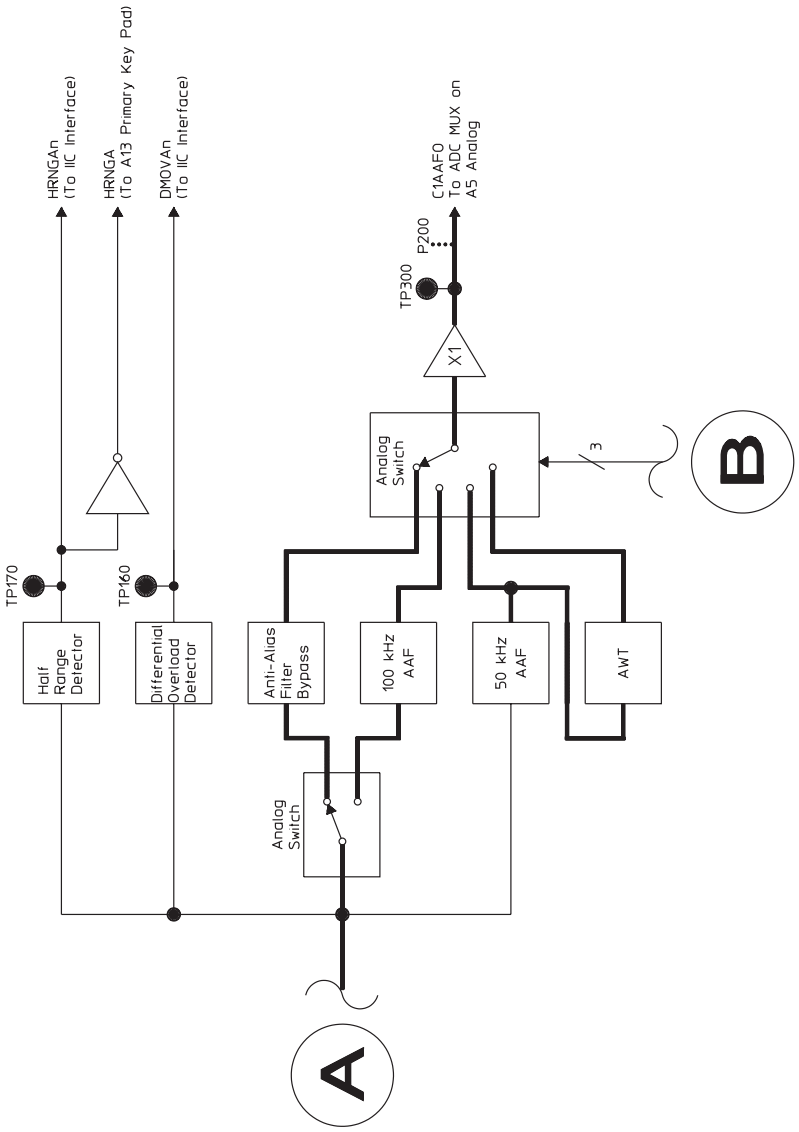
Four Channel Overall Block Diagram

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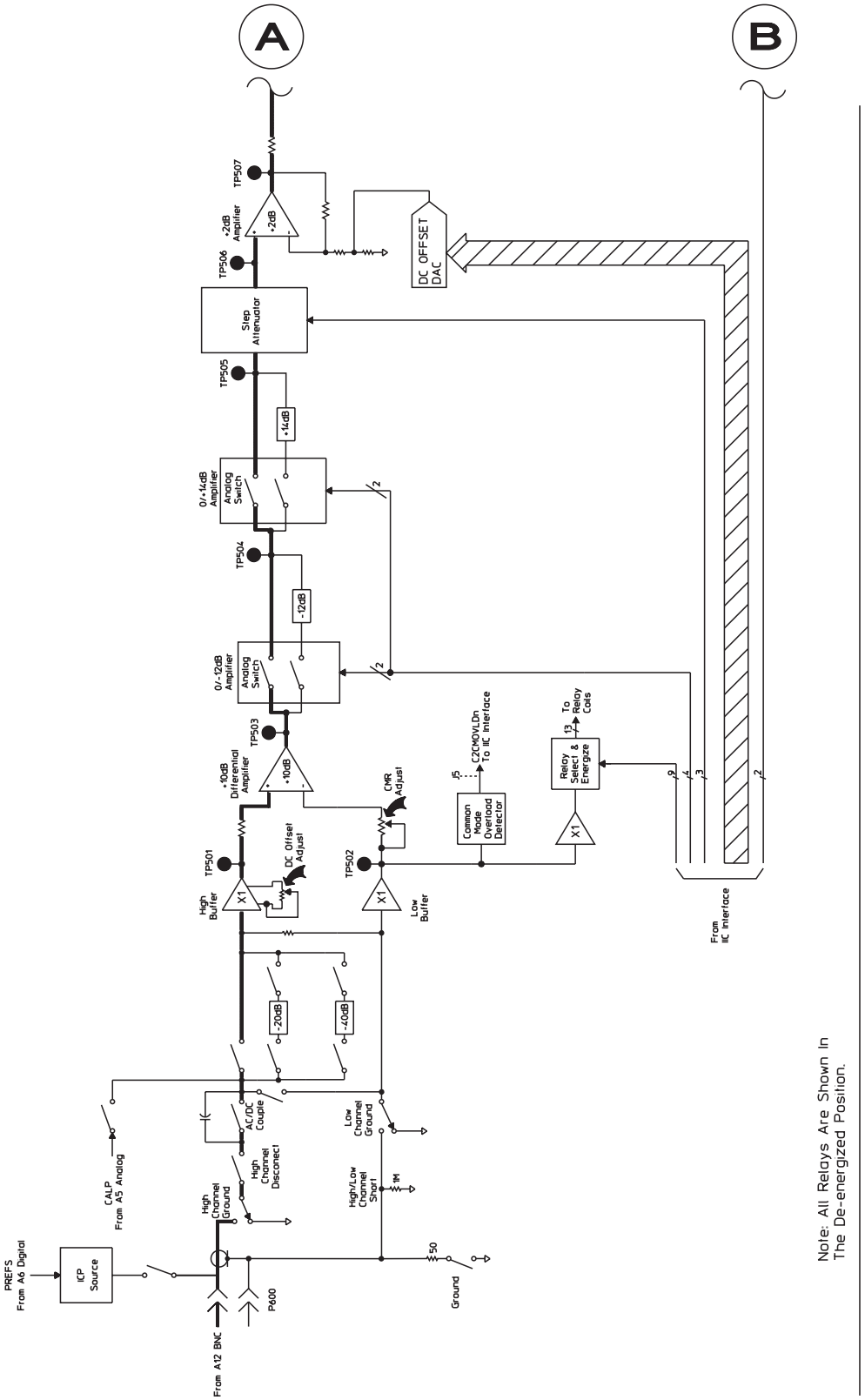
A1 Input Block Diagram: Channel 1

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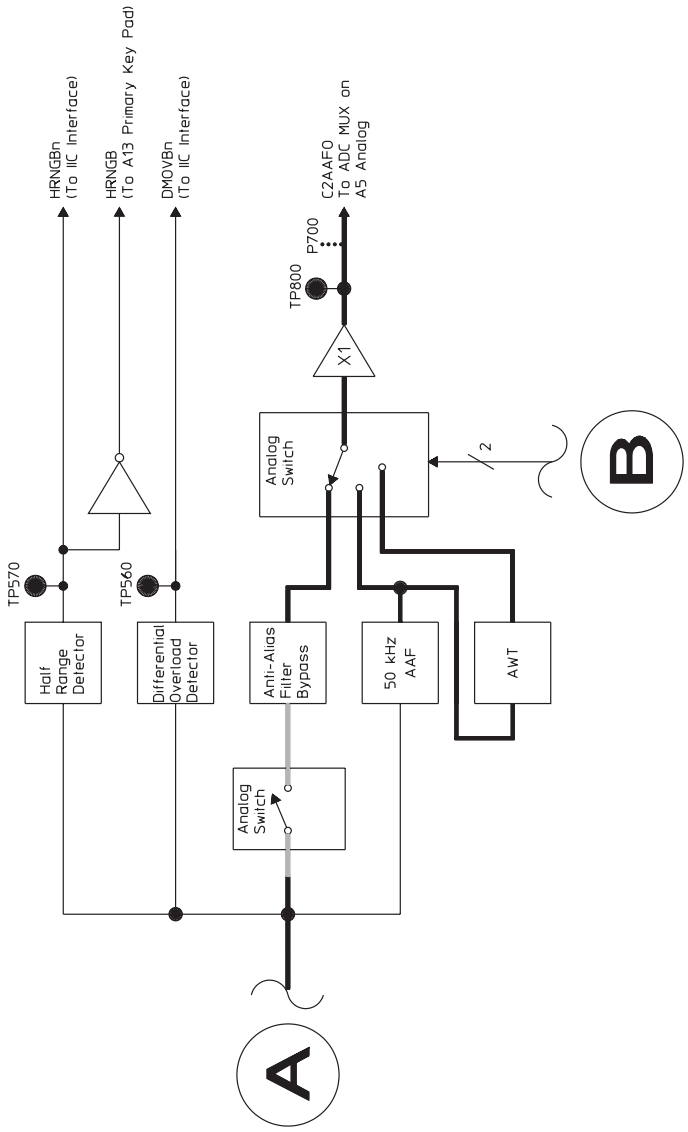
A1 Input Block Diagram: Channel 1 (continued)

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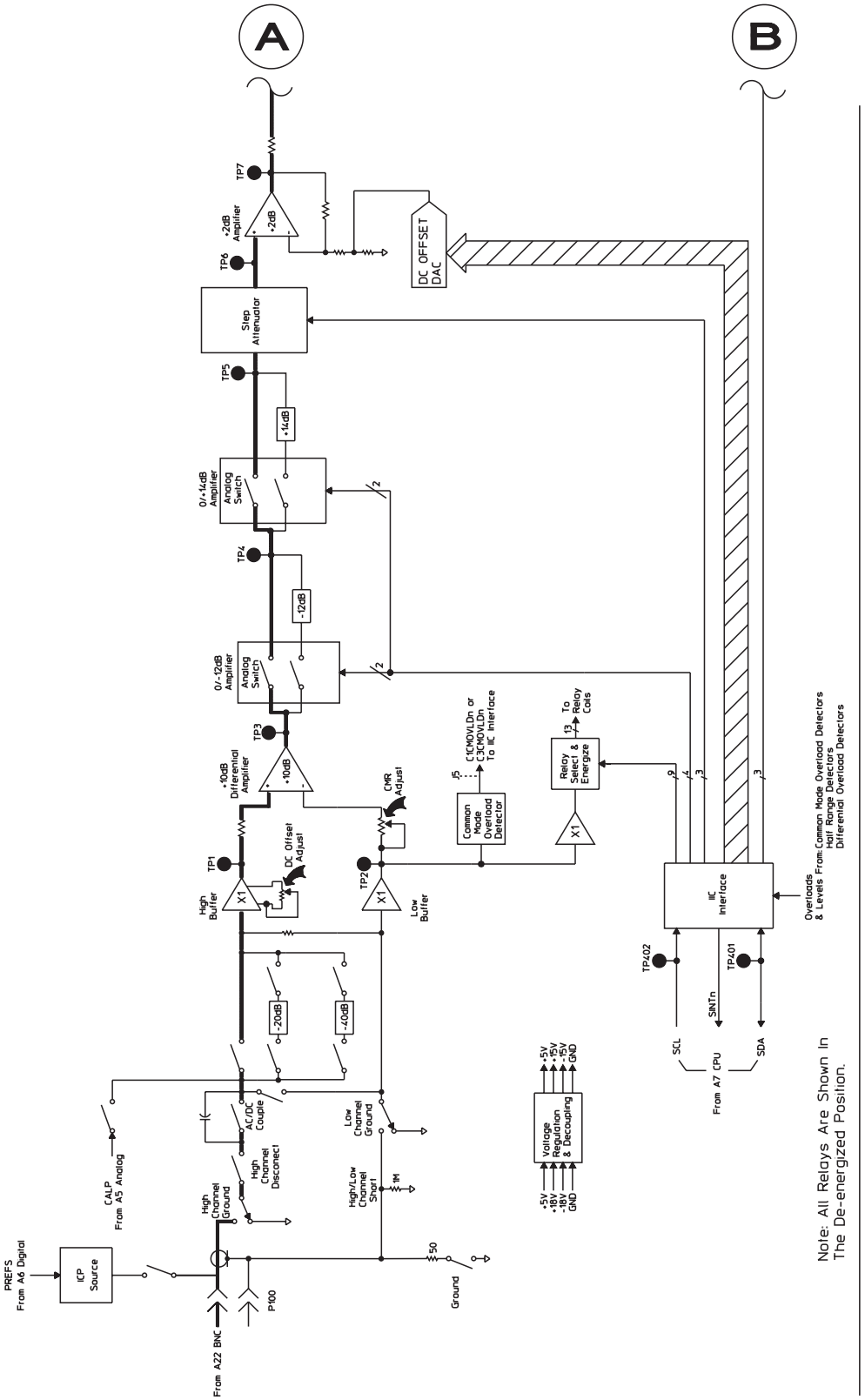
A1 Input Block Diagram: Channel 2

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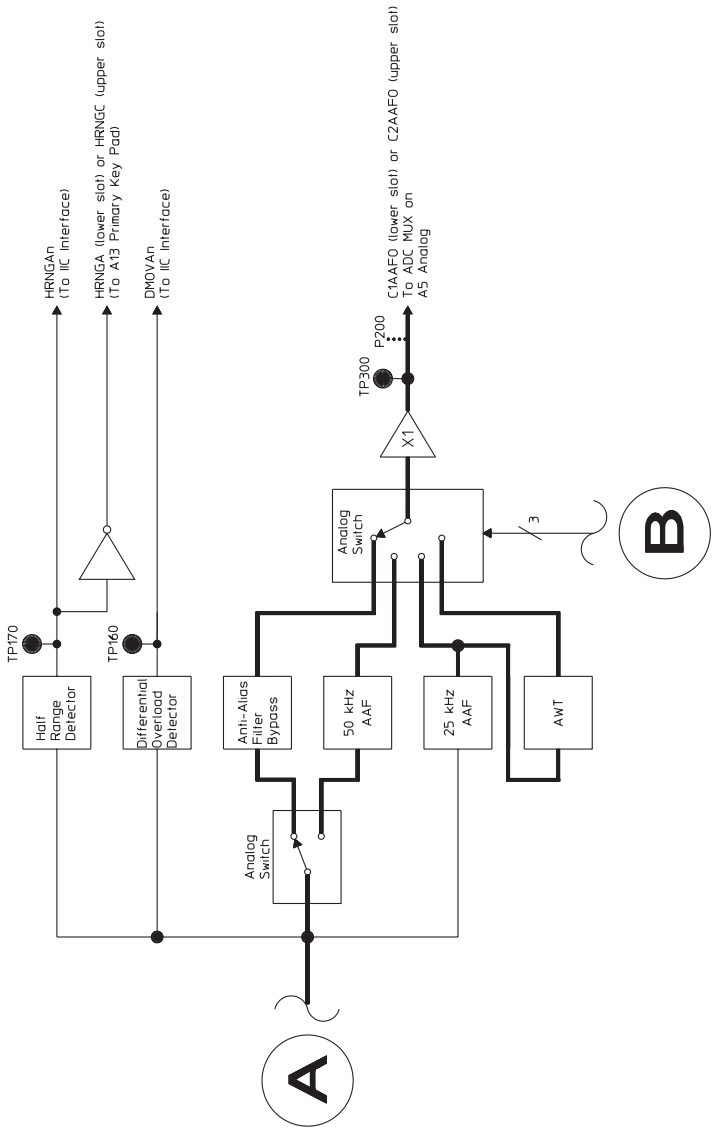
A1 Input Block Diagram: Channel 2 (continued)

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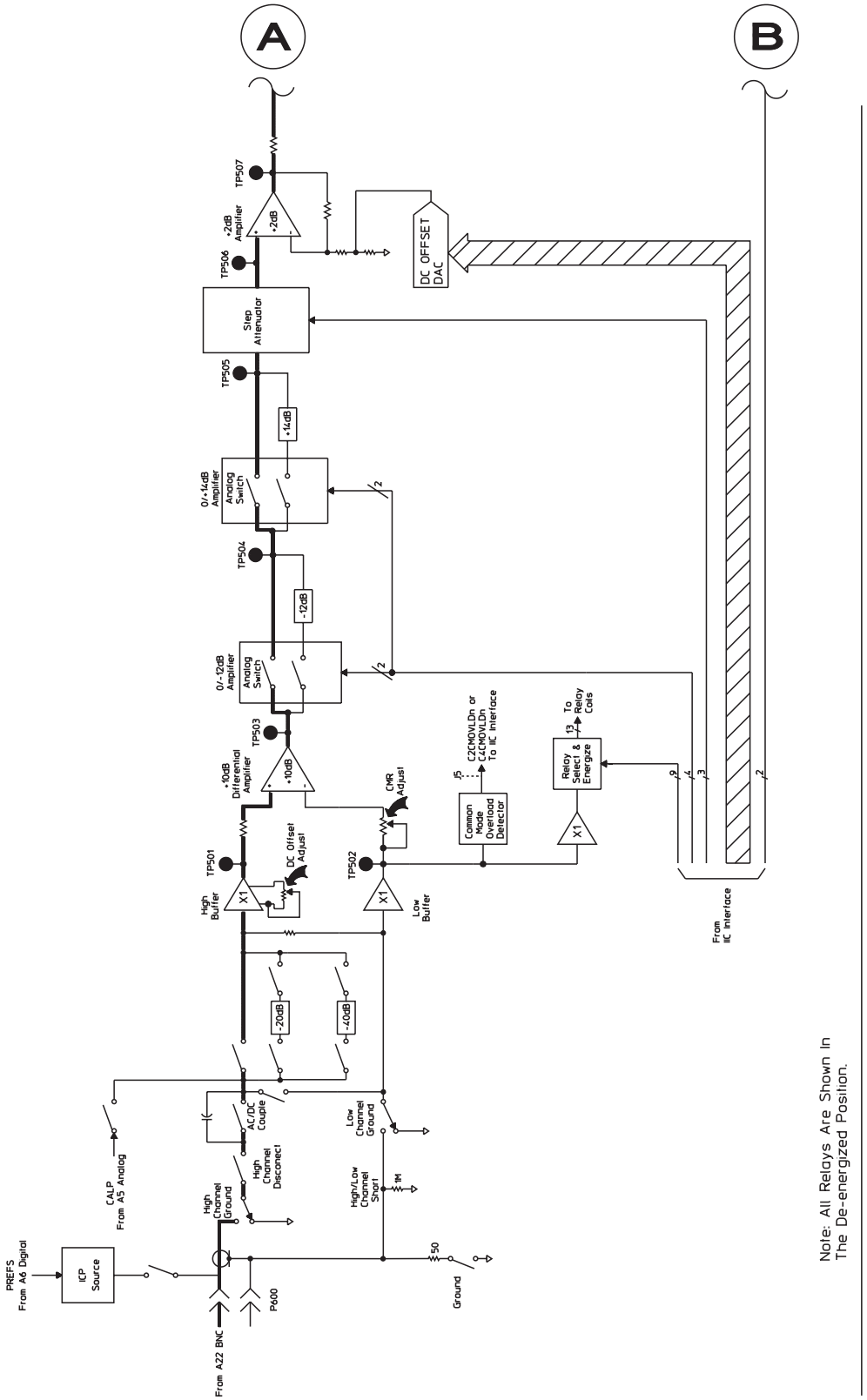
A2 Input Block Diagram: Channel 1 or Channel 3

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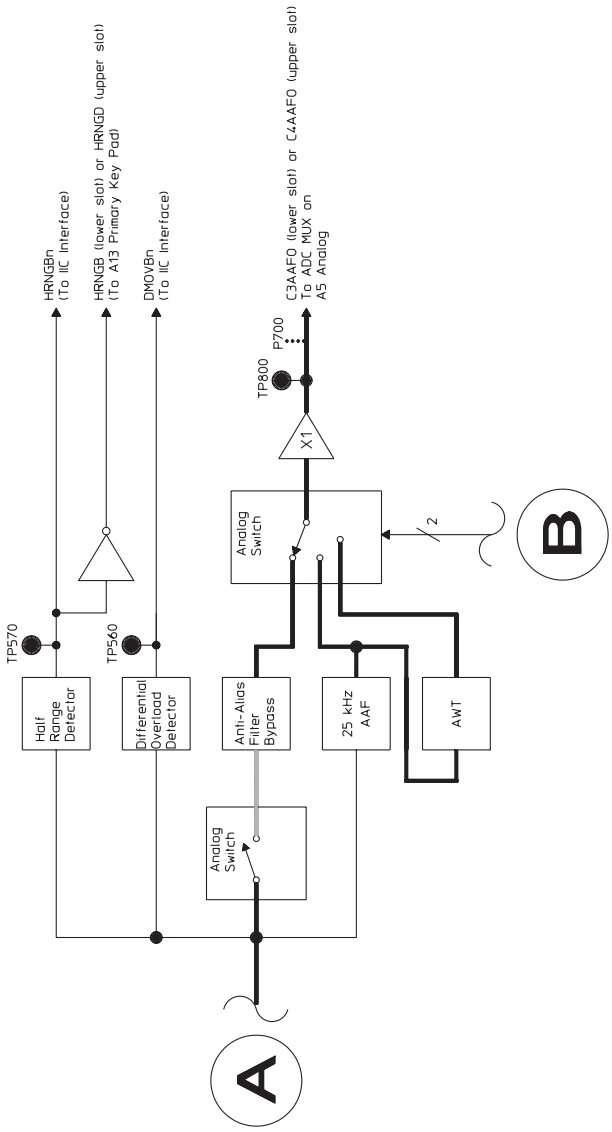
A2 Input Block Diagram: Channel 1 or Channel 3 (continued)

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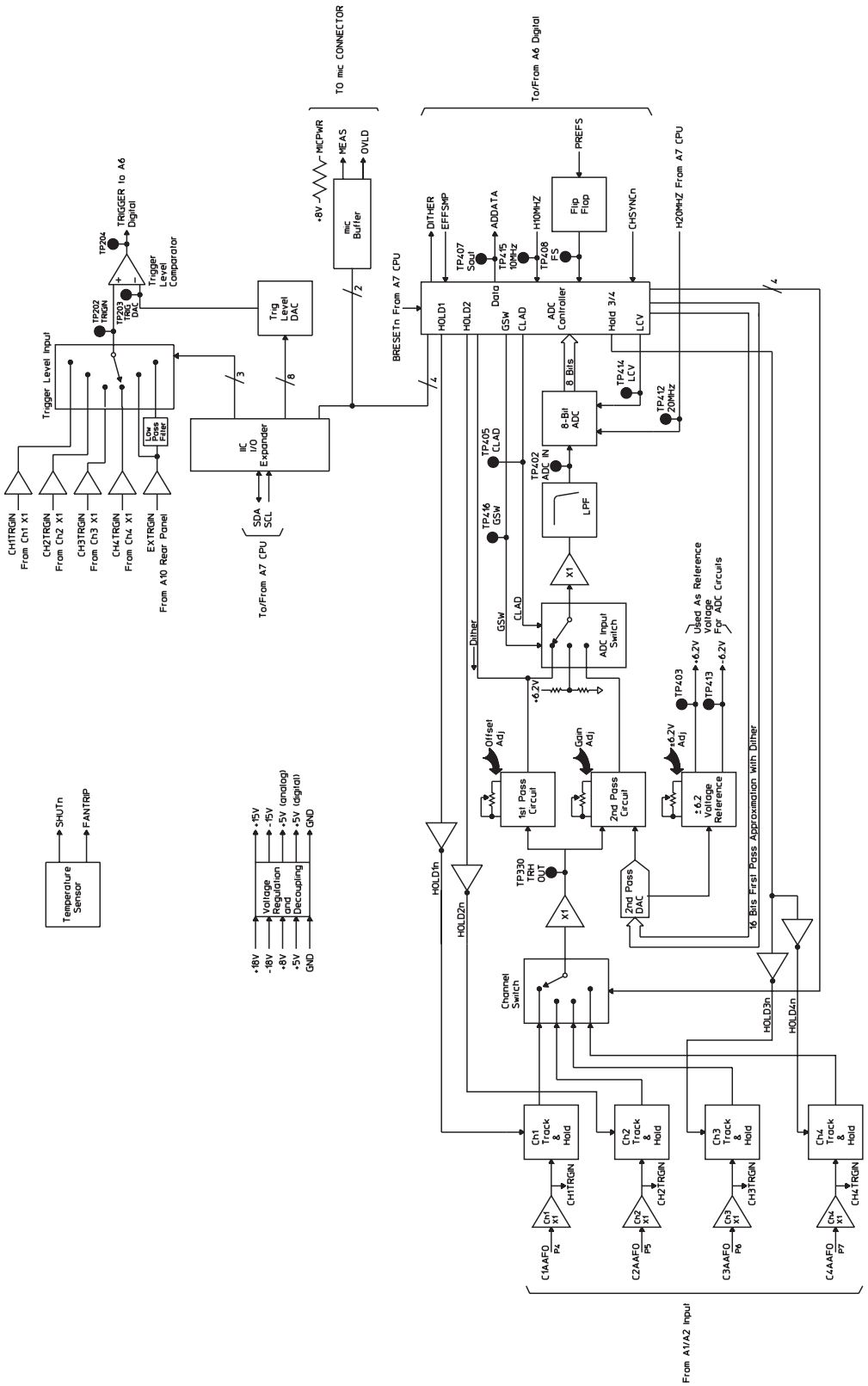
A2 Input Block Diagram: Channel 2 or Channel 4

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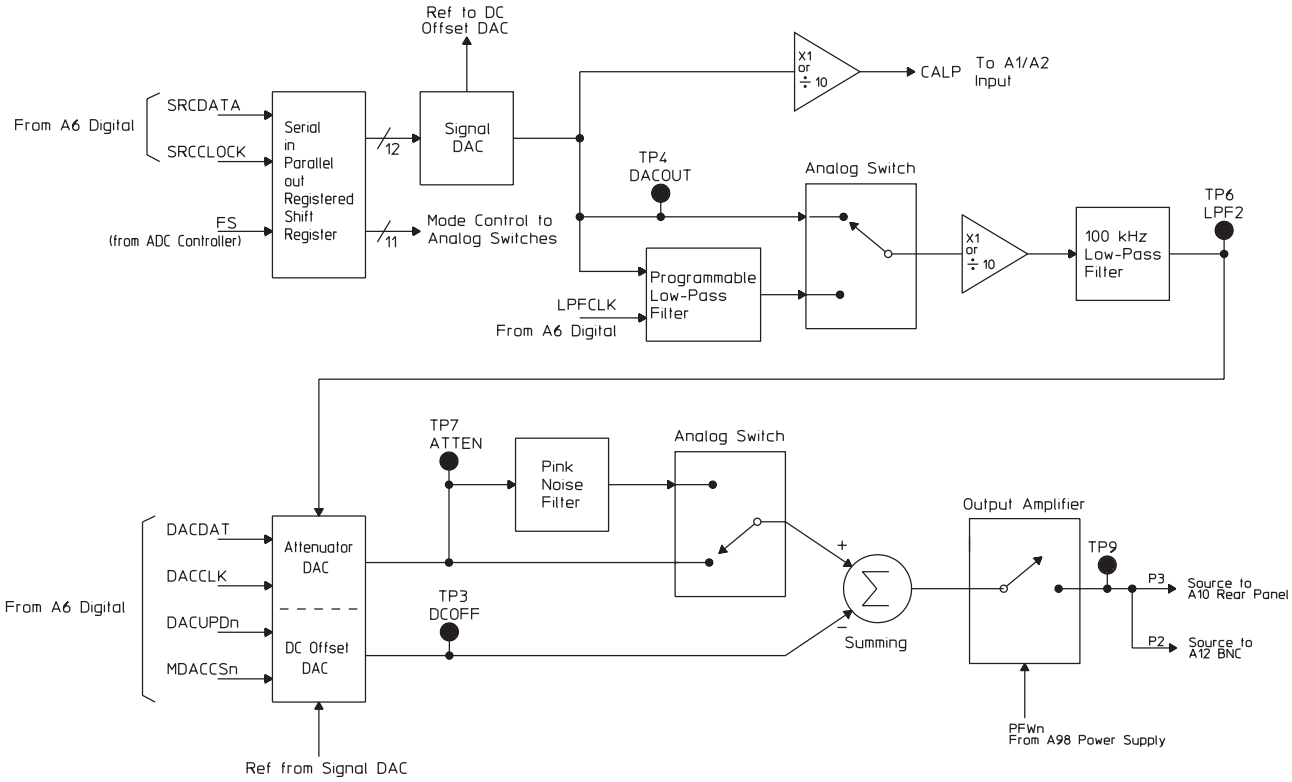
A2 Input Block Diagram: Channel 2 or Channel 4 (continued)

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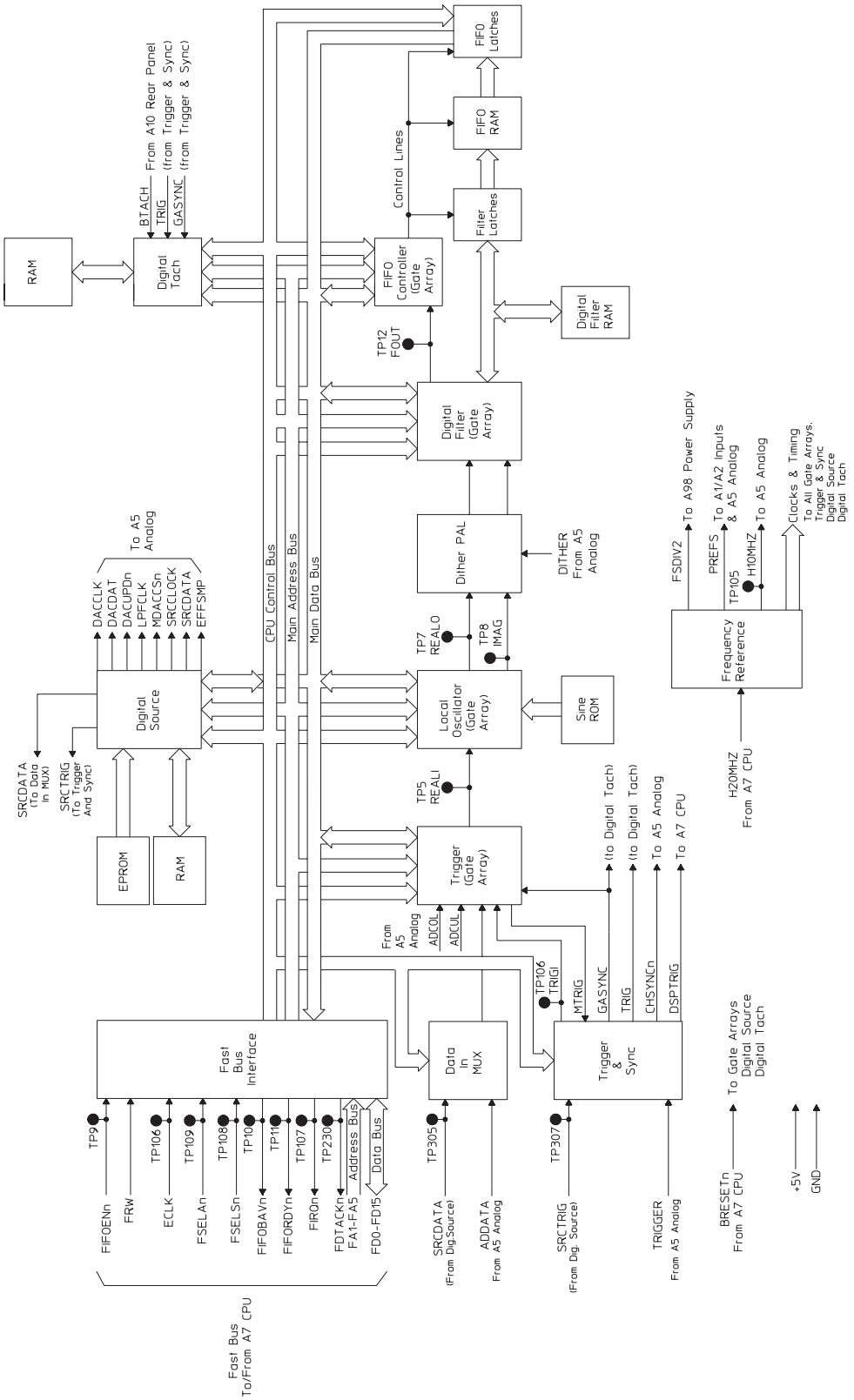
A5 Analog Block Diagram: ADC and Trigger

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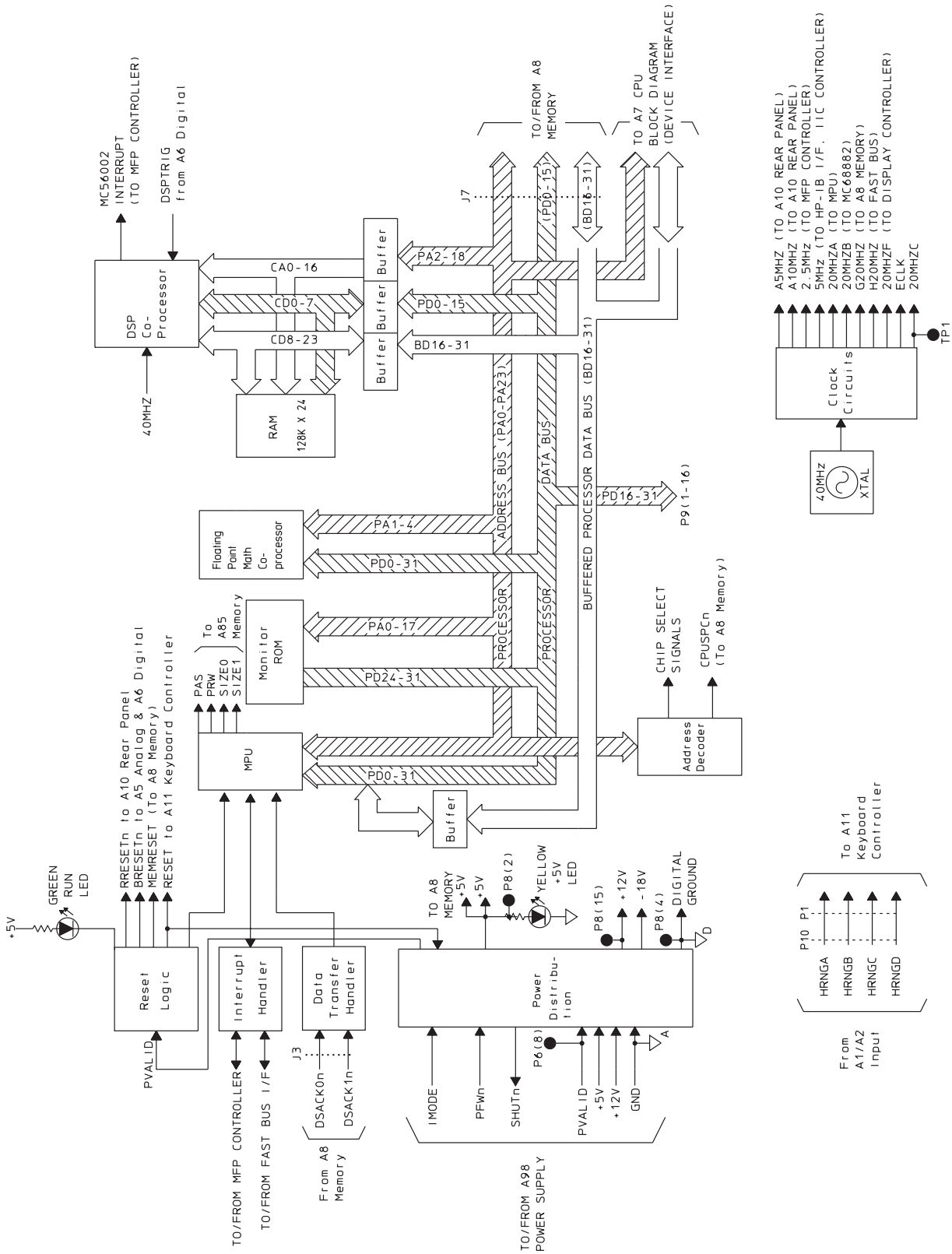
A5 Analog Block Diagram: Analog Source and Calibrator

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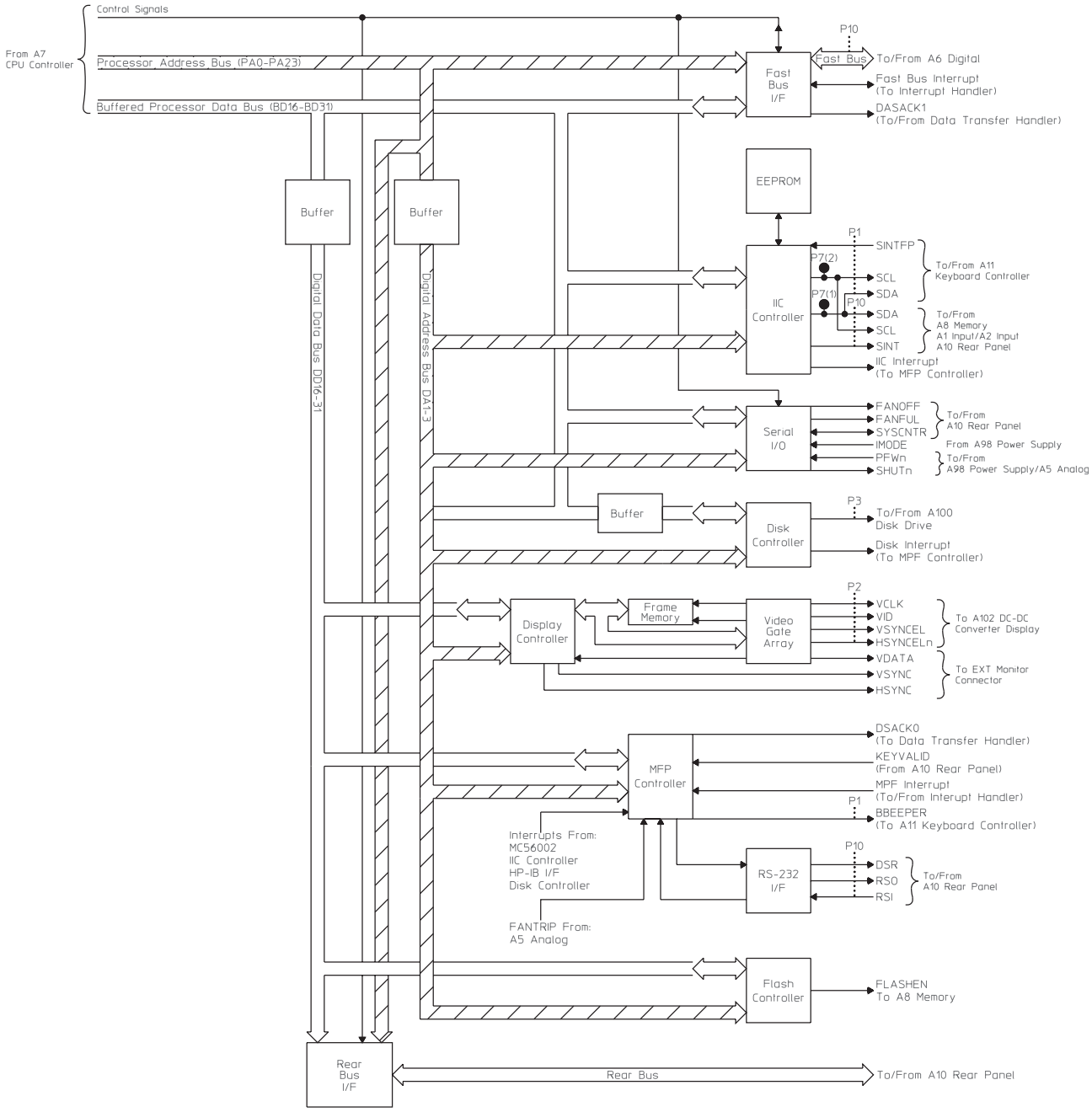
A6 Digital Block Diagram

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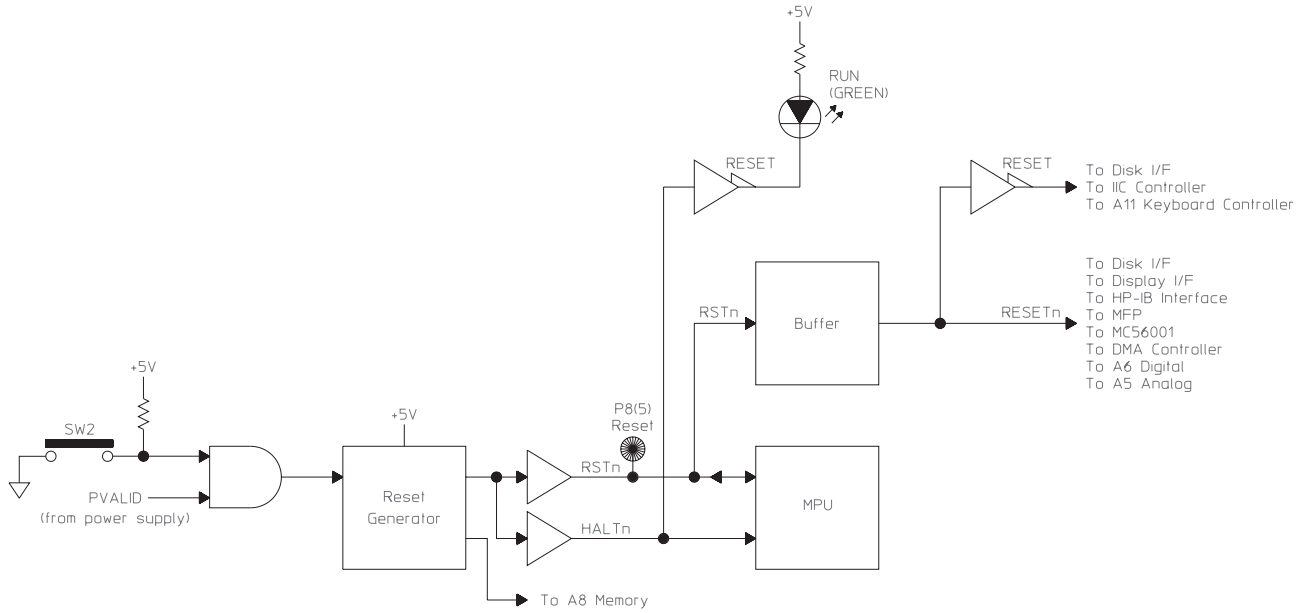
A7 CPU Block Diagram

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A7 CPU Block Diagram: Interface

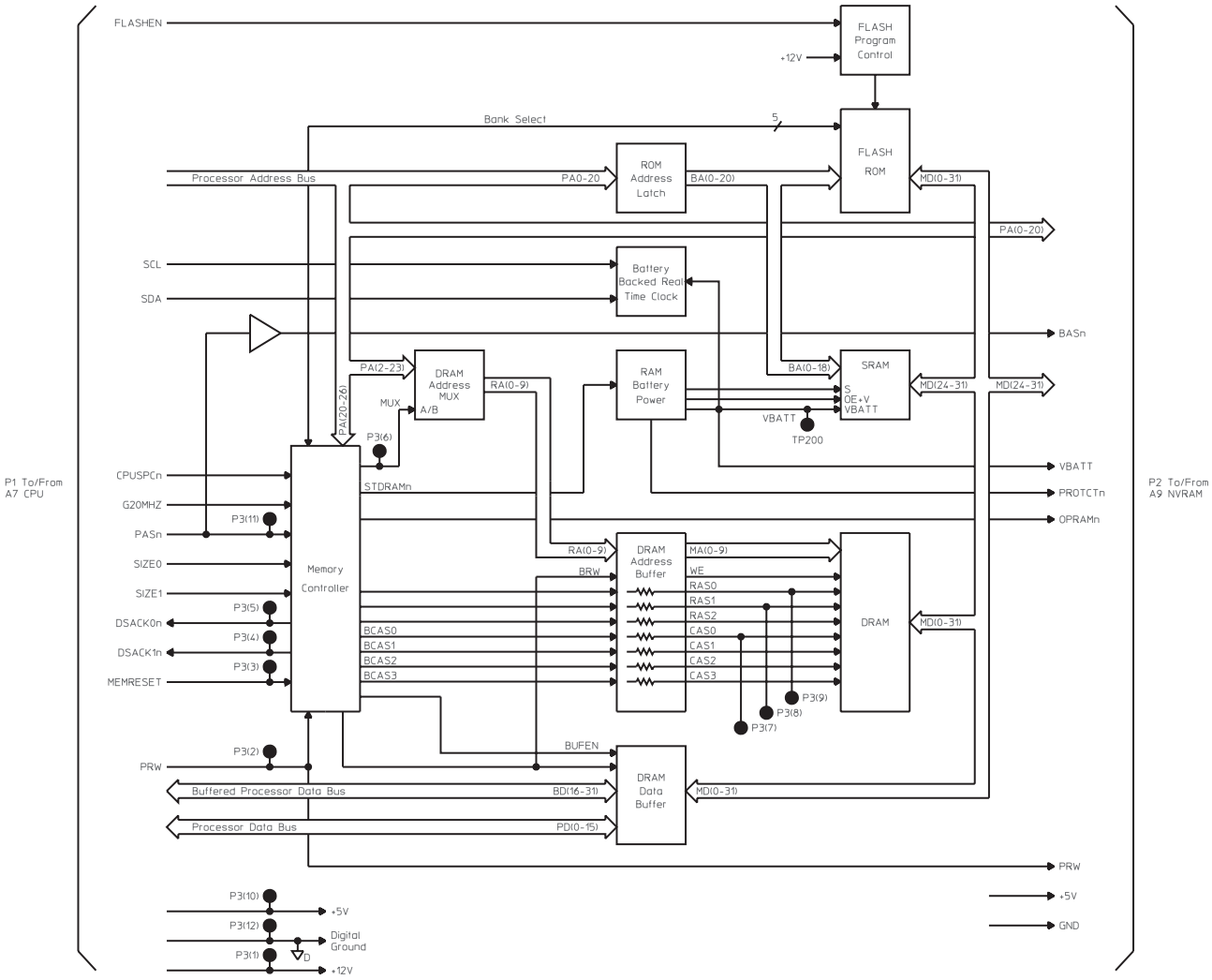
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Reset Logic

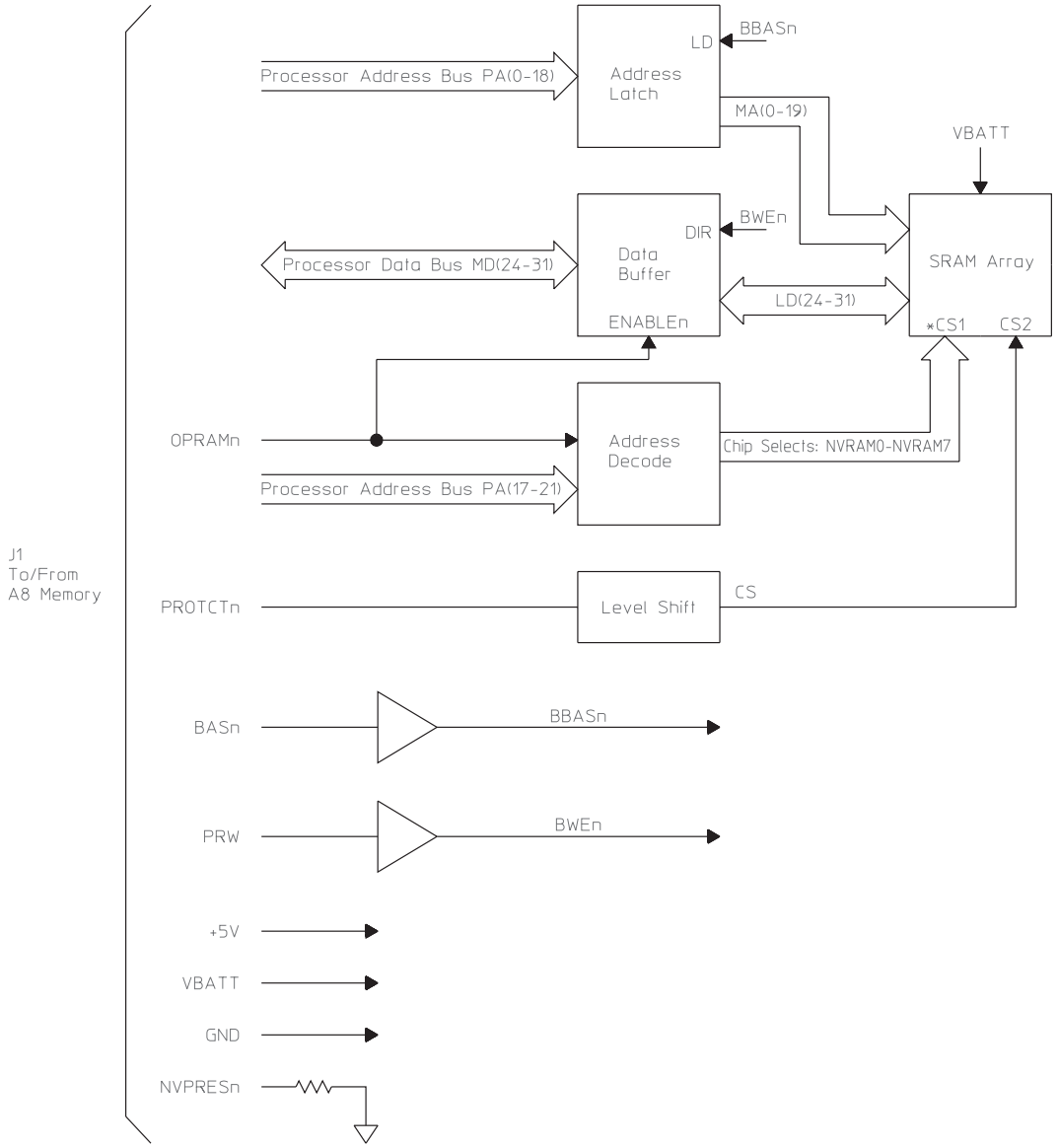
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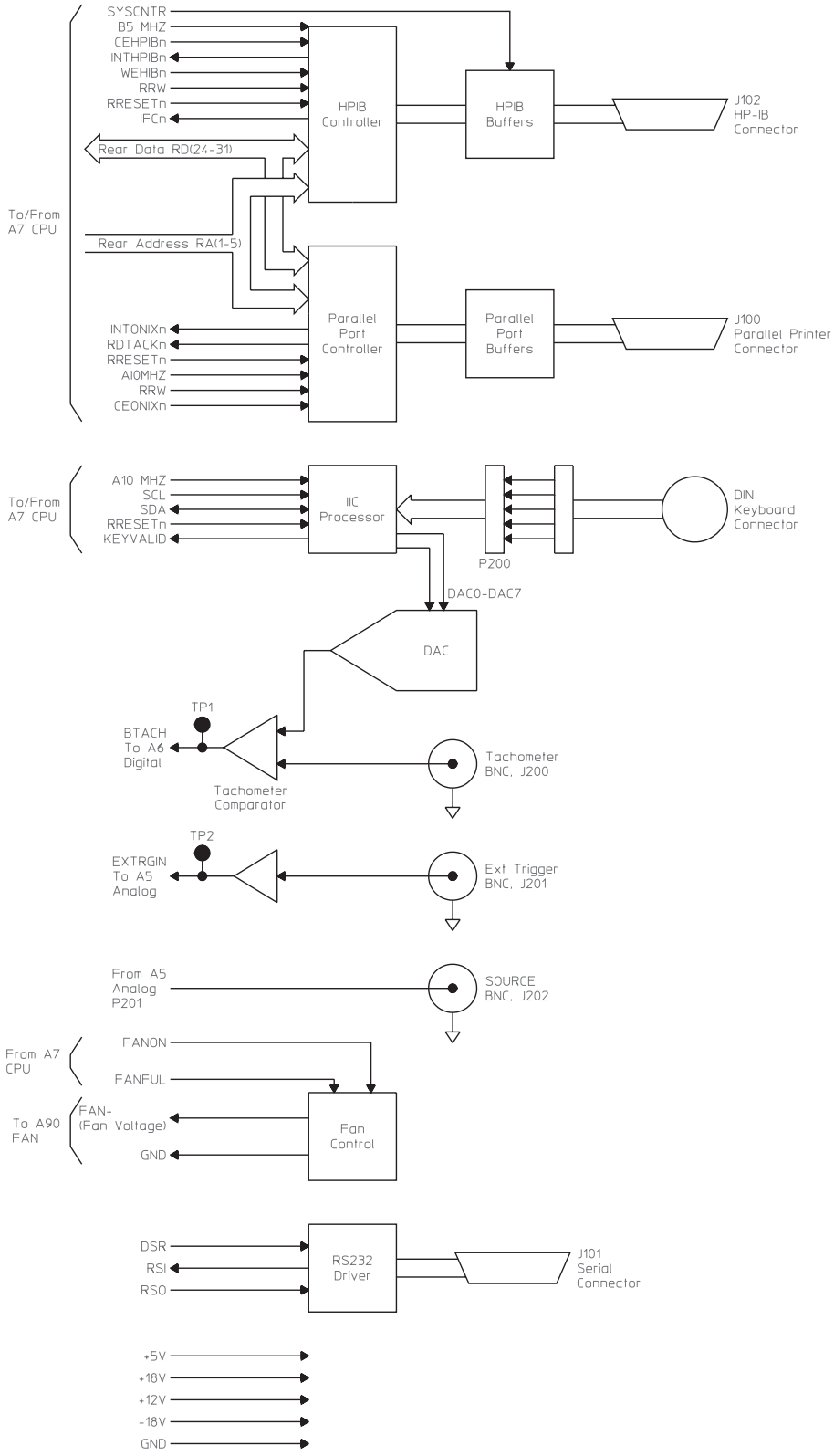
A8 Memory Block Diagram

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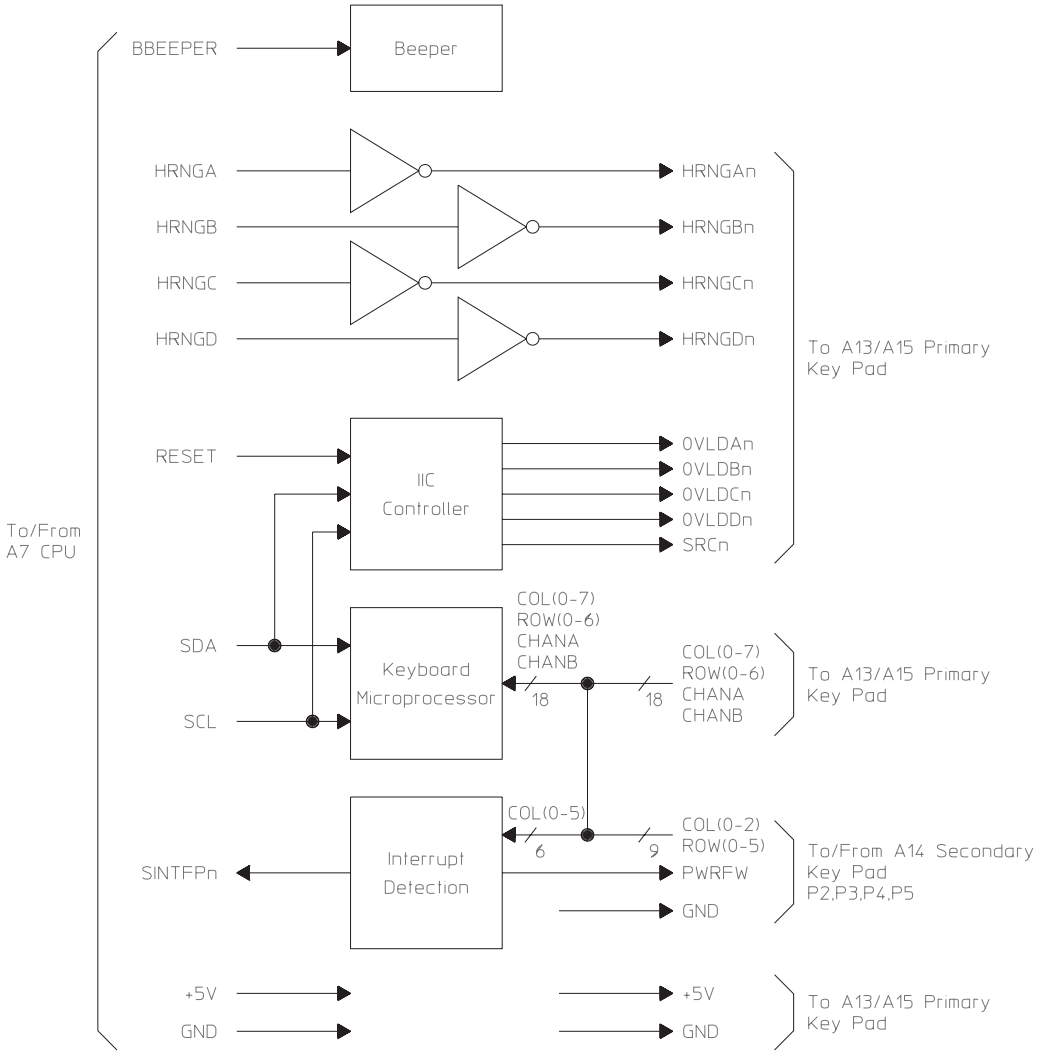
A9 NVRAM Block Diagram

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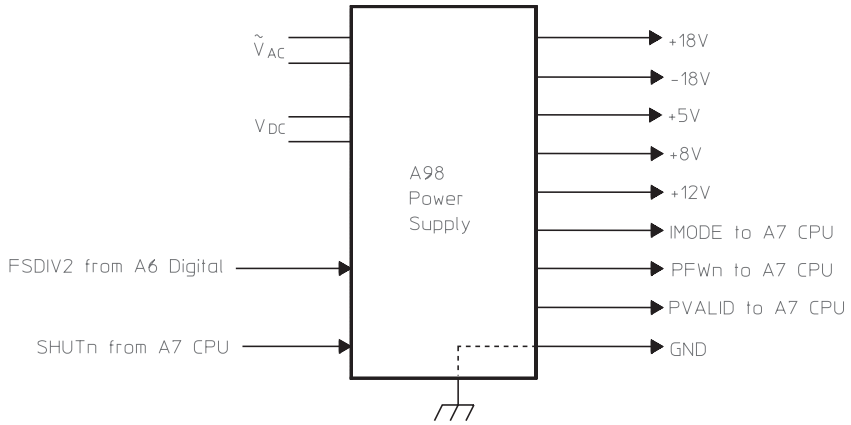
A10 Rear Panel Block Diagram

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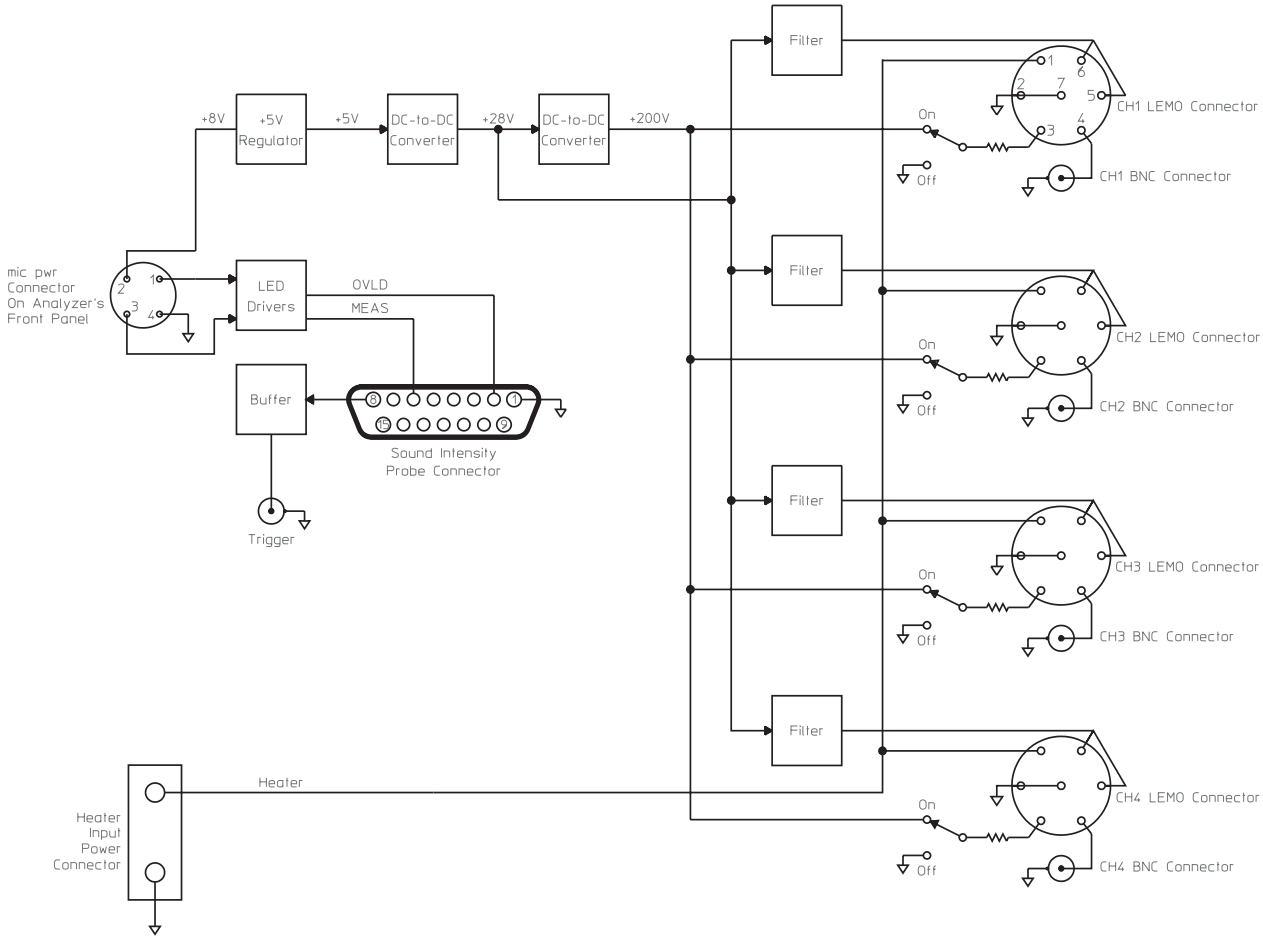


A11 Keyboard Controller Block Diagram

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A98 Power Supply Block Diagram



Option UK4 Microphone Adapter and Power Supply Block Diagram

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♦ Getting started	Make your first measurements with your new analyzer	*Agilent 35670A Quick Start Guide*
	Review measurement basics	*Agilent 35670A Operator's Guide*
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♦ Making measurements	Learn how to make typical measurements with the Agilent 35670A	*Agilent 35670A Operator's Guide*
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♦ Creating automated measurements	Learn the Instrument Basic interface	*Using Instrument Basic with the Agilent 35670A*
	Record keystrokes for a particular measurement	*Agilent 35670A Quick Start Guide*
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♦ Remote operation	Learn about the GPIB	*GPIB Programmer's Guide*
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	Find specific GPIB commands	*Agilent 35670A GPIB Commands: Quick Reference*
♦ Using analyzer data with a PC application	Display or plot analyzer data on or from a Personal Computer	*Standard Data Format Utilities: User's Guide*
	Transfer analyzer data to a PC sofware application forma	
	Transfer data from a PC software application format tothe analyzer (for example, to load data into a data register)	
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