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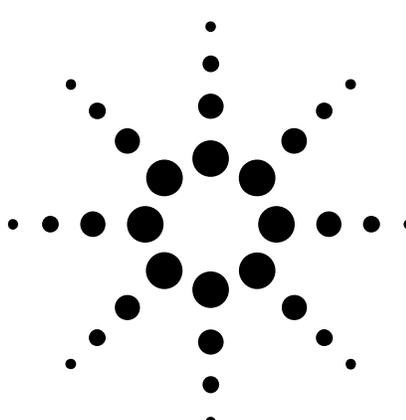
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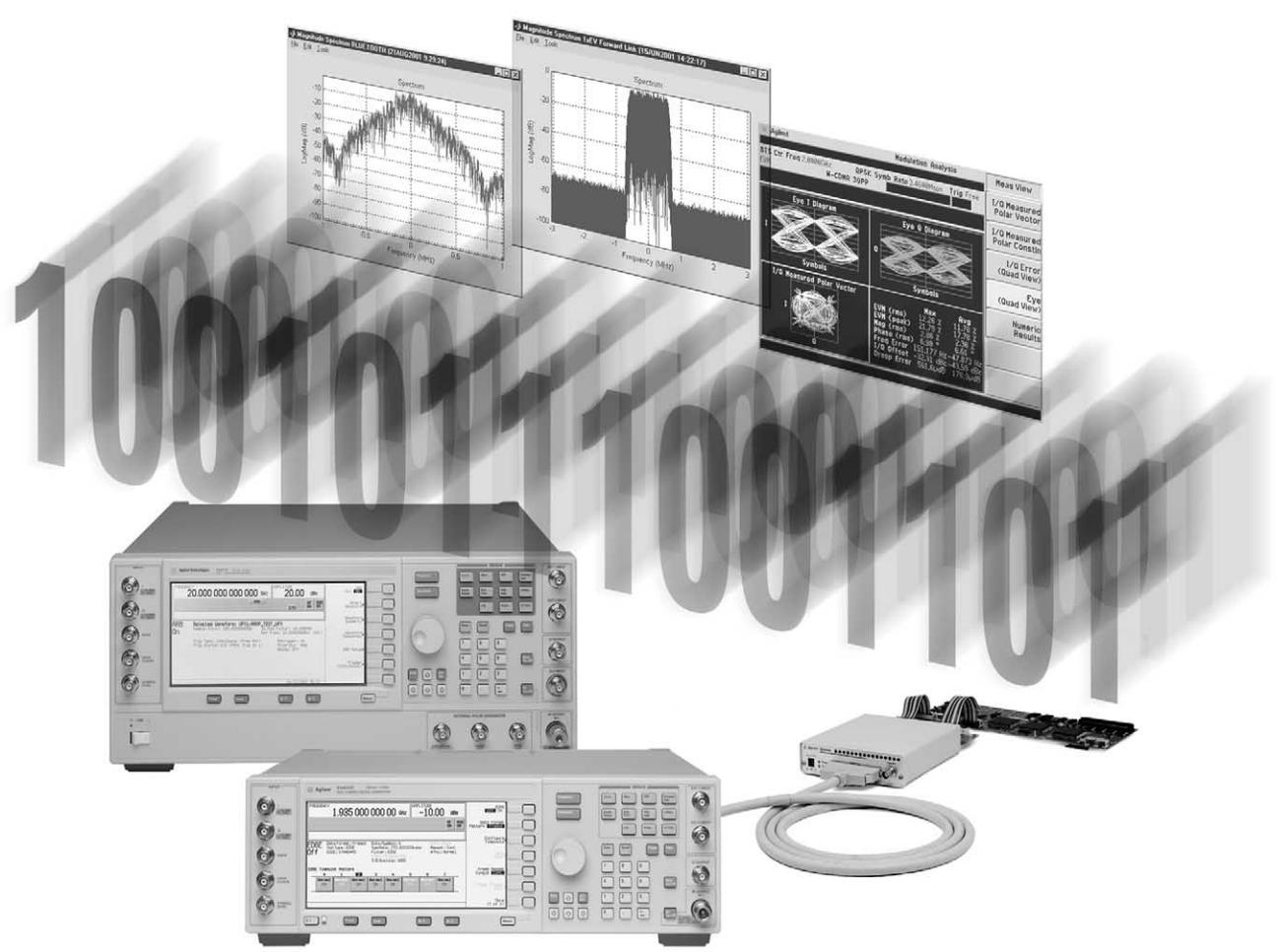
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Agilent Baseband Studio N5102A Digital Signal Interface Module

Technical Overview

The signals you need



...in the way you need them



Flexible Digital Test Stimulus



Figure 1. The interface module with the ESG and a single breakout board ready to be connected to a device under test.

The N5102A Baseband Studio digital signal interface module provides fast and flexible digital inputs or outputs for your E4438C ESG or E8267C PSG vector signal generator. In output mode, you can deliver realistic complex-modulated signals such as W-CDMA, 1xEV-DV, custom pulses, WLAN, TDMA and many others directly to your digital transceivers, components and subsystems. In the input mode, the interface module matches your digital input to the signal generator's baseband system, providing a flexible and calibrated way of upconverting to analog IF, RF or uW frequencies. The interface module adapts to your device with a wide variety of data formats, clock features, and signaling. With its selection of logic types and connector types, the interface module connects easily into your test system, in most cases eliminating the need for custom fixtures.

The digital signal interface module is just one of several Baseband Studio products. Agilent's Baseband Studio is a suite of baseband signal applications and accessories for the ESG and PSG vector signal generators that enhance Agilent's signal creation and signal generation tool set. For more details, see Additional Resources on page 8.

Key features

- ✓ Provides either digital inputs or digital outputs
- ✓ Flexible data formats
 - Variable 4 to 16 bit words on dual 16 bit buses
 - Serial, parallel, and parallel interleaved (DDR)
 - 2's complement and binary offset numbering
 - Selectable MSB or LSB
 - Digital IQ or digital IF¹
- ✓ Flexible clocking
 - Up to 400 MHz in serial mode, 100 MHz in parallel mode
 - Provision for internal, external, or device clocking
 - Independent data input and output rates
 - Adjustable clock phase and skew
 - Up to four clocks per sample²
- ✓ Flexible signal interface
 - Low voltage TTL, CMOS (1.5V, 1.8V, 2.5V, 3.3V) and LVDS
 - Single cable connects signal generator and interface module
 - Interchangeable break-out boards simplify device connection
- ✓ Simple user interface

Overcome Digital Design Challenges

Today's shortened design cycles leave little tolerance for empirical test and redesign. At the same time, every new project brings its own demands for different types of baseband devices with different operating parameters. Sharing common test signals between baseband and RF designers reduces the possibility of errors, and having a configurable device interface reduces the time spent developing custom fixtures.

Until now, you could only overcome one of these challenges at a time. Pattern generators provide flexible physical interfaces, but require you to create your own complex test signals. Signal generators and baseband products provide flexible, dependable IP, but require you to design your own physical interface.

With the Baseband Studio digital signal interface module, engineers in the RF and digital baseband design groups can share the same real-world signals to test transceiver performance or verify control algorithms. This allows test of early-stage digital components and subsystems, saving the time and expense of waiting for the design cycles to merge.

¹ IF is available only in output mode.

² Multiple clocks/sample only available in parallel and parallel interleaved output mode.

Bit Level Access to Agilent's Baseband Signals

In the output mode you get bit-level access to the entire set of complex test signals available in the high performance E4438C ESG and E8267C PSG vector signal generators. The ESG and PSG generate signals that simulate wireless communications, radar, or other real-world transmissions, and the interface module delivers the test signals to the device-under-test (DUT) as digital I/Q or digital IF data.

In the input mode, the module enables direct digital IQ input from your device into the ESG or PSG for upconversion to the desired RF or microwave frequencies. Your transmitter design can be realized by using the vector signal generator's fully calibrated RF path to substitute for your own RF section. This allows you to test your digital baseband subsystem without waiting for the RF section to be completed.

Why use Agilent's baseband generator?

The key benefit of testing with the same complex signal at RF and at baseband is reducing design iterations. Creating your own representations of real-world signals to do this requires a significant investment of time. Testing with a reliable industry-standard signal from Agilent reduces the probability that a component or a subsystem design will need to be revisited during interoperability testing at RF.

Agilent offers both real-time processing and arbitrary waveform capabilities in a single baseband generator. This technology gives you signals that are optimized for a wide array of applications in a single instrument.

Full signal coding

Most of Agilent's signal creation applications include full channel coding necessary for testing bit, block, packet, or frame error rates (BER/BLER/PER/FER). Fully-coded signals include interleaving, convolutional encoding and data modulation per physical layer standards for full decoding of the checksum, CRC, or data bits by receivers and ASICs.

Real-time advantages

Real-time signals are unconstrained by instrument memory limitations. The signals are not stored in memory; they are continually generated and transmitted. Whether you need one or one million frames, the signal is always continuous, with no repetition. This allows seamless data sequences for BER test, and the ability to pull data from a user file stored in the signal generator's memory.

Real-time signals update immediately when signal parameters are changed, without waiting for a waveform to be rebuilt. Applications include Signal Studio for 1xEV-DV, W-CDMA (in real-time mode), GSM/EDGE, and more.

Complex arbitrary waveforms

Agilent's arbitrary waveform (Arb) signal creation increases the complexity of the waveform that can be created. You can simulate wide bandwidth multicarrier signals containing hundreds of channels, add impairments,

and vary the parameters between carriers. Arb signals include W-CDMA (in Arb mode), *Bluetooth*[™], enhanced multitone and more.

Deep 64-MSa download memory

If you still need to create proprietary signals, you can do so with Agilent's Advanced Design System (ADS) software or other simulation tools, and download the waveforms into the ESG or PSG arbitrary waveform generator. ADS provides a convenient ESG/PSG link for easier downloads. MATLAB[®] downloads are facilitated using the free ESG/PSG Download Assistant (www.agilent.com/find/downloadassistant).

Pre-calculated waveforms are limited in size by the baseband generator's playback memory. With Option 602, the ESG and PSG offer one of the deepest playback memories in the industry, 64 megasamples (MSa).

Flexible Data Formats

Every new design seems to require data in a new form. To accommodate this shifting landscape, the interface module provides a direct digital connection to or from the ESG/PSG with a highly configurable interface.

Choose from a variety of word sizes

The interface module offers a choice of word sizes, anywhere from 4 to 16 bits.

Choose serial or parallel data

Support for both parallel and serial buses. In serial mode, a corresponding frame trigger is provided. In parallel mode, IQ and QI interleaving are supported, in which samples are transmitted on both positive and negative clock edges. This doubles the data rate on a single bus for support of double data rate (DDR) devices.

Choose your numeric format

Support for both 2's complement and offset binary numbering, for devices with either all positive or positive/negative numbering conventions.

Choose your bit order

Reorder the bits on the bus to transmit most or least significant bit first (MSB or LSB).

Choose IQ or IF

Support for both digital IQ and digital IF¹. In IF mode, the intermediate frequency is 1/4 of the clock rate.

Add or correct IQ impairments

The IQ data can be modified in amplitude and phase with features such as individual I and Q gain, phase rotation, negation and scaling. These features can help the device emulate real-world conditions.

¹ IF is available only in parallel and parallel interleaved output mode.

Flexible Clocking

Test equipment should conform to the needs of the DUT. The interface module's flexible clocking structure makes it easy to synchronize the module with the DUT.

Automatic data resampling

Whether the digital data is supplied from your device or delivered to your device, you never have to worry about rate matching. Simply set the clock rate of the interface module, and it takes care of the rest. Automatic resampling guarantees that data will be delivered at the rate you select.

Clock inputs

For easy synchronization with the test device, the module clock can be driven by a variety of sources.

- To use a clock from your test device, simply supply this clock as an input on the device interface bus that connects your device to the interface module, and connect its frequency reference to the ESG/PSG (Figure 2a).
- If you wish the interface module to supply a user-settable clock, simply specify the clock rate in the user interface, and connect the 10 MHz reference signal from the ESG/PSG to the Freq Ref port on the module's front panel (Figure 2b).
- If you want to supply an independent low jitter clock to both the device and the interface module, simply connect the clock to the Ext Clock In port on the rear panel, and connect its frequency reference to the ESG/PSG (Figure 2c).

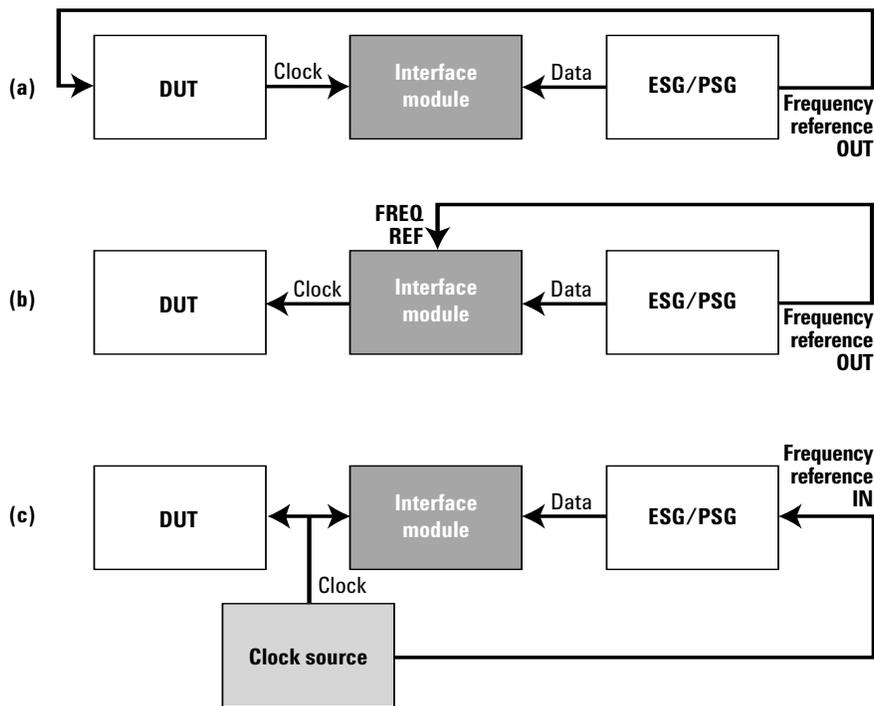


Figure 2. Choose from a variety of clocking options: (a) have the DUT drive the module, (b) use the internal clock from the module, or (c) have an external user-supplied clock source drive the module.

Flexible Signal Interface

Clock outputs

Multiple output clocks are available so that you can share a common clock with other devices in your system. A clock signal can be provided along with the digital data on the device interface bus. Alternately, the clock output can be taken from an SMA-type connector on the rear panel of the interface module.



Figure 3. Rear panel clock connectors. Clock the interface module through the device interface bus or the external clock input port. Take the output clock signal from the device interface bus or from the clock output port.

Adjustable clock phase and skew

The user interface makes it simple to align even high-speed clock edges to the valid portion of the data to meet the setup and hold criteria of your test device. For coarse adjustment of the clock edge, you can rotate the clock phase in 90° steps. For extremely fine adjustment at higher clock rates, you can control the clock-to-data skew in tenths of nanoseconds. As you adjust the clock phase and skew, graphics in the user interface show how the clock edges change relative to the data.

Multiple clocks per sample¹

For interfacing the module with over-clocked devices, the clock can be run at a rate two to four times the speed of the digital data throughput. In these cases, each data sample is held constant for two or four clock cycles.

A new design often means dealing with a new physical interface. Space requirements, heat dissipation, and noise immunity mean baseband designers require a variety of electrical and physical interfaces. The digital signal interface module can help meet this challenge by turning these into easy menu choices instead of requiring custom adapters and converters.

Electrical interfaces

Now you can test a variety of digital devices without the need for electrical conversions at the test interface. Both single-ended and differential logic types are supported, including low voltage TTL, CMOS (1.5V, 1.8V, 2.5V, 3.3V) and LVDS.

Simple and direct physical interface

The connections between the signal generator, interface module, and DUT are simple and direct – often no custom adapters are required. A single three-meter cable connects the module with the signal generator making it ideal for either rack or bench use. Several interchangeable breakout boards are provided with the module to mate with the following common connectors: 68-pin SCSI, Mictor, Samtec or 0.1 inch headers. If your connector type is not included, a spare header connector is provided to help you mate the module and device connectors.

Clear and convenient UI

The interface module features are easy to set up using simple menus in the ESG or PSG user interface. Using the ESG or PSG keys, you set up the signals you want, then configure the digital data and clock settings. To assist you, graphic displays update to reflect the current settings. The digital signal interface module transforms the incoming complex baseband signals into digital data with the data format, clock rate and electrical interface that you need.

¹ This feature is available only in parallel output mode.

Module Features

Data

ESG complex signal formats supported	3GPP W-CDMA, HSPDA, cdmaOne (IS-95A), cdma2000 (IS-2000), calibrated AWGN, GSM, EDGE, GPRS/EGPRS, NADC, PDC, PHS, DECT, TETRA, 1xEV-DV, multicarrier 1xEV-DO, TD-SCDMA, 802.11a/b/g WLAN, Bluetooth, enhanced multitone, noise power ratio, custom digital modulation, arbitrary waveform user file
PSG complex signal formats supported arbitrary waveform user file	custom digital modulation, two-tone, enhanced multitone, pulse building, noise power ratio,
Digital data format	User-selectable: 2's complement or binary offset, IQ (I, I-bar, Q, Q-bar) or digital IF ¹ (real, imaginary)
Data port	Dual 16-bit data buses support parallel, parallel IQ interleaved, parallel QI interleaved, or serial port configuration
(Device Interface) connector	144-pin Tyco Z-Dok+ connects to break-out boards (included) that interface with the following connector types: 68-pin SCSI 38-pin dual AMP Mictor 100-pin dual Samtec 20-pin dual 0.1 inch headers 40-pin dual 0.1 inch headers The Z-Dok+ mating connector is also included for custom interfacing.
Logic types	Single-ended: LVTTTL, 1.5V CMOS, 1.8V CMOS, 2.5V CMOS, 3.3V CMOS Differential: LVDS
Data output resampling	ESG/PSG baseband output is resampled to the arbitrary clock rate set by the user via real-time curve-fit calculations.

Clock

Clock input	User selectable: internal clock, device under test DUT clock (Device Interface connector), or external clock (Ext Clock In connector) SMA, 50 Ω , 0 dBm nominal, 1 to 400 MHz
Clock output	User selectable: Device Interface connector, or Clock Out connector SMA, 2 Vpp into load > 5K Ω from 1 to 100 kHz, 400 mVpp into 50 Ω load from 100 kHz to 400 MHz
Sample rate	User-selectable up to a maximum 100 MHz, but limited by other user settings. In serial mode, the maximum rate is 400 MHz/word size Tables 4-1 through 4-6 in the User's Guide (N5102-90001) supply a complete list of rates for every case.
Bit rate	
Serial	Up to 400 MHz per serial line (400 Mbps LVDS) or 150 MHz per serial line (150 Mbps (CMOS/LVTTTL) 32 lines available
Parallel	Up to 100 MHz x word size (1.6 Gbps LVDS, CMOS and LVTTTL) per parallel bus, 2 parallel buses available
Clocks per sample	In parallel output mode, the data sample can be held for 1, 2 or 4 clock cycles
Clock to data skew	Coarse adjustment in 90° steps from 0 to 270°; fine-adjustment in increments of 100 ps up to 5 ns
Clock polarity	Clock signals may be inverted
Frequency reference input	1 to 100 MHz BNC, 50 Ω , 3 dBm \pm 6 dB,
Power supply (included)	Input: 100 to 240 VAC, 0.7 A, 50 to 60 Hz Output: 5V, 4A DC

Signal generator connectivity

The ESG and PSG vector signal generators offer a wide array of I/O capabilities to simplify measurement setups. You can download waveforms to the instrument, upgrade the instrument firmware, or remotely control the instrument with SCPI commands using either 10BaseT LAN or IEEE-488 GPIB. LAN control requires the use of the L-version or later of Agilent IO libraries, downloadable from the Agilent web site: www.agilent.com/find/iolib

Many of Agilent's signal creation personalities come with user-friendly graphical user interfaces (GUIs) and application programming interfaces (APIs), so that you can control them from your PC or within your automated test environment.

¹ IF is only available in output mode.

Ordering Information

Digital signal interface module

Model/option	Description	Notes
N5102A	Digital signal interface module	Either an E4438C ESG or an E8267C PSG is also required

ESG configuration

Model/option	Description	Notes
E4438C	ESG vector signal generator	Firmware C.03.60 or later required
E4438C-003	Enables ESG digital outputs	Either 003 or 004 is required
E4438C-004	Enables ESG digital inputs	Either 003 or 004 is required
E4438C-506 (or substitute)	250 kHz to 6 GHz frequency range	Can substitute option 501, 502, 503 or 504 (lower frequencies)
E4438C-UNJ	Enhanced phase noise performance	Only required with E4438C-506
E4438C-602	Internal baseband generator, 64 MSa memory depth with digital bus capability	Can substitute E4438C-601 (baseband generator, 8 MSa memory with digital bus capability)

Optional signal creation applications:

E4438C-400	3GPP W-CDMA FDD	
E4438C-401	cdma2000 and IS-95A	
E4438C-402	TDMA: GSM/EDGE/NADC/PDC/PHS/TETRA/DECT	
E4438C-403	Calibrated noise	
E4438C-404	Signal Studio for 1xEV-DO	
E4438C-406	Signal Studio for Bluetooth	
E4438C-408	Signal Studio for enhanced multitone	
E4438C-411	Signal Studio for TD-SCDMA (TSM)	
E4438C-414	Signal Studio for 1xEV-DV and cdma2000	
E4438C-417	Signal Studio for 802.11 WLAN	
E4438C-418	Signal Studio for HSDPA over W-CDMA	
E4438C-421	Signal Studio for noise power ratio	

PSG configuration

Model/option	Description	Notes
E8267C	PSG vector signal generator	Firmware C.03.60 or later required
E8267C-003	Enables PSG digital outputs	Either 003 or 004 is required
E8267C-004	Enables PSG digital inputs	Either 003 or 004 is required
E8267C-520	250 kHz to 20 GHz frequency range	Required
E8267C-UNR	Enhanced phase noise performance	Optional
E8267C-602	Internal baseband generator, 64 MSa memory depth with digital bus capability	Required

Optional signal creation applications:

E8267C-408	Signal Studio for enhanced multitone	
E8267C-420	Signal Studio for pulse building	
E8267C-421	Signal Studio for noise power ratio	

ESG and PSG upgrade kits

If you currently own an E4438C ESG vector signal generator with Option E4438C-001 or -002, and wish to add the Option E4438C-601 or -602 baseband generator, please order the upgrade kit: Option E4438CK-601 or E4438CK-602.

If you currently own an E8267C PSG vector signal generator with Option E8267C-002, and wish to add the Option E8267C-602 baseband generator, please order the upgrade kit: Option E8267CK-602.

Additional Resources

Web:

www.agilent.com/find/basebandstudio

Baseband Studio is a suite of baseband signal applications and accessories that currently work with the E4438C ESG and E8267C PSG vector signal generators to emulate real-world signal conditions – simplifying the creation and verification of cellular, wireless networking, and aerospace/defense component and subsystem designs. The N5102A Baseband Studio digital signal interface module delivers ESG and PSG baseband signals as digital I/Q or IF data. A PC equipped with the N5101A Baseband Studio PCI card enables two new software applications: N5110A Baseband Studio for waveform streaming and N5115A Baseband Studio for fading. Baseband Studio for streaming lets you stream unique baseband waveform data of virtually unlimited length from a PC hard drive through an ESG or PSG for RF or microwave signal generation. Baseband Studio for fading provides digitally integrated fading of ESG baseband signals along with calibrated noise in a single easy-to-setup solution.

www.agilent.com/find/esg

www.agilent.com/find/psg

www.agilent.com/find/signalstudio

Literature:

E4438C ESG Vector Signal Generator, data sheet
Literature no. 5988-4039EN

E8267C PSG Vector Signal Generator, data sheet
Literature no. 5988-6632EN

Baseband Studio for Streaming, technical overview
Literature no. 5988-9493EN

Baseband Studio for Fading, technical overview
Literature no. 5988-9494EN

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(tel) 0800 047 866

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(fax) (65) 6836 0252

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