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Find the *Keysight / Agilent N5309A* at our website: *Click HERE*

N5309A: Exerciser, Protocol Test Card 2.0 and Compliance Tests Compliance Testing

General	• Compliance tests run on existing N5309A exerciser hardware • PCI Express Gen 1 and Gen 2 both supported • Easy to use GUI – Integrated into N5309A exerciser GUI – Run single tests, or select multiple tests for sequential execution – Test tagging at start and end of every test. Allowing easy capture and analysis with Agilent's protocol analyzer
Test support	• Two test packages available – E2969B PTC2 • Supports all 13 PCI-SIG mandatory test cases – N5309A-COM compliance assured test package with over 170 recommended tests • 70 transaction layer tests • 40 link layer test • 66 config space tests • 1 electrical test

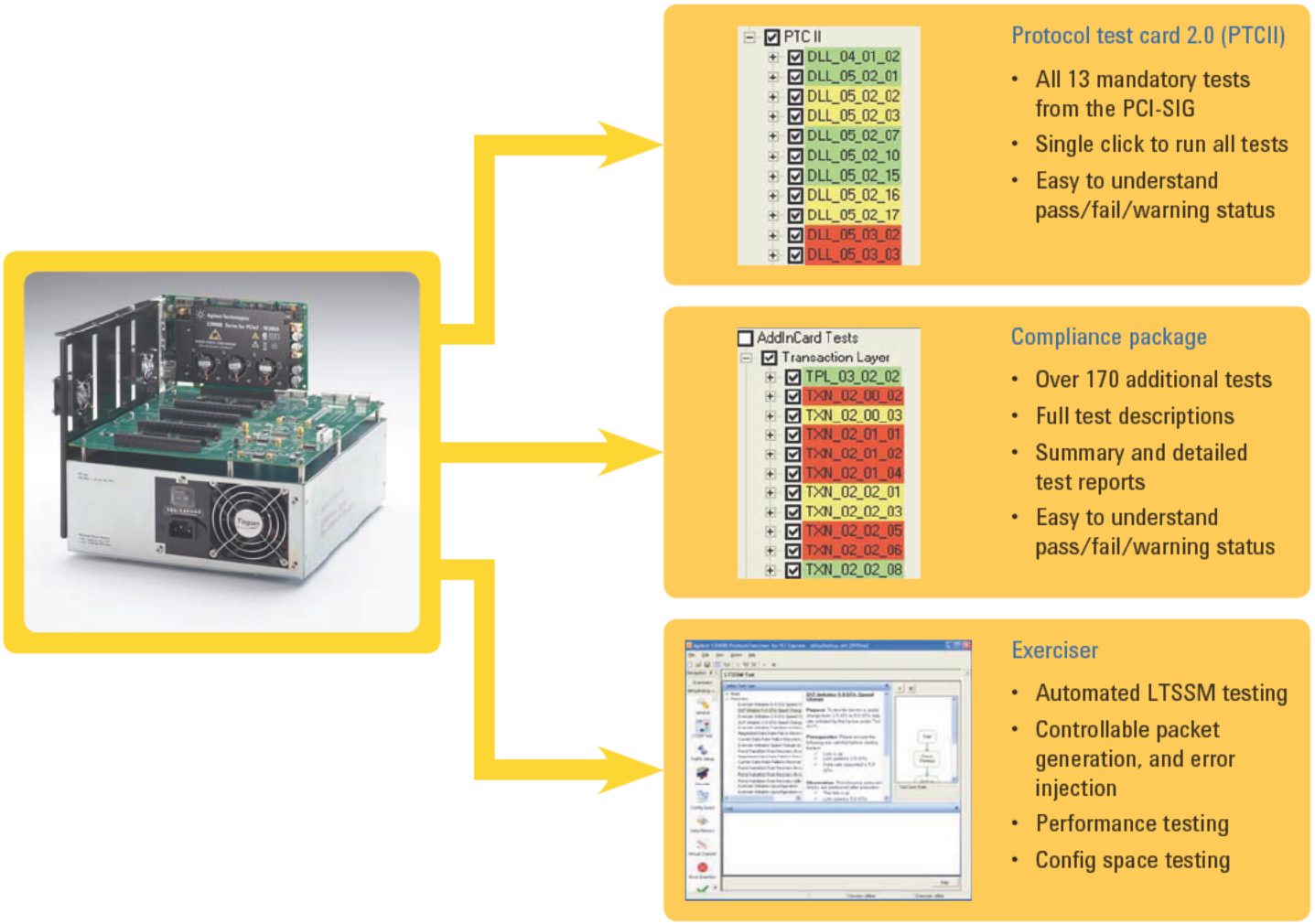


Figure 7. Exerciser and Compliance Test: one hardware, multiple applications

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N5309A: Exerciser, Protocol Test Card 2.0 and Compliance Tests

Exerciser Features

Physical layer	• Fully automated symbol encoding/decoding, generation, and validation of packet framing; ability to report framing errors to user • Scrambling can be turned on or off by user • Configurable, automatic link initialization and training: – Automatic Lane Polarity Detection (RX), separate for each lane – Programmable Lane Polarity Inversion (TX), separate for each lane – Automatic link width negotiation; link widths x1, x4, x8, x16 supported; user can configure which widths will be negotiated during link training – Programmable Tx Lane Reversal (Rx is automatic) – Programmable Lane Skew: (± 7 symbols, resolution: 1 symbol time) • Link Training and Status State Machine (LTSSM): Full support for states: detect, polling, configuration, recovery, L1, L0s, L0 • Programmable skip rate and number of SKPs per skip OS *Note concerning power management:* When exiting from L0s or L1 the exerciser's receiver may not be able to receive data until the second SKP ordered set. Packets might get lost, causing a retraining of the PCI Express link.
Data link layer	• Fully implemented data link control and management state machine • Automatic flow control initialization; programmable credits and flow control update rate • Automated generation of data link layer packets (DLLPs): ACK/NAK, Init/Update-FC • Automatic generation and checking of LCRC and sequence numbers; allows the insertion of incorrect LCRCs into TLPs for testing purposes; automatic retry function management
Transaction layer	• User software can define arbitrary sequences of transactions • "Send single packet" for simple packet transmission one memory for block transactions per virtual channel • Conditional start on RX pattern matcher, external trigger in and completion status • Generation and receipt of packets at maximum bandwidth (stress testing); up link width x8 at 5 GT/s • Infinite loop • One completer queue defines the way completion packets are sent out (e.g. lengths, errors inserted, partitions, etc) – Completions can be split into individual packets • Up to 32 outstanding requests can be "pending" (256 in extended mode) (request without completion) • Decoders (6 BARS + Expansion ROM decoder) • Payload generation and reception from/into data memory



Figure 8. N5309A exerciser and LTSSM exerciser

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N5309A: Exerciser, Protocol Test Card 2.0 and Compliance Tests

Exerciser Features

Packet generation	• Transmit modes – Send single packet – Block transfer – Import packet from captured analyzer trace • Sent single packet – Send any type of TLP, with control of all the fields – Create errors on the transmitted packet • Block transfer – Create large transfers (read or write), with configurable request size – Automatic data comparator to ensure no data corruption – Performance testing to ensure maximum data rates • Completion queues – Program any type of completion status
Error generation and analysis	Error insertion capabilities on the physical layer, data link layer and transaction layer • Physical layer: – Transmitter polarity inversion – Transmitter lane reversal – Determinant lane skew of up to 7 symbols – Link width and lane sequence negotiation emulating a x1, x4, x8, x16 device – Sending packets with incorrect “running disparity” – TX framing errors on TLPs • Data link layer: – Sending packets with incorrect LCRC – Systematically answers NAK instead of ACK, for retry buffer test – Wrong sequence numbers – Generate a free form DLLP with any bit changed • Transaction layer: – Arbitrary header field contents – Sending “nullified TLPs” – Sending “poisoned TLPs” – Advertised packet length (in TLP header) is different from actual packet length (by one word) – The transmitter ignores flow control credits – Completion loss/delay
Configuration space	• Can emulate the configuration of different types of PCI Express devices • Supports up to 6 base address registers and expansion ROM decoder • Full support for PCI Header type 0 configuration space • Supported capability structures: – PCI power management capability structure – MSI capability structure – PCI Express capability structure – Virtual Channel capability structure – Advanced error reporting structure
Display	Explorer like tree structure to select test Display of test log in GUI Feedback of state transitions performed Timestamp in [ns] for all states Link status indications Link width x1, x4, x8, x16
Debug support	External trigger on exit from L0 Log file output of LTSSM exerciser state transitions and timestamps Automatic flow control initialization with infinite credits
Supported states	Detect Polling Configuration L0, L0s, L1 Recovery
Easy software upgrade	Ability to upgrade from PTC II license to Compliance Assured Test Package licence to full exerciser and LTSSM software licence

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N5309A: Exerciser, Protocol Test Card 2.0 and Compliance Tests Specifications

System requirements

The N5309A is a standalone PCIe card that can be used for the PTCII, compliance assured test package and exerciser application. The software application that controls the N5309A card runs on a Windows XP or Windows 7 PC host connected via a USB 2.0 link. For more details regarding the PC controller, see related products section of the data sheet.

Environment

Temperature (AT-ETM757)	Operating: 0 °C to +55 °C Storage: –40 °C to +70 °C
Humidity (AT-ETM758)	Operating: 15 to 95% Operating soak: 90% (24 h)
Safety standards	Installation category: EN ISO/IEC 17025, IEC 61010-1/EN61010-1, II Pollution degree: 2 Environmental rating: Standard

General characteristics

Power requirements	100-240 Vac 130-160 VA 1.5 A maximum 47 to 63 Hz
Form factor	PCI Express standard height, half size card Length: 168 mm (6.6 inch) Height: 111 mm (4.37 inch) Component height on top side including heat sink: 19 mm (0.75 inch)
Connectors	Front bracket: • USB type B • Vin 18 V DC, 3.5 A • PCIe analysis output, proprietary Top connector: • PCIe, connector x16, only x1 lane connection Bottom connector: • PCIe, x1, x4, x8 or x16 (version dependent) Trigger in/out: • LVCMOS 2.5 V, see user guide • Vin maximum 3.0 V Power in: • ATX power connector to supply the top connector
SSC	Support for SSC
Data memory	160 kB

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N5309A: Exerciser, Protocol Test Card 2.0 and Compliance Tests Specifications

Electrical characteristics	
Data in	Input levels • Minimum: 100 mV • Maximum: 1.2 V Jitter tolerance • Compliant to PCIe Specification 2.0 Rev 0.9 Frequency • Minimum: 2.5 GHz –300 ppm*UI 5 GHz –300 ppm • Maximum: 2.5 GHz +300 ppm; 5 GHz +300 ppm SSC support • None
Data out	Output level • Minimum: 800 mV (full swing) • Typical: 1000 mV • Maximum: 1.2 V De-emphasis 3.5 dB • Typical: 3.5 dB De-emphasis 6 dB • Typical: 6.0 dB UI interval • Minimum: –300 ppm*UI • Maximum: +300 ppm*UI Total jitter • Typical: 0.3 UI Electrical idle • Typical: 20 mV
External clock in	Level • Minimum: 800 mVdiff • Maximum: 1200 mVdiff AC coupled Frequency: 100 MHz
Reference clock in	Compliant to PCIe Specification 2.0

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Ordering Information

Exerciser

Hardware		Description
	N5309A-E01	Half size exerciser and LTSSM module x1 for PCIe 5 Gb/s
	N5309A-E04	Half size exerciser and LTSSM module x4 for PCIe 5 Gb/s
	N5309A-E08	Half size exerciser and LTSSM module x8 for PCIe 5 Gb/s
	N5309A-E16	Half size exerciser and LTSSM module x16 for PCIe 5 Gb/s

Software		Description
Gen2 exerciser software	N5309A-EX2	Exerciser SW license: exerciser and LTSSM at 5 Gb/s
Gen2 Ready exerciser software	N5309A-EX1	Gen2 Ready exerciser SW license: exerciser and LTSSM at 2.5 Gb/s
Compliance tests	N5309A-PTC	Exerciser SW license: protocol test cards software (included with exerciser purchase)
	N5309A-COM	Exerciser SW license: compliance assured test package (over 170 pre-defined tests)

Accessories		Description
	N5316A	Test backplane for PCIe2

Protocol Test Cards		Description
PTC1	E2969A	Protocol test card for PCI Express Gen 1 (includes software and hardware)
PTC2	E2969B	Protocol test card for PCI Express Gen 2 (includes software and hardware)

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