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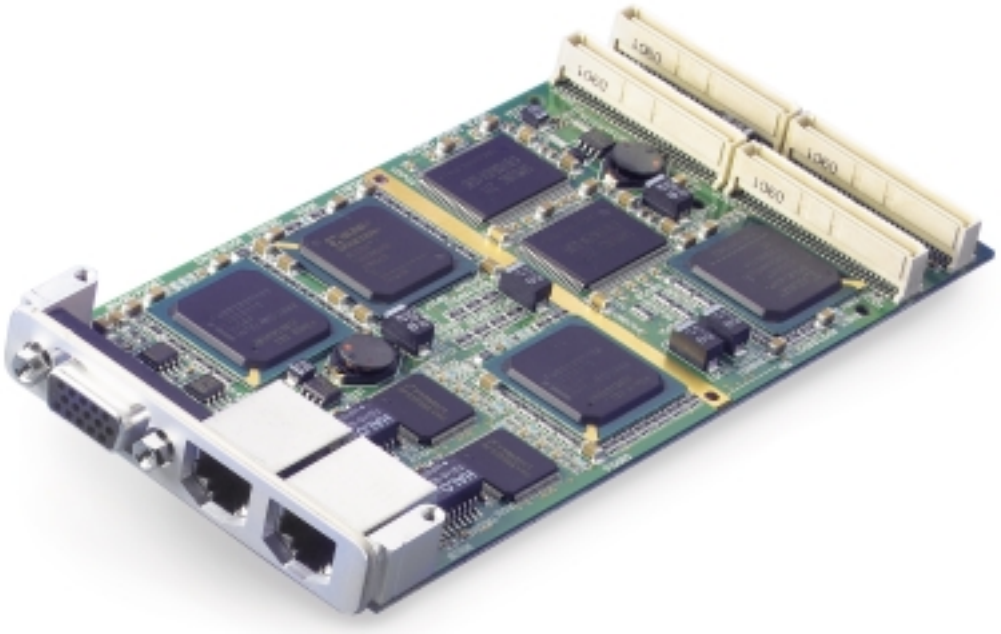
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data sheet

AMC-FDX-2

Two Port AFDX Test, Simulator and Monitor Module for PMC



Avionics Databus Solutions

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AMC-FDX-2

Two Port AFDX Test, Simulator and Monitor Module for PMC

product guide

General Features

The AMC-FDX-2 is AIM's new ultra high performance intelligent PMC (PCIbus Mezzanine Card) module offering full function test, simulation, monitoring and analyser functions for AFDX (Avionics Full Duplex Switched Ethernet) networks. It's unique on board processing capability, memory resources, customised AFDX MACs and IRIG-B time code decoder/ generator gives AFDX users unparalled features for the most demanding AFDX applications.



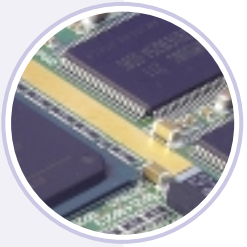
The AMC-FDX-2 PMC module provides two AFDX ports being configured as two single or one dual redundant ports each implementing a 100Mbit Full Duplex Ethernet interface.

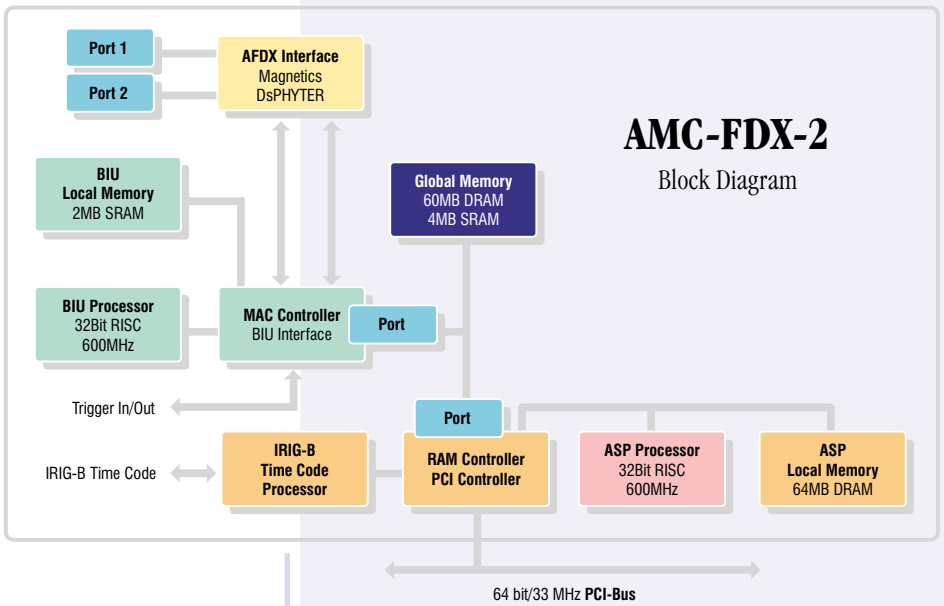
Ports can operate concurrently in Traffic Simulator or Receiver/ Monitor modes with support for AFDX port related Frame Statistics. Virtual Link (VL) packet capturing and monitoring features are complimented with powerful triggering and filtering capabilities.

The AMC-FDX-2 uses AIM's field proven 'Common Core' hardware design utilising two advanced RISC processors, one acting as Bus Interface Unit processor and one as Application Support Processor (ASP). The vast memory resources on board allow to implement large receive buffers and Complex Transmit scenarios on-board. An AFDX specific Physical Bus Interface implements two full duplex ports for connection to AFDX networks.

The AMC-FDX-2 module is available with the optional fdXplorer, the AFDX Network Analyser Software and the ParaView, the Parameter Visualiser Software for Windows.

- *Two advanced 600 MHz XSCALE Processors on board*
- *Designed for applications such as:*
  - *Test & Verification of 'End Systems'*
  - *'Switch' Testing*
  - *Monitoring of traffic between 'End Systems' & 'Switch'*
  - *Inter Switch Traffic Analysis*
  - *Multi Stream High Level System Integration*
- *Programmable Ports - Traffic Simulator and Receiver/Monitor Concurrently*
- *Synchronised Timing across Multiple Modules*
- *Driver Software for Windows, Linux, LynxOS and VxWorks*





AMC-FDX-2
Block Diagram

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Traffic Generation

The AMC-FDX-2 provides real time traffic generation on both ports concurrently. Transmitter operation allows users to fully programme all fields of the AFDX Frame including the Virtual Link Identifier, MAC Source Address, IP Structure, UDP Structure, Payload and Sequence number. Multiple modes of transmit sequencing are supported, these being Generic / Replay and UDP Port oriented shaped Transmissions. Users can programme Payload Data with User Defined or Fixed Data. Inserting the Time Tag in the Payload Data provides an elegant solution to measure frame transmit delays through the network. Synchronisation of transmissions across multiple ports is achieved by using Strobe Inputs/Outputs.

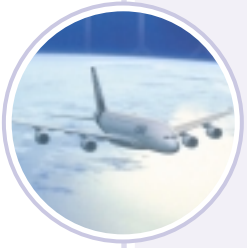
- *Programmable Timing & Sequencing of Frames*
- *Physical Error Injection - CRC, Gap, Size, Alignment*
- *Logical Error Injection on Layers 2, 3, 4*
- *Timing Error Injection - Violation of Bandwidth Allocation Gap (BAG)*
- *Autonomous Dynamic Data Generation*
- *UDP Port Simulation with Traffic Shaping & Sequence Numbering*
- *On-board support for sampling and queuing ports*

UDP/VL Receive Mode

The AMC-FDX-2 module ports can be configured to work in UDP / VL oriented receive mode. In this mode each UDP port has a separate buffer queue. Received frames are stored with frame headers containing time tag and status information. Frame header information can be stored and payload data optionally discarded for the testing of Switches and the complete network. With the Traffic shaping verification enabled, any violations are reported as errors in related frame headers.

- *VL oriented Filtering*
- *Second Level Filtering on Generic Frame Parameter*
- *Time Stamping of Received Packets with extended IRIG-B time code (1µs)*
- *Physical Error detection, Frame Level - CRC, Gap, Size and Alignment*
- *AFDX Specific Error Detection*
  - *Traffic Shaping Verification*
  - *Verification of MAC, IP and UDP Headers*
  - *VL oriented Integrity Checking*





Chronological Receive Mode

(Monitor Mode)

The AMC-FDX-2 module ports can be configured in Chronological Receive Mode to sequentially receive frames and store them in a circular buffer. The payload data can be discarded to optimise the use of the buffer for frame capture and analysis. Powerful Filtering, Triggering, Complex Triggering and Capture Modes allows users to select only the frames, data and errors of interest. Monitor Mode also provides activity monitoring and statistics for each VL recorded by the AMC-FDX-2 module. The interface modules report the number of frames received and the number of errors detected globally and in VL orientated format.

- *VL Orientated Receive and Filtering*
- *Second level filtering on Generic Frame Parameters*
- *Chronological Monitor with Time Stamping to 1µs*
- *Massive on-board Monitor Buffer*
- *Inter frame Gap time measurements with 40 nsec resolution*
- *Comprehensive Triggering / Filtering / Capturing*
- *Programmable Data Capture Modes - Trace after Trigger & Recording*
- *Physical Error Detection - CRC, Gap, Size and Alignment*
- *AFDX Specific Error Detection*

Application Support Processor

The 600 MHz Application Support Processor (ASP) provides unique on-module processing functions typically provided by host PC processing systems.

- *IP and UDP layer of the AFDX protocol*
- *Driver Software Execution on the board*
- *Dynamic Data Generation*
- *Loop / Pollution between Rx and Tx port*
- *Automatic Test Sequence Generation*
- *Program using Real Time operating systems*

IRIG-B Time Code Decoder

An on board IRIG-B Time Code decoder and generator allows synchronisation of multiple AFDX ports using multiple AMC-FDX-2 modules. Modules can be synchronised using an external IRIG-B time source or the on-board Time code generator of one module as the reference for accurate correlation of data across multiple AFDX ports.

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AMC-FDX-2

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Physical Bus Interface

The AMC-FDX-2 modules provide two AFDX ports which can be used as two single channel or as one dual redundant channel AFDX specific Physical Bus Interface.

- Customised Media Access Controllers (MAC's) implemented in FPGA optimised for AFDX
- 2 MByte Transmit / Receive Burst Buffer
- Physical Interface and Magnetics (COTS)
- 8-socket Network Interface connectors - RJ45
- Trigger, Strobe and Time Code I/O connector

Driver Software Support

The AMC-FDX-2 module is supplied with an Application Programming Interface (API) and Drivers compatible with Windows, Linux, LynxOS and VxWorks.

Technical Data

Sub-System Interface: 64 Bit / 33 MHz PCIbus (Revision 2.2) compliant

Processors: Two 32-bit, 600MHz RISC Processors

Memory: 64 MBytes Global RAM, 64 MBytes ASP RAM

Encoder/Decoder: Two AFDX specific Ethernet MAC's
- Inter Frame Gap generation and measurement with 40 nsec resolution

Time Tagging: 46 bit absolute IRIG-B Time with 1μsec resolution

Physical Bus Interface:
Two full duplex AFDX ports configurable to one dual-redundant AFDX port

Connectors:
- 4x Standard PMC Connectors
- 2 x 8 way RJ45 connectors, one per AFDX port
- 1 x 15 way HD-Sub connector (female) for Time Code and Trigger I/O

Dimensions: 149 x 74 mm Standard PMC Format

Power Consumption: typical 7 Watts (operating)

Operating Temp. Range:
Standard: 0°C... +55°C ambient. Extended: -15°C...+60°C ambient

Storage Temp. Range: -40°C ... +85°C ambient

Humidity: 0 to 95% non-condensing

Ordering Information

AMC-FDX-2
Two Port, PMC (PCI Mezzanine Module) to AFDX Interface:
Traffic Simulator, Receiver and Chronological Monitor including IRIG-B Time Code Decoder / Generator
64 MByte Global RAM, 64MByte ASP RAM
Available option: Conduction Cooled Configuration

AVC-2
VME (6U) Carrier Module with two PMC slots

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