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Hardware Manual

API1553-1/2

for
Single/Dual Stream
MIL-STD-1553
PCI Module



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API1553-1/2

Hardware Manual

for

Single/Dual Stream

MIL-STD-1553

PCI Module

V01.00 Rev. C

October 2010

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1. INTRODUCTION

1.1 General

This document comprises the Hardware User's Manual for the AIM PCI I-Architecture (API) 1553-1 and API1553-2 PCI-Bus modules. The API1553 modules are members of AIM's new family of advanced PCI-Bus modules for analyzing, simulating, monitoring and testing of avionic databus systems.

The API1553 modules are used to simulate, monitor and inject protocol errors of MIL-STD-1553A/B based databus systems. The API1553-2 offers an interface to two dual-redundant MIL-STD-1553 bus channels (streams) using a full sized single card PCI Bus slot of an IBM compatible PC, whereas the API1553-1 implements one dual-redundant data stream on a short form factor PCI-card.

The hardware architecture provides enough resources (i.e. processing capability and memory) to guarantee, that all specified interface functions on all channels are fully available concurrently. The on-board processing capabilities and the large memory size of the DRAM enables autonomous operation with a minimal interaction of the PC host processor.

The advanced architecture uses three processors (two on the API1553-1). A powerful 64bit RISC processor (ASP) assists and supports the application and driver software tasks, and expands the capability of the API1553 modules to that of a high level instrument. To fulfill the real-time requirements of avionic type databus systems a high performance 32bit RISC processor (BIP) is implemented for each Bus Interface Unit (BIU).

An IRIG B Time Code Decoder is implemented on the API1553 boards to satisfy the requirements of 'multi-channel time tag synchronization' on system level.

1.2 How This Manual is Organized

This API1553 Hardware Manual is comprised of three main sections.

Section 2 - **Installation** - describes the steps required to install the API1553 device, and connect the device to other external interfaces including the MIL-STD-1553 Bus, IRIG-B, and RS-232 signals

Section 3 - **Structure of the API1553 1/2** - describes the physical hardware interfaces on the API1553 using a block diagram and a description of each main component

Section 4 - **Technical Data** - describes the technical specification of the API1553.

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1.3 Applicable Documents

The following documents shall be considered to be a part of this document to the extent that they are referenced herein. In the event of conflict between the documents referenced and the contents of this document, the contents of this document shall have precedence.

1.3.1 Industry Documents

MIL-STD-1553B, Department of Defense Interface Standard for Digital Time Division Command/Response Multiplex Data Bus, Notice 1-4, January 1996

PCI LOCAL BUS Specification Revision 2.1, June 1, 1995.

IDT79RV4640 and IDT79R4650 RISC Processor Hardware User's Manual Version 1.1, November 1995

Digital Semiconductor SA-110 Microprocessor, Technical Reference Manual, Revision B of a preliminary document, June 1996.

Technical Reference Manual GT64011 PCI and System Controller for R4640 Processors, Preliminary Revision 1.2 , 2.7.97

1.3.2 Product Specific AIM Documents

AIM - API/ACI 1553 Getting Started Manual
Assists first time users with software installation, hardware setup and starting a sample project.

AIM - Reference Manual API1553 Application Interface Library
Provides a detailed description of the programming interface between the PC and the onboard driver software.

AIM - User's Manual 'ASP Boot Monitor Program'
Provides a description of the Debug Monitor commands and functions.

AIM - User Manual 'PBA-2000 PC Based Bus Analyzer Software Package' (Delivered with software package)

AIM - User Manual 'PBA-2000P PC Based Bus Visualizer Software Package' (Delivered with software Package.

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2. INSTALLATION

The API1553 features full PCI ***Plug-and Play*** capability. There are no jumpers or switches on the board which have to be modified by the user.

Installing the API1553 card in your system is simple, please follow the instructions carefully.

▶ **To install the card:**

a. Switch off your system and all peripheral devices. Unplug the power cord from the wall outlet.

b. Touch a metal plate on your system to ground yourself and discharge any static electricity.

c. Remove the cover from your system.

d. Find a free PCI-expansion slot in your system with suitable size.

e. Remove the metal plate from the slot you have chosen and put the screw aside.

f. Align the API1553 cards slot connector with the PCI expansion slot and gently lower the card into the free slot.

g. Secure the card to the expansion slot with the screw you removed from the metal plate.

h. Replace the cover of your system.

2.1 Connecting to other Devices

The API1553 interfaces to external devices via two standard DSUB connectors.

2.1.1 Connecting to the MIL-STD-1553 Bus

The MIL-STD-1553 connection is done via a DSUB-9 female connector. The pinout of the connector is shown below:

Table 2.1.1-I - Pin, Signal and Description

Pin No.	Signal	Description	
1	MILBUS	Channel 1 Bus A (true)	
2	MILBUSx	Channel 1 Bus A (complement)	
3	Shield		
4	MILBUS	Channel 1 Bus B (true)	
5	MILBUSx	Channel 1 Bus B (complement)	
6	MILBUS	Channel 2 Bus A (true)	(API1553-2 only)
7	MILBUSx	Channel 2 Bus A (complement)	(API1553-2 only)
8	MILBUS	Channel 2 Bus B (true)	(API1553-2 only)
9	MILBUSx	Channel 2 Bus B (complement)	(API1553-2 only)

Optional a Breakout cable can be ordered with four two-meter stub cables terminated with trumpeter PL-75 plugs.

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2.1.2 Connecting the IRIG B, Trigger or RS232 Signals

The General Purpose Connector is implemented as a DSUB-15 female connector. The connector comprises the trigger input- and output signals, the IRIG-B input and output and the RS232 signals. The pinout of the connector is shown below:

Table 2.1.2-I – IRIG B, Trigger and RS232 Signals

Pin No.	Signal
1	Trigger Output BC, Channel 1
2	Trigger Output RT, Channel 1 / RS232 TXD
3	Trigger Output BM, Channel 1
4	IRIG Input
5	IRIG Output
6	Trigger Output BM, Channel 2 (API1553-2 only)
7	Trigger Output RT, Channel 2 / RS232 RXD
8	Trigger Output BC, Channel 2 (API1553-2 only)
9	Trigger Input BC, Channel 1
10	Trigger Input RT, Channel 1
11	Trigger Input BM, Channel 1
12	GND
13	Trigger Input BM, Channel 2 (API1553-2 only)
14	Trigger Input RT, Channel 2 (API1553-2 only)
15	Trigger Input BC, Channel 2 (API1553-2 only)

Note: During power-up and board initialization the RS232 signals are connected to the general purpose connector and voltages of appr. +/- 12 Volts can be seen on this output.

The IRIG-IN and IRIG-OUT signals shall be connected depending on the timetag method used as shown below.

a. Single AIM-Module no external IRIG-B source

- No connection required

b. Multiple AIM-Modules with no common synchronization requirement

- No connection required

c. Single or multiple AIM-Module(s) with external IRIG-B source

- Connect external IRIG-B source to IRIG-IN and GND of all modules

d. Multiple AIM-Modules with no external IRIG-B source internally synchronized.

- Connect the IRIG-OUT signal and the GND of the module you have chosen as the time master to all IRIG-IN signals (including the time master).

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2.1.3 Front Panel LED's

Four subminiature LED's indicates the various conditions of the module at the front panel. The LED's are located in a quadruple LED- Array on the physical interface daughterboard.

Table 2.1.3-I - LED Descriptions

LED Name	Color	Description
FAIL1	Red	LED illuminates if an Error during the BIU 1 selftest occurs.
COUPLED / ACTIVITY 1	Green	LED illuminates permanently if the MILbus channel 1 is connected. LED flashes if any MILbus Activity is detected by the Encoder/Decoder of the MILbus channel 1.
FAIL2	Red	LED illuminates if an Error during the BIU 2 selftest occurs.
COUPLED / ACTIVITY 2	Green	LED illuminates permanently if the MILbus channel 2 is connected. LED flashes if any MILbus Activity is detected by the Encoder/Decoder of the MILbus channel 2.

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3. STRUCTURE OF THE API1553-1/2

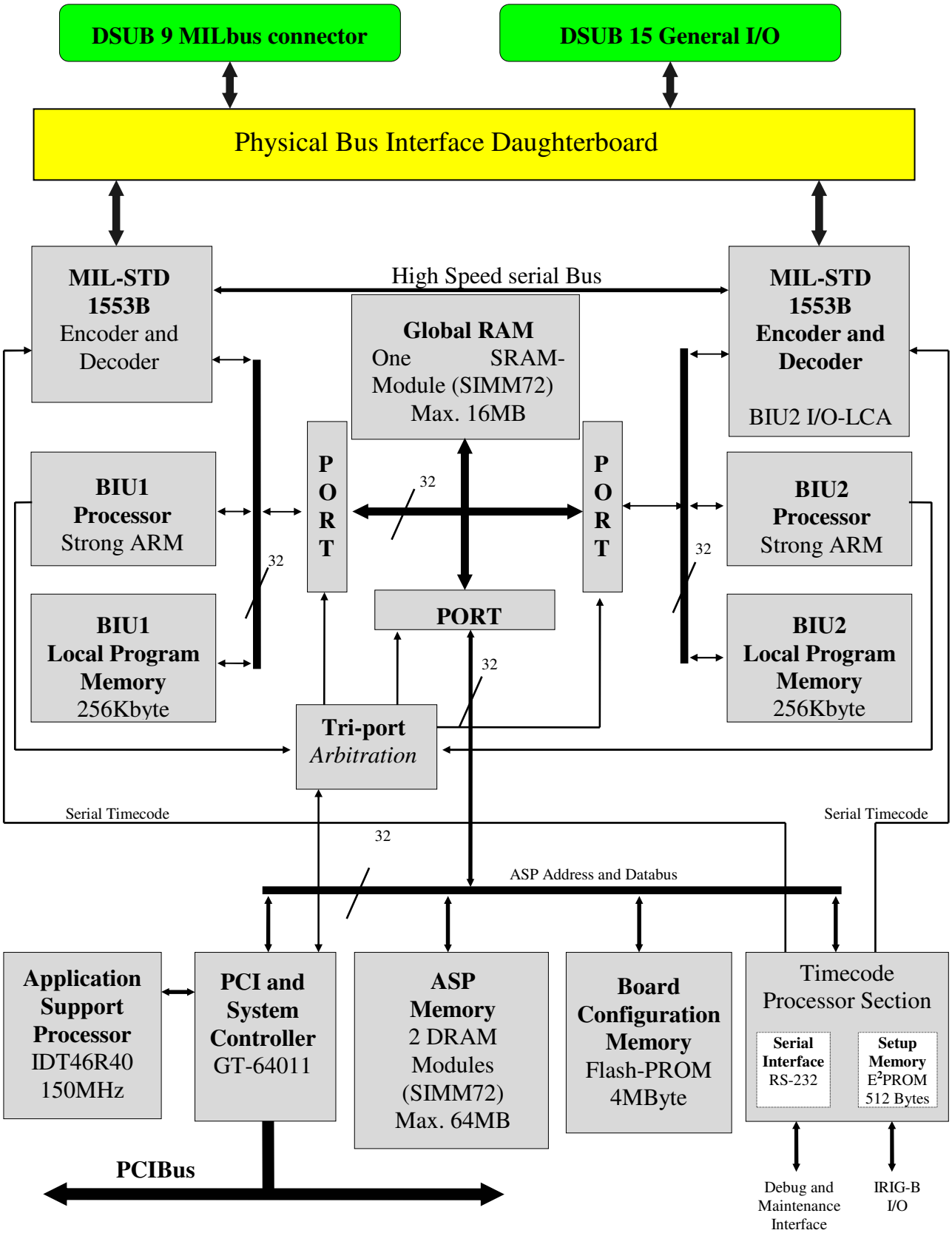
The structure of the API1553-2 board is shown in the block diagram on the next page. The API1553-1 implements only the BIU 1 section.

The API1553 comprises five main sections:

❑ ASP Section	ASP with local Program Memory, PCI System Controller, and Board Configuration Memory
❑ BIU Section(s)	BIP with local Program Memory and I/O-LCA
❑ Global RAM	Tri-port Arbitration Logic, Global RAM
❑ Time Code Section	Time Code Generation, RS232 and E2PROM
❑ Physical Bus Interface	Transceivers, Transformers, relays and connectors on a daughterboard

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Figure 3-1 API1553-1/2 Block Diagram



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3.1 Application Support Processor Section

The ASP-Section is divided in six subsections:

a. ASP Processor

b. PSC (PCI and System Controller)

c. ASP Program Memory

d. Board Configuration Memory

e. Time Code Processor Section with Board Setup Memory (E2PROM) and Debug and Maintenance Serial Interface (RS-232)

f. Global RAM Port

3.1.1 Application Support Processor (ASP)

The ASP is a 64bit IDT79RV4640 Processor based on the MIPS RISC architecture with a internal core speed of 150 MHz and a external Memory bus speed of 50Mhz.The Processor incorporates a 32 bit single precision floating point coprocessor on chip. Double precision floating point operations are supported via a software library.

The ASP is the master control processor and performs the following tasks:

a. Run the on board driver software

b. Setup the Global RAM for BIU Processor operation

c. Control the RS-232 Maintenance and Debug Interface

d. Configuration of the programmable BIU I/O LCAs with the Bitstream data from FLASH

e. Provides the program data for the BIU Processors (stored in the FLASH)

3.1.2 PCI and System Controller (PSC)

The GT-64011 provides a single-chip solution for building a system with memory, I/O devices and PCI Bus interface around the IDT-79RV4640 processor.

The GT-64011 has a three-bus architecture:

a. A 32 bit address and databus interface to the IDT-79RV4640.

b. A 22 bit address and a 32 bit databus interface to the memory and I/O devices.

c. A 32 bit address and databus interface to the PCI Bus.

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3.1.3 Time Code Generation

The Time Code generation is based on an IRIG B Time Code decoder. The Time Code Information is used for time-tagging and multi-channel synchronization.

The time tag on the board is generated in the following format:

Table 3.1.3-I – Time Elements and Bits

Time Element	Number of bits
DAYS of year	9
HOURS of Day	5
MINUTES of Hour	6
SECONDS of Minute	6
MICROSECONDS of Second	20
Summary	46 (6 Bytes, stored in two 32bit words)

This comprehensive time tag information allows the API1553 a flexible, application dependent time tagging of the avionic databus traffic.

3.1.4 Debug and Maintenance Interface

For debugging during hardware and firmware integration as well as for maintenance purposes, a serial RS-232 interface is provided.

3.1.5 Global RAM Port

The Global RAM is shared between both BIU processors (BIP), the ASP and the PCI Bus. The ASP has access to the common Global RAM via a 32 bit wide data and 24 bit wide address port. The arbitration implements a round robin scheme to guarantee maximum latencies for all requests.

3.1.6 PCI Interface

The PSC interfaces directly with the PCI bus. The PSC can be either a master initiating a PCIbus operation, or a target responding to a PCIbus operation. The PSC incorporates 96-bytes of posted write and read prefetch buffers for efficient data transfer between the ASP / DMA to PCIbus, and PCIbus to host memory. The PSC becomes a PCIbus master when the ASP or the internal DMA engine initiates a bus cycle to a PCIbus device. The PSC configuration register set is PCI Plug and Play compatible.

3.2 Bus Interface Unit (BIU)

One or two Bus Interface Units (BIUs) are implemented on the API1553 module. Both BIUs implement exactly the same functionality therefore only one BIU is described in detail herein. Each BIU handles one dual-redundant MIL-STD-1553 channel. The BIU provides a StrongArm RISC processor, a fast program and data memory, a large programmable Gate Array for I/O functions, and a fast port to the Global RAM.

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3.2.1 Bus Interface Processor (BIP)

The BIP handles the real time critical control of one dual-redundant MIL-STD-1553 channel. The BIP has access to the Global RAM and receives its program (firmware) from the ASP during the initialization phase of the API1553 module.

The BIP performs the following main tasks:

a. Initialize BIU hardware including encoders and decoder.

b. Execute a BIU power-up selftest.

c. Service the encoders and decoders to handle the demanded bus traffic in real time.

d. Stores the received data in the Global RAM as demanded.

The features of the used StrongARM processor include full 32 bit operation at a core speed of 200Mhz with a very low power consumption due to the 2.0V core power supply.

3.2.2 Program and Data Memory

A fast RAM is implemented as the program and data memory for the BIP using a single 64kx32 non pipelined synchronous static burst RAM (SSRAM) device. The RAM uses power saving 3.3V technique and is housed in a space saving high density 100-lead TQF-Package.

3.2.3 MIL-STD-1553 Encoder

The MIL-STD-1553 encoder comprises a Manchester Encoder with full error injection capability. The encoder is used to generate faulty (or fault free) command and data words on the bus. This encoder allows to insert protocol error as required by the 'Remote Terminal Production Test Plan'.

3.2.4 MIL-STD-1553 Decoder

The Manchester decoder samples the incoming serial data stream. The decoder detects the synchronization pattern (Command/Status and Data Sync.), converts 16 bit Manchester encoded serial data to parallel and receives the parity bit. The decoder indicates the sync. pattern and error information (parity error, Manchester error, framing error) via dedicated bits in a readable error register.

3.2.5 External Trigger-Inputs and Outputs

For Bus Controller (BC), Remote Terminal (RT) and Bus Monitor (BM) triggering three trigger inputs and three trigger outputs are provided at each MILbus channel (one trigger input and one trigger output for each operational mode). Buffers and filter circuitry is provided at the trigger inputs and outputs to avoid EMC problems.

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3.2.6 Global RAM Interface

The BIP has fast access to the Global RAM of the API1553 module. This memory is shared between the two BIU processors, the ASP and the PCI master of the PC.

3.3 Global RAM

The Global RAM is shared between the BIUs (one or two), the local bus of the ASP section and the PCI interface. The databus of the memory is 32bit wide. The arbiter is running with a frequency of 50 MHz. and handles the prioritization of the bus requester in a round robin process. A standard high-speed static RAM is used for the Global RAM. On the API1553-1 the SRAM is directly soldered on the board, whereas on the API1553-2 the RAM is implemented on a high-density 72-lead SIMM, which offers the capability to increase the memory size in the field. The SIMM socket on the API1553-2 is a low profile 22° single row socket. The arbiter and control logic does the arbitration between the three ports.

3.4 Time Code Processor Section

The various functions of the Time Code Processor Section are:

a. IRIG-B compatible Time Code Decoder and Encoder function.

b. UART with an RS-232 interface for debug and maintenance purposes.

c. E^2PROM to save module specific parameters.

This functionality is based on the single chip microcontroller that provides or can emulate most of the functions above. To transfer data between the microcontroller and the ASP an eight bit wide I/O port of the microcontroller is connected to the local bus of the ASP Section.

3.5 Voltage Supplies

All voltages needed on the board other than the standard +5V and +/-12 Volts from the PC-Supply are generated on the board. Several devices on the board require a +3.3V voltage, which is generated from +5V using a DC-DC Converter. The 2.0V needed for the StrongARM processors are generated from +3.3V using a linear regulator.

3.6 Physical Bus Interface MIL-STD-1553 Board

The Physical Bus Interface (PBI) is a plug-in board, which is mounted on the API1553 main board. There are two MIL-STD-1553 PBI- types implemented:

a. Programmable-PBI MIL-STD-1553

b. Standard-PBI MIL-STD-1553

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Both PBI's are identical, except the Standard-PBI will not be fully assembled and thus it provides less functionality as the Programmable-PBI.

3.6.1 Programmable-PBI MIL-STD-1553 Features

Programmable-PBI MIL-STD-1553 contains one or two dual redundant MIL-STD-1553 channels which each comprises a dual-redundant transceiver, transmitter amplitude control circuitry's, a dual bus coupling transformer and the coupling relays with the MILbus network emulation circuitry.

The MIL-STD-1553 trapezoidal dual transceivers offer the capability to control the output amplitude on the MILbus via the voltage control pins. The output amplitude of the MILbus transceiver can be adjusted by the software. The MILbus coupling network of the Programmable-PBI consists of sophisticated relay circuitry which offers various coupling capabilities. The different coupling modes can be programmed by the software:

a. Transformer coupled.

b. Direct coupled.

c. Transformer coupled with resistive network emulation.

d. Isolated (Internal termination).

In the network emulation mode, the MILbus emulation circuitry emulates a transformer-coupled network without the use of MILbus couplers (using a resistor network). Thus, an external dual-redundant MIL-STD-1553 Terminal can be directly connected to the module.

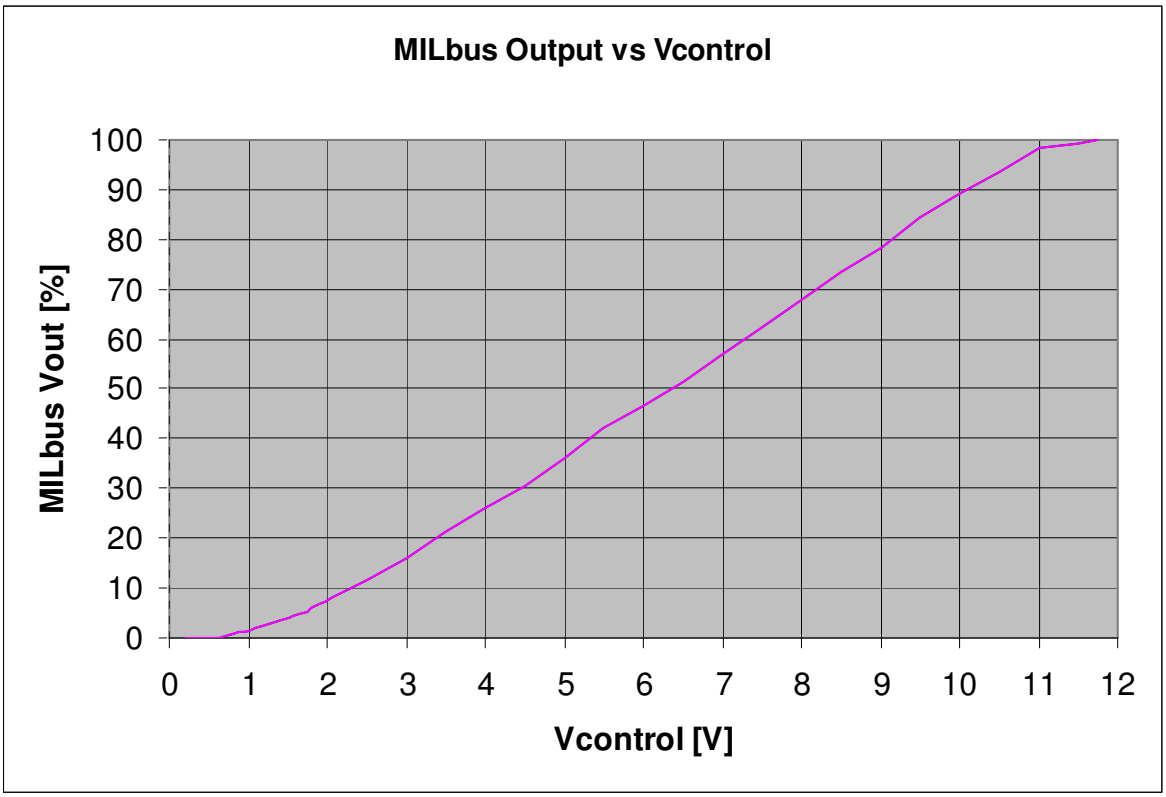
The diagram on the next page shows the typical MILbus output amplitude function dependent on the voltage on the Vcontrol Input. The Vcontrol input follows the following formula

Vcontrol = 2.56 x 5V x (Input Value / 256)

The **Input Value** in this formula is the digital eight bit value (0..255) written to the onboard digital to analog converters. The 100% value depends on the transceiver type, the coupling mode and the bus termination. A typical value is 22Volts for a transformer coupled stub terminated with 70 Ohm.

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Figure 3.6.1-1 MILBus Output vs Vcontrol



3.6.2 Standard –PBI MIL-STD-1553 Features

The Standard-PBI contains one or two dual redundant MIL-STD-1553 channels which each comprises a dual-redundant transceiver, a dual bus coupling transformer and the coupling relays. The MIL-STD-1553 trapezoidal dual transceiver has a fixed output amplitude on the MILbus.

The MILbus coupling network of the Standard-PBI consists of a reduced relay circuitry which offers the following coupling capabilities:

a. Transformer coupled.

b. Direct coupled.

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4. TECHNICAL DATA

PCI Interface:	Fully compatible with PCI Standard (Revision 2.1) 5V card, 33Mhz, 32bit operation Clock speed up to 33MHz with no wait states Supports burst operation on PCI for efficient data transfer Supports fast back-to-back transactions One interrupt output to PCI bus. Full PCI-Bus master capability.
ASP Section:	One 64bit RISC Processor IDT-79RV4640, with a core speed of 150 MHz and a external bus speed of 50 MHz, Implements 8Kbyte of internal instruction- and 8 Kbyte of data-cache. Integrates a 64 bit integer and a 32 bit (IEEE single precision) floating point unit. Low power dissipation of max. 2W @ 3.3V
Memory:	**API1553-1** Eight Megabyte of 32 bit wide ASP local dynamic memory Eight Megabyte 32 bit wide ASP-PCI shared dynamic memory One Megabyte of 32 bit wide fast Global Static RAM shared between ASP, PCI and BIU processor. 256 Kbyte local SSRAM for BIU processor. **API1553-2** Eight Megabyte of 64 bit wide ASP local dynamic memory expandable to 64 MB. Eight Megabyte 64 bit wide ASP-PCI shared dynamic memory expandable to 64 MB. Two Megabyte of 32 bit wide fast Global Static RAM shared between ASP, PCI and BIU ‘ processors (upgradeable to 16 Mbyte) Two times 256 Kbyte local SSRAM for BIU’ processors

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BIU-Section:	32 bit RISC Processor ARM-SA-110-CA with a core speed of 200MHz, an external bus speed of 50MHz,16kbyte of internal instruction and 16Kbyte of data-cache, low power dissipation of max 0.9W @ 2.0V. Large (20000 gates) programmable Gate Array implements the 1553 Encoder / Decoder functionality and all BIU specific hardware.
Encoder:	For each BIU one Manchester Encoder with Parity generator and error injection. - Single implementation with bus switching logic (not redundant) - Response time support via eight bit timer with 250ns resolution **Error Injection:** - Parity error on selected word - SYNC pattern definable on half bit basis on selectable word - Manchester stuck at low or high error in selectable word and bit position - Gap error between selected words from 0.5 to 7.5 µs in 0.5µs steps - Bitcount error on selected word +/- 3 bits
Decoder:	For each BIU one Manchester Decoder with Parity checker and error detection. - Single implementation with bus switching logic (not redundant) - Full error detection and indication. - Interword gap timer with 250ns resolution (nine bit).

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<table>
<tr><td>Time Tagging:</td><td>IRIG B Time Tag

For absolute time tagging a special time code processor implements an IRIG-B decoder. If no external IRIG-B source is available a time code in IRIG B like format is generated and can be used to synchronize multiple boards or modules.

Decoder:
Resolution : 1 µs
Width: 1 Year (46 Bit)
Signal Waveform: Amplitude modulated sinewave or square wave
Modulation Ratio: 3:1 to 6:1
Input Amplitude: 0.5V_{p-p} to 5V_{p-p}
Input Impedance: > 10k Ohm
Coupling: AC coupled
Time Jitter: +/- 5 µs (typical, module to module) depending on input signal quality
Lock time: 1 to 5 seconds depending on input signal quality

Encoder:
Format: AIM Standard (based on IRIG B format)
Absolute Accuracy: +/-50ppm
Signal Waveform: Amplitude modulated square wave
Output Amplitude: 0.5V_{p-p} to 3V_{p-p} at 2kOhms Load
Carrier Frequency: 1kHz +/-50ppm</td></tr>
<tr><td>Gap and Response time measurement</td><td>For relative response and intermessage gap measurement (<=100µs) an internal timer is used with 250ns resolution.</td></tr>
<tr><td>Maintenance:</td><td>Except for the Emergency Boot Monitor Program the BIU firmware, ASP driver software and hardware configuration data for the programmable logic is downloaded via the PCI Bus or the RS-232 maintenance and debug interface.</td></tr>
<tr><td>Bus Front end:</td><td>The interface specific components are located on a Physical BusInterface (PBI) daughterboard. One dual-redundant transceiver per BIUisimplemented. Both transceivers and couplings are individually</td></tr>
</table>

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	controllable. Two different PBIs are available
Programmable-PBI:	Programmable Output Voltage: appr. 2 to 22 Volts pp transformer coupled into 70 OHM. Programmable Bus Coupling options: - Transformer coupled. - Direct coupled. - Transformer coupled with on-board network emulation. - Isolated.
Standard-PBI:	Fixed Output Amplitude: appr. 22 Volts pp transformer coupled into 70 OHM Programmable Bus Coupling options: - Transformer coupled. Direct coupled.
Connectors:	Two standard DSUB connectors, located on the PBI One 9-pin DSUB connector for the Mil-Bus Signals One 15-pin DSUB connector for the Triggers and the IRIG signals Bus : MIL-STD-1553 transformer or direct coupled stub connections. Emulates a 70 Ohm transformer coupled network stub if programmed accordingly (programmable PBI only) Trigger In: TTL-Input, 1.5 K Pulldown and 220pf EMV capacitor. Rising Edge sensitive, Pulsewidth > 75ns Trigger Out: TTL- Output with 82 Ohm series resistor, 220pf EMV capacitor, High Pulse width strobe, 250ns duration. IRIG-IN: AC-coupled appr. 10Kohm, 220pf EMV capacitor. 0.5 to 5.0 Vpp input voltage IRIG-OUT: DC-coupled appr. 250 Ohm, 220pf EMV capacitor
Dimensions:	**API1553-1** PCI standard 'SHORT CARD', 174.6mm x 106.7mm. **API1553-2** PCI standard 'LONG CARD', 312.0mm x 106.7mm.
Supply Voltage:	Standard PC – Supply 5.0V +/- 5%, +/-12 Volt +/- 5%

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<table>
<tr><td>Power (typical):</td><td>
<table>
<tr><th></th><th></th><th>API1553-2</th><th>API1553-1</th></tr>
<tr><td>5V :</td><td>Idle:</td><td>12.5 Watts</td><td>7.5 Watts</td></tr>
<tr><td></td><td>Operating:</td><td>15.0 Watts</td><td>10.0 Watts</td></tr>
<tr><td>12V:</td><td>Idle:</td><td>1.0 Watts</td><td>0.5 Watts</td></tr>
<tr><td></td><td>Operating:</td><td>4.0 Watts</td><td>2.0 Watts
(50% Transmit)</td></tr>
</table>
Note: Less than 20 mA is drawn from the -12V supply which is typically weak on standard desktop or portable PC's.
</td></tr>
<tr><td>Weight:</td><td>API1553-1 appr. 250g
API1553-2 appr. 400g</td></tr>
<tr><td>Temperature:</td><td>0 to +45°C. Standard Operating
-15 to +60°C Extended Temperature
-40 to +85°C Storage.</td></tr>
<tr><td>Humidity:</td><td>0 to 95% (non condensing)</td></tr>
</table>

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5. NOTES

5.1 Acronyms

ADC	Analog to Digital Converter
ALBI	ASP Local Bus Interface
API	AIM PCI I-Architecture
ARM	Advanced RISC Machine
ASP	Application Support Processor
BIP	Bus Interface Processor
BIU	Bus Interface Unit
DAC	Digital to Analog Converter.
DRAM	Dynamic Random Access Memory
EDO	Enhanced Data Output
EEPROM	Electrically Erasable and Programmable Read Only Memory
EPROM	Erasable Programmable Read Only Memory
IRIG	Inter Range Instrumentations Group
IRIG B	Inter Range Instrumentations Group Time code Format Type B
LCA	Logic Cell Array (XILINX - Programmable Gate Array)
LED	Light-emitting Diode
MIL-STD	Military Standard
PBI	Physical Bus Interface
PC	Personal Computer
PROM	Programmable Read Only Memory
PCI	Peripheral Component Interconnect
PSC	PCI and System Controller
RAM	Random Access Memory
RISC	Reduced Instruction Set Computer
RS232	Hardware Interface Protocols
RTPTP	Remote Terminal Production Test Plan
SIMM	Single Inline Memory Module
SRAM	Static Random Access Memory
SSRAM	Synchronous Static Random Access Memory
TCP	Time Code Processor
UART	Universal Asynchronous Receiver and Transmitter
FLASH	Page oriented electrical erasable and programmable memory
I/O	Input / Output

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