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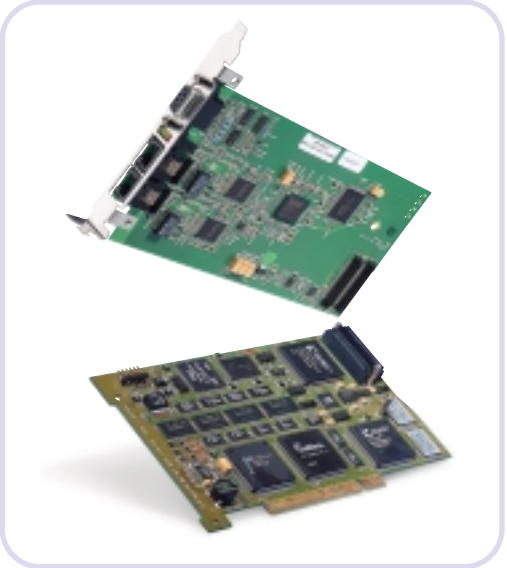
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data sheet

API-FDX-2

Two Port AFDX Test, Simulator and Monitor Module for PCI







Avionics Databus Solutions

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product guide

API-FDX-2

Two Port AFDX Test, Simulator and Monitor Module for PCI

General Features

The API-FDX-2 is one of AIM's new generation intelligent AFDX interface modules offering full function test, simulation, monitoring and analyser functions for AFDX (Avionics Full Duplex Switched Ethernet) networks. The API-FDX-2 PCI module provides two AFDX ports being configured as two single or one dual redundant ports each implementing a 100Mbit Full Duplex Ethernet interface.

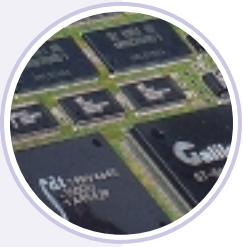


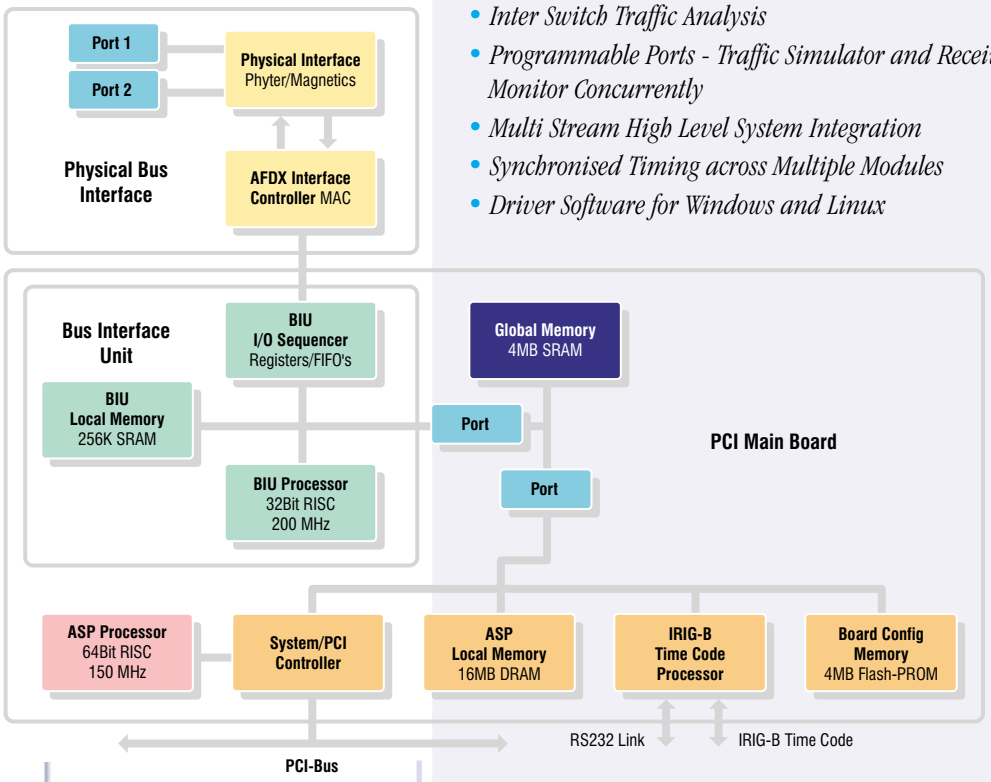
Ports can operate concurrently in Traffic Simulator or Receiver/ Monitor modes with support for AFDX port related Frame Statistics. Virtual Link (VL) packet capturing and monitoring features are complimented with powerful triggering and filtering capabilities.

The API-FDX-2 uses AIM's field proven 'Common Core' hardware design utilising multiple RISC processors, an on board Application Support Processor (ASP), scalable memory and an IRIG-B Time Code Decoder/ Processor. An AFDX specific Physical Bus Interface (PBI) piggy back board implementing two full duplex ports is used for connection to AFDX networks.

The API-FDX-2 module is available with the optional fdXplorer, the AFDX Network Analyser Software and the ParaView, Parameter Visualiser Software for Windows.

- *Test & Verification of 'End Systems'*
- *'Switch' Testing*
- *Monitoring of traffic between 'End Systems' & 'Switch'*
- *Inter Switch Traffic Analysis*
- *Programmable Ports - Traffic Simulator and Receiver/ Monitor Concurrently*
- *Multi Stream High Level System Integration*
- *Synchronised Timing across Multiple Modules*
- *Driver Software for Windows and Linux*





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Traffic Generation

The API-FDX-2 provides real time traffic generation on both ports concurrently. Transmitter operation allows users to fully programme all fields of the AFDX Frame including the Virtual Link Identifier, MAC Source Address, IP Structure, UDP Structure, Payload and Sequence number. Two modes of transmit sequencing are supported, these being Generic / Replay and UDP Port oriented shaped Transmissions. Users can programme Payload Data with User Defined or Fixed Data. Inserting the Time Tag in the Payload Data provides an elegant solution to measure frame latency delays through the network. Synchronisation of transmissions across multiple ports is achieved by using Strobe Inputs/Outputs.

- *Programmable Timing & Sequencing of Frames*
- *Physical Error Injection - CRC, Gap, Size, Alignment*
- *Logical Error Injection on Layers 2, 3, 4*
- *Timing Error Injection - Violation of Bandwidth Allocation Gap (BAG)*
- *Autonomous Dynamic Data Generation*
- *UDP Port Simulation with Traffic Shaping & Sequence Numbering*
- *On-board support for sampling and queuing ports*

UDP / VL Receive Mode

The API-FDX-2 module ports can be configured to work in UDP / VL oriented receive mode. In this mode each UDP port has a separate buffer queue. Received frames are stored with frame headers containing time tag and status information. Frame header information can be stored and payload data optionally discarded for the testing of Switches and the complete network. With the Traffic shaping verification enabled, any violations are reported as errors in related frame headers

- *VL oriented Filtering*
- *Second Level Filtering on Generic Frame Parameter*
- *Time Stamping of Received Packets with extended IRIG-B time code (1µs)*
- *Physical Error detection, Frame Level - CRC, Gap, Size and Alignment*
- *AFDX Specific Error Detection*
  - *Traffic Shaping Verification*
  - *Verification of MAC, IP and UDP Headers*
  - *VL oriented Integrity Checking*





Chronological Receive Mode
(Monitor Mode)

The API-FDX-2 module ports can be configured in Chronological Receive Mode to sequentially receive frames and store them in a circular buffer. The payload data can be discarded to optimise the use of the buffer for frame capture and analysis. Powerful Filtering, Triggering, Complex Triggering and Capture Modes allows users to select only the frames, data and errors of interest. Monitor Mode also provides activity monitoring and statistics for each VL recorded by the API-FDX-2 module. The interface modules report the number of frames received and the number of errors detected globally and in VL orientated format.

- *VL Orientated Receive and Filtering*
- *Second level filtering on Generic Frame Parameters*
- *Chronological Monitor with Time Stamping to 1µs*
- *Massive on-board Monitor Buffer*
- *Inter frame Gap time measurements with 40 nsec resolution*
- *Comprehensive Triggering / Filtering / Capturing*
- *Programmable Data Capture Modes - Trace after Trigger & Recording*
- *Physical Error Detection - CRC, Gap, Size and Alignment*
- *AFDX Specific Error Detection*

Application Support Processor

The 150 MHz Application Support Processor (ASP) provides unique on-module processing functions typically provided by host PC processing systems.

Operational features include:

- *IP and UDP layer of the AFDX protocol*
- *Driver Software Execution on the board*
- *Control of RS232C debug Port for Firmware Updates*
- *Dynamic Data Generation*
- *Loop / Pollution between Rx and 1 Tx port*
- *Automatic Test Sequence Generation*
- *Program using Real Time operating systems*

IRIG-B Time Code Decoder

An on board IRIG-B Time Code decoder and generator allows synchronisation of multiple AFDX ports using multiple API-FDX-2 modules. Modules can be daisy chained using an external IRIG-B time source or the on-board Time code generator of one module as the reference for accurate correlation of data across multiple AFDX ports.

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Two Port AFDX Test, Simulator and Monitor Module for PCI

AIM Office Contacts:

AIM GmbH
Sasbacher Str.2
79111 Freiburg
Germany
Tel: +49 761 45 22 90
Fax: +49 761 45 22 93 3
email: sales@aim-online.com

Vertriebsbüro München
Terofalstrasse 23 a
80689 München
Germany
Tel: +49 89 70 92 92 92
Fax: +49 89 70 92 92 94
email: salesgermany@aim-online.com

AIM UK
Cressex Enterprise Centre
Lincoln Road
High Wycombe
Bucks, HP12 3RB
UK
Tel: +44 1494 446844
Fax: +44 1494 449324
email: salesuk@aim-online.com

AIM USA
69 Ginger Woods Road
PO Box 338
Valley, NE 68064
USA
Tel: 1-866-AIM-1553
1-866-AIM-A429
Fax: 1-402-359-5410
email: salesusa@aim-online.com

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Physical Bus Interface

The API-FDX-2 module has one AFDX specific Physical Bus Interface piggy back board installed. The PBI comprise:

- *Customised Media Access Controllers (MAC's) implemented in FPGA optimised for AFDX*
- *2 MByte Burst Buffer*
- *Physical Interface and Magnetics (COTS)*
- *8-socket Network Interface connectors - RJ45*
- *Trigger, Strobe and Time Code I/O connector*
- *Status LED's*

Driver Software Support

The API-FDX-2 module is supplied with an Application Programming Interface (API) and Drivers compatible with Windows and Linux.

Technical Data

Sub-System Interface: PCIbus Master & Slave (Revision 2.1, June, 1995)

Processors: One 32-bit, ARM 200MHz RISC Processor.
One 64-bit, MIPS 150MHz RISC Processor

Memory: 4 MBytes Global RAM, 16 MBytes ASP RAM

Encoder/Decoder: Two Ethernet MAC's

Time Tagging: 46 bit absolute IRIG-B Time with 1μsec resolution
Inter Frame Gap generation and measurement with 40 nsec resolution

Physical Bus Interface (PBI):
One Physical Bus Interface (PBI) daughter board,Two full duplex AFDX ports

Connectors:

- *PCI back plane connector.*
- *2 x 8 way RJ45 connectors, one per AFDX port*
- *1 x 9 way D-Sub connector (female) for Time Code and Trigger I/O*

Dimensions: 175 x 107 mm "short length" Standard PCI Format

Power Consumption: Typical 12 Watts (operating)

Operating Temp. Range:
Standard: 0°C...+55°C ambient. Extended: -15°C...+60°C ambient

Storage Temp. Range: -40°C ... +85°C ambient

Humidity: 0 to 95% non-condensing

Ordering Information

API-FDX-2
Two Port, PCI to AFDX Interface:
Traffic Simulator, Receiver and Chronological Monitor
Including IRIG-B Time Code Decoder and Generator
4 MByte Global RAM, 16MByte ASP RAM

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