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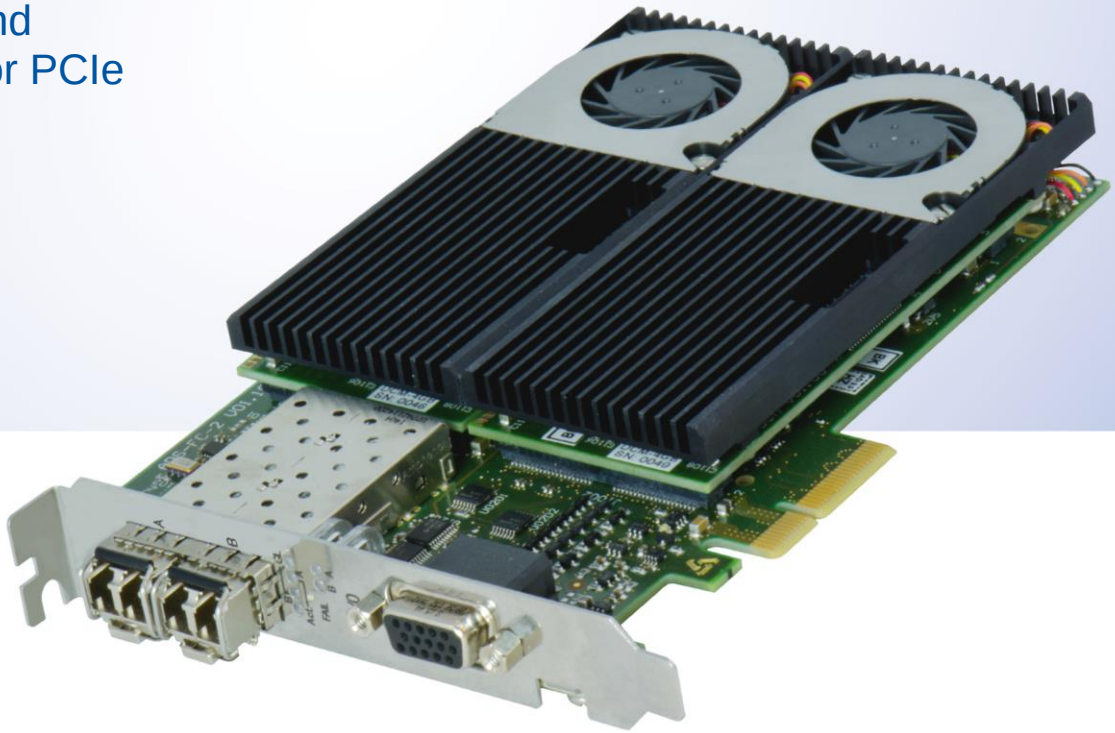
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Avionics Databus Solutions

APS-FC-2

2 Port 4GFC Fibre Channel Test, Simulator and Monitor Module for PCIe



Hardware Manual

V01.10 Rev. A
March 2019

www.aim-online.com

APS-FC-2

Two Port 4GFC Fibre Channel Module for PCIe

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V01.10 Rev. A
March 2019

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01.10 Rev A	19.03.2019	Marco Maier	Layout update, added Technical Data

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1 INTRODUCTION

1.1 General

This document comprises the Hardware User's Manual for the APS-FC-2 PCIe Card, consisting of the APS-FC-2 electronic module. The document covers the hardware installation, the board connections, a general description of the hardware architecture and the technical data of the APS-FC-2. For programming information please refer to the according documents listed in the 'Applicable Documents' section.

The APS-FC-2 is AIM's new high performance intelligent PCIe module offering two ports with full function test, simulation, monitoring and analyser functions for Fibre Channel networks. The APS-FC-2 is a powerful State-of-the-Art 4-lane PCIe 2.0 compliant board with a maximum bandwidth of up to 2000MByte/s concurrently in each direction. The architecture of the APS-FC-2 provides a Dual-Core Processor for each port and dedicated DDR3 RAM for handling Receiver and Transmitter tasks. Each port provides 4GB of low-power DDR3 RAM, summarizing to 8GB for the complete 2-Port module. This separation of the processing capabilities and On-Board RAM per port makes each port operating independent from the other port. Two high performance FPGAs implementing the customized Fibre Channel Interfaces enables the board to analyse incoming and modify outgoing data in real time.

The ports can operate concurrently in Traffic Simulator or Receiver/ Monitor modes with support for port related Frame Statistics. The TAP mode provides a possibility of monitoring traffic between two Fibre Channel ports without interacting to the attached Ports. Source or destination ID packet capturing and monitoring features are complimented with powerful triggering and filtering capabilities. Supported Fibre Channel Network Topologies are Point-to-Point, Switched Fabric and Arbitrated Loop. Service Classes 1, 2 and 3 are fully supported, Link Level Parameters are user-definable. 4GB DDR3 RAM is provided for each port to implement large receive buffers and complex transmit scenarios onboard.

The flexible frontend implementation allows the user to select the Fibre Channel Network Speed of 1 to 4 GFC by software command. The APS-FC-2 module provides two Fibre Channel ports implementing either an optical or electrical full duplex interface. The SFP cage makes it suitable for different media types as optical or electrical network technologies.

A free wheeling IRIG B Time Code Decoder is implemented on the APS-FC-2 boards to satisfy the requirements of 'multi-channel time tag synchronization' on system level.

1.2 How This Manual is Organized

This APS-FC-2 Hardware Manual is comprised of the following sections.

Section 1 - *INTRODUCTION* - contains an overview of this manual.

Section 2 - *INSTALLATION* - describes the steps required to install the APS-FC-2 device, and connect the device to other external interfaces FC network, IRIG-B, and triggers.

Section 3 - *STRUCTURE OF THE APS-FC-2* - describes the physical hardware interfaces on the APS-FC-2 using a block diagram and a description of each main component

Section 4 - *TECHNICAL DATA* - describes the technical specification of the APS-FC-2.

1.3 Applicable Documents

The following documents shall be considered to be a part of this document to the extent that they are referenced herein. In the event of conflict between the documents referenced and the contents of this document, the contents of this document shall have precedence.

1.3.1 Industry Documents

ANSI INCITS 373-2003
Fibre Channel – Framing and Signalling

INCITS TR-42-2007
Fibre Channel Avionics Environment Upper Layer Protocol (FC-AE-1553)

INCITS TR-41-2006/AM1-2008
Fibre Channel Avionics Environment Anonymous Subscriber Messaging / Amendment 1 (FC-AE-ASM)

INCITS 356-2002 (R2007)
Fibre Channel Audio Video (FC-AV)

SAE AS5653
High-Speed Network for MIL-STD-1760

IRIG-B Standard 200-4
Timing Committee, Telecommunications and Timing Group, Range commanders council

PCI Express Base Specification; PCI-SIG
Revision 2.0a

1.3.2 Product Specific Documents

AIM - Reference Manual APS-FC-2 Application Interface Library
Detailed description of the programming interface between the PC and the onboard driver software.

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2 INSTALLATION

2.1 Preparation and Precaution for Installation

The APS-FC-2 features full PCI **Plug-and Play** capability. There are no jumpers or switches on the board which have to be modified by the user.

It is recommended to use a wrist strap for any installations. If there is no wrist strap available, then touch a metal plate on your system to ground yourself and discharge any static electricity during the installation work.

2.2 Cooling Requirements

Caused by the power dissipation, the Board gets warmed up and needs a continuous air flow to avoid overheating. Therefore the PC where the APS-FC-2 is installed to, should be equipped with a separate well working and continuously running air flow system for the PCIe-Slots.
In case of doubt, an additional Fan must be installed for a continuous air flow to the board.

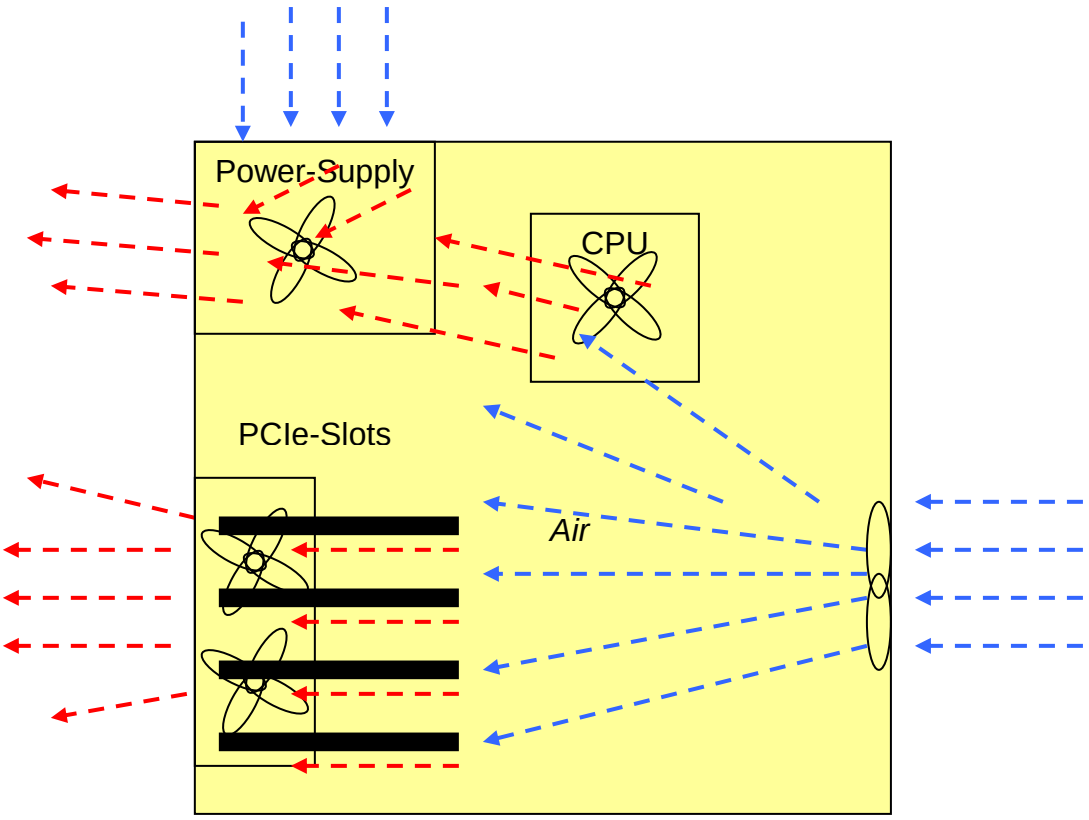


Figure 2.2.1 APS-FC-2 Cooling Requirements

2.3 Installation Instructions

The following instructions describe how to install the APS-FC-2 module in your system. Please follow the instructions carefully, to avoid any damage on the device.

▶ To Install the APS-FC-2

1. Shutdown your system and all peripheral devices.
2. Unplug the power cord from the wall outlet. (Inserting or removing modules with power applied may result in damage to module devices).
3. Remove the system cover to gain access to the system slots.
4. Find a free peripheral slot in your system with suitable size for APS-FC-2 card
   Note: The APS-FC-2 is a 4-Lane PCIe Card. This means, the card mechanically fits at least in a 4-Lane PCIe Slot, but can also be plugged into a slot with a higher lane count (e.g. 8-Lane ore 16-Lane). Downward Compatibility to 1-Lane Host Slots depends on the Host Slot mechanics, but is fully supported by the module.
   Note: In some PC systems, there are PCIe Slots specially dedicated for use as graphic adapter slot. These slots are not suitable to host the APS-FC-2.
5. Align the APS-FC-2 card slot connector with the PCIe expansion slot and gently lower the card into the free slot. Secure the card to the expansion slot with the screw you removed from the metal plate.
6. Replace the cover of your system.
7. Connect the system to the power source. Turn on the power to your system.

2.4 Connecting to other Devices

The external interfaces of the APS-FC-2 consist of the following connections:

- The Fibre Channel connections are done via standard SFP Modules, either electrical or optical.
- Trigger In/Output signals
- IRIG In/Out interface for multi-channel time tag synchronization.

Note:

- For the 1-Channel Board, Port A is on the SFP Slot next to the DSUB Connector
- For the 2-Channel Board, Port A is on the Top of the Module

2.4.1 APS-FC-1 Front Panel view

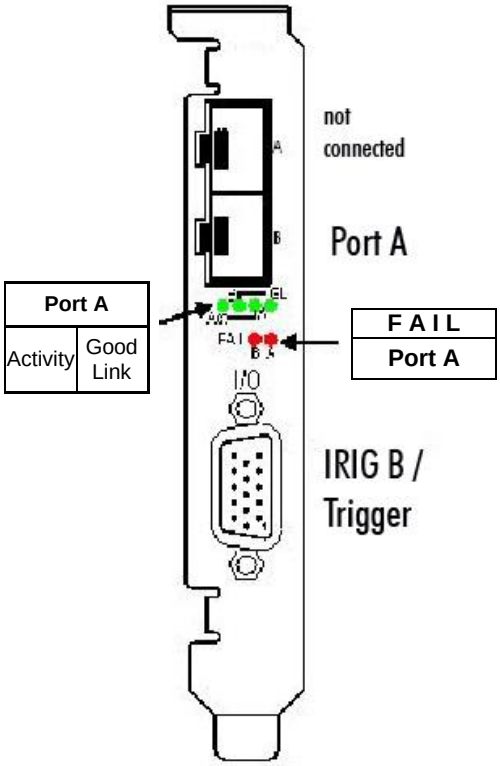


Figure 2.4.1 APS-FC-1 Front Panel View

Green LED – Status

GL – Good Link: Shows if the Port State Machine has a valid link
Act – Activity: Shows receive or transmit Port activity

Red LED – Status

FAIL – Failure: During Board power up the FAIL switches of if successfully booted
After power up the FAIL LED's show error on received frames

2.4.2 APS-FC-2 Front Panel view

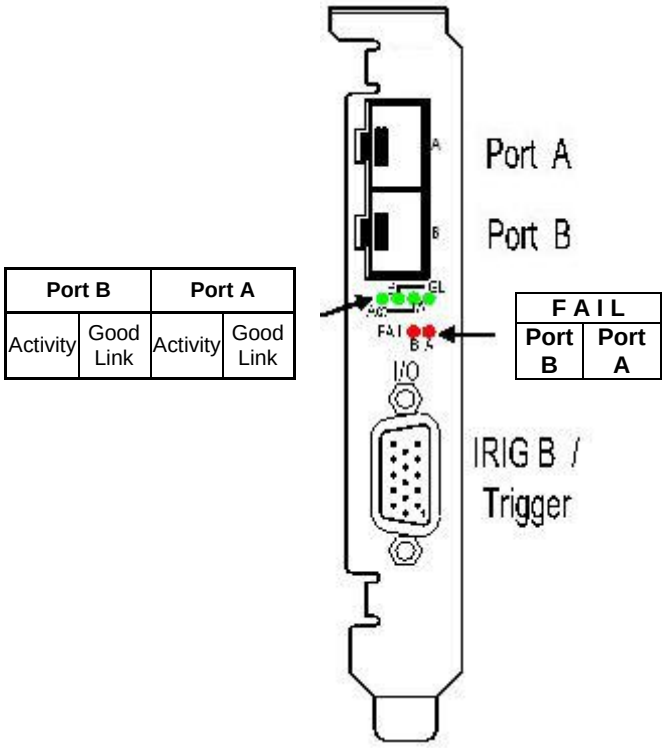


Figure 2.4.2 APS-FC-2 Front Panel View

Green LED – Status

GL – Good Link: Shows if the Port State Machine has a valid link
Act – Activity: Shows receive or transmit Port activity

Red LED – Status

FAIL – Failure: During Board power up the FAIL switches of if successfully booted
After power up the FAIL LED's show error on received frames

2.4.3 Fibre Channel Connection

Fibre Channel connections can be done with copper SFP modules, or with optical SFP modules. For coaxial SFP modules, AIM provides interface cables to connect to standard coaxial connectors on request.

2.4.3.1 Optical Fibre Channel Connection

The optical connection is done with standard optical SFP modules suitable for up to 4GFC applications. For AIM tested optical SFP modules see the appendix. The optical modules are connected via LC Duplex 62.5/125 µm optical cable.

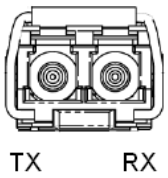


Figure 2.4.3 SFP Optical Connector

2.4.3.2 Coaxial Fibre Channel Connection

The coaxial connection is done with standard coaxial SFP modules suitable for 1GFC applications. AIM provides coaxial SFP modules as part of the delivery when ordered. Interface cable sets to standard BNC connectors are also available on request. The connector at the SFP module is of type DIN1.0/2.3 according to DIN47297.

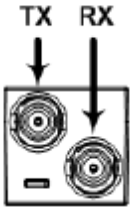


Figure 2.4.4 SFP Coaxial Connector

2.4.4 Trigger and IRIG connector for APS-FC-2

The Trigger and IRIG Connector provides an input for the onboard IRIG-decoder and an output for inter-board synchronization. The output format is an AIM specific IRIG coded signal.
The connector also provides eight discrete Trigger input/output signals, which can be used with dedicated applications. This connector is implemented by a 3 row 15pin., female DSUB Connector (mechanical same as VGA / VESA DDC Connector).

The pin assignment of the Trigger and IRIG connector is shown in Figure 2.4.4-1.

Pin No.	Type	Signal
1	I	IRIG Input
2	O	IRIG Output
3	-	Res. Do not connect
4	-	Res. Do not connect
5	Power	GND
6	-	Res. Do not connect
7	I	Trigger Input1
8	O	Trigger Output1
9	I	Trigger Input2
10	O	Trigger Output2
11	I	Trigger Input3
12	O	Trigger Output3
13	I	Trigger Input4
14	O	Trigger Output4
15	-	Res. Do not connect

Table 2-1: Trigger and IRIG Connector Pinout

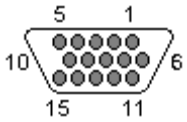


Figure 2.4.5 15 Pin DSub

Trigger In: TTL compatible Input Level and fast ESD protection diodes.
Rising Edge sensitive, Pulsewidth > 75 ns

Trigger Out: TTL- Output with fast ESD protection diodes.
High Pulse width strobe, 250 ns duration.

The IRIG-IN and IRIG-OUT signals shall be connected depending on the Timetag method used as shown below.

1. **Single AIM-Module no external IRIG-B source**

   No connection required

2. **Multiple AIM-Modules with no common synchronization requirement**

   No connection required

3. **Single or multiple AIM-Module(s) with external IRIG-B source**

   Connect external IRIG-B source to IRIG-IN and GND of all modules

4. **Multiple AIM-Modules with no external IRIG-B source internally synchronized.**

   Connect the IRIG-OUT signal and the GND of the module you have chosen as the time master to all IRIG-IN signals (including the time master).

3 STRUCTURE OF THE APS-FC-2

The structure of the APS-FC-2 board is shown in Figure 3-1. The APS-FC-2 is built with one or two Digital Core Modules (DCM), representing one or two Fibre Channel interface ports. Each DCM is comprised of three main sections:

- Processing System — Data processing (low and high level)
  Dual Core Processor running at up to 1GHz
  Dedicated 1GByte DDR3 RAM
- Front End Interface — Customized Fibre Channel Interface implemented in FPGA
  Multi-Speed Fibre Channel Transceivers
  Function dedicated DDR3 RAM (1GByte TX / 2GByte RX)
  Trigger In/Outputs
- Time Code Section — Time Code Generation
  IRIG B Encoder and Decoder

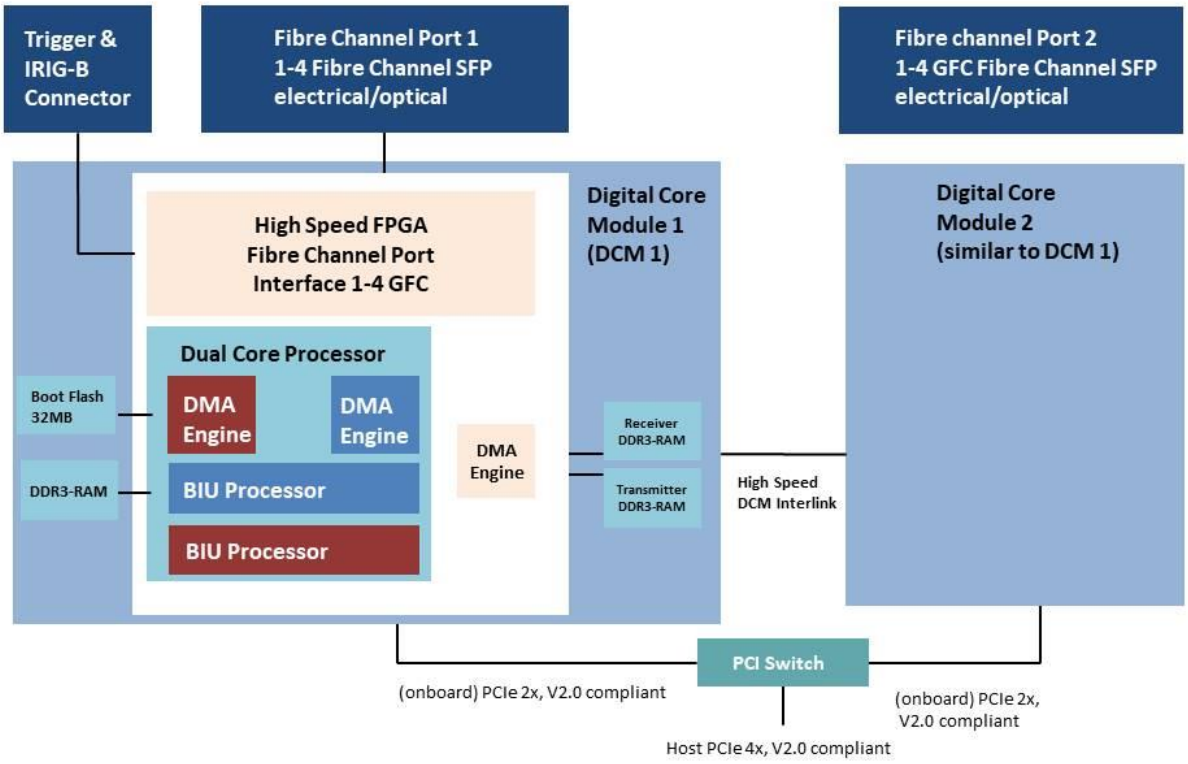


Figure 3.1 APS-FC-2 Block Diagram

3.1 Processing System

The Processing System is booted by an onboard 32MB Flash automatically after power up. It consists of a dual-core hard coded ARM Cortex® A9 processor core running at up to 1GHz per core. The Processing System has an own 1GByte DDR3 RAM directly attached to it, storing the executable code and application specific data. Due to its close attachment over several AXI Bus Interfaces to the programmable logic, the access latency is minimized.
After loading the Programmable Logic and the Operating System with the application, the processing system is responsible for the following sub-tasks.

3.1.1 Application Specific Processor (ASP)

The ASP performs the following main tasks:

- Run the application based on the Operating System
- Set up DMA and Interrupt Environment
- Establish a Host Communication together with the Host System Driver
- Relieve the Host processor and fasten up the board and expands the capability of the APS-FC-2 modules to that of a high level instrument.

3.1.2 Bus Interface Unit (BIU)

The BIU performs the following main tasks:

- Execute a Frontend and RAM power-up Selftest.
- Initialise hardware related functionality
- Communication with the FPGA Frontend Transceivers and Port State Machine

3.2 High Speed FPGA

The programmable device implements the following features.

- One fully independent Fibre Channel Ports per DCM (Digital Core Module)
- Independent DMA units for each Transmitter and Receiver
- Large On-chip FIFOs for data buffering
- Hard-wired PCIe interface to Dual Core Processor
- TCP Unit with IRIG Free Wheeling support

3.3 On-Board RAM

The On-Board RAM is used mainly for data buffering and storing the executable code. Each DCM has a total of 3 independent DDR3 RAM Ports for connecting the Shared RAM (1GByte), the Receiver RAM (2GByte) and the Transmitter RAM (1GByte). The separation of the dedicated RAM devices into RX, TX and Processing System RAM allow full performance analysing of up to 4GFC Fibre Channel networks without influence on other board operations.

3.4 Fibre Channel Port Features

The FPGA contains one Fibre Channel Port which can receive and check the Fibre Channel frames for physical errors.

The decoder in each Port receives, analyses and stores data with a data rate of up to 4Gbit per second. The gap between two frames is measured in Fibre Channel Transmission Word (4 Byte) units. Each received message is checked for errors in the Fibre Channel header and for errors on the physical bus. Every received frame is stored with a time stamp.

3.5 Time Code Processor Section

An internal timer with 10 ns resolution is implemented on the APS-FC-2 board for time stamping Fibre Channel data in IRIG-B format. The internal timer can be set by the host.

The time tag on the board is generated in the following format:

Figure 3.5.1 Binary coded Time Tag format

Time Element	Number of bits
DAYS of year	9
HOURS of Day	5
MINUTES of Hour	6
SECONDS of Minute	6
MICROSECONDS of Second	20
10 NANOSECONDS of Microsecond	7
Summary	53 bit (stored in two 32 bit words)

This comprehensive time tag information allows the APS-FC-2 a flexible, application dependent time tagging of the avionic Databus traffic.

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4 TECHNICAL DATA

PCI Interface:

Compliant to PCI Express Base Specification 2.0a
4-Lane Interface with up to 2GByte Bandwidth in each direction (up/downstream)

Note: The APS-FC-2 is a 4-Lane PCIe Card. This means, the card mechanically fits at least in a 4-Lane PCIe Slot, but can also be plugged into a slot with a higher lane count (e.g. 8-Lane ore 16-Lane). Downward Compatibility to 1-Lane Host Slots depends on the Host Slot mechanics, but is fully supported by the module.
Note: In some PC systems, there are PCIe Slots specially dedicated for use as graphic adapter slot. These slots are not suitable to host the APS-FC-2.

Memory:

A total of 4096 MB DDR3-SD RAM per DCM, summarizing to 8GB for the APS-FC-2 Dedicated RAM Ports for RX and TX functions

Processor:

Dual Core Cortex® A9 with a core speed of up to 1000 MHz

Fibre Channel Encoder:

One FC Encoder per DCM with error injection

- Service the FC Port to handle the demanded bus traffic in real time.
- Data rate of 1,0625 to 4,25 Gbit per second (1-4GFC)
- Interframe gap timer with FC Transmission Word (4Byte) resolution
  (37,64ns @1GFC).

Error Injection:

- CRC Error
- Long Frame Error
- Invalid Symbol

Fibre Channel Decoder:

One FC Decoder per DCM with time stamp and error detection

- Service the FC Port to handle the demanded bus traffic in real time.
- Data rate of 1,0625 to 4,25 Gbit per second (1-4GFC)
- time stamp for received frames
- Frame length statistic

Error Detection:

- CRC Error
- Physical bus errors (Invalid Symbol)
- Unaligned Byte

Time Tagging:

IRIG B Time Tag For absolute time tagging, a special time code processor implements an IRIG-B encoder/decoder. If no external IRIG-B source is available a time code in IRIG B format is generated and can be used to synchronize multiple boards or modules.

IRIG Decoder:

Resolution:	10 ns
Width:	1 Year (46 Bit)
Signal Waveform:	Amplitude modulated sine wave
Modulation Ratio:	3:1 to 6:1
Input Amplitude:	$0.5V_{p-p}$ to $5V_{p-p}$
Input Impedance:	> 10k ohm
Coupling:	AC coupled
Time Jitter:	+/- 500ns (depending on the input signal quality)
Lock time:	< 5s Free wheeling accuracy after 10 Minutes < 1ppm (assuming input signal accuracy better than 50ppm)

IRIG Encoder:

Format:	AIM Standard (based on IRIG-B122 format)
Absolute Accuracy:	+/-50ppm (standard Oscillator)
Output Amplitude:	~ 3 $V_{p-p,}$ High voltage level
Modulation Ratio:	~ 3:1
Carrier Frequency	1kHz +/-50ppm

Physical Bus Interface: The Board implements one/two Physical Ports for 1-4GFC Fibre Channel network

APS-FC-2 Connectors: Optical SFP: LC Ethernet connector
Electrical SFP: Coaxial DIN1.0/2.3 Connector According to DIN47297

Trigger Connector: 3 row 15pin., female DSUB Connector

Trigger In: TTL compatible Input Level and fast ESD protection diodes. Additional Varistors nearby connector to suppress peaks of glitches.
Rising Edge sensitive, Pulsewidth > 75 ns

Trigger Out: Output with TTL Level and fast ESD protection diodes. Additional Varistors nearby connector to suppress peaks of glitches. High Pulsewidth strobe, 500 ns duration.

IRIG-IN: AC-coupled Input resistor ~ 10KΩ, with high speed EMV Varistor. 0.5 to 5.0 Vpp input voltage

IRIG-OUT: AC-coupled Output resistor ~ 51Ω, with high speed EMV Varistor. ~ 4.5 Vpp output voltage

Dimensions: PCIe standard, 174.6mm x 106.7mm

Supply Voltage: PC – Supply 3.3V+/- 5%, 12.0V+/- 5%

Power Consumption:

APS-FC-1:

+3.3V	Idle:	5.7W
	Operating (1GFC)	5.8W
	Operating (4GFC)	6W
+12V	Idle:	3.6W
	Operating (1GFC)	3.8W
	Operating (4GFC)	3.9W

APS-FC-2:

+3.3V	Idle:	11W
	Operating (1GFC)	11.3W
	Operating (4GFC)	11.4W
+12V	Idle:	6W
	Operating (1GFC)	6.9W
	Operating (4GFC)	7.2W

Temperature:

0	to	+45°C	Standard Operating
-40	to	+85°C	Storage

Note: To avoid overheating, a continuous air flow must be provided by the host system. See Chapter 2.2, Cooling Requirements

Humidity: 0 to 95% non condensing

Weight: APS-FC-2: appr. 250g (without SFP Modules)

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5 NOTES

5.1 Acronyms

ADC	Analog to Digital Converter
ARM	Advanced RISC Machine
ASP	Application Support Processor
BIP	Bus Interface Processor
BIU	Bus Interface Unit
BM	Bus Monitor
BSP	Board Software Package
DAC	Digital to Analog Converter.
DDRRAM	Double Data Rate Random Access Memory
DRAM	Dynamic Random Access Memory
EEPROM	Electrically Erasable and Programmable Read Only Memory
FC	Fibre Channel
FLASH	Page oriented electrical erasable and programmable memory.
FPGA	Field programmable gate array
FRU	Field Replaceable Unit
FW	Firmware
GFC	Gigabit Fibre Channel, measures the speed of a FC link
GTP	Gigabit Transceiver
GND	Ground
IRIG B	Inter Range Instrumentations Group Time code Format Type B
I/O	Input / Output
JTAG	Joint Test Action Group (IEEE 1149.1 Boundary Scan)
LCA	Logic Cell Array (XILINX - Programmable Gate Array)
LED	Light-emitting Diode
MGT	Multi Gigabit Transceiver
MIL-STD	Military Standard
MILbus	MIL-STD-1553 bus
NTRAM	No Turnaround Random Access Memory
PBI	Physical Bus Interface
PROM	Programmable Read Only Memory
PCI	Peripheral Component Interconnect
PCIe	Peripheral Component Interconnect Express
PMC	PCI Mezzanine Card
PSC	PCI and System Controller
RAM	Random Access Memory
RISC	Reduced Instruction Set Computer
RS232	Hardware Interface Protocols
SMD	Surface Mounted Device
SoC	System on Chip
SRAM	Static Random Access Memory
SSRAM	Synchronous Static Random Access Memory
TCP	Time Code Processor
UART	Universal Asynchronous Receiver and Transmitter
XMC	PCI Express Mezzanine Card

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6 APENDIX

6.1 Certificate of Volatility for APS-FC-2

Model: APS-FC-2
Part-Number: 1D1Bx-100

Manufacturer: AIM GmbH
Sasbacher Str. 2
D-79111 Freiburg / Germany

Volatile Memory				
Does the item contain volatile memory (i.e., memory whose contents are lost when power is removed)? ☒ Yes ☐ No				
Description of used volatile memory:				
Type: DDR3-RAM	Size: 2 GByte	User Modifiable: ☒ Yes ☐ No	Function: OS Memory, Global RAM	Process to Sanitize: Power off / on (Power Cycle)
Type: DDR3-RAM	Size: 2 GByte	User Modifiable: ☒ Yes ☐ No	Function: Descriptors, TX Data	Process to Sanitize: Power off / on (Power Cycle)
Type: DDR3-RAM	Size: 4 GByte	User Modifiable: ☒ Yes ☐ No	Function: RX RAM	Process to Sanitize: Power off / on (Power Cycle)
Non-Volatile Memory				
Does the item contain non-volatile memory (i.e., memory whose contents are retained when power is removed)? ☒ Yes ☐ No				
Description of used non-volatile memory:				
Type: Serial SPI-Flash	Size: 64MByte	User Modifiable: ☐ Yes ☒ No	Function: SoC Boot	Process to Sanitize: erase
Type: Serial EEPROM	Size: 2KByte	User Modifiable: ☐ Yes ☒ No	Function: Configuration	Process to Sanitize: erase
Media				
Does the item contain media storage capability (i.e., removable or non-removable disk drives, tape drives, memory cards, etc.)? ☐ Yes ☒ No				
Test Engineer				
Name: Marco Maier		Title: Hardware Developer		Date of Certification: 20.03.19

All operating Data for handling the I/O Protocol will be stored in volatile memory only. No Transfer data is stored in Non-Volatile Memory. The Non-Volatile Memory only contains production relevant data for board personalisation, FPGA Logic or Firmware Code for the on board Microcontroller.

6.2 Certificate of Volatility for APS-FC-1

Model: APS-FC-1
Part-Number: 1D1Bx-100

Manufacturer: AIM GmbH
Sasbacher Str. 2
D-79111 Freiburg / Germany

Volatile Memory				
Does the item contain volatile memory (i.e., memory whose contents are lost when power is removed)? ☒ Yes ☐ No				
Description of used volatile memory:				
Type: DDR3-RAM	Size: 1 GByte	User Modifiable: ☒ Yes ☐ No	Function: OS Memory, Global RAM	Process to Sanitize: Power off / on (Power Cycle)
Type: DDR3-RAM	Size: 1 GByte	User Modifiable: ☒ Yes ☐ No	Function: Descriptors, TX Data	Process to Sanitize: Power off / on (Power Cycle)
Type: DDR3-RAM	Size: 2 GByte	User Modifiable: ☒ Yes ☐ No	Function: RX RAM	Process to Sanitize: Power off / on (Power Cycle)
Non-Volatile Memory				
Does the item contain non-volatile memory (i.e., memory whose contents are retained when power is removed)? ☒ Yes ☐ No				
Description of used non-volatile memory:				
Type: Serial SPI-Flash	Size: 32MByte	User Modifiable: ☐ Yes ☒ No	Function: SoC Boot	Process to Sanitize: erase
Type: Serial EEPROM	Size: 1KByte	User Modifiable: ☐ Yes ☒ No	Function: Configuration	Process to Sanitize: erase
Media				
Does the item contain media storage capability (i.e., removable or non-removable disk drives, tape drives, memory cards, etc.)? ☐ Yes ☒ No				
Test Engineer				
Name: Marco Maier		Title: Hardware Developer		Date of Certification: 20.03.19

All operating Data for handling the I/O Protocol will be stored in volatile memory only. No Transfer data is stored in Non-Volatile Memory. The Non-Volatile Memory only contains production relevant data for board personalisation, FPGA Logic or Firmware Code for the on board Microcontroller.

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