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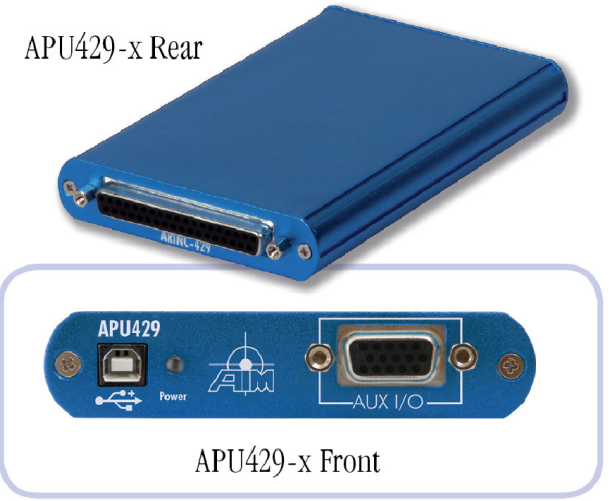
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Hardware Manual

APU429

Four/Eight/Sixteen Channel ARINC 429 Module for USB 2.0



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V02.00 Rev. C

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APU429

Hardware Manual

Four/Eight/Sixteen Channel ARINC 429 Module

for

USB 2.0

V02.00 Rev. C

December 2011

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V01.00 Rev E	March 2010	M. Maier	Technical Details: USB-Cable Small IRIG corrections
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V02.00 Rev A	December 2010	M. Maier	Board Relayout Changes New USB Connector Case dimensions IRIG coupling corrected
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1. INTRODUCTION

1.1 General

This document comprises the Hardware User's Manual for the APU429 USB2.0 module. The document covers the hardware installation, board connections, technical data and a general description of the hardware architecture. For programming information please refer to the documents listed in the 'Applicable Documents' section.

The APU429 module is a member of AIM's new family of advanced USB2.0 modules compliant to the latest USB2.0. The board runs without extra Power Supply.

On the transmit channels, the APU429 acts as an autonomously operating bus traffic simulator, supporting multiple modes of transmission sequencing. Full error injection capabilities are available, whereby the error injection is programmable individually for each channel and label. For special transmission operating modes the parity bit can be used alternatively as an additional data bit. The rise and fall time of the bus signals are individually programmable by software for each transmit channel.

For the receive channels, the APU429 provides an advanced monitor and analyzer function with unique on-board error detection, triggering and filtering capabilities. Monitor and analyzer functions are available concurrently and independent from each other. The hardware architecture provides resources to guarantee that the performance of one function is not affected by the current load of the other function. The rise and fall times of the bus signals are individually programmable for each receive channel. To adapt to different transmit speeds, the transmission rate can be varied in discrete steps between approximately 90 and 120Kbits on the high speed bus and between 11.5 and 16.0 on the low speed lines. The discrete steps are global for all channels.

The advanced architecture uses a special processor for the ARINC 429 stream. A powerful Controller and Memory Arbiter are implemented in a Field Programmable Gate Array (FPGA). The FPGA supports the interface to the application and driver software tasks running on the host computer and assists the communication for data transfer. This feature expands the capability of the APU429 module to that of a high level instrument.

A free wheeling IRIG-B Timecode Encoder/Decoder (1 ppm accuracy) is implemented on the APU429 boards to satisfy the requirements of 'multi-channel time tag synchronization' on a system level. The IRIG-B output allows the synchronization of any external module implementing IRIG-B time stamping. The card implements three trigger I/O's and 8 user-defined Discrete-I/O signals. All signals are available on off-the-shelf available D-SUB connectors.

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1.2 How This Manual is Organized

This APU429 Hardware Manual is comprised of the following sections.

Section 1 - *INTRODUCTION* - contains an overview of this manual.

Section 2 - *INSTALLATION* - describes the steps required to install the APU429 device, and connect the device to other external interfaces including ARINC 429 interfaces, IRIG-B, and triggers.

Section 3 - *STRUCTURE OF THE* APU429 - describes the physical hardware interfaces on the APU429 using a block diagram and a description of each main component

Section 4 - *TECHNICAL DATA* - describes the technical specification of the APU429.

For programming information please refer to the Reference Manual APU429 Application Interface Library.

1.3 Applicable Documents

The following documents shall be considered to be a part of this document to the extent that they are referenced herein. In the event of conflict between the documents referenced and the contents of this document, the contents of this document shall have precedence.

1.3.1 Industry Documents

USB2.0 Standard, Revision 2.0, April 2000

ARINC Specification 429-14
March 1993

1.3.2 Product Specific Documents

AIM - Reference Manual for the Application Interface Library
Detailed description of the programming interface between the Host Carrier board and the onboard driver software.

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2. INSTALLATION

2.1 Installation Instructions

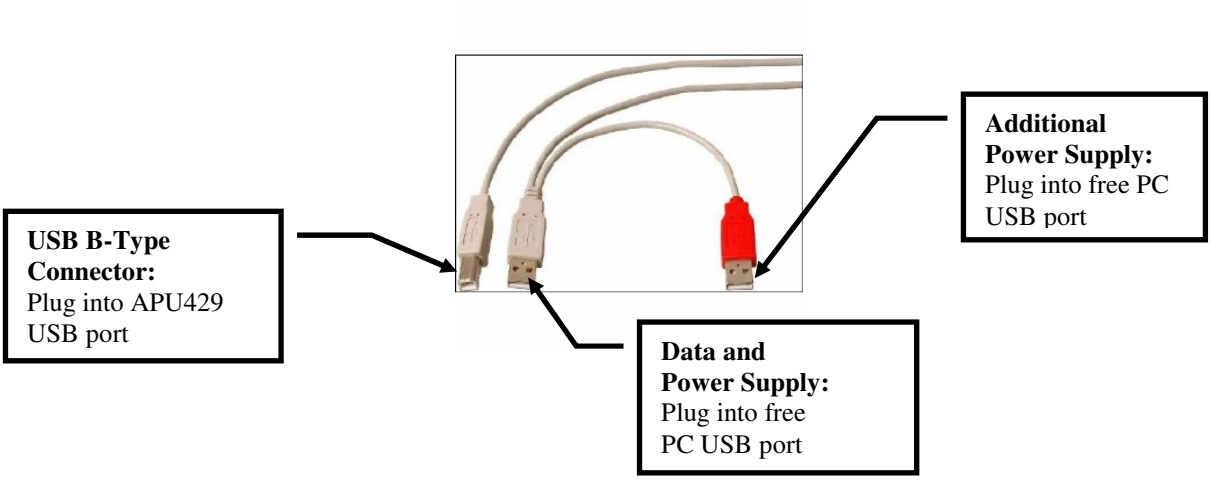
The APU429 features ***Hot Plug and Play*** capability. The APU429 may be plugged into a suitable USB2.0 port at any time with the PC in operating state or switched off.

To Install the APU429

1. Before connecting the APU429, please insert the Driver-CD and install the latest Board-Software Package. Follow the installing procedure prompted by Pop-Up window.

2. With the BSP installation the Getting Started Manual was installed too. This document describes the further installing procedure detailed. Please follow the prompted steps in this manual.

3. After successful BSP installation the PC is prepared for initial connecting the APU429 to the USB port of the Host-PC.
   First plug in the PC side of the Y-Cable. For proper operation, both ports of the Y-Cable must be plugged into free PC ports. We strongly recommend to use the provided cable for proper full performance operation. When using other cable make sure that the cable length does not exceed 1,20m.
   After this, plug in the USB B-Type Connector into the USB port of the APU429. The host PC will recognize the APU429 automatically.



4. To install the APU429 driver software correct, please follow the further installing procedure, prompted by Pop-Up window. See detailed information about this installation in the Getting Started Manual.

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5. After successful software installation and a proper APU429 detection by Host, the APU429 is listed in the system device manager and is ready for use now.
   As indicator for successful board initialization, the green LED will be switched on.

6. To remove the module from the computer, please close all software applications first. Depending on your operating system you must press the “eject or stop card” icon on your screen to disable the module before safe removal. For details, please refer to the manual of your operating system.

7. The module can now be plugged off.

8. The module can be plugged in again after a few seconds without rebooting the computer.

Note: It is recommended to plug max 2 APU Devices to one PC or Notebook. Performance Issues or insufficient power Supply may be seen if plugging more than two APU devices into one PC.
A USB hub may be used as APU port if the hub itself is directly plugged into a Notebook or PC and the hub is a “self powered device” using an own power adaptor. In this case, a maximum of 2 APU devices may be used via one USB hub.
It is not recommended to plug the hub into another hub. Power and performance issues may be the result.

2.2 Connecting to Other Devices

All signals are available at standard off-the-shelf D-SUB connectors. All ARINC signals, IRIG IN/OUT and one trigger input/output are routed to a 37 pin D-SUB connector. The AUX I/O connector contains the eight Discrete I/O lines, two further trigger input/output and also the IRIG IN/OUT lines. For Pinout description, see later in this chapter. The following two pictures show the front and rear view of the module.

Figure 2-1 APU429 Front View

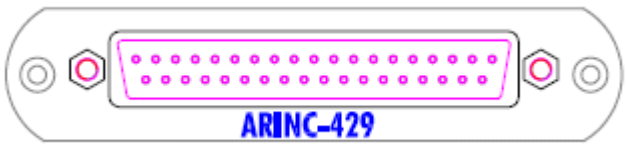
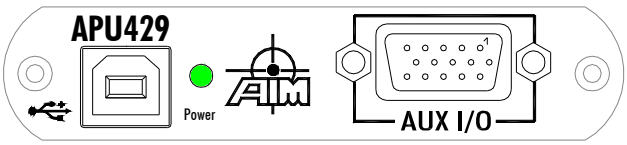


Figure 2-2 APU429 Rear View



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2.2.1 APU429 37 pin D-SUB connector

The ARINC external interface of the APU429 consists of a female 37pin D-SUB connector with a screw lock mechanism.

The interface includes the following signal/bus functionality.

- Up to 8 transmit and 8 receive ARINC 429 channels
- One Trigger In/Out signals
- IRIG In/Out interface for multi-channel time tag synchronization.

The Pinouts for the different ordering variants are displayed in the following tables.

Table 2.2.1-I APU429-4 37pin DSUB Connector Pinout

Pin	Signal Description	Pin	Signal Description
1	TX Channel 1 (True)	20	TX Channel 1 (Complement)
2	TX Channel 2 (True)	21	TX Channel 2 (Complement)
3	Reserved	22	Reserved
4	Reserved	23	Reserved
5	Reserved	24	Reserved
6	Reserved	25	Reserved
7	Reserved	26	Reserved
8	Reserved	27	Reserved
9	Trigger In 0	28	IRIG Out
10	Ground		Reserved
11	Trigger Out 0	29	IRIG In
12	Rx Channel 3 (True)	30	Rx Channel 3 (Complement)
13	Rx Channel 4 (True)	31	Rx Channel 4 (Complement)
14	Reserved	32	Reserved
15	Reserved	33	Reserved
16	Reserved	34	Reserved
17	Reserved	35	Reserved
18	Reserved	36	Reserved
19	Reserved	37	Reserved

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Table 2.2.1-II APU429-8 37pin DSUB Connector Pinout

Pin	Signal Description	Pin	Signal Description
1	TX Channel 1 (True)	20	TX Channel 1 (Complement)
2	TX Channel 2 (True)	21	TX Channel 2 (Complement)
3	TX Channel 3 (True)	22	TX Channel 3 (Complement)
4	TX Channel 4 (True)	23	TX Channel 4 (Complement)
5	Reserved	24	Reserved
6	Reserved	25	Reserved
7	Reserved	26	Reserved
8	Reserved	27	Reserved
9	Trigger In 0	28	IRIG Out
10	Ground		
11	Trigger Out 0	29	IRIG In
12	Rx Channel 5 (True)	30	Rx Channel 5 (Complement)
13	Rx Channel 6 (True)	31	Rx Channel 6 (Complement)
14	Rx Channel 7 (True)	32	Rx Channel 7 (Complement)
15	Rx Channel 8 (True)	33	Rx Channel 8 (Complement)
16	Reserved	34	Reserved
17	Reserved	35	Reserved
18	Reserved	36	Reserved
19	Reserved	37	Reserved

Table 2.2.1-III APU429-16 37pin DSUB Connector Pinout

Pin	Signal Description	Pin	Signal Description
1	TX Channel 1 (True)	20	TX Channel 1 (Complement)
2	TX Channel 2 (True)	21	TX Channel 2 (Complement)
3	TX Channel 3 (True)	22	TX Channel 3 (Complement)
4	TX Channel 4 (True)	23	TX Channel 4 (Complement)
5	TX Channel 5 (True)	24	TX Channel 5 (Complement)
6	TX Channel 6 (True)	25	TX Channel 6 (Complement)
7	TX Channel 7 (True)	26	TX Channel 7 (Complement)
8	TX Channel 8 (True)	27	TX Channel 8 (Complement)
9	Trigger In 0	28	IRIG Out
10	Ground		
11	Trigger Out 0	29	IRIG In
12	Rx Channel 9 (True)	30	Rx Channel 9 (Complement)
13	Rx Channel 10 (True)	31	Rx Channel 10 (Complement)
14	Rx Channel 11 (True)	32	Rx Channel 11 (Complement)
15	Rx Channel 12 (True)	33	Rx Channel 12 (Complement)
16	Rx Channel 13 (True)	34	Rx Channel 13 (Complement)
17	Rx Channel 14 (True)	35	Rx Channel 14 (Complement)
18	Rx Channel 15 (True)	36	Rx Channel 15 (Complement)
19	Rx Channel 16 (True)	37	Rx Channel 16 (Complement)

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2.2.2 Auxiliary I/O Connector Pin Assignment

The pin assignment for the 15 pin female HDSUB connector of the module is shown in Table 2.2.2-I.

Table 2.2.2-I 15pin HDSUB Auxiliary I/O Connector Pinout

Pin	Signal
1	IRIG In
2	IRIG Out
3	Trigger OUT 1
4	Trigger IN 1
5	GND
6	Discrete I/O 1
7	Discrete I/O 2
8	Trigger OUT 2
9	Trigger IN 2
10	Discrete I/O 3
11	Discrete I/O 4
12	Discrete I/O 5
13	Discrete I/O 6
14	Discrete I/O 7
15	Discrete I/O 8

2.2.3 IRIG Connection

The IRIG IN and OUT lines can be used to synchronize several modules to one time base.
The IRIG-IN and IRIG-OUT signals shall be connected depending on the Timetag synchronization method used as shown below.

Please Note: Although this module has two connections to IRIG IN and to IRIG OUT, always use only one of them at this module! Otherwise time synchronization cannot be guaranteed.

1. **Single AIM-Module no external IRIG-B source**

   No connection required

2. **Multiple AIM-Modules with no common synchronization requirement**

   No connection required

3. **Single or multiple AIM-Module(s) with external IRIG-B source**

   Connect external IRIG-B source to the IRIG IN and GND of all modules

4. **Multiple AIM-Modules with no external IRIG-B source internally synchronized.**

   Connect the IRIG-OUT signal and the GND of the module you have chosen as the time master to all IRIG-IN signals (including the time master).

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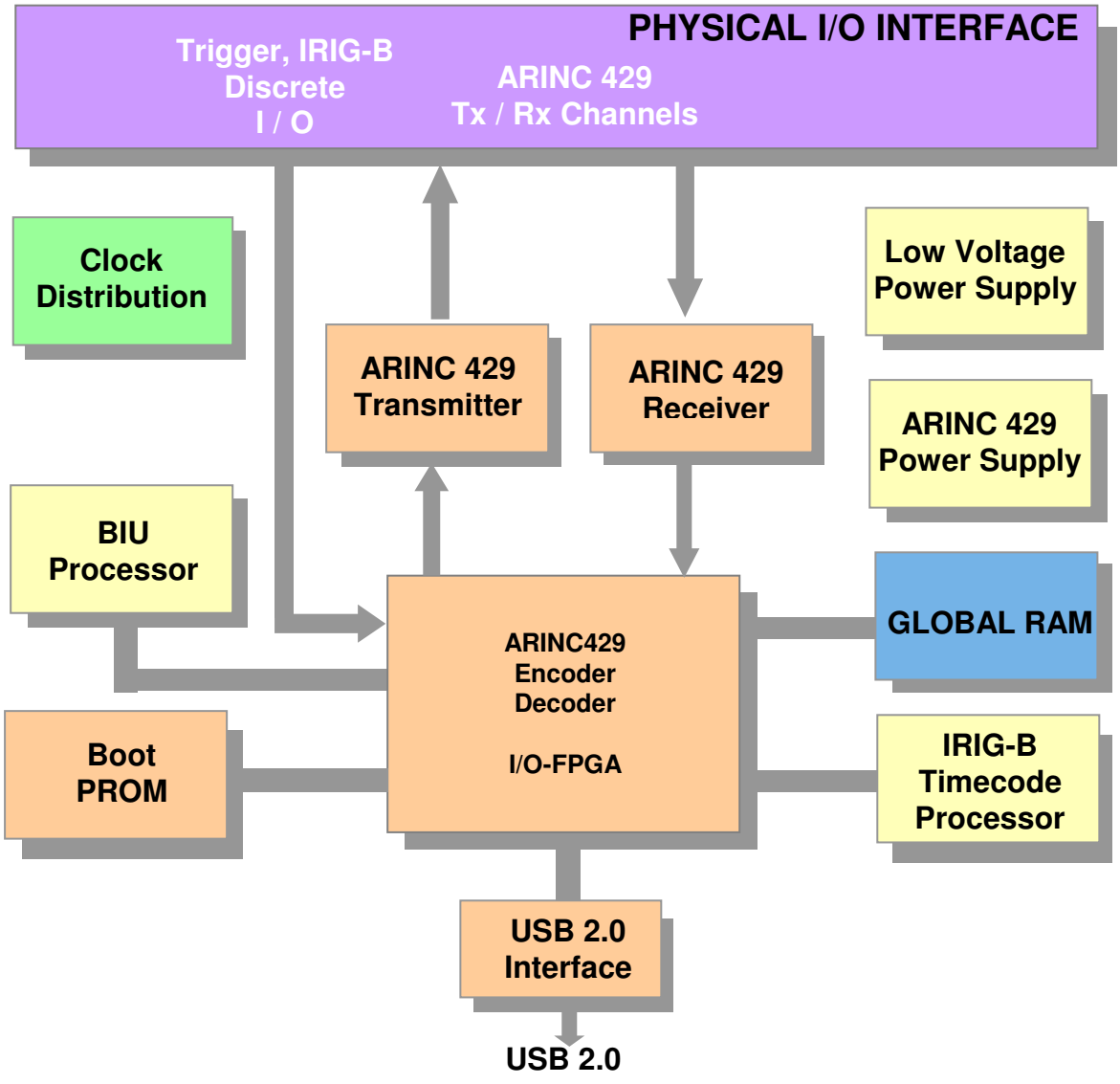
3. STRUCTURE OF THE APU429

The structure of the APU429 board is shown in Figure 3-I.

The APU429 is comprised of the following main sections:

- USB2.0 Interface
- Control and BIU-IO FPGA
- Global RAM
- BIU Processor Section
- Physical I/O interface with 4/8/16 ARINC 429 channels
- IRIG- Time Code Processor with Free Wheeling Function and Sine Wave Output
- JTAG Port for Boot-PROM Update Programming.

Figure 3-1 APU429 Block Diagram



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3.1 Control and BIU-I/O FPGA

The new common FPGA architecture of AIM includes the Interface to the USB controller and the BIU processor logic. This programmable device implements also features like the ARINC Encoders and Decoder logic, IRIG circuitry and Trigger and Discrete signals.

3.2 Global RAM

The Global RAM is shared between both BIU processors (BIP) and the Host-CardBus. The arbitration is handled by the common FPGA. The FPGA accesses the common Global RAM via a 32 bit wide data port.

3.3 Bus Interface Unit (BIU)

One Bus Interface Unit (BIU) is implemented on the module. It handles the ARINC 429 receive and transmit channels and provides the trigger signals. The control logic is implemented in the common FPGA.

3.3.1 Bus Interface Processor (BIP)

The BIU consists of an ultralow power, high performance 32bit RISC processor.

3.3.2 ARINC429 Encoder

The encoder converts the parallel data into a serial ARINC429 encoded data stream and appends the parity and the gap bits. The programmable frame times between two labels can be set in the range from 0 up to 255 ARINC429 bits.
The encoder provides the following error injection capabilities:

- Gap Error (-1 bit)
- Bitcount Error (+/- 1 bit)
- Coding Error (fixed at bit position 12)
- Parity Error (if no special transmission mode is chosen)

3.3.3 ARINC429 Decoder

The decoder converts the serial received data stream into a parallel data double word and generates an additional 16 bit report for each received label. The decoder measures the gap time between two labels for gap error detection and bus load traffic detection.

The decoder provides the following error detection capabilities:

- Gap Error Detection
- Bit count Error Detection
- Coding Error Detection
- Parity Error Detection (if no special transmission mode is chosen)

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3.3.4 External Trigger Inputs and Outputs

Three trigger inputs and three trigger outputs are provided. Filter circuitry is provided at the trigger inputs and outputs to cover EMC aspects.

3.3.5 Eight user definable Discrete I/Os

The PC-Card provides eight user definable Discrete I/O signals. Each Discrete signal can be programmed to act as input or output signal with Low Voltage TTL compatible output level. EMC aspects are covered by filter circuitry.

3.4 IRIG-B and Time Code

The main functions of the Time Code Processor (TCP) Section are:

- IRIG-B compatible Time Code Decoder
- IRIG-B compatible Encoder

3.4.1 Time Code Encoder and Decoder

The generated time code signal is an IRIG-B compatible sine wave. The time code information can be used for time-tagging and multi-channel synchronization. A new generation IRIG-B section is implemented with a free wheeling IRIG functionality. If no external IRIG signal is detected, the TCP switches automatically to the fee wheeling mode. If an external IRIG-B signal is detected in free wheeling mode, the Timetag is automatically synchronized to this external IRIG signal.

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4. TECHNICAL DATA

USB Controller Interface (UCI)

USB Specification Version 2.0 Compliant (high and full speed)
Supports USB High (480 Mb/sec) and Full (12 Mb/sec) speeds

Memory One Megabyte of 32 bit wide fast Global Static RAM shared between BIU processor and Host application

BIU-Section 32 bit RISC Processor provides low power and high performance
400 MHz core speed

Encoder Programmable Bitrate High / Low Speed (100 / 12.5 Kbit/sec)
Programmable gap between two labels in the range from 0 up to 255 ARINC 429 bits.
ARINC429-Label Bit-32 programmable as Parity or additional Data Bit

Error injection capabilities:

Gap Error	(-1 bit)
Bitcount Error	(+/- 1 bit)
Coding Error	(fixed at bit position 12)
Parity Error	(if no special transmission mode is chosen)

Decoder Valid Receive Range Transmission speed select +/- appr. 10%
ARINC429-Label Bit-32 programmable as Parity or additional Data Bit
Measurement of gap between two labels in the range from 0.0 to 58.75 bits with 0.25bit resolution.

Error detection capabilities:

Gap Error Detection
Bitcount Error Detection
Coding Error Detection
Parity Error Detection (if no special transmission mode is chosen)

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Time Tagging:

IRIG B

For absolute time tagging a special time code processor implements an IRIG-B encoder/ decoder. If no external IRIG-B source is available a time code in IRIG B like format is generated and can be used to synchronize multiple boards or modules.

Decoder:

Resolution:	1 µs
Width:	1 Year (46 Bit)
Input Signal Frequency:	1KHz +-50ppm
Signal Waveform:	Amplitude modulated sine wave or square wave
Modulation Ratio:	3:1 to 6:1
Input Amplitude:	0.5Vp-p to 5Vp-p
Input Impedance:	> 10k Ohm
Coupling:	AC coupled
Time Jitter:	+-500ns
Lock time:	< 5sec.

Free wheeling accuracy (excluding oscillator drift): <1ppm
Time to highest precision: approx. 10 Minutes

Encoder:

Format:	IRIG-B
Absolute Accuracy:	+/-50 ppm
Signal Waveform:	Amplitude modulated sine wave
Output Amplitude:	approx. 3Vp-p
Modulation Ratio:	approx. 3.2:1
Carrier Frequency:	1kHz +/-50ppm

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Connectors

USB2.0 Connector

Standard USB B-Type connector

37pol. female D-Sub

ARINC429:	Up to Sixteen (eight each) receive and transmit lines.
Line Transmitter:	Transmitter channel Fixed output amplitude of ± 11 V Output impedance 75 Ohm differential High / Low Speed: Rise and Fall time automatically switched via Analogue Switches to meet the requirement for High / Low Speed operation
Line Receiver:	Input Impedance A to B: typ. 50 kΩ Input Impedance A/B to GND: typ. 25 kΩ
Trigger In:	TTL-Input with 220 Ohm series resistor, 4.7K Ohm pulldown and 220pf EMV capacitor. Rising Edge sensitive, Pulsewidth > 75ns
Trigger Out:	TTL- Output with 82 Ohm series resistor, 220pf EMV capacitor, High Pulse width strobe, 250ns duration.
IRIG-IN:	DC-coupled 82 Ohm series resistor, 220pf EMV capacitor. 0.5 to 5.0 Vpp input voltage
IRIG-OUT:	DC-coupled 82 Ohm series resistor, 33pf EMV capacitor

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15pol. female HDSUB (AUX I/O)

Trigger In:	TTL-Input with 220 Ohm series resistor, 4.7K Ohm pulldown and 220pf EMV capacitor. Rising Edge sensitive, Pulsewidth > 75ns
Trigger Out:	TTL- Output with 82 Ohm series resistor, 220pf EMV capacitor. High Pulse width strobe, 250ns duration.
IRIG-IN:	DC-coupled 82 Ohm series resistor, 220pf EMV capacitor. 0.5 to 5.0 Vpp input voltage
IRIG-OUT:	DC-coupled 82 Ohm series resistor, 33pf EMV capacitor
Discrete I/O:	TTL-Level, 33 Ohm Series Resistor, 220pF EMV capacitor

Supply Voltage

+5V Standard USB Supply
For proper operation, two USB ports with 5 Unit Loads (500mA) each are needed. Otherwise supply current may be insufficient for high channel, high load operation. Y-Cable is provided.

Note: It is recommended to plug max 2 APU Devices to one PC or Notebook. Performance Issues or insufficient power Supply may be seen if plugging more than two APU devices into one PC.
A USB hub may be used as APU port if the hub itself is directly plugged into a Notebook or PC and the hub is a “self powered device” using an own power adaptor. In this case, a maximum of 2 APU devices may be used via one USB hub.
It is not recommended to plug the hub into another hub. Power and performance issues may be the result.

USB Cable

AIM provides a proofed Y-Cable for connecting the APU429 to the host. When using other cables than the provided, make sure that the maximum cable length does not exceed 1,20m. We cannot guarantee full performance functionality with other than the provided cable.

Dimensions

160mm x 85mm x 23mm
(case dimensions with I/O connectors)

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Thermal Power Dissipation

3.5 Watt Idle
5 Watt max

Operating Temperature Range

Standard:	0°C to +50°C
Extended:	-15°C to +60°C

Storage Temperature -40°C to +85°C

Humidity 0 to 95% non-condensing

Weight approx. 200 grams

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5. NOTES

5.1 Acronyms

ARINC	AERONAUTICAL RADIO, INC.
ADC	Analog to Digital Converter.
ARM	Advanced RISC Machine
ASP	Application Support Processor
BC	Bus Controller
BIP	Bus Interface Processor.
BIU	Bus Interface Unit.
BM	Bus Monitor
DAC	Digital to Analog Converter.
DRAM	Dynamic Random Access Memory
EEPROM	Electrically Erasable and Programmable Read Only Memory
EMC	Electromagnetic Compatibility
EPROM	Erasable Programmable Read Only Memory
FLASH	Page oriented electrical erasable and programmable memory.
IRIG	Inter Range Instrumentations Group
IRIG B	Inter Range Instrumentations Group Time code Format Type B
I/O	Input / Output
LCA	Logic Cell Array (XILINX - Programmable Gate Array)
MAC	Media Access Controller
PBI	Physical Bus Interface
PMC	PCI Mezzanine Card
PC	Personal Computer
PROM	Programmable Read Only Memory
PCI	Peripheral component interconnect
PSC	PCI and System Controller
RAM	Random Access Memory
RISC	Reduced Instruction Set Computer
RT	Remote Terminal
SDRAM	Synchronous Dynamic Random Access Memory
SIMM	Single Inline Memory Module
SSRAM	Synchronous Static Random Access Memory
TCP	Time Code Processor
UART	Universal Asynchronous Receiver and Transmitter

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