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AXI1553-x

Single or Dual Stream MIL-STD-1553A/B Test & Simulation Module for VXIbus

General Features

The AXI1553-1/2 module is part of a new family of VXIbus cards offering full function Test, Simulation, Monitoring and databus analyser functions for MIL-STD-1553A/B applications. Two independent and dual redundant MIL-STD-1553A/B databus streams are provided on the AXI1553-2 module and one dual redundant MIL-STD-1553A/B databus stream is provided on the AXI1553-1 module (when partially equipped) outlined as a C-sized VXI standard module.

The AXI1553-1/2 can be used for Protocol Testing and Simulation of MIL-STD-1553A/B Bus Controller, Multiple Remote Terminals and Chronological Monitoring at full bus load. All operations are performed concurrently with no degradation of performance in any operating mode. The AXI1553-1/2 module incorporates full protocol error injec-tion and detection features with software programmable output amplitude and bus coupling modes of the electrical bus signals. The module fully supports the Protocol Testing requirements defined by the RT and BC Production Test Plans according to SAE-AS 4112/ 4114.

An on-board IRIG-B time decoder and genera-tor allows users to accurately synchronise single or multiple AXI1553-1/2 modules to a common time source

The use of an Application Support Processor (ASP) executing the Driver Software allows user specific functions to be processed on-board significantly off-loading the host processor. This new concept allows users to implement application specific system level functionality on a single interface card. To provide I/O and processing expansion capabilities a PMC slot is available on the AXI1553-1/2 module.

The AXI1553-1/2 uses a ‘Common Core’ hardware design utilising multiple RISC processors. A Physical Bus Interface (PBI) daughter board provides MIL-STD-1553A/B bus connections including a resistive terminated bus network.

The AXI1553-1/2 module is a ‘Register based Device’ and can be easily integrated into VXI Systems as an off-the-shelf module supported by a VXI plug&play; driver software package. Furthermore the AXI1553-1/2 operates with the optional PBA-2000 Databus Analyser Software for Windows 95/98 and NT.

Bus Controller

The AXI1553-1/2 module provides real time Bus Controller (BC) functions on one or two dual redundant MIL-STD-1553A/B databus systems concurrently with Multiple Remote Terminal (RT’s) and Chronological Monitor operation. A 200MHz RISC Processor provides true simulation of Bus Controller operations without host computer interaction. The BC mode makes use of double buffering for message data and may generate dynamic data functions.

Key Features of BC Mode include:

- Autonomous Operation including sequencing of Minor/ Major Frames
- Support for acyclic message insertion/deletion
- Programmable BC Retry without host interaction
- Full Error Injection down to word and bit level (AS 4112 compliant)
- Multi-Buffering for data consistency and Message Multiplexing
- Synchronisation of BC operation to external trigger inputs
- 4 µs Intermessage Gaps

Multiple Remote Terminal

The AXI1553-1/2 simulates up to 31 Remote Terminals including all sub-addresses on one or two MIL-STD-1553A/ B bus systems concurrently with BC and Chronological Monitor operation. Alternatively each of the 31 RT’s can operate in a message oriented ‘Mailbox Monitor Mode’ to monitor non-simulated RT’s.

Key Features of MRT Mode include:

- Programmable RT Response Time down to 4 µs for each simulated RT
- Programmable & Intelligent Response to Mode Codes
- Full Error Injection down to word and bit level (AS4112 compliant)

- Multi-Buffering with Real Time Data Buffer Updates

Chronological Bus Monitor

The AXI1553-1/2 offers single or dual stream bus monitoring and analysis with programmable trigger and capture features. The Bus Monitor provides accurate Time Tagging of all bus traffic to 1 µs resolution including response time and gap time measurements down to 0.25 µs resolution concurrently with BC and Multiple RT operation.

Key Features of Chronological Monitor Mode include:

- 100% Data Capture on two streams at full bus rates
- Autonomous message synchronisation and Full Error Detection
- Two Static/ Dynamic Complex Triggers with up to 8 sequences
- Message Filter and Selective Capture
- Bus Activity recording independent from trigger and capture mode
- External Trigger Inputs and Outputs Programmable Response Time Out

Physical Bus Replay

The AXI1553-1/2 module is able to electrically reconstruct previously recorded MIL-STD-1553A/ B databus traffic physically to the bus with excellent timing accuracy. Recorded data files can be selected for Physical Bus Replay with the ability to disable any or all RT respon-ses from the recorded file to perform systems integration and test.

IRIG-B Time Code Decoder

An on-board IRIG-B time code decoder and generator allows synchronization of MIL-STD-1553A/B bus traffic using single or multiple AXI1553-1/2 modules. Multiple AXI1553-1/2 modules can be daisy chained using one common IRIG-B time source or the on-board Time Code Generator of one AXI1553-1/2 master module as the reference for accurate correlation of data across multiple MIL-STD-1553A/B data streams.

Application Support Processor

A 150 MHz 64 bit RISC processor provides unique on-board processing functions typically provided by the host processing systems.

Operational features include:

- Driver Software execution on-board
- Control of RS232C debug port for firmware updates
- Dynamic data generation
- Automatic test sequence generation
- Future Support for real-time Operating Systems on-board

Driver Software Support

With the AXI1553-1/2 module a VISA compatible VXI ‘plug&play;’ driver software package is included. Soft Front Panels and Function Panels processed under LabWindows/CVI are also provided.

MIL-STD-1553A/B Physical Bus Interface

One or two Physical Bus Interface (PBI) daughter boards are providing dual redundant MIL-STD-1553A/B transformer or direct coupled bus connection with variable output transceivers plus a resistive terminated bus network to enable the direct connection of external BC or RT devices. The coupling to the external bus is software programmable. The standard PBI provides an additional stub to minimize the external harness required and implements twinax connectors for all bus connections. Optionally the AXI1553-1/2 is available without additional stub and with D-Sub connectors only providing enhanced Trigger I/O facilities compared to the standard version.

Technical Data

SUB-SYSTEM INTERFACE:
VMEbus Slave, Options D8, D16, D32, A32 or A24
1 interrupt level used ‘Interrupt Release on Acknowledge
Register based VXI device

PROCESSORS:
Two 32 bit StrongARM 200MHz Processors
One 64 bit MIPS IDT 150MHz Processor

MEMORY:
2 MByte Global RAM
16 MByte ASP RAM

ENCODER/DECODER:
One MIL-STD-1553A/B Encoder / Decoder per BIU
with full Error Injection & Detection Capability

TIME TAGGING:
46 Bit absolute IRIG-B Time with 1µsec resolution

PHYSICAL BUS INTERFACE (PBI PROGRAMMABLE):
Dual MIL-STD-1553A/B Transceivers with variable Output
Amplitude, Programmable Bus Coupling and on-board
terminated Bus Network and additional Bus stub

CONNECTORS:
2 x 96 pin VMEbus backplane connectors
Standard PBIs:
• 4 Twinax Connectors (Bus & Stub) for bus connections
Optional PBIs (-D):
• 1 x 9 Way D-Sub for bus connections
• 1 x 15 Way D-Sub for Trigger and Timecode I/O
1 x 9 way D-Sub Connector (common) for Trigger and Time Code I/O and RS232 I/F

DIMENSIONS:
C-sized VXI Module
340mm x 233,4mm x 30mm

POWER CONSUMPTION:
AXI1553-1: 12,5 Watts typical @ 5 VDC
AXI1553-2: 17,5 Watts typical @ 5 VDC

OPERATING TEMP. RANGE:
Standard: 0°C ... +45°C ambient
Extended: -15°C ... +60°C ambient

STORAGE TEMP. RANGE:
-40°C ... +85°C ambient

HUMIDITY:
0 to 95% non-condensing

Ordering Information

AXI1553-1
Single Stream, Dual Redundant VXIbus to MIL-STD-1553A/B Interface including IRIG-B Time Decoder. BC, Multi-RT Simulator with Chronological Monitor. Variable Output transceivers. 2MByte Global RAM, 16MByte ASP RAM. AXI1553S-1
Single Stream, Dual Redundant VXIbus to MIL-STD-1553A/B Interface including IRIG-B Time Decoder. BC, Multi-RT Simulator with Mailbox Monitor only. Fixed Output Transceivers. 2MByte Global RAM, 16 MByte ASP RAM.

AXI1553-2
Dual Stream, Dual Redundant VXIbus to MIL-STD-1553A/B Interface including IRIG-B Time Decoder. BC, Multi-RT

Simulator with Chronological Monitor. Variable Output transceivers. 2MByte Global RAM, 16MByte ASP RAM.

AXI1553S-2
Dual Stream, Dual Redundant VXIbus to MIL-STD-1553A/B Interface including IRIG-B Time Decoder. BC, Multi-RT Simulator with Mailbox Monitor only. Fixed Output Transceivers. 2MByte Global RAM, 16 MByte ASP RAM.

For option with D-Sub connectors on the PBIs and enhanced Trigger I/O but without additional stub add -D to the part number.

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