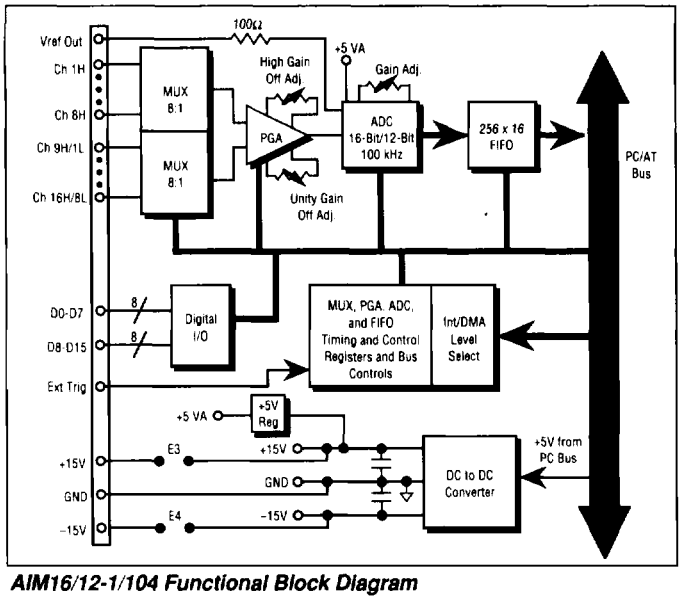
16- and 12-Bit, 16-Channel, 100 kHz PC/104 Analog Input Boards

Conform to the PC/104 Standard

Introduction

The Analogic AIM16-1/104 and AIM12-1/104 are 16-channel, 16- and 12-bit, 100 kHz analog input boards that conform to the PC/104 standard. The AIM16/12-1/104 Series provides 16 bits of digital I/O, flexible triggering options, direct memory access (DMA), and interrupt operation. This series was designed specifically for embedded applications requiring high speed and high resolution characteristics. The analog input multiplexer is software-configurable for up to 16 single-ended or 8 differential channels, with an on-board programmable gain amplifier (PGA) providing bipolar or unipolar input ranges of 10V, 5V, 2.5V, and 1.25 V for the AIM16-1/104, and 10V, 1V, and 100 mV for the AIM12-1/104. The PGA, programmable "on the fly", drives a 16-bit or 12-bit, 100 kHz sampling ADC capable of 85 dB of spurious free dynamic range for the AIM16-1/104, and 75 dB for the AIM12-1/104. The data is first passed through a 256 x 16 bit FIFO before transferring to the host via programmed I/O or DMA in 16-bit format. The AIM16/12-1/104 series also provides 16 digital I/O bits that can be programmed as inputs and/or outputs in 8-bit bytes.

Noise immunity within the AIM16/12-1/104 series is achieved by use of proven high frequency layout techniques, including short, guarded signal paths, and use of separate power and ground planes within the printed circuit board. The use of an on-board DC-to-DC converter, powered from a single +5V supply, provides noise isolation from the system switching power supply.



AIM16/12-1/104 Functional Block Diagram

Features

- 12- or 16-Bit Resolution
- On-Board Sample and Hold Amplifier and DC/DC Converter
- 100 kHz Throughput Rate
- 8 Differential or 16 Single-ended Inputs
- Software-Selectable Input Ranges -
  AIM16-1/104:
  10V, 5V, 2.5V, and 1.25V
  AIM12-1/104:
  10V, 1V, and 100 mV
- PC/AT Stack-Through Configuration
- Operates from Single +5V Supply
- DMA and Interrupt Operation
- Flexible Triggering Capabilities
- 16 Digital I/O lines
- Conforms to PC/104 Standard

AIM16-1/104
AIM12-1/104
Specifications[1]

	AIM16-1/104	AIM12-1/104
ANALOG INPUTS [2]		
Resolution	16 Bits	12 Bits
Analog Input Voltage Range		
AIM16/12-1/104B	±1.25V, ±2.5V, ±5V, ±10V	±100 mV, ±1V, ±10V
AIM16/12-1/104U	0V to +1.25V, 0V to +2.5V, 0V to +5V, 0V to +10V	0V to +100 mV, 0V to +1V, 0V to +10V
Maximum Input Without Damage		
With power applied	±35V	±35V
With power off	±20V	±20V
Input Configuration	16 SE or 8 Diff. Channels	16 SE or 8 Diff. Channels
Input Impedance	100 MΩ//50pF Typ.	100 MΩ//50pF Typ.
Input Bias Current	100 nA Max.	100 nA Max.
Small Signal Bandwidth	1 MHz Typ.	
Large Signal Bandwidth	100 kHz Typ.	1 MHz (10V and 1V ranges) 500 kHz (100 mV ranges)
Common Mode Rejection from DC to 60 Hz with 1KΩ Source Imbalance	–80 dB Min., -100 dB Typ.	–70 dB Min., -100 dB Typ.
Integral Nonlinearity	±0.0045% Max.	±0.024% Max.
Differential Nonlinearity	±0.0045% Max.	±0.024% Max.
Monotonicity	Guaranteed	Guaranteed
Missing Codes over Specified Temperature Range	None	None
Absolute Accuracy, Software Calibration	±3 LSB	±1 LSB
Offset Error before Software Calibration	±3 mV Max.	±3 mV Max.
Offset Tempco	±150 µV/°C Max. RTO	±150 µV/°C Max. RTO
Gain Error before Software Calibration	±0.15% FSR Max.	±0.15% FSR Max.
Gain Tempco	±25 PPM/°C Max.	±25 PPM/°C Max.
Noise (RTI)		
20V p-p FSR	1.5 LSBs RMS Max.	1.0 LSB RMS Max.
10V p-p FSR	2.0 LSBs RMS Max.	N/A
5V p-p FSR	2.6 LSBs RMS Max.	N/A
2.5V p-p FSR	4.0 LSBs RMS Max.	N/A
2V p-p FSR	N/A	2.0 LSBs RMS Max.
200 mV p-p FSR	N/A	3.0 LSBs RMS Max.
Maximum Throughput Rate	100 kHz Min.	100 kHz Min
Signal to Noise Ratio 1 kHz Input @ -1 dB [3]	80 dB Min.	67 dB Min.
SFDR @ 1 kHz Input @ -1 dB [4]	85 dB Min.	75 dB Min.
THD @ 1 kHz Input @ -1 dB [5]	–80 dB Max.	–74 dB Max.
Channel-to-Channel Crosstalk	–70 dB @ 10 kHz input	–70 dB @ 10 kHz input
Step Response, Max.	±2 LSBs for 1/2 FSR Step	±2 LSBs for 1/2 FSR Step

DATA TRANSFER		
Output Coding	Offset Binary, Binary, 2's Complement	Offset Binary, Binary, 2's Complement
Transfer to Host	PI/O or DMA (3 Channels)	PI/O or DMA (3 Channels)
Interrupts	6-Level (jumper-selectable)	6-Level (jumper-selectable)
FIFO [6]	256 x 16	256 x 16
TRIGGERING OPTIONS (SOFTWARE-PROGRAMMABLE)		
External		
Polarity	Negative Slope	Negative Slope
Minimum Pulse Width	100 nS	100 nS
Loading	1 CMOS Load	1 CMOS Load
Aperture Delay (Mode 0)	40 ns	40 ns
24-Bit Counter, Internal		
Minimum Timing	10 µs	10 µs
Maximum Timing	1.67 Sec.	1.67 Sec.
Host Software	Programmable	Programmable
DIGITAL INPUT/OUTPUTS		
Compatibility	TTL, HCT, and ACT	TTL, HCT, and ACT
Number of I/O Lines (configurable as Inputs or outputs)	Two 8-bit bytes	Two 8-bit bytes
Input Load	1 CMOS Load	1 CMOS Load
Fanout	±10 mA sink/source	±10 mA sink/source
Logic "0" Input	+0.8V Max.	+0.8V Max.
Logic "1" Input	+2.0V Min.	+2.0V Min.
POWER REQUIREMENTS & ENVIRONMENTAL		
+5V @ 0.5A (PC/AT bus)	±5%	±5%
Total Power Consumption	2.5W Typ.	2.5W Typ.
±15V Current Externally Available	3 mA Max.	3 mA Max.
Operating Temperature Range	+5°C to +50°C	+5°C to +50°C
Dimensions, PC/104 Stack-through Configuration	3.6" x 3.8" (91.44 mm x 96.52 mm)	3.6" x 3.8" (91.44 mm x 96.52 mm)
MTBF @ 40°C per MIL HDBK 217F	280,000 Hrs	280,000 Hrs

NOTES:

1. All specifications guaranteed at 25°C unless otherwise noted and power supply at +5.0V. Subject to change without notice.
2. All dynamic characteristics measured on the ±5V input range.
3. Signal to Noise Ratio represents the ratio, expressed in dB, between the RMS value of the signal and the total RMS noise below the Nyquist rate. Note that all frequency bins that are correlated with the test frequency are removed and replaced with an average of the remaining bins.
4. SFDR (Spurious Free Dynamic Range) represents the ratio, expressed in dB, between the RMS value of the full scale input signal and the RMS value of the highest spurious spectral component below the Nyquist rate.
5. THD (Total Harmonic Distortion) represents the ratio, expressed in dB, between the RMS sum of all harmonics up to the 100th harmonic and the RMS value of the signal.
6. For larger FIFO requirements, consult factory.

Modes of Operation

The AIM16-1/104 and AIM12-1/104 boards offer three software-selectable acquisition modes of operation. Interface to the host is by programmed I/O or DMA.

Mode 0

This mode of operation initiates a conversion each time any one of three preselected trigger signals occur. There are two programmable selections: a burst mode.and a non-burst mode. In the non-burst mode, only one conversion is made on one preprogrammed channel for each trigger. The conversion is synchronized to the trigger signal. In the burst mode, each preprogrammed channel will be converted once at a 100 kHz rate for each trigger signal.

Mode 1

This mode uses the external trigger or the software trigger to enable the 24-bit on-board trigger counter. The counter is loaded with a preset value and clocked until it overflows. Each time the counter overflows, a burst of conversions is initiated and each preprogrammed channel will be converted once at a 100 kHz rate. Conversions are synchronized to the on-board 10 MHz clock. The conversion process stops until the counter overflows again. This process continues until the software stops it by resetting the GO Bit.

Mode 2

This mode provides a means for taking continuous conversions through all preprogrammed channels at the maximum rate of the card. There are two programmable options to this mode. One uses the external trigger or the software trigger as a gate for taking conversions. The process continues until the external trigger or the software trigger is reset. The other option allows the internal trigger counter to set the GO Bit and start the conversion process. Conversions continue until the counter overflows stopping the process. All conversions in Mode 2 are synchronized to the on-board 10 MHz clock.

I/O Header

All I/O analog and digital signals are interfaced through a 40-pin right angle male header. The pinout is as follows.

AGND	1	2	Vref
Ch0	3	4	Ch 8 HI, 0 LO
Ch1	5	6	Ch 9 HI, 1 LO
Ch 2	7	8	Ch 10 HI, 2 LO
Ch 3	9	10	Ch 11 HI, 3 LO
Ch 4	11	12	Ch 12 HI, 4 LO
Ch 5	13	14	Ch 13 HI, 5 LO
Ch 6	15	16	Ch 14 HI, 6 LO
Ch 7	17	18	Ch 15 HI, 7 LO
AGND	19	20	+15V
−15V	21	22	DGND
D0	23	24	D1
D2	25	26	D3
D4	27	28	D5
D6	29	30	D7
D8	31	32	D9
D10	33	34	D11
D12	35	36	D13
D14	37	38	D15
Ext Trig	39	40	DGND

Software Description

"C" functions, with source code to control low level board interfacing, are provided with the AIM16-1/104 and AIM12-1/104 boards. Two sample routines (one acquisition under programmed I/O), the other under DMA are also provided.

WHAT IS PC/104?

The Need for an Embedded-PC Standard

Over the past decade, the PC architecture has become an accepted platform for far more than desktop applications. Dedicated and embedded applications for PCs are beginning to be found everywhere! PCs are used as controllers within vending machines, laboratory instruments, communications devices, and medical equipment, to name a few examples.

By standardizing hardware and software around the broadly supported PC architecture, embedded system designers can substantially reduce development costs, risks, and time. This means faster time to market and hitting critical market windows with timely product introductions. Another important advantage of using the PC architecture is that its widely available hardware and software are significantly more economical than traditional bus architectures such as STD, VME and Multibus. This means lower product costs.

For these reasons, companies that embed microcomputers as controllers within their products seek ways to reap the benefits of using the PC architecture. However, the standard PC bus form factor (12.4" x 4.8") and its associated card cages and backplanes are too bulky (and expensive) for most embedded control applications.

The only practical way to embed the PC architecture in space- and power-sensitive applications has been to design a PC — chip-by-chip — directly into the product.

But this runs counter to the growing trend away from "reinventing the wheel." Wherever possible, top management now encourages out-sourcing of components and technologies to reduce development costs and accelerate product design cycles.

A need therefore arose for a more compact implementation of the PC bus, satisfying the reduced space and power constraints of embedded control applications. Yet these goals had to be realized without sacrificing full hardware and software compatibility with the popular PC bus standard. This would allow the PC's hardware, software, development tools, and system design knowledge to be fully leveraged.

PC/104 was developed in response to this need. It offers full architecture, and hardware and software compatibility with the PC bus, but in ultra-compact (3.6" x 3.8") stackable modules. PC/104 is therefore ideally suited to the unique requirements of embedded control applications.

A Proposed Extension to IEEE-P996

Although PC/104 modules have been manufactured since 1987, a formal specification was not published until 1992. Since then, interest in PC/104 has skyrocketed, with numerous PC/104 modules introduced by more than one hundred manufacturers of PC/104-compatible products. Like the original PC bus, PC/104 is thus the expression of a de facto standard, rather than the invention and design of a committee.

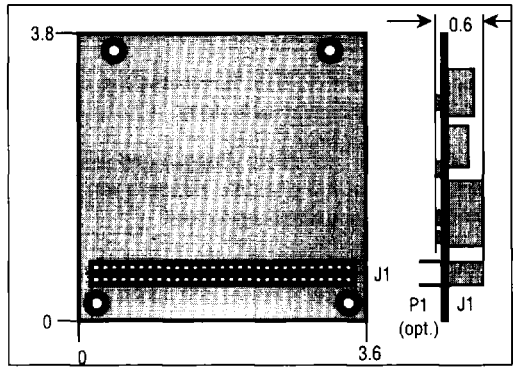


Figure 1. Basic Mechanical Dimensions (8-bit Version)

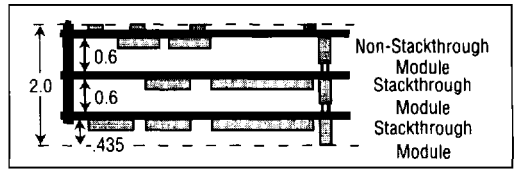


Figure 2. Standalone Board Stacks.

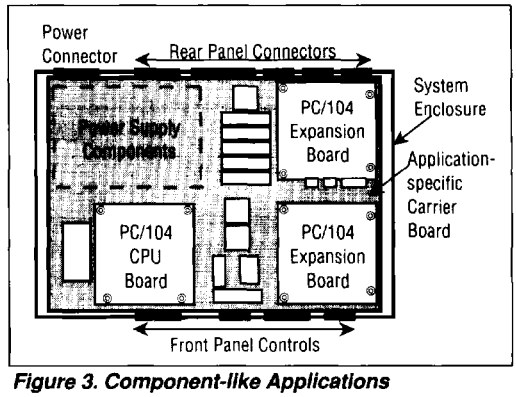


Figure 3. Component-like Applications

In 1992, the IEEE began a project to standardize a reduced form factor implementation of the IEEE P996 (draft) specification for the PC and PC/AT buses, for embedded applications. The PC/104 Specification has been adopted as the "base document" for this new IEEE draft standard, called the P996.1 Standard for Compact Embedded-PC Modules.

The key differences between PC/104 and the regular PC bus (IEEE P996) are:

- Compact form factor. Size reduces to 3.6 by 3.8 inches.
- Unique self-stacking bus. Eliminates the cost and bulk of backplanes and card cages.
- Pin-and-socket connectors. Rugged and reliable 64- and 40-contact male/female headers replace the standard PC's edgecard connectors.
- Relaxed bus drive (6 mA). Lowers power consumption (to 1-2 watts per module) and minimizes component count.

By virtue of PC/104, companies embedding PC technology in limited space applications can now benefit from a standardized system architecture complete with a wide range of multi-vendor support.

Two Ways to Use PC/104 Modules

Although configuration and application possibilities with PC/104 modules are practically limitless, there are two basic ways they tend to be used in embedded system designs:

Standalone Module Stacks: As shown in Figure 2, PC/104 modules are self-stacking. In this approach, the modules are used like ultra-compact bus boards, but without needing backplanes or card cages. Stacked modules are spaced 0.6 inches apart. (The three-module stack shown in Figure 2 measures just 3.6 by 3.8 by 2 inches.) Companies using PC/104 module stacks within their products frequently create one or more of their own application-specific PC/104 modules.

Component-Like Applications: Another way to use PC/104 modules is illustrated in Figure 3. In this configuration, the modules function as highly integrated components, plugged into custom carrier boards which contain application-specific interfaces and logic. The modules' self-stacking bus can be useful for installing multiple modules in one location. This facilitates future product upgrades or options, and allows temporary addition of modules during system debug or test.

About the PC/104 Consortium

The purpose of the PC/104 Consortium is to establish PC/104 as a broadly supported industry standard architecture for embedded-PC applications. The PC/104 Consortium maintains and distributes the PC/104 Specification and other PC/104-related documents, serves as a liaison to standards bodies such as IEEE P996.1, and engages in a variety of public relations activities on behalf of PC/104. Consortium membership is open to companies who offer or use PC/104 modules, as well as to companies who provide products that target PC/104 applications.

"What is PC/104?" reprinted courtesy of the PC/104 Consortium.

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Ordering Guide

Specify:	
12-Bit, 16-Ch., Bipolar Analog Input Module	**AIM12-1/104B**
12-Bit, 16-Ch., Unipolar Analog Input Module	**AIM12-1/104U**
16-Bit, 16-Ch., Bipolar Analog Input Module	**AIM16-1/104B**
16-Bit, 16-Ch., Unipolar Analog Input Module	**AIM16-1/104U**
AIM16/12-1/104 User Manual	**16-400626**

(A manual is included free of charge with the placement of an initial order. To receive additional manuals, order 16-400626)