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Find the *Aitech Defense Systems TM925* at our website: *Click HERE*

C925

PowerQUICCIII- MPC8548E 3U CompactPCI® SBC



- *Rugged 3U CompactPCI SBC*
- *Ideal for DO-178/DO-254 Applications*
- *PowerQUICC-III MPC8548E @ 800MHz (optional* 666MHz, 1.2 GHz)*
- *400 MHz Core Complex Bus (CCB) Speed*
- *One Standard PMC/XMC Slot*
- *XMC J5 Optional Configurations* :*
  - *1, 2, 4, 8 Lanes PCI-E*
  - *1,2, 4 Lanes PCI-E and 4 Lanes SRIO*
  - *4 Lanes SRIO*
- *PICMG 2.0, Rev. 3.0 Compliant*
- *System Controller or Peripheral (Auto)*
- *1GB of DDR2 SDRAM at 400MHz with ECC*
- *64 MB Boot Flash Memory*
- *128 MB User Flash Memory*
- *64 MB User Protected Flash Memory*
- *512 KB Autostore NVSRAM with Power Saving Support*
- *Two 10/100/1000 Mbps Ethernet Ports*
- *Two USB 2.0 Ports, Two CAN 2.0B Ports*
- *Two Async RS-232/422/485 Ports*
- *Eight Single Ended TTL or Four RS-422/485 Differential Discrete I/O Lines*
- *Four High Performance DMA Engines*
- *Four Timers (Internal to the CPU)*
- *Three Watchdog Timers, Elapsed Time Recorder*
- *Real Time Clock*
- *Three On-board Temperature Sensors*
- *VxWorks 6.x RTOS Support*
- *Conduction and Air Cooled Versions*

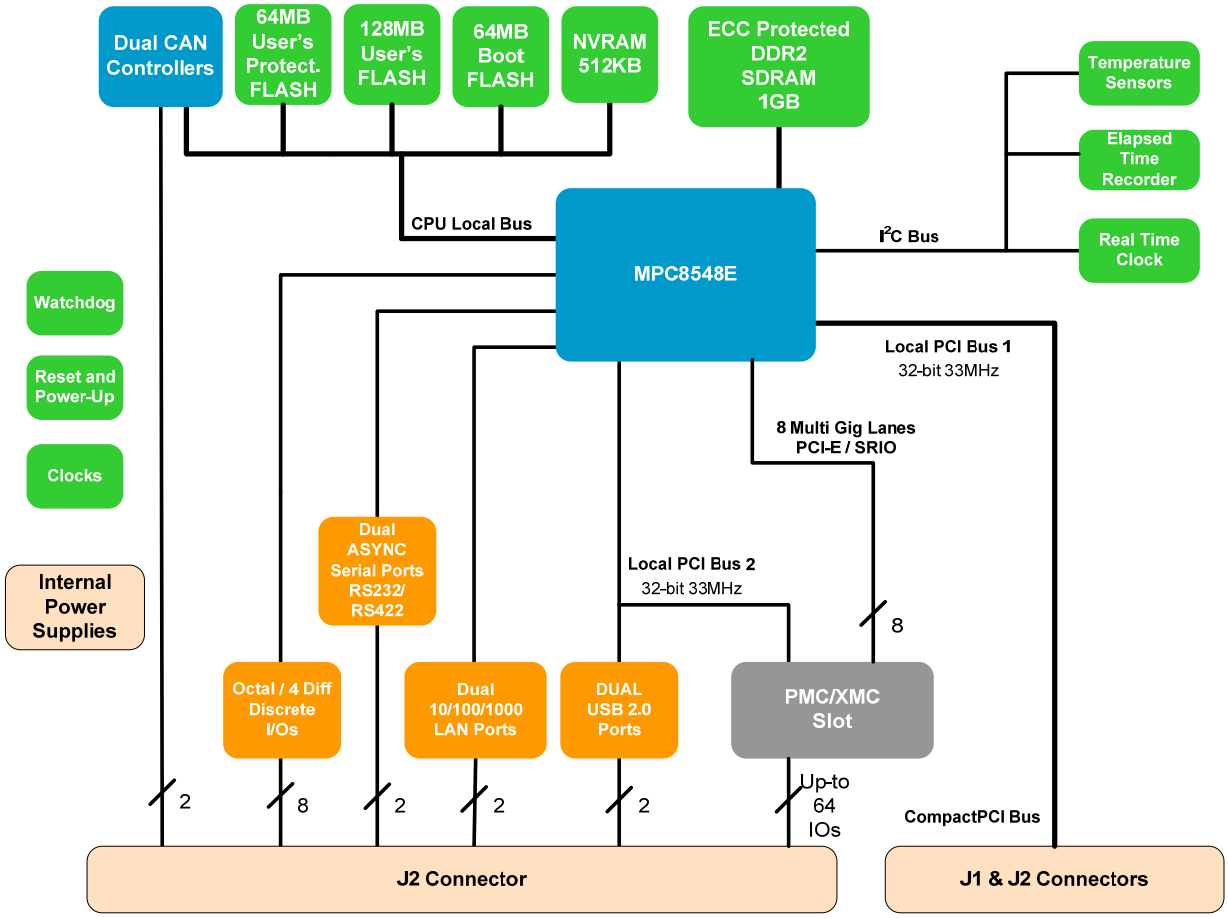
** Factory Configuration*

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C925 Powerful Processing in Compact Form Factor

Aitech's C925 3U CompactPCI SBC is an evolution from the C900/C901 SBC. Modifications included a processor upgrade to the Freescale's PowerQUICC III MPC8548E – e500 System on Chip, an additional Flash memory bank, a larger nvRAM and a dual CAN bus interfaces. With the processor upgrade, the C925 has increased processing performance while maintaining or reducing the power requirements.

The MPC8548E has an on-chip 32K instruction and 32KB Data L1 caches as well as a 512KB L2 cache. The CPU speed can be configured to between 666MHz and 1.2GHz. And the CPU Core Complex Bus (CCB) can be configured to 333 or 400MHz.



For systems requiring maximum processing power, the C925 processor can be configured to 1.2GHz with CCB speed of 400MHz.

The C925 backplane connections were designed such that the C925 can be configured as a one to one drop in replacements for the C900/C901.

The C925 implements large on-board memory arrays to support the processor and user application needs. Memory resources include up to 1 GB fast DDR2 (Double Data Rate) SDRAM with ECC protection, 128 MB User Flash, 64 MB Boot Flash, 64 MB User Protected Flash bank and 512 KB NVRAM for user/application specific parameter storage.

C925 onboard I/O capabilities include two Gigabit Ethernet ports, two high-speed serial communications ports, two USB 2.0 ports, two CAN Bus ports and up to eight general-purpose discrete I/O channels. To further expand its capabilities, the C925 is equipped with an industry standard PMC/XMC slot allowing for installation of additional modules and functionality.

The C925 may perform as either the CompactPCI system controller or as a peripheral board. When configured as system controller, the C925 can support up to five additional cards on the CompactPCI backplane, providing clock, arbitration and interrupt capabilities.

The highly integrated design of the C925 guarantees performance and versatility for rugged conduction or air-cooled CompactPCI SBC applications.

Functional Description

Processor and System Architecture

The C925 is a powerful processing platform achieved by combining a high performance PowerQUICC processor and extensive supporting memory arrays. In addition the board's architecture was designed to utilize all bus interfaces to the maximum.

Processor

The C925 features Freescale's high performance MPC8548 PowerQUICC® 32-bit processor. Integrating both L1 (32 kB instruction/data) and L2 (512 kB) caches on chip supports its powerful e500 processing core.

The processor operates at 800 MHz with Core Complex Bus supporting running at 400 MHz speed. (The processor operating speed is optionally available at 666MHz or 1.2 GHz.)

It provides DDR2 controller bus and a scalable, flexible local bus to interface to memories such Flash SRAM and peripherals.

The processor provides a large numbers of peripheral interfaces such as dual serial ports, Ethernet ports, dual I^2C buses, General Purpose I/Os, dual PCI buses and up-to eight PCI-Express lanes or four Serial Rapid IO (SRIO) lanes.

Memory

The C925 is equipped with large memory arrays providing the user with extensive volatile and non-volatile memory resources. These arrays include up to 1 GB fast DDR2 (Double Data Rate) SDRAM operating at 400 MHz, three banks totaling 256 MB of Flash memory, and 512 kB of NVRAM. The DDR2 is connected directly to the processors DDR controller while the other memory resources reside on the processor's local bus.

The DDR2 SDRAM bank is ECC protected providing high data integrity. The DDR bus is 72 bit wide – 64-bit data and 8-bit ECC. It is hardware configured to operate at 333 MHz or at 400 MHz data rates.

The Flash memory is divided into three separate banks:

The 64 MB Boot Flash (16-bit wide data array) is dedicated to firmware storage, freeing all the other arrays for user applications only.

The second Flash bank is for user programs and storage. It has 128 MB storage and is 32-bit wide.

The third Flash bank is also for user application but has an extra access protection. It has 64 MB storage and is 16 bit wide.

The 512 kB NVRAM (Non-Volatile RAM) has a fast EEPROM Shadow memory with a hardware "auto store" capability that stores all NVRAM contents to its shadow memory at the detection of a power failure, without the need for an external power supply. Upon the resumption of power, the shadow memory content is moved automatically back into the RAM storage.

CompactPCI Backplane

The C925 utilizes one of the processor's PCI bus ports for the CompactPCI backplane interconnection, implementing a standard 32-bit/33 MHz PCI interface, in accordance with the PCI specification.

In a CompactPCI subsystem, the C925 is capable of performing either as a system controller, or as a peripheral card. As system controller, the C925 supports up to five additional cards on the PCI backplane providing them with clock signals and arbitration support.

Note: The C925 cPCI interface supports only 3.3V signaling levels.

I/O Interfaces

In addition to its superior processing power, the C925 provides many I/O capabilities (relative to its small form factor).

Secondary PCI Bus interface

The C925 utilizes the second processor's PCI bus port for a PMC expansion site and also to interface with a dual USB ports Host controller, implementing a standard 32-bit/33 MHz PCI interface, in accordance with the PCI specification.

PMC/XMC Expansion

The C925 provides one IEEE 1386-2001 or ANSI/VITA 20-2001 compliant PMC expansion slot for extended flexibility and integration of additional I/O to the board.

The PMC is bus is 32 bit wide operating at 33 MHz.

The C925 connects 27 dedicated PMC I/Os and optionally up-to 64 I/Os to the backplane.

The PMC site supports also an XMC VITA 42 single connector (J5) for multi-gigabit serial interfaces.

The XMC interface types supported by hardware configuration (factory modified) are:

- 8, 4, 2, and 1 (auto negotiated) PCI-Express lanes
- 4 SRIO lanes on the connector S0 segment
- Up-to 4 PCI-E lanes on the connector S0 segment and 4 SRIO lanes on the S1 segment

Note: The PMC/XMC interface supports only 3.3 V signaling level.

Dual USB 2.0 Ports

The second PCI bus entity is a USB Host controller which provides the C925 with two EHCI/OHCI USB ports.

The controller's ports support data transfer rates of 480 Mbit/s, 12 Mbit/s and 1.5 Mbit/s. They comply with the USB Rev.2.0 and are backward compliant with Rev. 1.0 and 1.1.

The C925 is capable of providing power to downstream devices. The controller is a PCI device capable of high data transfer rates using its internal FIFOs and DMA engine.

Dual Ethernet Ports

Two 10BaseT, 100BaseTX and 1000BaseT interfaces are provided on the C925.

The Gigabit Ethernet controllers (MAC) are integrated in MPC8548E processor with internal FIFOs and DMA engines, allowing high bandwidth for data transfer through these interfaces. High performance physical layer devices complete this fast interface.

Dual Serial Communication Ports

The C925 provides two serial ports supporting RS-232/422/485 physical interfaces.

Dual CAN Bus Ports

Two stand-alone CAN Bus controllers reside on the processor local bus. They are compliant with the CAN 2.0B protocol and the PeliCAN mode extensions. They support bit rate up-to 1 Mbits/s with 11-bit and 29-bit identifiers.

Discrete I/O

There are eight discrete I/O channels that are divided into four groups, each controlling two signals. Each group can be configured as two single-ended TTL channels or a single differential RS-422/485 channels.

Each group can be configured independently as input or output. The configured input lines can be programmed to generate interrupts on any level shift event.

I/O Routing

All I/O interface signals are available at the C925 J2 CompactPCI rear panel connectors. PMC I/O may also be routed to the J2 connector at the expense of on-board I/O connectivity.

System Support Devices

Watchdog Timers

The C925 provides three watchdog timers. One is built in the MPC8548 processor which, when enabled, generates an internal CPU interrupt after the first internal timer expiration period and a hardware reset request after the second expiration period. The expiration period is programmable.

The second Watchdog timer is external to the processor. When enabled, it resets the whole board after the first expiration period.

The third watchdog timer resides in the nvRAM and consists of free running counter. When enabled, a programmable value is loaded by the user into the Watchdog counter and upon the expiration of the counter an internal flag is set and an optional interrupt may be sent to the processor.

Real time Clock

A Real Time Clock counters reside in the nvRAM and support time keeping of seconds, minutes, hours, days, months, years and dates. The RTC is backed up either by a large capacitor and can withstand a couple of hours of power loss and/or be connected to an external auxiliary 3.3V power supply provided through the C925 backplane.

Elapsed Time Recorder

The recorder detects and records the numbers of events and the total cumulative event time since it was last reset to 0. An alarm interrupts the processor when the total time accumulated equals the user-programmed alarm value. The device maintains its data in the absence of power.

Software

Test and Diagnostic Features

The C925 is supplied with an extensive firmware package, including startup firmware (boot software), AIMon monitor/debugger tool, AIDiag diagnostic tool, and BIT. BIT may be executed during power-up or at any time after the board has been booted.

A JTAG/COP interface to the processor is provided for debugging and development purposes.

Operating Systems

The C925 comes with complete Board Support Packages (BSP) for WindRiver VxWorks Version 6.6. (The BSP package can be optionally available for Green Hills Integrity upon request),

BSPs include drivers for all on-board resources, allowing the user to take full advantage of the C925's powerful features.

Mechanical Features

The C925 is available in two mechanical formats:

- Air-cooled: per PICMG 2.0 R3.0
- Conduction cooled: per ANSI/VITA 30.1-2002

Both mechanical formats are single slot 3U modules with dimensions in accordance with the referenced specifications.

A custom metal frame provides excellent rigidity and shock resistance. The frame also provides an array of stiffeners to support rugged PMC boards.

Thermal Management

Careful mechanical design, including custom heatsink modules combined with a metal frame, allow for optimal heat dissipation and relief of the board. The C925 is also equipped with three temperature sensors, located at temperature-critical locations, to monitor board temperature and provide temperature data to user application software. The sensors can be polled by the processor or send an alarm interrupt to the processor when they reach a certain temperature threshold.

Power Requirements

The C925 receives power from the CompactPCI backplane and generates its specific power supplies on-board.

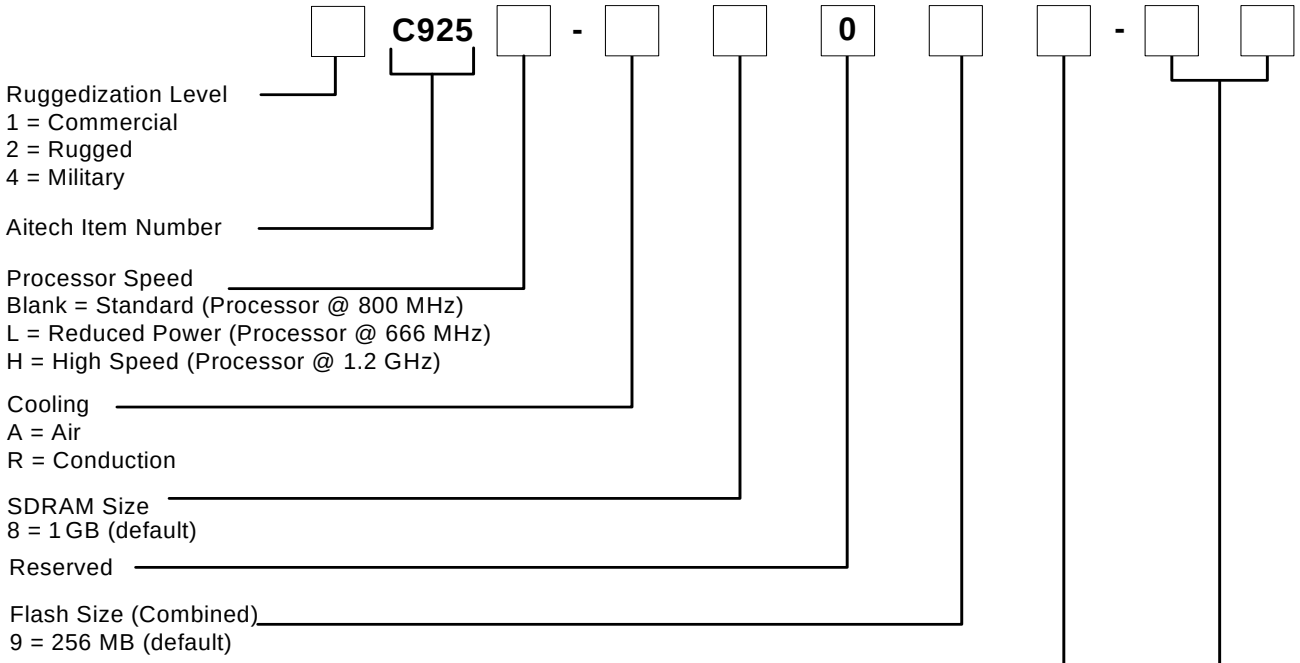
Power consumption for a fully populated C925 with 1 GB DRAM (no PMC installed):

		C925L @ 800/400 MHz	
		Typical	Maximum
3.3	Vdc	0.5A	0.6A
5	Vdc	1.7A	2.5A
±12	Vdc	0 A	0 A
Power		10.2W	14.5W

Environmental Features

Please Refer to the Aitech Ruggedization Datasheet.

Ordering Information for the C925



Variant**	1	2	3	4
cPCI System/Peripheral* **				
CompactPCI System Slot	x	x		
CompactPCI Peripheral Slot			x	x
I/O Routed to J2				
GB Ethernet	2	1	2	1
CAN BUS	2		2	
USB	2	2	2	2
Standard UARTs	2	2	2	2
FLASH/nvRAM Write Protect	1		1	
User's Memory Protect	1		1	
Discrete I/O Channels	8	4	8	4
PMC I/O Pins (J4)	29	51	41	64

Example: 2C925-R8091-00

** Contact the factory for possible options

*** When plugged into a cPCI System Slot the board is configured automatically to function as a System controller.

For more information about the C925 or any Aitech product, please contact Aitech Defense Systems sales department at (888) Aitech-8 (248-3248).

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