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ADC-PMC2
User Manual



Version 1.0

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1. Introduction

1.1. About the Hardware

The ADC-PMC2 is a 64-bit PCI carrier card for PMC modules. It can be used in 3V and 5V signalling environments and in both 32 and 64-bit slots. There are two PMC slots on the standard card and these can also support 32 or 64-bit operation. The secondary bus VIO can be configured in the factory for 5V or 3V operation. The default is 3V operation.

The ADC-PMC2 carrier card also supports features of the ADM-XRC FPGA board in a PCI environment with the provision of Pn4 routing between the two PMC sites and selectively to a 64-way header.

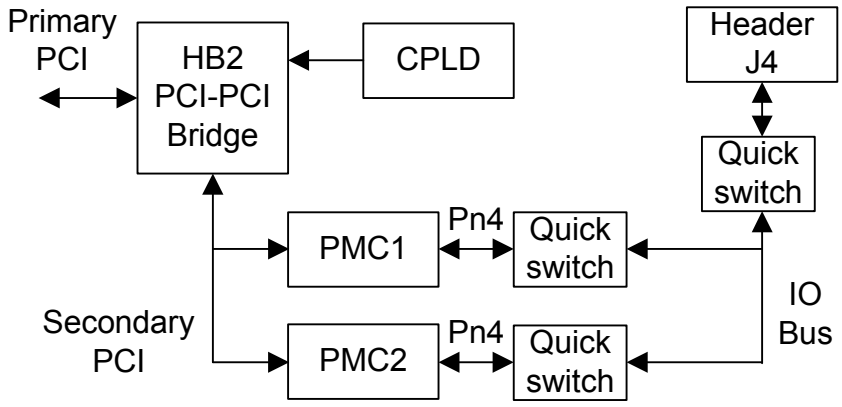
Both primary and secondary bus interfaces are rated at up to 66MHz operation.

1.2. Description

The ADC-PMC2 is based on the HiNT HB2 64-bit PCI-PCI bridge. This device supports 64 or 32 bit primary PCI and 64 or 32-bit secondary PCI.

Each of the two primary PMC sites supports Pn4 IO with quick-switch isolation to permit various IO combinations. A set of jumpers on the board enables each of the quick-switch blocks.

The IO-Bus is 64 bits wide and connects to all 64 signals from the Pn4 connector of each PMC site. Further, all of the IO-Bus can be routed to the J4 header through a quick-switch block that provides a level of protection to the IO bus signals by limiting the external signal levels.



2. Installation

In order to ensure that the board operates correctly first time, please read these instructions completely before attempting installation. It will also help you to read the whole manual first so that you know how you want the board to be set up. Figure 1 shows the physical layout of the board. The installation instructions for your PC should be followed at all times.

2.1. Into a PC

The ADC-PMC2 is a universal PCI device meaning that it can be used in both 3V and 5V signalling environments.

2.2. Adding PMC cards

Fit any PMC modules that are required. If only one PMC module is to be fitted, either site can be used. PMC site #1 is positioned so that an I/O connector on the module aligns with the aperture in the ADC-PMC2's edge panel. The PMC modules should be supplied with mounting kits, which normally include spacers, nuts, bolts and washers. Figure 1 shows the typical assembly of a PMC to the ADC-PMC2. It is recommended that washers be used on both sides of the ADC-PMC2 to avoid damage to the PCB.

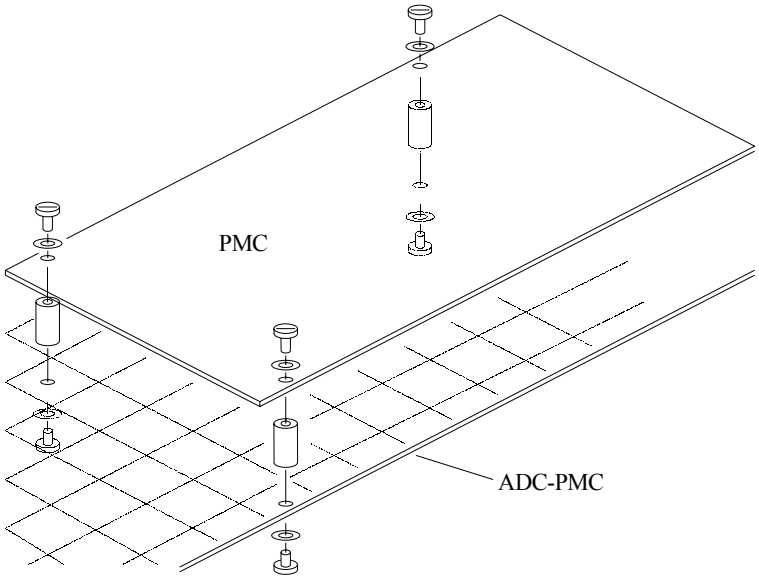


Figure 1 Assembly of a PMC to the ADC-PMC2

2.3. Software Support

The ADC-PMC2 uses a HinT HB2 64-bit bridge device that is compatible with most operating systems that adhere to the PCI Bios specification.

No software is required to enable operation of the ADC-PMC2.

3. Hardware Pin-out Information

3.1. Jumpers

There are 10 jumper sites on the board that are used for configuration settings.

Jumper	Usage	Fitted	Not Fitted
JP1	Secondary PCI bus clock select	33MHz PMC Bus	Auto select PMC clock
JP2	PMC1 Monarch	Not supported	
JP3	Option1	PMC1 Pn4 connected to IO bus	PMC Pn4 isolated
JP4	PMC2 Monarch	Not supported	
JP5	Option2	PMC2 Pn4 connected to IO bus	PMC2 Pn4 isolated
JP6	PMC3 Monarch	Not supported	
JP7	Option3	Header J4 connected to IO bus	Header J4 isolated
JP8	Option4	Not supported	
JP9	Option5	Not supported	
JP10	Option6	Not supported	

Notes.

- JP2, JP4, JP6 and JP8-10 are reserved for future use. Do not fit links in these positions.
- JP3, JP5 and JP7 can be fitted in any combination. Check the Pn4 information for the PMC's that are fitted to ensure there are no contention issues.

3.2. JP1 Additional Notes

JP1 is connected to the M66EN signal of the secondary PCI bus connecting the bridge to the PMC sites. It is necessary to fit this link if the ADC-PMC2 is fitted to 33MHz PCI slots and there are only 66MHz capable cards fitted to the PMC slots. In all other cases the link can be removed for automatic PCI clock control.

3.3. J1 PCI Connector

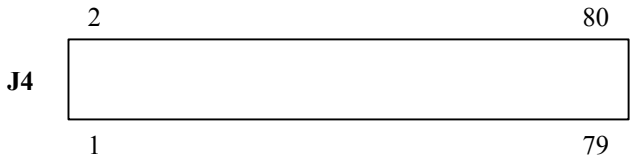
This is a standard edge connector for PCI and is compatible with 32-bit slots with 3V or 5V signalling and 64-bit slots with 3V signalling.

3.4. J2 JTAG Connector

This connector provides access to the CPLD, U2, and should only be used in manufacturing as changes to this device could cause system failure.

3.5. J4 Header Configuration

The IO header, J4, is suitable for mating with IDC connectors and is a RN P50E-080-P1-SR1-TG or equivalent.



gnd	1	2	gnd
gnd	3	4	gnd
gnd	5	6	gnd
gnd	7	8	gnd
gnd	9	10	gnd
hdr_io0	11	12	hdr_io1
hdr_io2	13	14	hdr_io3
hdr_io4	15	16	hdr_io5
hdr_io6	17	18	hdr_io7
hdr_io8	19	20	hdr_io9
hdr_io10	21	22	hdr_io11
hdr_io12	23	24	hdr_io13
hdr_io14	25	26	hdr_io15
hdr_io16	27	28	hdr_io17
hdr_io18	29	30	hdr_io19
hdr_io20	31	32	hdr_io21
hdr_io22	33	34	hdr_io23
hdr_io24	35	36	hdr_io25
hdr_io26	37	38	hdr_io27
hdr_io28	39	40	hdr_io29
hdr_io30	41	42	hdr_io31
hdr_io32	43	44	hdr_io33
hdr_io34	45	46	hdr_io35
hdr_io36	47	48	hdr_io37
hdr_io38	49	50	hdr_io39
hdr_io40	51	52	hdr_io41
hdr_io42	53	54	hdr_io43
hdr_io44	55	56	hdr_io45
hdr_io46	57	58	hdr_io47
hdr_io48	59	60	hdr_io49
hdr_io50	61	62	hdr_io51
hdr_io52	63	64	hdr_io53
hdr_io54	65	66	hdr_io55
hdr_io56	67	68	hdr_io57
hdr_io58	69	70	hdr_io59
hdr_io60	71	72	hdr_io61
hdr_io62	73	74	hdr_io63
gnd	75	76	gnd
gnd	77	78	gnd
gnd	79	80	gnd

The IO header is optimised for LVDS pairing to ADM-XRC-II Pn4 connections. All even number hdr_io signals are “P” with odd numbers being “N”. For example hdr_io0/1 are a P/N pair.

Revision History

Date	Rev	Comment
July-2002	1.0	Initial release

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