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ADM-XRC-II Pro
(ADM-XP)
Hardware Manual



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Revision History

Revision	Date	Comments
0.1	Jul-04	Initial
0.1+		DATA1, DATA8 DATA13 and DATA15 – polarity swapped DATA38 pin nos swapped in Manual Clock pins updated for XP pinouts (were XPL pinouts)
0.2	Nov-04	Removed XRM-Pro Debug Section – added XRM ETH

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1 Introduction

The ADM-XP (XP) is an advanced PCI Mezzanine card (PMC) supporting Xilinx Virtex-II PRO™ (V2PRO) devices, the latest development in FPGA technology. The XP supports 2VP70, 2VP100 or 2VP125 devices with two embedded PowerPC processors.

The XP utilises an FPGA PCI bridge developed by Alpha Data supporting 64 bit PCI at up to 66MHz. Future enhancements will provide compatibility with PCI-X. A high speed multiplexed address and data bus connects the bridge to the target FPGA.

Memory resources provided on-board include DDR SDRAM, DDR2 SSRAM and flash, all of which are optimised for direct use by the FPGA using IP and toolkits provided by Xilinx.

Flexible I/O is the key to the ADM-XRC-II series of boards and the XP is compatible with a wide selection of XRM modules that use the 180 pin Samtec interface.

1.1 Specifications

The ADM-XP supports high performance PCI operation without the need to integrate proprietary cores into the FPGA.

- Physically conformant to IEEE P1386 Common Mezzanine Card standard
- High performance PCI and asynchronous local bus
- Local bus speeds of up to 80MHz
- Four banks of 256K * 32 bits of DDR2 SSRAM – option for 512K * 32 bits
- Two banks of 64MB DDR SDRAM – option for 128MB
- Two flash devices of 16MB each for bridge and target devices
- User clock programmable between 5MHz and 200MHz
- User front panel adapter with up to 146 free IO signals
- Supports 3.3V PCI or PCIX at 64 bits
- On board 125MHz LVPECL oscillator
- 8 x RocketIO Multi-Gigabit Transceiver Connections (optional) @ 2.5Gb/s

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2 Installation

This chapter explains how to install the ADM-XP onto a PMC motherboard.

2.1 Motherboard requirements

The XP is a 3.3V only PCI device and is not compatible with systems that use 5V signalling.
The XP must be installed in a PMC motherboard that supplies 3.3V power to the PMC connectors. Ensure that the motherboard satisfies this requirement before powering it up.

2.2 Handling instructions

Observe precautions for preventing damage to components by electrostatic discharge. Personnel handling the board should take SSD precautions.
Avoid flexing the board.

2.3 Installing the ADM-XP onto a PMC motherboard

Note: This operation should not be performed while the PMC motherboard is powered up.
The ADM-XP must be secured to the PMC motherboard using M2.5 screws in the four holes provided. The PMC bezel through which the I/O connector protrudes should be flush with the front panel of the PMC motherboard.

2.4 Installing the ADM-XP if fitted to an ADC-PMC

The ADM-XP can be supplied for use in standard PC systems fitted to an ADC-PMC carrier board. The ADC-PMC can support up to two ADC-PMC cards whilst maintaining host PC PCI compatibility. If you are using a ADC-PMC64 refer to the supplied documentation for information on jumper settings. With the ADC-PMC64 all that is required for installation is a 5V or 3V PCI slot that has enough space to accommodate the full-length card.

It should be noted that the ADC-PMC uses a standard bridge to provide a secondary PCI bus for the ADM-XP and that some older BIOS code does not set up these devices correctly. Please ensure you have the latest version of BIOS appropriate for your machine.

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3 Hardware Overview

The XP is based on the architecture of the ADM-XRC-II with changes to accommodate the enhanced resources and needs of the Virtex-II PRO device.

The XP follows the architecture of the ADM-XRC series and decouples the “target” FPGA from the “bridge” device to allow the entire target to be available for user applications. This ensures the user can be up and running with the minimum of effort and without the complexity of PCI design.

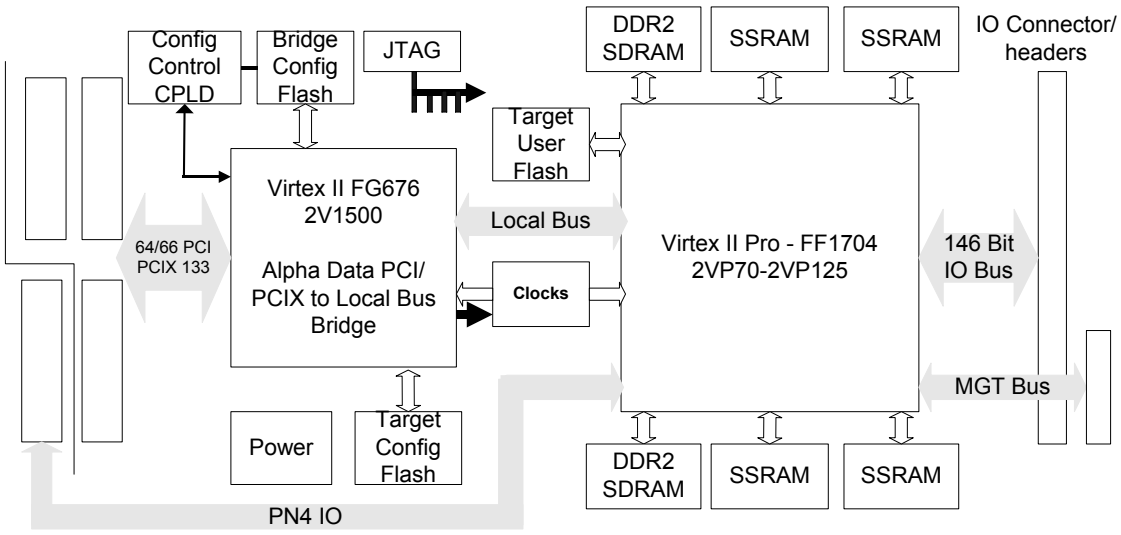
The bridge includes local bus control and monitoring together with flexible configuration options for the bridge and the target device.

The bridge is capable of 66MHz PCI or PCI-X operation with 64-bit or 32-bit operation. The local bus supports 64-bit at upto 80Mhz

The target FPGA is a Virtex-II-PRO device incorporating FPGA fabric, multi-gigabit transceivers and two PowerPC cores.

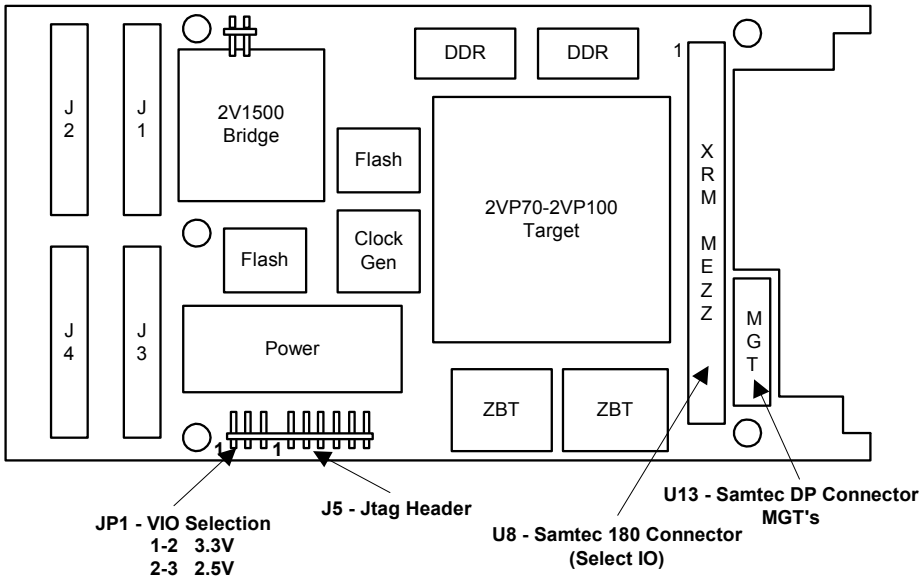
DDR SDRAM, ZBT and flash memory connect to the target FPGA and are supported by Xilinx or third party IP.

IO functionality is provided using XRM modules connecting to the 180 pin SAMTEC QSE and 28 pin SAMTEC QSE DP connectors.



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The physical layout is shown in the diagram below. The DDR DRAM and DDR2 SSRAM devices are clam shelled and appear on both sides of the board.

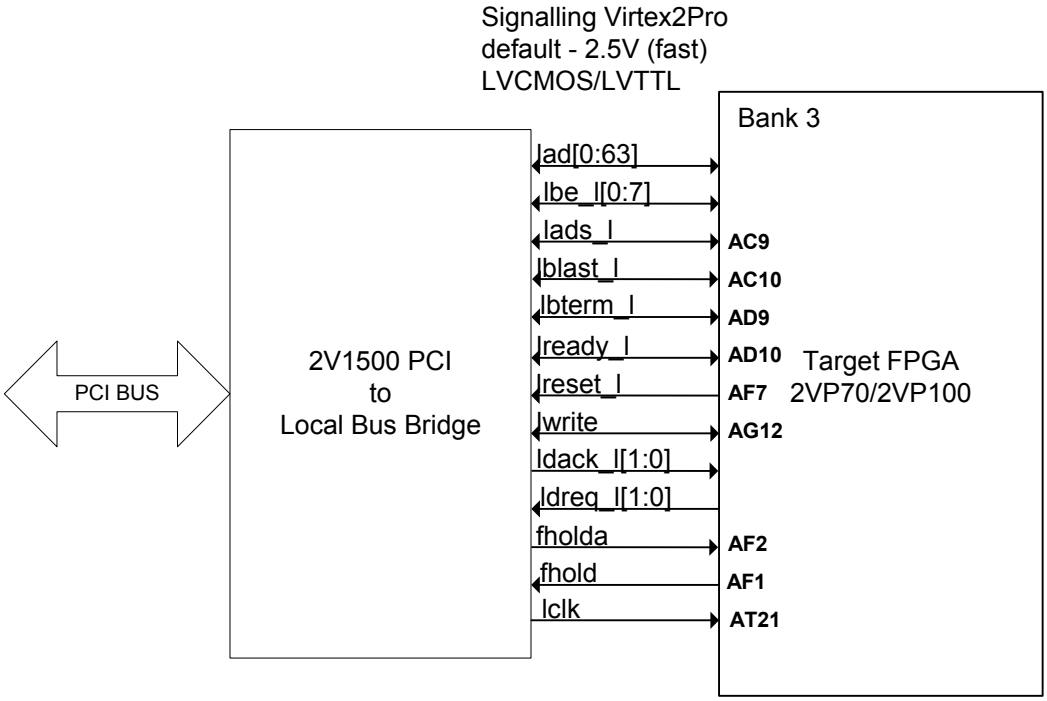


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4 Local Bus Architecture

The XP implements a multi-master local bus between the bridge and the target FPGA using a 32 or 64 multiplexed address and data path. The bridge design is asynchronous and allows the local bus to be run faster or slower than the PCI bus clock to suit the complexity of the user design.

4.1 Local Bus signals



Signal	Type	Purpose
lad[0:63]	bidir	Address and data bus.
lreset_l	unidir	Reset to target
lads_l	bidir	Indicates address phase
lblast_l	bidir	Indicates last word
lbterm_l	bidir	Indicates ready and requests new address phase
lready_l	bidir	Indicates that target accepts or presents new data
lclk	unidir	Clock to synchronise bridge and target
lbe_l[0:7]	bidir	Byte qualifiers
dreq_l[0:1]	unidir	DMA request from target to bridge
dack_l[0:1]	unidir	DMA acknowledge from bridge to target
fhold	unidir	Target bus request
fholda	unidir	Bridge bus acknowledge

4.2 Local Bus Transfers

Please refer to the ADM-XRC SDK Help for Windows supplied with the XP for information on local bus transfers.

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5 Target FPGA

The target FPGA is a V2PRO 2VP70, 2VP100 or 2VP125 (when available) in an FF1704 package. On the XP, all of the resources such as DDR, DDR2 SSRAM, IO and Flash are available no matter what device is fitted.

The V2PRO has 8 banks of I/O and banks 0 and 1 provide the User IO to the front panel . The VCCIO voltage for banks 0 and 1 is selectable using JP1.

JP1 Link Posn	VCCIO – Front IO
1-2	+3V3
2-3	+2V5

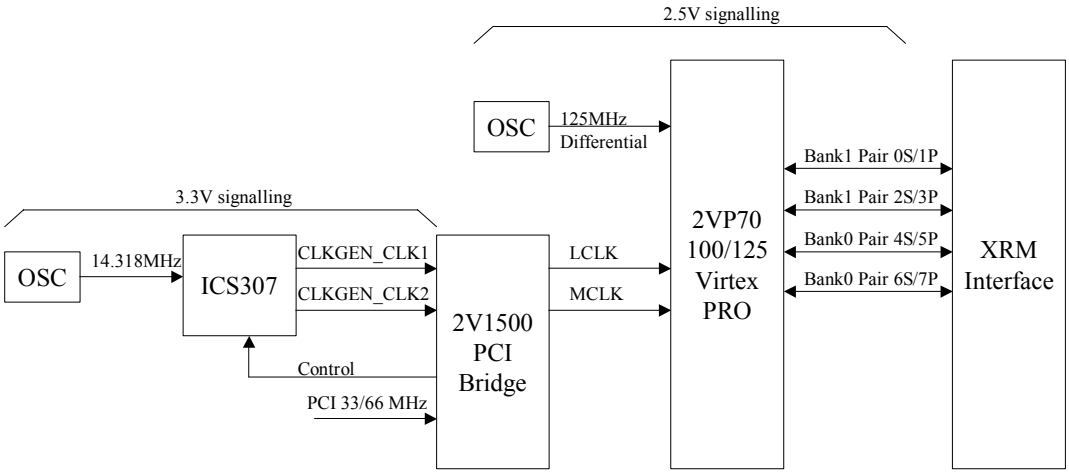
5.1 Configuration

The target FPGA can be configured using two primary mechanisms. In the first, JTAG from the J6 header can be used to perform downloading of bit-streams as well as remote debug using tools such as GDB and ChipScope / Pro. The drawback of using JTAG is that a download cable must be connected to the board.

The XP provides a SelectMAP port between the bridge and the target device mapped to the PCI bus. This enables very rapid download of configuration data controlled by driver and API code in the host. The maximum speed that can be achieved is 33 Mbytes per second.

5.2 Clocks

There are a number of clock sources in the XP as shown in the diagram below. Although the ICS307 is shown connected to the bridge, which may appear differently from the block diagram in the previous section, the purpose is to provide level translation between the 3.3V output of the clock generator and the 2.5V inputs of the 2VP70.



The V2PRO has a dedicated clock for gigabit operation using the Epson 2121CA 125MHz device. This is input on GCLK4S/5P in bank 5 and should be received in differential LVDS mode. Because of the routing limitations

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within the V2Pro device and the allocation of the MGT resources on the board the MGT's are currently limited to 2.5GBps operation using the REFCLK input to the transceivers.

The MCLK signal is input to the FPGA to provide a user clock of between 10 and 200MHz, single ended. The local bus uses LCLK to synchronize transfers between the bridge and the target and is derived from MCLK by a divide by 2 in the ICS307. Although the clocks are related, phase is not guaranteed.

A summary of the clock pins is shown in the table below.

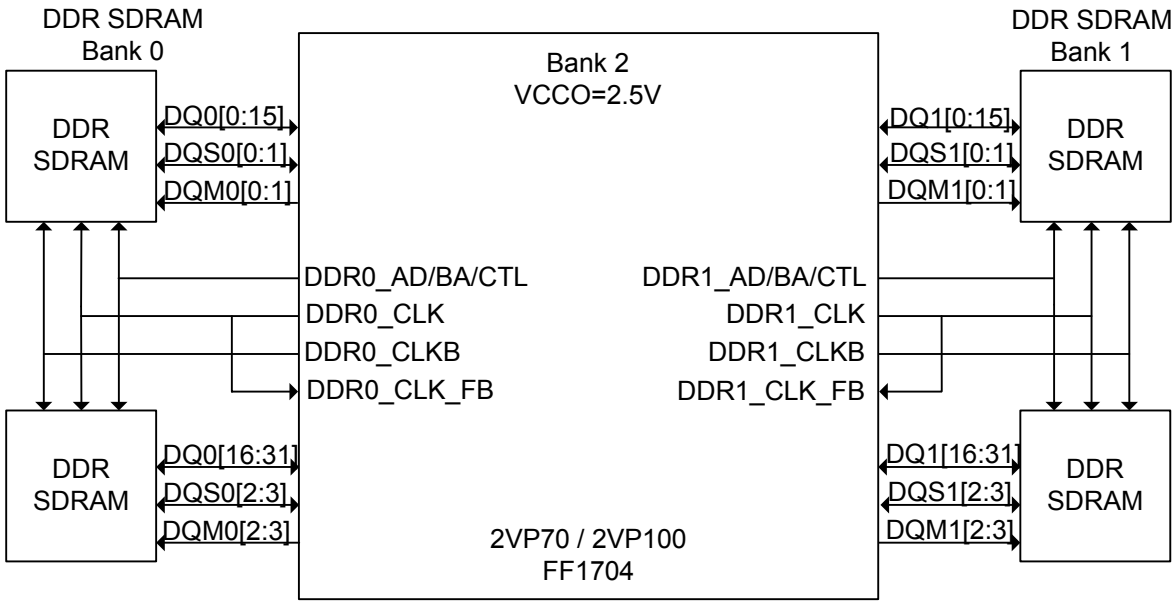
Bank	VCCO	GCLK	Pin	Signal	Description
0	JP1 select	7P	K22	IO_74N_0/GCLK7P	User clocks to / from XRM
0	JP1 select	6S	J22	IO_74P_0/GCLK6S	
0	JP1 select	5P	F22	IO_75N_0/GCLK5P	
0	JP1 select	4S	G22	IO_75P_0/GCLK4S	
1	JP1 select	0S	K21	IO_74P_1/GCLK0S	
1	JP1 select	1P	J21	IO_74N_1/GCLK1P	
1	JP1 select	2S	F21	IO_75P_1/GCLK2S	
1	JP1 select	3P	G21	IO_75N_1/GCLK3P	
4	2.5V	0P	AT21	LCLK	Local Bus Clock :- MCLK divided by 2
4	2.5V	1S	AU21	MCLK	User programmable up to 200MHz. Default is 66MHz
4	2.5V	2P	AP21	DDR2_clk	Clock feedback DDR DRAM 1
4	2.5V	3S	AN21	DDR1_clk	Clock feedback DDR DRAM 0
2	2.5V	-	AB12	DDR1_clk	Used for clock forwarding of DDR clock outputs
2	2.5V	-	AA12	DDR1_clkb	
2	2.5V	-	AA10	DDR2_clk	
2	2.5V	-	AA9	DDR2_clkb	
5	2.5V	6P	AU22	MGT_clk	Clock for the MGTs
5	2.5V	7S	AT22	MGT_clkb	
5	2.5V	4P	AN22	PN4 fpga_P3	PN4 IO clocks
5	2.5V	5S	AP22	PN4 fpga_N3	

If required, XRM related clocks should be terminated on the XRM itself. No terminations are provided on the XP main board.

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5.3 SDRAM DDR Memory

The XP provides 2 independent banks of 64MB of DDR SDRAM with the option of 128MB when devices become available. Two Micron MT46V16M16 devices are fitted and are organised as 4Mx16x4. These devices can be operated at between 75MHz and 133MHz and depending on resource usage within the FPGA, a 2VP70 can easily achieve 100MHz (DDR200) operation. Both banks are driven from Bank2 of the V2Pro.



The pins required for the SDRAM controller for each bank are listed below.

Name	Type
DDR_ad[0:12]	Output
DDR_dq[0:31]	Bidir
DDR_dqs[0:3]	Bidir
DDR_rasb	Output
DDR_casb	Output
DDR_web	Output
DDR_ba[0:1]	Output
DDR_clk	Output
DDR_clkb	Output
DDR_csb	Output
DDR_cke	Output
DDR_dm[0:1]	Output
DDR_clk_fb	Input

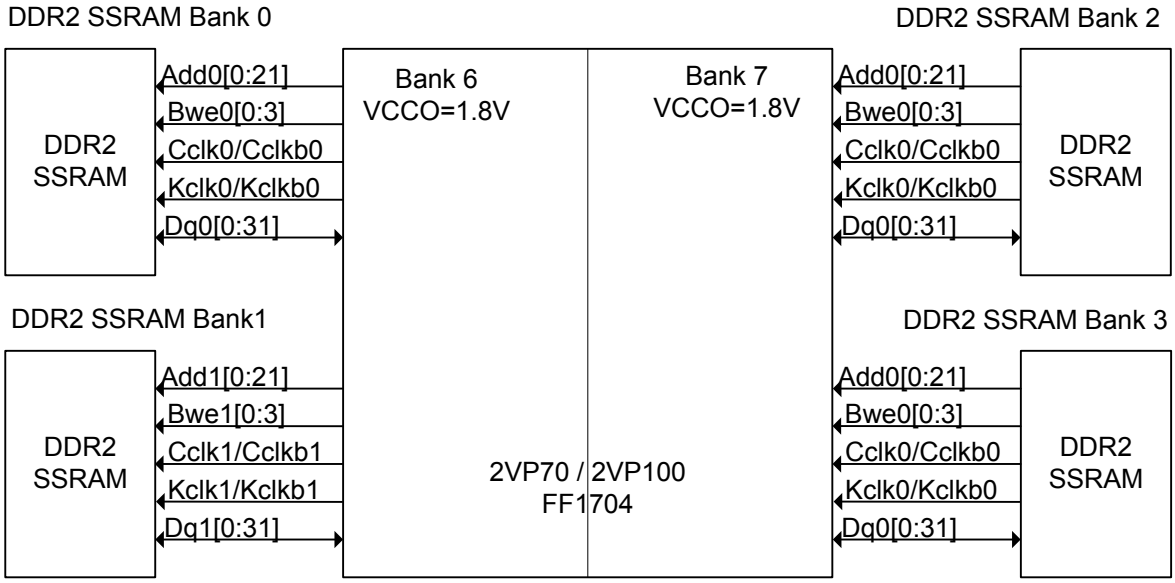
The DDR controller uses SSTL1 IOB's for data and control and SSTL1 for address and clocks - Please refer to the UCF for locations of the DDR pins. Please note that the FPGA requires the Vref pins to be connected for correct data reception on bank 3 when using SSTL standard. Additionally, bank 4 Vref pins connect to board Vref but are not required for user applications. These pins should not be configured with pull-up or pull-down options otherwise the Vref level will be set incorrectly.

The XP is designed to support DDR interface cores supplied by Xilinx using 90 degree phase shifted clocks for DQS during write operations. This requires DQS pins occupy IOB's that do not share a clock signal with DQ pins. In the XP, DQS[0:1] and DQS[2:3] occupy pairs of IOB's sharing a common clock. Note A trace delay has been incorporated on the DQS lines of approx 1.5ns to allow the use of local clocking within the FPGA

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5.4 DDR2 SSRAM

The XP supports four independent banks of CIO DDR2 SSRAM memory. The devices fitted are Samsung 512K *36 (K7I163684-FC16) parts or a functional equivalent. As an upgrade option 1Mx36 (K7I323684-FC16) devices can also be fitted.



The pins required for each SSRAM controller bank are listed below.

Name	FPGA Pin Type	Description
ZBTx_ad[0:21]	Output	Address bus
ZBTx_dq[0:31]	Bidir	Data bus
ZBTx_rw	Output	Read(1) / Write(0)
ZBTx_bwe{0..3]	Output	Byte enables for writes
ZBTx_nld	Output	Initiates a transaction
ZBTx_Cclk/ZBTx_nCclk	Output	SSRAM Output Data Clock
ZBTx_Kclk/ZBTx_nKclk	Output	SSRAM Clock for Inputs
ZBTx_DOFF	Output	SSRAM DLL Enable

The SSRAM pins should be configured for HSTL_II_18 operation

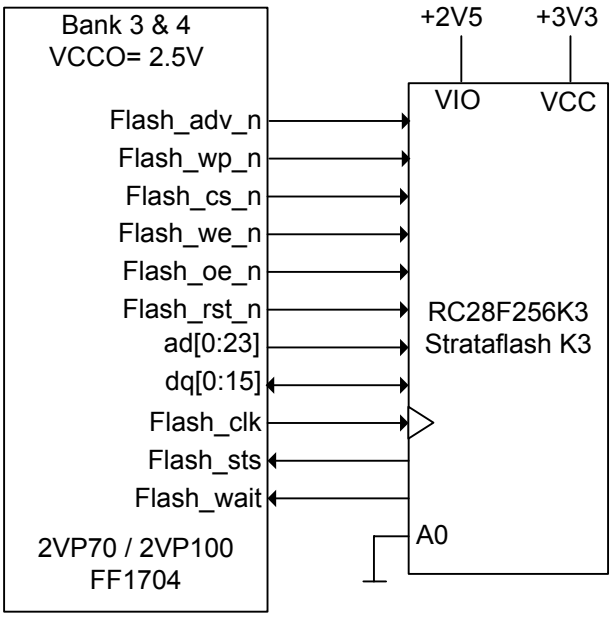
The SSRAM clock Cclks and Kclks are intended to be used with clock-forwarding implemented in a DDR IOB with a DCM used to adjust for SSRAM clock to output delays on the data input path to the FPGA.

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5.5 Flash Memory

The XP supports a flash device connected to the V2PRO for general purpose applications. Typically in applications that use a PPC core the flash is used to hold bootstrap or application code.

The flash memory has its own set of pins located within banks 3 and 4 of the V2Pro and the IO voltage on the Flash device is set at 2.5V. It is recommended that the LVCMOS_25 V2Pro IO standard be used for the Flash Interface.



5.6 Power Supply

The PMC connectors supply +5V and +3V3 to the XP and both of these rails are used with the card.

The +5V rail is used to provide FPGA VIO supplies of 2.5V @ 8A max and 1.8V at 6A max each.
The +3V3 rails is used to provide the FPGA VCC core of 1.5V @ 9A max. These are maximum values for the individual supply circuits but consideration must be taken to the power envelope that the PMC card is being deployed

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6 Front Panel I/O

The XP supports standard XRM's used on the ADM-XRC-II and ADM-XPL cards and also has an additional connector that brings 7 MGT channels upto the XRM Module site using a differential 28 pin Samtec QSE-DP series connector to maintain signal integrity.

The XP supports the standard Samtec 180 pin connector but using either with 2.5V or 3.3V signalling which is globally selected using JP1

JP1 Link Posn	VCCIO – Front IO
1-2	+3V3
2-3	+2V5

6.1 Samtec 180 connector - U8

The table below details the I/O signals that are available on the Samtec 180 connector along with the FPGA pin that each connects to.

FPGA Pin	Signal	Connector Pins		Signal	FPGA Pin
D10	IO_8N_1	1	2	IO_35N_1	C13
E10	IO_8P_1	3	4	IO_35P_1	D13
F11	IO_19N_1	5	6	IO_30P_1	H13
E11	IO_19P_1	7	8	IO_30N_1	G13
J10	IO_6N_1	9	10	IO_58N_1	M19
H10	IO_6P_1	11	12	IO_58P_1	L19
G10	IO_7N_1	13	14	IO_54N_1	L18
F10	IO_7P_1	15	16	IO_54P_1	K18
G9	IO_1P_1	17	18	IO_34P_1	E13
H9	IO_1N_1	19	20	IO_34N_1	F13
J12	IO_25N_1	21	22	IO_2N_1	E9
H12	IO_25P_1	23	24	IO_2P_1	F9
M13	IO_28N_1	25	26	IO_29P_1	K13
L13	IO_28P_1	27	28	IO_29N_1	J13
L12	IO_21N_1	29	30	IO_20P_1	C11
K12	IO_21P_1	31	32	IO_20N_1	C10
G17	IO_49N_1	33	34	IO_26N_1	F12
F17	IO_49P_1	35	36	IO_26P_1	G12
D16	IO_50P_1	37	38	IO_75P_1	F21
	+3V3	39	40	IO_75N_1	G21
	+3V3	41	42	Serial_ID	
	+3V3	43	44	Nc	
	+5V	45	46	Vref1	Note 1
	+5V	47	48	+2V5	
	Vbatt	49	50	+2V5	
	+12V	51	52	+2V5	
	+12V	53	54	-12V	
	Presence	55	56	TDI	
	TCK	57	58	TRST	
	TMS	59	60	TDO	

Note 1. Vref1 can be provided by the XRM if required and is applied to banks 0 and 1 in common.
Note 2. TCK, TMS, TDI and TDO are connected to the Coolrunner and not the V2PRO.

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(Continued)

FPGA Pin	Signal	Connector Pins		Signal	FPGA Pin
D20	IO_73N_1	61	62	IO_68N_1	H20
C20	IO_73P_1	63	64	IO_68P_1	J20
K17	IO_47N_1	65	66	IO_37N_1	F15
L17	IO_47P_1	67	68	IO_37P_1	E15
J17	IO_48N_1	69	70	IO_38N_1	C15
H17	IO_48P_1	71	72	IO_38P_1	C14
H18	IO_55N_1	73	74	IO_39P_1	L16
G18	IO_55P_1	75	76	IO_39N_1	M16
E17	IO_56P_1	77	78	IO_43N_1	K16
E18	IO_56N_1	79	80	IO_43P_1	J16
K19	IO_59N_1	81	82	IO_44P_1	H16
J19	IO_59P_1	83	84	IO_44N_1	G16
H19	IO_60N_1	85	86	IO_46N_1	M17
G19	IO_60P_1	87	88	IO_46P_1	M18
K21	IO_74P_1	89	90	IO_65N_1	C19
J21	IO_74N_1	91	92	IO_65P_1	D19
E19	IO_64P_1	93	94	IO_37N_0	E28
F19	IO_64N_1	95	96	IO_37P_0	F28
G22	IO_75P_0	97	98	IO_38N_0	C29
F22	IO_75N_0	99	100	IO_38P_0	C28
H27	IO_44N_0	101	102	IO_74P_0	J22
G27	IO_44P_0	103	104	IO_74N_0	K22
J27	IO_43N_0	105	106	IO_39N_0	L27
K27	IO_43P_0	107	108	IO_39P_0	M27
D29	IO_85N_0	109	110	IO_67N_1	L20
E29	IO_85P_0	111	112	IO_67P_1	K20
K29	IO_78N_0	113	114	IO_78N_1	L14
L29	IO_78P_0	115	116	IO_78P_1	K14
BB40	MGT_SYS_TXP23	**117	**118	MGT_SYS_RXP23	BB39
BB41	MGT_SYS_TXN23	**119	**120	MGT_SYS_RXN23	BB38

** - Additional MGT channel provided using these pins

FPGA Pin	Signal	Connector Pins		Signal	FPGA Pin
K26	IO_47P_0	121	122	IO_35P_0	C30
L26	IO_47N_0	123	124	IO_35N_0	D30
L24	IO_58N_0	125	126	IO_46P_0	M26
M24	IO_58P_0	127	128	IO_46N_0	M25
E25	IO_56P_0	129	130	IO_48P_0	J26
E26	IO_56N_0	131	132	IO_48N_0	H26
H31	IO_25N_0	133	134	IO_59N_0	J24
J31	IO_25P_0	135	136	IO_59P_0	K24
G33	IO_7P_0	137	138	IO_73N_0	C23
F33	IO_7N_0	139	140	IO_73P_0	D23
E34	IO_2P_0	141	142	IO_60N_0	G24
F34	IO_2N_0	143	144	IO_60P_0	H24
H33	IO_6N_0	145	146	IO_29P_0	K30
J33	IO_6P_0	147	148	IO_29N_0	J30
C32	IO_20P_0	149	150	IO_54N_0	K25
C33	IO_20N_0	151	152	IO_54P_0	L25
H34	IO_1P_0	153	154	IO_64N_0	E24
G34	IO_1N_0	155	156	IO_64P_0	F24
E33	IO_8N_0	157	158	IO_67N_0	K23
D33	IO_8P_0	159	160	IO_67P_0	L23
C24	IO_65P_0	161	162	IO_30N_0	G30
D24	IO_65N_0	163	164	IO_30P_0	H30
E30	IO_34N_0	165	166	IO_55N_0	G25
F30	IO_34P_0	167	168	IO_55P_0	H25
K31	IO_21N_0	169	170	IO_26N_0	G31
L31	IO_21P_0	171	172	IO_26P_0	F31
F26	IO_49N_0	173	174	IO_28N_0	L30
G26	IO_49P_0	175	176	IO_28P_0	M30
E32	IO_19N_0	177	178	IO_68N_0	J23
F32	IO_19P_0	179	180	IO_68P_0	H23

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6.2 RocketIO Multi-Gigabit Transceivers – U13

The ADM-XP provides an additional connection upto the XRM module site which provides 7 MGT connection from the Virtex II pro device. This enables customisable Mulit Gigabit IO capability using XRM modules interfacing to the additional samtec QSE-DP connector.

Details of the connections to for the XRM MGT signalling is given below :-

FPGA Pin	Signal	Connector Pins		Signal	FPGA Pin
A40	MGT_SYS_TXP2	1	2	MGT_SYS_RXP2	A39
A41	MGT_SYS_TXN2	3	4	MGT_SYS_RXN2	A38
A36	MGT_SYS_TXP3	5	6	MGT_SYS_RXP3	A35
A37	MGT_SYS_TXN3	7	8	MGT_SYS_RXN3	A34
BB4	MGT_SYS_TXP14	9	10	MGT_SYS_RXP14	BB3
BB5	MGT_SYS_TXN14	11	12	MGT_SYS_RXN14	BB2
BB8	MGT_SYS_TXP15	13	14	MGT_SYS_RXP15	BB7
BB9	MGT_SYS_TXN15	15	16	MGT_SYS_RXN15	BB6
A8	MGT_SYS_TXP10	17	18	MGT_SYS_RXP10	A7
A9	MGT_SYS_TXN10	19	20	MGT_SYS_RXN10	A6
A4	MGT_SYS_TXP11	21	22	MGT_SYS_RXP11	A3
A5	MGT_SYS_TXN11	23	24	MGT_SYS_RXN11	A2
BB36	MGT_SYS_TXP22	25	26	MGT_SYS_RXP22	BB35
BB37	MGT_SYS_TXN22	27	28	MGT_SYS_RXN22	BB34

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7 User IO – PMC PN4 (rear panel)

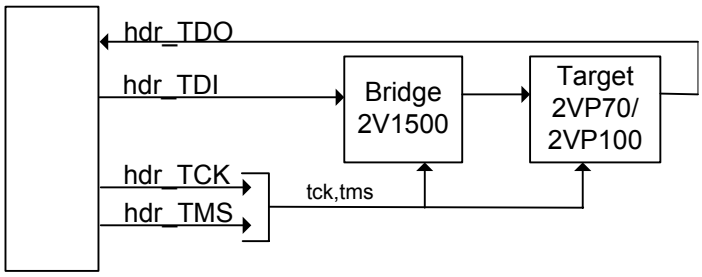
User I/O is presented on the User Connector Pn4 via a standard 64-way PMC connector. This should be routed via a suitable CMC compliant motherboard to an external I/O adapter.

FPGA Pin	Signal	Pn4 Pin	Pn4 Pin	Signal	FPGA Pin
AY23	REARIO[1]	1	2	REARIO[0]	AW23
AP23	REARIO[3]	3	4	REARIO[2]	AR23
AN22 (gclk)	REARIO[5]	5	6	REARIO[4]	AP22(gclk)
AW24	REARIO[7]	7	8	REARIO[6]	AY24
AV24	REARIO[9]	9	10	REARIO[8]	AU24
AT24	REARIO[11]	11	12	REARIO[10]	AR24
AP24	REARIO[13]	13	14	REARIO[12]	AN24
AM24	REARIO[15]	15	16	REARIO[14]	AL24
AV26	REARIO[17]	17	18	REARIO[16]	AV25
AT25	REARIO[19]	19	20	REARIO[18]	AR25
AN25	REARIO[21]	21	22	REARIO[20]	AM25
AU26	REARIO[23]	23	24	REARIO[22]	AT26
AR26	REARIO[25]	25	26	REARIO[24]	AP26
AM26	REARIO[27]	27	28	REARIO[26]	AN26
AL25	REARIO[29]	29	30	REARIO[28]	AL26
AR27	REARIO[31]	31	32	REARIO[30]	AT27
AP27	REARIO[33]	33	34	REARIO[32]	AN27
AM27	REARIO[35]	35	36	REARIO[34]	AL27
AY29	REARIO[37]	37	38	REARIO[36]	AY28
AV28	REARIO[39]	39	40	REARIO[38]	AU28
AW30	REARIO[41]	41	42	REARIO[40]	AY30
AV30	REARIO[43]	43	44	REARIO[42]	AU30
AT30	REARIO[45]	45	46	REARIO[44]	AR30
AP30	REARIO[47]	47	48	REARIO[46]	AN30
AM30	REARIO[49]	49	50	REARIO[48]	AL30
AT31	REARIO[51]	51	52	REARIO[50]	AU31
AR31	REARIO[53]	53	54	REARIO[52]	AP31
AN31	REARIO[55]	55	56	REARIO[54]	AM31
AY33	REARIO[57]	57	58	REARIO[56]	AY32
AV32	REARIO[59]	59	60	REARIO[58]	AU32
AV33	REARIO[61]	61	62	REARIO[60]	AW33
AR33	REARIO[63]	63	64	REARIO[62]	AP33

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8 JTAG Access

The XP provides JTAG access for the fabric of the board through J6. This header will connect to Xilinx download cables using 3V3 signalling levels and has the following devices present in the scan chain :-



The standard XP is configured with the JTAG chain as shown in the table below.

TDI->	2V1500	
	2VP70/100	-> TDO

8.1 JTAG Header (J6)

The table below shows the pin-out for J5, the primary JTAG connector.

Pin	Function
1	+3V3
2	GND
3	nc
4	TCK
5	nc
6	TDO
7	TDI
8	POL
9	TMS

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9 XRM-ETH

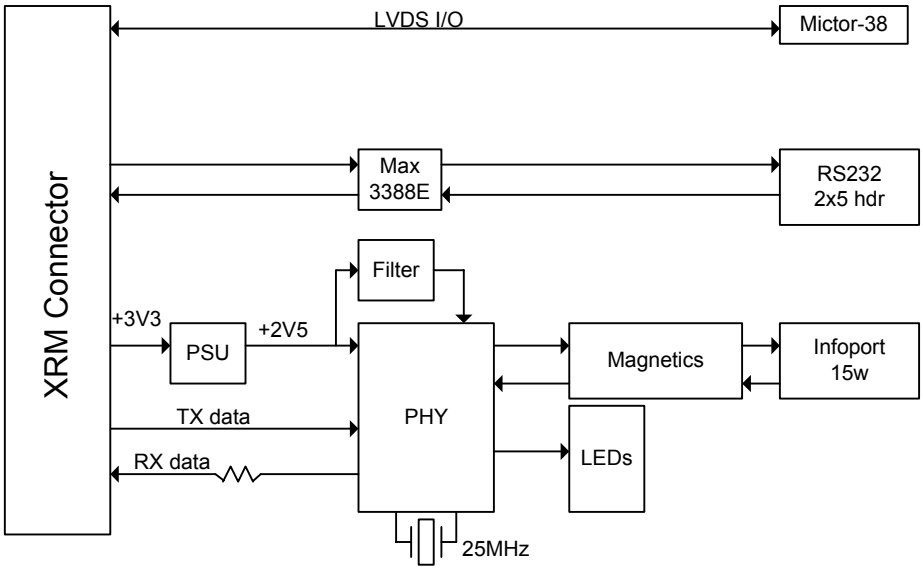
9.1 Introduction

The XRM-ETH is a general-purpose adaptor for the ADM-XPL and ADM-XRC-II series of PMC modules. It provides 10/100 Ethernet, RS-232 and general purpose I/O for use with a wide variety of IP.

The XRM-ETH is supplied with two cables to enable connections from the XRM-ETH to 15 way PC COM ports and RJ45 Ethernet.

XRM-ETH-CAB01 for Ethernet
XRM-ETH-CAB02 for RS232

IMPORTANT. The XRM-ETH REV 1 requires the use of 2.5V signalling over the XRM connector and this should be checked prior to power up.



9.2 General Purpose I/O

The XRM-ETH provides 18 pairs of differential-capable I/O plus two single-ended signals on a 38 pin Mictor connector. This connector is compatible with a wide range of Mictor connectors and is well suited to cabling systems from Precision Interconnect.

The differential pairs are routed on the XRM-ETH with 100 Ohm impedance and are not terminated to enable direct routing to the FPGA. The user has the choice of using Virtex DCI or DT termination schemes to provide the correct termination for each signal pair. For DCI termination the resistor pairs R1/R2 and R4/R5 should be set to the appropriate value for the desired termination value. By default these resistors are all 100Ohm. The DT scheme can only be used with some Virtex-II PRO devices and provides a fixed 100R termination for LVDS and LDT I/O standards without the power requirement of the DCI option.

9.3 RS232 I/O

The XRM-ETH provides two transmit and two receive RS232 signals that can be used for connection to other XPLs or PC COM ports. The supplied cable connects TX0 and RX0 to a standard 15 pin connector suitable for use with a PC. Baud rates up to 115K are supported.

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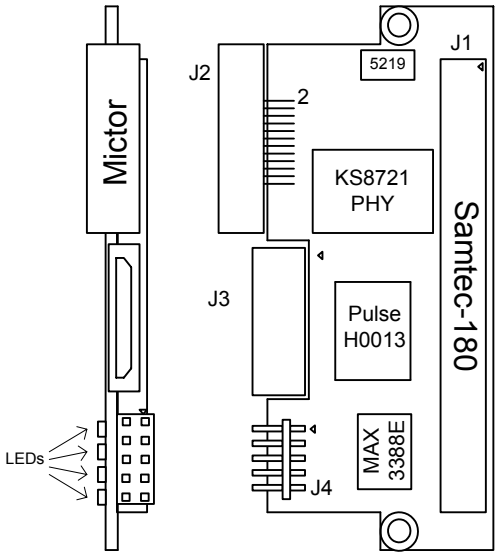
9.4 10/100 Ethernet

The XRM-ETH Ethernet capability is supported by a Kendin KS8721B 2.5V PHY. This device is capable of auto-sensing 10 or 100Mb networks and has a standard MII interface suitable for connection to MAC IP in the FPGA. A management interface and reset is also provided.

LEDS are provided on the board and these indicate the following conditions when lit.

D1	Collision
D2	Full Duplex
D3	Speed is 100
D4	Activity

An Ethernet MAC such as the PLB or OPB Ethernet version supplied with EDK6.1i is compatible with this interface.



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9.5 Input and Output Assignments (ADM-XP)

9.5.1 Mictor I/O

FPGA		XRM-ETH		
Bank	Pin	Samtec	J2 Mictor	Signal
1	E10	3	1	PAIR_1_P
1	D10	1	3	PAIR_1_N
1	D13	4	2	PAIR_2_P
1	C13	2	4	PAIR_2_N
1	E11	7	5	PAIR_3_P
1	F11	5	7	PAIR_3_N
1	H13	6	6	PAIR_4_P
1	G13	8	8	PAIR_4_N
1	H10	11	9	PAIR_5_P
1	J10	9	11	PAIR_5_N
1	L19	12	10	PAIR_6_P
1	M19	10	12	PAIR_6_N
1	F10	15	13	PAIR_7_P
1	G10	13	15	PAIR_7_N
1	K18	16	14	PAIR_8_P
1	L18	14	16	PAIR_8_N
1	C20	63	17	PAIR_9_P
1	D20	61	19	PAIR_9_N
1	F9	24	18	PAIR_10_P
1	E9	22	20	PAIR_10_N
1	L17	67	21	PAIR_11_P
1	K17	65	23	PAIR_11_N
1	C11	30	22	PAIR_12_P
1	C10	32	24	PAIR_12_N
1	J19	83	25	PAIR_13_P
1	K19	81	27	PAIR_13_N
1	G12	36	26	PAIR_14_P
1	F12	34	28	PAIR_14_N
1	G19	87	29	PAIR_15_P
1	H19	85	31	PAIR_15_N
1	M18	88	30	PAIR_16_P
1	M17	86	32	PAIR_16_N
1	K21	89	33	CLK2
1	J21	91	35	CLK3
1	F21	38	34	CLK0
1	G21	40	36	CLK1
1	F19	95	37	SINGLE_37
1	E19	93	38	SINGLE_38

9.5.2 DCI Terminations

These pins should be prohibited for place and route. These pins have no other purpose on the XRM-ETH.

FPGA		XRM-ETH		
Bank	Pin	Samtec	Value	Signal
0	G27	103	100	VRN_0
0	H27	101	100	VRP_0
1	G9	17	100	VRN_1
1	H9	19	100	VRP_1

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9.5.3 Ethernet MAC

All of these signals use VCCFPIO signalling levels. The VCCO selected by the jumper on the XRC-II/XPL should match the IOSTANDARD for these pins.

FPGA		XRM-ETH		
Bank	Pin	Samtec	MAC Signal	Comment
1	H20	62	RXC	O-ST
1	G20	64	TXC	O-ST
1	F15	66	PD	I
1	E15	68	TXER	I
1	C19	90	RXDV	O-PD
0	G22	97	RXD3	O-PD
0	F22	99	RXD2	O-PD
1	D19	92	RXD1	O-PD
0	E28	94	RXD0	O-PD
0	F28	96	TXEN	I
0	C29	98	TXD0	I
0	C28	100	TXD1	I
0	J22	102	TXD2	I
0	K22	104	TXD3	I
0	L27	106	COL	O-PD
0	K27	107	CRS	O-PD
1	E13	18	MDC	I-PU
1	F13	20	MDIO	IO-PU
1	K13	26	RST_N	I-PU
1	J13	28	RXER	O

Key

I	Input
O	Output
O-PD	Output with 2K pulldown
O-ST	Output with 25R source resistor

9.5.4 RS232

FPGA		XRM-ETH		
Bank	Pin	Samtec	J4 Header	Signal
0	C30	122	1	TX0
0	D30	124	3	RX0
0	M26	126	7	TX1
0	M25	128	9	RX1

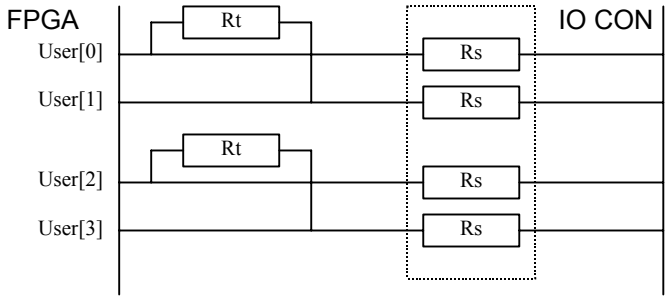
The header pin-out is show below.

Signal	Pin	Samtec	Signal
GND	2	1	TX0
GND	4	3	RX0
POL	6	5	NC
GND	8	7	TX1
GND	10	9	RX1

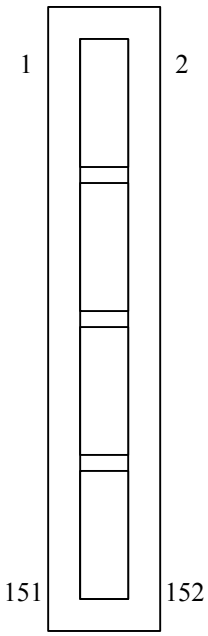
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10 User I/O XRM IO146 Front Panel Variant – Rev2.0

There are 146 I/O signals available on the front panel connector and these can be used individually or in pairs. All of these pins are compatible with 2.5V and 3.3V signaling (dependant on IO voltage setting on JP1). Care must be taken when using these signal pins not to exceed the maximum ratings for the V2PRO device.
Each pair of I/O signals is routed as shown below.



The default manufacturing option is Rs=0R and Rt not fitted. Other options are available. Rs can be used to provide series damping in point to point applications but for LVDS is 0R. Rt is required for LVDS inputs to provide the termination voltage from the line current.



Pin numbering looking into front of XRM IO146 connector

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Pin	Function	UCF name	Term Res	VII Pro Pin	Pin	Function	UCF name	Term Res	VII Pro Pin
1	Data[0] +ve	User[0]	R1	E10	2	Data[1] -ve	User[2]	R4	H13
3	Data[0] –ve	User[1]	-	D10	4	Data[1] +-ve	User[3]	-	G13
5	Data[2] +ve	User[4]	R3	E11	6	Data[3] +ve	User[6]	R2	D13
7	Data[2] –ve	User[5]	-	F11	8	Data[3] -ve	User[7]	-	C13
9	Data[4] +ve	User[8]	R5	H10	10	Data[5] +ve	User[10]	R6	L19
11	Data[4] –ve	User[9]	-	J10	12	Data[5] -ve	User[11]	-	M19
13	Data[6] +ve	User[12]	R7	F10	14	Data[7] +ve	User[14]	R8	K18
15	Data[6] –ve	User[13]	-	G10	16	Data[7] -ve	User[15]	-	L18
17	Data[8] +ve	User[16]	R9	G9(5)	18	Data[9] +ve	User[18]	R10	E13
19	Data[8] –ve	User[17]	-	H9(5)	20	Data[9] -ve	User[19]	-	F13
21	Data[10]+ve	User[20]	R11	H12	22	Data[11] +ve	User[22]	R12	F9
23	Data[10] –ve	User[21]	-	J12	24	Data[11] -ve	User[23]	-	E9
25	Data[12]+ve	User[24]	R14	L13	26	Data[13] +ve	User[26]	R15	K13
27	Data[12] –ve	User[25]	-	M13	28	Data[13] -ve	User[27]	-	J13
29	Data[14]+ve	User[28]	R16	K12	30	Data[15] +ve	User[30]	R17	C11
31	Data[14] –ve	User[29]	-	L12	32	Data[15] -ve	User[31]	-	C10
33	Single 0	User[34]	N/a	D16	34	Clock[0] +ve	User[32]	R64	F21
35	Single 1	User[35]	N/a	E19	36	Clock[0] -ve	User[33]	-	G21
37	+5V fused				38	Single 2	User[36]	N/a	C19

Pin	Function	UCF name	Term Res	VII Pro Pin	Pin	Function	UCF name	Term Res	VII Pro Pin
39	Data[16] +ve	User[40]	R19	F17	40	Data[17] +ve	User[42]	R20	G12
41	Data[16] –ve	User[41]	-	G17	42	Data[17] -ve	User[43]	-	F12
43	Data[18] +ve	User[44]	R23	C20	44	Data[19] +ve	User[46]	R22	J20
45	Data[18] –ve	User[45]	-	D20	46	Data[19] -ve	User[47]	-	H20
47	Data[20] +ve	User[48]	R25	L17	48	Data[21] +ve	User[50]	R24	E15
49	Data[20] –ve	User[49]	-	K17	50	Data[21] -ve	User[51]	-	F15
51	Data[22] +ve	User[52]	R27	H17	52	Data[23] +ve	User[54]	R26	C14
53	Data[22] –ve	User[53]	-	J17	54	Data[23] -ve	User[55]	-	C15
55	Data[24] +ve	User[56]	R29	G18	56	Data[25] +ve	User[58]	R28	L16
57	Data[24] –ve	User[57]	-	H18	58	Data[25] -ve	User[59]	-	M16
59	Data[26] +ve	User[60]	R37	E17	60	Data[27] +ve	User[62]	R30	J16
61	Data[26] –ve	User[61]	-	E18	62	Data[27] -ve	User[63]	-	K16
63	Data[28] +ve	User[64]	R41	J19	64	Data[29] +ve	User[66]	R38	H16
65	Data[28] –ve	User[65]	-	K19	66	Data[29] -ve	User[67]	-	G16
67	Data[30] +ve	User[68]	R44	G19	68	Data[31] +ve	User[70]	R42	M18
69	Data[30] –ve	User[69]	-	H19	70	Data[31] -ve	User[71]	-	M17
71	Single 3	User[37]	N/a	J27	72	Clock[1] +ve	User[72]	R67	K21
73	Single 4	User[38]	N/a	K27	74	Clock[1] –ve	User[73]	-	J21
75	+5V fused				76	Single 5	User[39]	N/a	F19

Pin	Function	UCF name	Term Res	VII Pro Pin	Pin	Function	UCF name	Term Res	VII Pro Pin
77	Data[32] +ve	User[74]	R48	G27	78	Data[33] +ve	User[76]	R45	C28
79	Data[32] –ve	User[75]	-	H27	80	Data[33] -ve	User[77	-	C29
81	Data[34] +ve	User[78]	R50	K26	82	Data[35] +ve	User[80]	R49	C30
83	Data[34] –ve	User[79]	-	L26	84	Data[35] -ve	User[81]	-	D30
85	Data[36] +ve	User[82]	R52	M24	86	Data[37] +ve	User[84]	R51	M26
87	Data[36] –ve	User[83]	-	L24	88	Data[37] -ve	User[85]	-	M25
89	Data[38] +ve	User[86]	R54	E26	90	Data[39] +ve	User[88]	R53	J26
91	Data[38] –ve	User[87]	-	E25	92	Data[39] -ve	User[89]	-	H26
93	Data[40] +ve	User[90]	R56	J31	94	Data[41] +ve	User[92]	R55	K24
95	Data[40] –ve	User[91]	-	H31	96	Data[41] -ve	User[93]	-	J24
97	Data[42] +ve	User[94]	R58	G33	98	Data[43] +ve	User[96]	R57	D23
99	Data[42] –ve	User[95]	-	F33	100	Data[43] -ve	User[97]	-	C23
101	Data[44] +ve	User[98]	R60	E34	102	Data[45] +ve	User[100]	R59	H24
103	Data[44] –ve	User[99]	-	F34	104	Data[45] -ve	User[101]	-	G24
105	Data[46] +ve	User[102]	R62	J33	106	Data[47] +ve	User[104]	R63	L25
107	Data[46] –ve	User[103]	-	H33	108	Data[47] -ve	User[105]	-	K25
109	Single 6	User[108]	N/a	D19	110	Clock[2] +ve	User[106]	R46	G22
111	Single 7	User[109]	N/a	E28	112	Clock[2] -ve	User[107]	-	F22
113	+5V fused				114	+5V fused			

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Pin	Function	UCF name	Tem Res	VII Pro Pin	Pin	Function	UCF name	Tem Res	VII Pro Pin
115	Data[48] +ve	User[110]	R65	C32	116	Data[49] +ve	User[112]	R61	K30
117	Data[48] -ve	User[111]	-	C33	118	Data[49] -ve	User[113]	-	J30
119	Data[50] +ve	User[114]	R68	H34(5)	120	Data[51] +ve	User[116]	R66	F24
121	Data[50] -ve	User[115]	-	G34(5)	122	Data[51] -ve	User[117]	-	E24
123	Data[52] +ve	User[118]	R71	D33	124	Data[53] +ve	User[120]	R69	L23
125	Data[52] -ve	User[119]	-	E33	126	Data[53] -ve	User[121]	-	K23
127	Data[54] +ve	User[122]	R73	C24	128	Data[55] +ve	User[124]	R72	H30
129	Data[54] -ve	User[123]	-	D24	130	Data[55] -ve	User[125]	-	G30
131	Data[56] +ve	User[126]	R77	F30	132	Data[57] +ve	User[128]	R74	H25
133	Data[56] -ve	User[127]	-	E30	134	Data[57] -ve	User[129]	-	G25
135	Data[58] +ve	User[130]	R79	L31	136	Data[59] +ve	User[132]	R78	F31
137	Data[58] -ve	User[131]	-	K31	138	Data[59] -ve	User[133]	-	G31
139	Data[60] +ve	User[134]	R81	G26	140	Data[61] +ve	User[136]	R80	M30
141	Data[60] -ve	User[135]	-	F26	142	Data[61] -ve	User[137]	-	L30
143	Data[62] +ve	User[138]	R84	F32	144	Data[63] +ve	User[140]	R21	H23
145	Data[62] -ve	User[139]	-	E32	146	Data[63] -ve	User[141]	-	J23
147	Single 8	User[144]	N/a	F28	148	Clock[3] +ve	User[142]	R47	J22
149	Single 9	User[145]	N/a	L27	150	Clock[3] -ve	User[143]	-	K22
151	+5V fused				152	+5V fused			

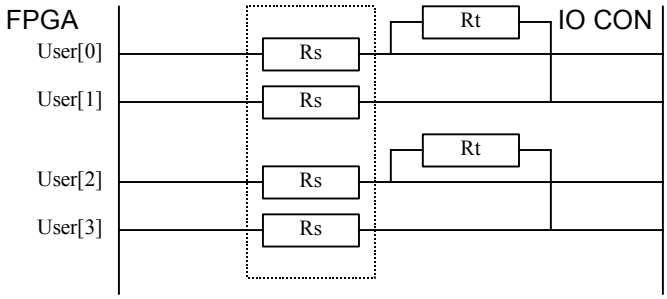
Notes

1) Data[] signals can be used for differential Pairs or single ended signals
2) Clock[] can be used for differential clocks or single ended clock signals
3) XRM I0146 connector – AMP/TYCO 767044-4 152 pin Mictor Receptacle
4) Suggested mating part – AMP/TYCO 1-767007-1 152 pin Mictor Plug or similar
5) When using the Virtex II Pro DCI these pins are not available for IO

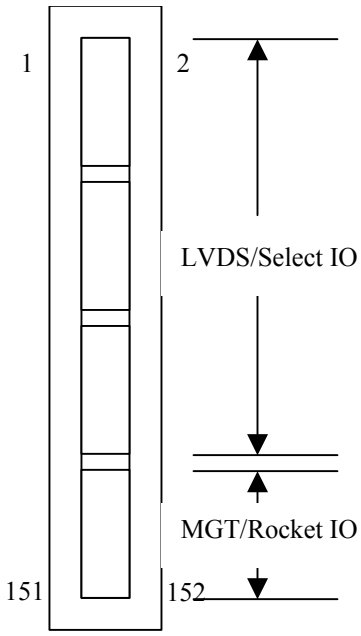
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11 User I/O XRM IO146 – Rocket

The XRM-IO146 - Rocket is based on the XRM-IO146 module but has bank 4 on the mictor used to bring out the 7 MGT channels available on the ADM-XP boards. The termination scheme on the differential and single ended IO has also been changed from the standard XRM-IO146 allowing termination for LVPECL and BLVDS standards to be implemented on the XRM module rather than externally.



The default manufacturing option is Rs=0R and Rt not fitted. Other options are available. Rs can be used to provide series damping in point to point applications but for LVDS is 0R. Rt is required for LVDS inputs to provide the termination voltage from the line current.



Pin numbering looking into front of XRM IO146 – Rocket connector

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Pin	Function	UCF name	Term Res	VII Pro Pin	Pin	Function	UCF name	Term Res	VII Pro Pin
1	Data[0]+ve	User[0]	R1	E10	2	Data[1]-ve	User[2]	R4	H13
3	Data[0]–ve	User[1]	-	D10	4	Data[1]+ve	User[3]	-	G13
5	Data[2]+ve	User[4]	R3	E11	6	Data[3]+ve	User[6]	R2	D13
7	Data[2]–ve	User[5]	-	F11	8	Data[3]-ve	User[7]	-	C13
9	Data[4]+ve	User[8]	R5	H10	10	Data[5]+ve	User[10]	R6	L19
11	Data[4]–ve	User[9]	-	J10	12	Data[5]-ve	User[11]	-	M19
13	Data[6]+ve	User[12]	R7	F10	14	Data[7]+ve	User[14]	R8	K18
15	Data[6]–ve	User[13]	-	G10	16	Data[7]-ve	User[15]	-	L18
17	Data[8]-ve	User[16]	R9	L20	18	Data[9]+ve	User[18]	R10	E13
19	Data[8]+ve	User[17]	-	K20	20	Data[9]-ve	User[19]	-	F13
21	Data[10]+ve	User[20]	R11	H12	22	Data[11]+ve	User[22]	R12	F9
23	Data[10]–ve	User[21]	-	J12	24	Data[11]-ve	User[23]	-	E9
25	Data[12]+ve	User[24]	R14	L13	26	Data[13]-ve	User[26]	R15	K13
27	Data[12]–ve	User[25]	-	M13	28	Data[13]+ve	User[27]	-	J13
29	Data[14]+ve	User[28]	R16	K12	30	Data[15]-ve	User[30]	R17	C11
31	Data[14]–ve	User[29]	-	L12	32	Data[15]+ve	User[31]	-	C10
33	Data[48]+ve	User[34]	N/a	C32	34	Clock[0]+ve	User[32]	R64	F21
35	Data[48]-ve	User[35]	N/a	C33	36	Clock[0]-ve	User[33]	-	G21
37	+5V fused				38	Single1	User[36]	N/a	D16

Pin	Function	UCF name	Term Res	VII Pro Pin	Pin	Function	UCF name	Term Res	VII Pro Pin
39	Data[16]+ve	User[40]	R19	F17	40	Data[17]+ve	User[42]	R20	G12
41	Data[16]–ve	User[41]	-	G17	42	Data[17]-ve	User[43]	-	F12
43	Data[18]+ve	User[44]	R23	C20	44	Data[19]+ve	User[46]	R22	J20
45	Data[18]–ve	User[45]	-	D20	46	Data[19]-ve	User[47]	-	H20
47	Data[20]+ve	User[48]	R25	L17	48	Data[21]+ve	User[50]	R24	E15
49	Data[20]–ve	User[49]	-	K17	50	Data[21]-ve	User[51]	-	F15
51	Data[22]+ve	User[52]	R27	H17	52	Data[23]+ve	User[54]	R26	C14
53	Data[22]–ve	User[53]	-	J17	54	Data[23]-ve	User[55]	-	C15
55	Data[24]+ve	User[56]	R29	G18	56	Data[25]+ve	User[58]	R28	L16
57	Data[24]–ve	User[57]	-	H18	58	Data[25]-ve	User[59]	-	M16
59	Data[26]+ve	User[60]	R37	E17	60	Data[27]+ve	User[62]	R30	J16
61	Data[26]–ve	User[61]	-	E18	62	Data[27]-ve	User[63]	-	K16
63	Data[28]+ve	User[64]	R41	J19	64	Data[29]+ve	User[66]	R38	H16
65	Data[28]–ve	User[65]	-	K19	66	Data[29]-ve	User[67]	-	G16
67	Data[30]+ve	User[68]	R44	G19	68	Data[31]+ve	User[70]	R42	M18
69	Data[30]–ve	User[69]	-	H19	70	Data[31]-ve	User[71]	-	M17
71	Data[49]+ve	User[37]	N/a	K30	72	Clock[1]+ve	User[72]	R67	K21
73	Data[49]-ve	User[38]	N/a	J30	74	Clock[1]–ve	User[73]	-	J21
75	+5V fused				76	Single12	User[39]	N/a	E24

Pin	Function	UCF name	Term Res	VII Pro Pin	Pin	Function	UCF name	Term Res	VII Pro Pin
77	Data[32]+ve	User[74]	R48	G27	78	Data[33]+ve	User[76]	R45	C28
79	Data[32]–ve	User[75]	-	H27	80	Data[33]-ve	User[77	-	C29
81	Data[34]+ve	User[78]	R50	K26	82	Data[35]+ve	User[80]	R49	C30
83	Data[34]–ve	User[79]	-	L26	84	Data[35]-ve	User[81]	-	D30
85	Data[36]+ve	User[82]	R52	M24	86	Data[37]+ve	User[84]	R51	M26
87	Data[36]–ve	User[83]	-	L24	88	Data[37]-ve	User[85]	-	M25
89	Data[38]+ve	User[86]	R54	E25	90	Data[39]+ve	User[88]	R53	J26
91	Data[38]–ve	User[87]	-	E26	92	Data[39]-ve	User[89]	-	H26
93	Data[40]+ve	User[90]	R56	J31	94	Data[41]+ve	User[92]	R55	K24
95	Data[40]–ve	User[91]	-	H31	96	Data[41]-ve	User[93]	-	J24
97	Data[42]+ve	User[94]	R58	G33	98	Data[43]+ve	User[96]	R57	D23
99	Data[42]–ve	User[95]	-	F33	100	Data[43]-ve	User[97]	-	C23
101	Data[44]+ve	User[98]	R60	E34	102	Data[45]+ve	User[100]	R59	H24
103	Data[44]–ve	User[99]	-	F34	104	Data[45]-ve	User[101]	-	G24
105	Data[46]+ve	User[102]	R62	J33	106	Data[47]+ve	User[104]	R63	L25
107	Data[46]–ve	User[103]	-	H33	108	Data[47]-ve	User[105]	-	K25
109	Data[50]+ve	User[108]	N/a	J22	110	Clock[2]+ve	User[106]	R46	G22
111	Data[50]-ve	User[109]	N/a	K22	112	Clock[2]-ve	User[107]	-	F22
113	+5V fused				114	+5V fused			

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Pin	Function UCF name	Tem Res	VII Pro Pin	Pin	Function UCF name	Tem Res	VII Pro Pin
115	MGT_SYS_RXP22	N/a	BB35	116	MGT_SYS_TXP22	N/a	BB36
117	MGT_SYS_RXN22	N/a	BB34	118	MGT_SYS_TXN22	N/a	BB37
119	MGT_SYS_RXP11	N/a	A3	120	MGT_SYS_TXP11	N/a	A4
121	MGT_SYS_RXN11	N/a	A2	122	MGT_SYS_TXN11	N/a	A5
123	Single 5	R71	D19	124	Single 7	R69	F28
125	Single 4	-	C19	126	Single 6	-	E28
127	MGT_SYS_RXP10	N/a	A7	128	MGT_SYS_TXP10	N/a	A8
129	MGT_SYS_RXN10	N/a	A6	130	MGT_SYS_TXN10	N/a	A9
131	MGT_SYS_RXP15	N/a	BB7	132	MGT_SYS_TXP15	N/a	BB8
133	MGT_SYS_RXN15	N/a	BB6	134	MGT_SYS_TXN15	N/a	BB9
135	MGT_SYS_RXP14	N/a	BB3	136	MGT_SYS_TXP14	N/a	BB4
137	MGT_SYS_RXN14	N/a	BB2	138	MGT_SYS_TXN14	N/a	BB5
139	MGT_SYS_RXP3	N/a	A35	140	MGT_SYS_TXP3	N/a	A36
141	MGT_SYS_RXN3	N/a	A34	142	MGT_SYS_TXN3	N/a	A37
143	MGT_SYS_RXP2	N/a	A39	144	MGT_SYS_TXP2	N/a	A40
145	MGT_SYS_RXN2	N/a	A38	146	MGT_SYS_TXN2	N/a	A41
147	Single 11	N/a	M27	148	Single 2	R47	E19
149	Single 10	N/a	L27	150	Single 3	-	F19
151	Single 9 *			152	Single 8 *		

Notes

1) Data[] signals can be used for differential Pairs or single ended signals
2) Clock[] can be used for differential clocks or single ended clock signals
3) XRM I0146 connector – AMP/TYCO 767044-4 152 pin Mictor Receptacle
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