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ADM-XRC-7Z1
User Manual

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1 Overview

1.1 Introduction

The **ADM-XRC-7Z1** ("**7Z1**") is a high-performance Processor XMC for applications using Zynq-7000 SoCs from Xilinx.

1.2 Key Features

Key Features

- Single-width XMC, compliant to VITA Standard 42.0, 42.3 and 42.10d12
- Zynq Z-7045 EPP in FFG900 package
- Processing System (PS) Block consisting of:
  - 1 bank of DDR3 SDRAM, 512MB
  - Quad SPI Flash memory, two 256Mb devices in dual-stacked configuration
  - Removable Secure Digital (SD) Flash memory (Commercial Spec Option)
  - Ethernet interface to rear-panel P4 connector
  - Serial COM port connection to rear P4 connector
  - Two USB ports to rear P4 connector
  - One USB port to micro USB connector (Commercial Spec Option)
- Programmable Logic (PL) Block consisting of:
  - 2 banks of DDR3 SDRAM, 256MB per bank
  - Ethernet interface to rear-panel P4 connector
  - Serial COM port connection to rear P4 connector
- "XRM" Front Panel IO Interface with:
  - 146 GPIO configurable as single-ended or differential signals
  - Up to 8 multi-gigabit High-Speed Serial IO (HSSIO)
  - Mux option for direct connections of Ethernet, USB and COM ports to Processor System
  - Reference clocks
- XMC Rear IO Interface P5:
  - VITA 42.3 Pinout
  - 8 HSSIO links to FPGA for PCI Express or user defined interface
  - PCI Express reference clock input
- XMC Rear IO Interface P6:
  - VITA 46.9d23 X38s+X12d+X8d compatible pinout
  - 8 HSSIO links (mux with XRM interface)
  - 38 GPIO
  - Reference clock input
- PMC Rear IO Interface P4:
  - Two Gigabit Ethernet interfaces
  - Two USB Ports

. Two Serial COM ports

- Platform manager with system monitoring

1.3 Order Code

ADM-XRC-7Z1/z-y(c)

Name	Symbol	Configurations
Kintex-7 Device	z	Z045 , Z100
Kintex-7 Speed	y	1 , 2 , 3
Cooling	c	blank = air cooled commercial /ACE = Extended air cooled commercial /AC1 = air cooled industrial /CC1 = conduction cooled industrial

Table 1 : Build Options

Not all combinations are available. Please check with Alpha Data sales for details.

1.4 References & Specifications

ANSI/VITA 42.0	*XMC Standard*, December 2008, VITA, ISBN 1-885731-49-3
ANSI/VITA 42.3	*XMC PCI Express Protocol Layer Standard*, June 2006, VITA, ISBN 1-885731-43-4
ANSI/IEEE 1386-2001	*IEEE Standard for a Common Mezzanine Card (CMC) Family*, October 2001, IEEE, ISBN 0-7381-2829-5
ANSI/IEEE 1386.1-2001	*IEEE Standard Physical and Environmental Layers for PCI Mezzanine Cards (PMC)*, October 2001, IEEE, ISBN 0-7381-2831-7
ANSI/VITA 20-2001 (R2005)	*Conduction Cooled PMC*, February 2005, VITA, ISBN 1-885731-26-4

Table 2 : References

2 PCB Information

2.1 Physical Specifications

Form Factor	Single Width XMC
Length (air-cooled)	149.0 mm
Length (conduction-cooled)	143.75 mm
Width	74.0 mm
Height	10.0 mm
Weight (air-cooled)	TBD
Weight (conduction-cooled)	TBD

Table 3 : Physical Specifications

2.2 Motherboard / Carrier Requirements

The **7Z1** is a single width XMC.3 mezzanine with P5, P6 and P4 connectors.

The **7Z1** is compatible with either 5V or 12V on the "VPWR" power rail.

The Primary XMC connector, P5, is compatible with the XMC.3 (VITA 42.3) specification for PCI Express applications.

The Secondary XMC connector, P6 also has a pinout compatible with XMC.3. Since carriers may have differing pinouts on this connector, it is important to check compatibility prior to installation. If in doubt, please contact Alpha Data for assistance.

IMPORTANT
Connector P6 on the card is not compatible with the VITA 42.10 (XMC GPIO) Standard. In particular, USB VCC must not be applied on this connector.

The PMC connector, P4, has the main interfaces to the ARM Processing System (PS): Ethernet, USB and serial ports. The pinout of this connector is compatible with other commercially available PrPMCs but is not defined by a VITA standard. It is important to check carrier card compatibility prior to installation. If in doubt, please contact Alpha Data for assistance.

IMPORTANT
Connector P4 has +5V (power) -/+6V (serial port) levels. It must not be connected to the Alpha Data ADM-EMC-II or ADM-XMC-II carrier cards. Please contact Alpha Data for carrier card compatibility.

2.3 Power Requirements

The power dissipation of the board is highly dependent on the Target FPGA application. A power estimator spreadsheet is available on request from Alpha Data. This should be used in conjunction with Xilinx's power estimation tools to determine the exact current requirements for each power rail.

3 Installation

3.1 Software Installation

Please refer to the Software Development Kit (SDK) installation CD. The SDK contains drivers, examples for host control and FPGA design and comprehensive help on application interfacing.

3.2 Hardware Installation

3.2.1 Handling Instructions

The components on this board can be damaged by electrostatic discharge (ESD). To prevent damage, observe ESD precautions:



- Always wear a wrist-strap when handling the card
- Hold the board by the edges
- Avoid touching any components
- Store in ESD safe bag.

3.2.2 Installation in ADC-XMC-Breakout Carrier

Note:
Note: This operation should only be performed while the ADC-XMC-Breakout carrier is not powered.

The **7Z1** should be secured to the **ADC-XMC-Breakout** carrier using M2.5 screws in the four holes provided.

Refer to the **ADC-XMC-Breakout** carrier documentation for switch configurations.

4 Functional Description

4.1 Overview

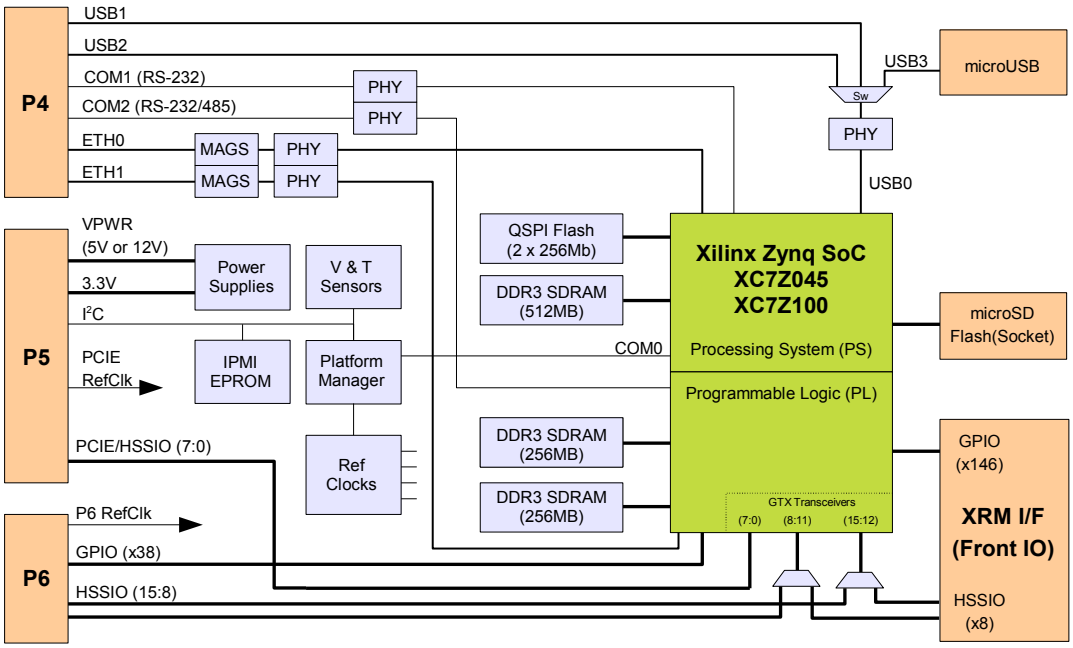


Figure 1 : ADM-XRC-7Z1 Block Diagram

4.1.1 Switch Definitions

There are two sets of 8-way DIP switches for configuring the board.

Switch 1 Ref.	Function	OFF State	ON State
SW1-1	Reserved	-	-
SW1-2	Flash Boot Inhibit	Allow PS to boot PL from flash	Prohibit PS booting PL from flash
SW1-3	System Monitor Upgrade	Normal Operation	Reserved for factory use
SW1-4	Reserved	-	-
SW1-5	XMC JTAG	Isolate JTAG chain from P5	Connect JTAG chain to P5
SW1-6	MGT(3:0) Mux Sel	MGT(3:0) routed to P6	MGT(3:0) routed to XRM
SW1-7	MGT(7:4) Mux Sel	MGT(7:4) routed to P6	MGT(7:4) routed to XRM
SW1-8	Reserved	-	-

Table 4 : Switch 1 Definitions

Switch 1 Ref.	Function	OFF State	ON State
SW2-1	BootSel 0	See Table 15	
SW2-2	BootSel 1	See Table 15	
SW2-3	Independent JTAG	Single (cascaded) JTAG chain at J4	Independent JTAG chains
SW2-4	PLL Bypass	PS PLL is used	PS PLL is bypassed
SW2-5	InhExtRst	Do not mask MRSTI#	Mask MRSTI# when ROOT# is asserted
SW2-6	Reserved	-	-
SW2-7	USB3 Mode	Zynq PS is USB Host and USB3 is downstream port	USB3 is OTG port
SW2-8	System Reset	Normal operation	PS System Reset

Table 5 : Switch 2 Definitions

4.1.2 LED Definitions

There are seven LEDs to provide a visual indication of the board status.

Their locations are shown in Figure 2

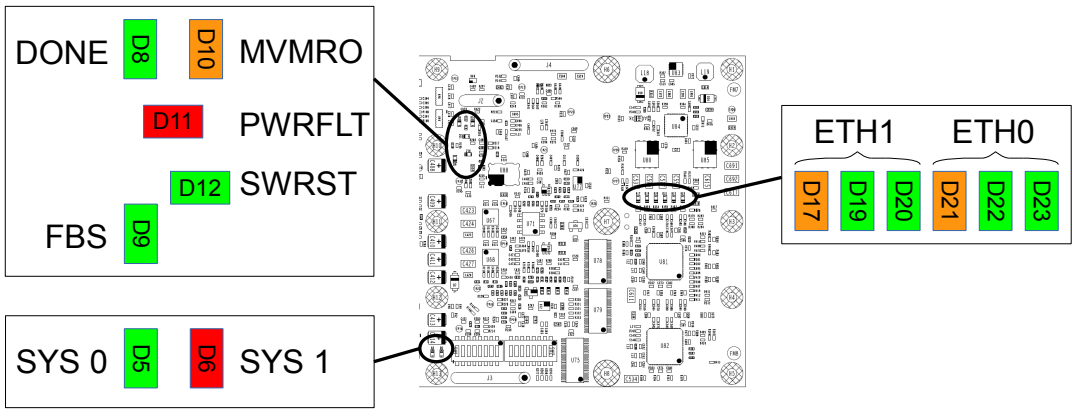


Figure 2 : LED Locations

Comp. Ref.	Function	ON State	Off State
D5 (Green)	System Monitor Status	See Table 23	
D6 (Red)	System Monitor Status	See Table 23	
D8 (Green)	FPGA (PL) Done	PL is configured	PL is not configured
D9 (Green)	Flash Boot Enable	Enable PS booting PL from flash	Disable PS booting PL from flash
D10 (Amber)	MVMRO	Enable writes to non-volatile memories	Inhibit writes to non-volatile memories
D11 (Red)	Power Fault	Power Supply Fault	Power Supplies off or within range
D12 (Green)	System Reset	PS is in Reset	PS is not in Reset

Table 6 : Main LED Definitions

A further two sets of three LEDs provide an indication of the status of the two Ethernet interfaces

Comp. Ref.	Function	ON State	Off State
D23 (Green)	Ethernet 0 LED0	See Table 16	
D22 (Green)	Ethernet 0 LED1	See Table 16	
D21 (Amber)	Ethernet 0 LED2	See Table 16	
D20 (Green)	Ethernet 1 LED0	See Table 16	
D19 (Green)	Ethernet 1 LED1	See Table 16	
D17 (Amber)	Ethernet 1 LED2	See Table 16	

Table 7 : Ethernet LED Definitions

4.2 Primary XMC Connector P5

Full pinout information for this connector is listed in Table 24

4.2.1 XMC Platform Interface

4.2.1.1 IPMI I2C

A 2 Kbit I2C EEPROM (type M24C02) is connected to the XMC IPMI. This memory contains board information (type, voltage requirements etc.) as defined in the XMC based specification.

4.2.1.2 MBIST#

Built-In Self Test. This output signal is not used and is driven inactive (high) by the CPLD when the board is powered.

4.2.1.3 MVMRO

XMC Write Prohibit. This signal is an input from the carrier. When asserted (high), all writes to non-volatile memories are inhibited. Amber LED D10 indicates a warning when this signal is not set and writes to non-volatile memory are enabled. The signal has a 100k pull-up resistor to assert it by default.

This signal cannot be internally driven or over-ridden. A buffered version of the signal is connected to the Zynq PS at MIO50 (pin A19).

4.2.1.4 MRSTI#

XMC Reset In. This signal is an active low input from the carrier and should be used to reset any PCIE endpoint. It is translated to 1.5V levels and connected to the Zynq PL at pin K2.

MRSTI# can also be used to fully reset the board by asserting the Zynq PS_POR_B input. This may not be desirable and can be inhibited by turning switch SW2-5 ON.

4.2.1.5 MRSTO#

XMC Reset Out. This optional output signal is connected to the Zynq PL at pin J4. It should only be driven when the board is connected to a master or Root Complex carrier slot.

4.2.1.6 MPRESENT#

Module Present. This output signal is connected directly to 0V.

4.2.1.7 JTAG

See Section Section 4.5

4.2.2 P5 HSSIO Links

Eight pairs of HSSIO links from the Zynq PL are routed to XMC connector P6.

The pinout and coupling of these links are compatible with PCI Express.

The Transmit (Tx) side of all eight lanes are AC coupled by 100nF capacitors, placed at the output from the PL.

The Receive (Rx) side of all eight lanes are directly connected from the connector to the PL.

Alternative coupling options are available as a special ordering option. Please contact Alpha Data for details.

4.3 Secondary XMC Connector P6

Full pinout information for this connector is listed in Table 25

4.3.1 P6 HSSIO Links

Eight pairs of HSSIO links from the Zynq PL can be routed to XMC connector P6.

HSSIO Lanes (3:0) are routed to either P6(3:0) or XRM(3:0) using DIP switch SW1-6. (See Table 4)

HSSIO Lanes (7:4) are routed to either P6(7:4) or XRM(7:4) using DIP switch SW1-7. (See Table 4)

The Tx side of all eight lanes are directly connected from the PL to the connector.

The Rx side of all eight lanes are AC coupled by 100nF capacitors, placed at the input to the PL.

Alternative coupling options are available as a special ordering option. Please contact Alpha Data for details.

4.3.2 P6 GPIO Signals

There are 38 GPIO signals connected between P6 and the Zynq PL high-range bank 10.

The signals are routed differentially and can therefore can be used as 38 single-ended signals or as 19 differential pairs.

The signals are connected through level-clamping quick-switches to give 3.3V compatibility at the XMC interface. Input signals are clamped at 2.5V by the quick-switches, while 2.5V outputs from the PL are passed straight through.

The quick-switches have a very low ON resistance and are suitable for high-speed LVDS interfacing in either direction.

4.4 PrPMC Connector P4

PrPMC connector P4 has two sets of Ethernet, Serial COM port and USB interfaces.

Details of the Ethernet interfaces are given in Section 4.8.3

Details of the Serial COM Ports are given in Section 4.8.4

Details of the USB Ports are given in Section 4.8.5

Full pinout information for this connector is listed in Table 26

4.5 JTAG Interfaces

4.5.1 On-board Interface

By default, the **7Z1** is configured to have a single (cascaded) JTAG scan chain connected to header J4. This allows the connection of the Xilinx JTAG cable for debug using the Xilinx ChipScope tools.

The board can also be set to have two independent scan chains using DIP switch SW2-3. (See Table 5). In independent mode, the main chain (with the Zynq PL, CPLD and XRM interface) is connected to J4, while the Zynq PS is connected to header J3.

If the cascaded or main scan chain is connected to the XMC connector (when SW1-5 is ON), header J4 should not be used.

4.5.2 XMC Interface

The JTAG interface on the XMC connector is normally unused and XMC_TDI connected directly to XMC_TDO.

The interface can be connected to the cascaded or main interface (through level-translators) by switching SW1-5 ON. See Table 4

4.5.3 JTAG Voltages

The on-board JTAG scan chains uses 1.8V. The Vcc supply provided on J3 and J4 to the JTAG cable is +1.8V and is protected by a poly fuse rated at 350mA. 3.3V signals must not be used at header J3 or J4.

The JTAG signals at the XMC interface use 3.3V signals and are connected through level translators to the on-board scan chain.

The JTAG signals at the XRM2 interface use the adjustable voltage XRM_VIO.

4.6 Clocks

The board has nine reference clocks: two from the carrier, and seven generated on-board.

The clocks MGTCLK250M, PROGCLK, REFCLK200M and ETH_CLK25M are generated by a single Silicon Labs Si5338B and are all synchronous.

Note:
Clock Termination
The LVDS clocks do not have termination resistors on the circuit board. On-die terminations in the FPGA must be enabled by setting the attribute "DIFF_TERM = TRUE". This can either be set in the source code when instantiating the buffer, or in the design constraints file.

4.6.1 PCIe Reference Clock (PCIEREFCLK)

The 100MHz PCI Express reference clock is provided by the carrier card through the Primary XMC connector, P5, at pins A19 and B19. This is connected to the Zynq PL via 10nF AC coupling capacitors. On the Zynq PL, it is connected to GTX Quad 112 to allow its use as reference for the eight GTX lanes on Quads 111 and 112.

Signal	Target FPGA Input	IO Standard	"P" pin	"N" pin
PCIEREFCLK	MGTREFCLK0_112	HSCL	N8	N7

Table 8 : PCIEREFCLK Connections

4.6.2 P6 Reference Clock (P6REFCLK)

A reference clock can be provided by the carrier card through the Secondary XMC connector, P6, at pins A19 and B19. This is connected to the Zynq PL via 10nF AC coupling capacitors. On the Zynq PL, it is connected to GTX Quad 109 to allow its use as reference for the eight GTX lanes on Quads 109 and 110.

Signal	Target FPGA Input	IO Standard	"P" pin	"N" pin
P6REFCLK	MGTREFCLK0_109	LVDS or HSCL	AD10	AD9

Table 9 : P6REFCLK Connections

4.6.3 MGTCLK250M

The fixed 250.0MHz reference clock, MGTCLK250M, is a differential clock signal using LVDS. Two phase matched copies are MGTREFCLK inputs on the Zynq PL at GTX Quad 109 and 111. Since each input can clock the adjacent GTX Quads, this clock can be used by all GTX links on the board.

Signal	Target FPGA Input	IO Standard	"P" pin	"N" pin
MGTCLK250M_A	MGTREFCLK0_111	LVDS_25	U8	U7
MGTCLK250M_B	MGTREFCLK1_109	LVDS_25	AF10	AF9

Table 10 : MGTCLK250M Connections

4.6.4 PROGCLK

The programmable clock, PROGCLK, is a differential clock signal using LVDS. It is connected to MGTREFCLK inputs on the Zynq PL at GTX Quad 110. Since this input can clock the adjacent GTX Quads, it can be used by the GTX links on quads 109 and 111.

Signal	Target FPGA Input	IO Standard	"P" pin	"N" pin
PROGCLK	MGTREFCLK1_110	LVDS_25	AC8	AC7

Table 11 : PROGCLK Connections

4.6.5 REFCLK200M

The fixed 200MHz reference clock, REFCLK200M, is a differential clock signal using LVDS. Three phase-matched copies are distributed to Global Clock inputs on the Zynq PL.

This clock can be used to generate application-specific clock frequencies using the PLLs within the Zynq PL. It is also suitable as the reference clock for the IO delay control block (IDELAYCTRL) and memory interfaces.

Signal	Target FPGA Input	IO Standard	"P" pin	"N" pin
REFCLK200M_A	IO_L13_MRCCC_10	LVDS_25	AG17	AG16
REFCLK200M_B	IO_L12_MRCC_33	SSTL15	G5	G4
REFCLK200M_C	IO_L13_MRCC_33	SSTL15	F5	E5

Table 12 : REFCLK200M Connections

4.6.6 PS_CLK33M3

The Zynq PS is provided with a 33.333MHz reference clock at the PS_CLK input on pin A22. This clock is asynchronous to the clocks generated by the Si5338B.

Signal	Target FPGA Input	IO Standard	"P" pin	"N" pin
PS_CLK33M3	PS_CLK_500	LVCMOS18	A22	-

Table 13 : PS_CLK33M3 Connections

4.6.7 USB_REFCLK24M

The USB PHY and hub are provided with an independent 24.0MHz reference clock. This clock is asynchronous to the clocks generated by the Si5338B and is not connected to the Zynq SoC.

4.6.8 ETH_CLK25M

The Ethernet PHYs are provided with 25.0MHz reference clocks generated by the Si5338B. These are not connected to the Zynq SoC.

4.6.9 ETH1_CLK125M

The Ethernet PHY 1 generates a 125MHz reference clock that is connected to the Zynq PL at pin AF14.

Signal	Target FPGA Input	IO Standard	"P" pin	"N" pin
ETH1_CLK125M	IO_L12_MRCC_10	LVCMOS25	AF14	-

Table 14 : ETH1_CLK125M Connections

4.7 Resets

The Zynq PS can be reset using the System Reset switch, SW2-8.

4.8 Zynq PS Block

4.8.1 Boot Modes

BootSel1 (SW2-2)	BootSel0 (SW2-1)	Boot Mode
OFF	OFF	JTAG
OFF	ON	Quad SPI
ON	OFF	SD Flash
ON	ON	Reserved

Table 15 : Boot Mode Selection

4.8.2 PS Memory Interfaces

4.8.2.1 Quad SPI Flash Memory

512Mb of QSPI flash memory (Micron N25Q256A11E1240E/MT41K128M16JT) is attached to the PS, and is used to store Zynq boot images, FPGA bitstreams and data.

4.8.2.2 MicroSD Flash Memory

An on-board microSD card holder is available to store Zynq boot images, FPGA bitstreams and data.

4.8.2.3 PS DDR3 Memory

The PS has one bank of DDR3 memory, consisting of 2 16-bit wide memory devices in parallel to provide a 32-bit data-path capable of running up to 533MHz (DDR-1066). 2Gb devices (Micron MT41K128M16JT-125) are fitted as standard to provide 512MB per bank.

4.8.3 Ethernet Interfaces

The **7Z1** has two 1000BASE-T Ethernet Interfaces at rear connector P4. Interface ETH0 is connected to the Zynq PS, while ETH1 is connected to the PL

Both interfaces have a Marvell 88E1512 PHY, connected to the Zynq via RGMII.

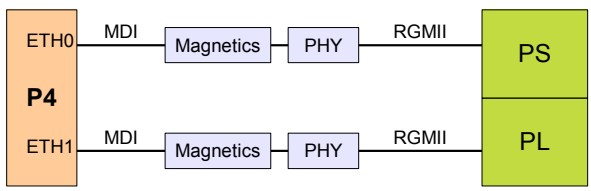


Figure 3 : Ethernet Interfaces

Each interface has three status LEDs. The functions of these are shown in Table 16 below.

LED	Colour	Function
0	Green	
1	Green	
2	Amber	

Table 16 : Ethernet Status LEDs

4.8.4 Serial COM Ports

There are two serial COM ports connected to PMC connector P4, as shown in Figure Serial COM Ports.

COM2 uses RS-232 by default but may be configured for RS-485 operation. Please contact Alpha Data for further details of the RS-485 mode.

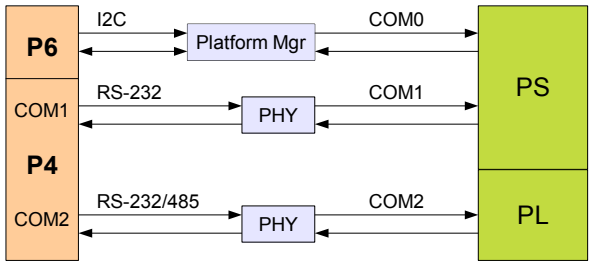


Figure 4 : Serial COM Ports

4.8.5 USB Interfaces

The **7Z1** has three external USB interfaces. Interfaces USB1 and USB2 are connected to rear connector P4, and USB3 is connected to microUSB connector J1.

By default, the Zynq PS is configured as the USB host to the three external interfaces. However, USB3 can be set as the host interface by turning on Switch SW2-7. In this case, interface USB0 to the Zynq PS becomes a downstream port.

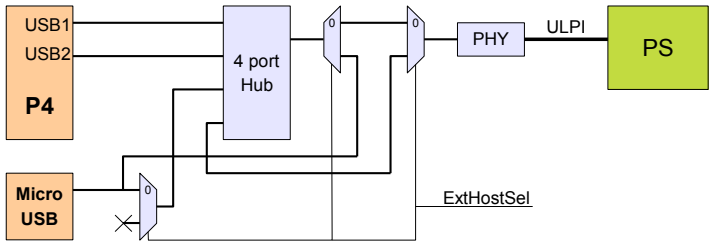


Figure 5 : USB Interfaces

4.9 Zynq PL Block

4.9.1 PL DDR3 Memory

The PL has two banks of DDR3 memory, each consisting of a single 16-bit wide memory device, capable of running up to 800MHz (DDR-1600). 2Gb devices (Micron MT41J64M16-187E) are fitted as standard to provide 256MB per bank.

The memory banks are arranged for compatibility with the Xilinx Memory Interface Generator (MIG). Full details of the interface, signalling standards are provided in the example design.

4.9.2 XRM Interface and Front-Panel I/O

The XRM interface provides a high-performance and flexible front-panel interface through a range of interchangeable XRM modules. Further details of the XRM modules can be found on the Alpha Data website.

The XRM interface consists of two Samtec connectors, CN1 and CN2.

4.9.2.1 XRM Connector, CN1

Connector CN1 is for general purpose signals, power and module control. The connector is a 180-way Samtec connector with 3 fields.

The part fitted to the **ADM-XRC-KU1** is Samtec QSH-090-01-F-D-A-K.

Full pinout information for this connector is listed in XRM Connector CN1, Field 1 to XRM Connector CN1, Field 3.

4.9.2.2 XRM Connector CN2

Connector CN2 is for the high-speed serial (MGT) links.

The part fitted to the **ADM-XRC-KU1** is Samtec QSE-014-01-F-D-DP-A-K.

Full pinout information for this connector is listed in Secondary XMC Connector, P6.

4.9.2.3 XRM I/F - GPIO

The general purpose IO (GPIO) signals are connected in 4 groups to the Target FPGA. Each group consists of 16 standard I/O pairs, a Regional Clock Capable pair and either 2 or 4 single-ended signals. There are no on-board terminations on the pairs and any can be used in single-ended modes.

To allow fast data transfer, all of the GPIO signals within a group are delay matched to within 100ps.

All the XRM GPIO signals and FPGA IO banks share a common voltage, XRM_VIO, that can be either 1.8V, 1.5V or 1.2V. The required voltage is stored within the platform management PROM on the XRM.

Group	FPGA Bank	Name	Function
Group A	16-17	XRM_DA (15:0)	16 diff. Pairs / 32 single-ended
		XRM_DA_CC (16)	Regional Clock / GPIO pair / 2 single-ended
		SA (1:0)	2 single-ended GPIO
Group B	15-16	XRM_DB (15:0)	16 diff. Pairs / 32 single-ended
		XRM_DB_CC (16)	Regional Clock / GPIO pair / 2 single-ended
		SB (1:0)	2 single-ended GPIO
Group C	15	XRM_DC (15:0)	16 diff. Pairs / 32 single-ended
		XRM_DC_CC (16)	Regional Clock / GPIO pair / 2 single-ended
		SC (1:0)	2 single-ended GPIO
Group D	17	XRM_DD (15:0)	16 diff. Pairs / 32 single-ended
		XRM_DD_CC (16)	Regional Clock / GPIO pair / 2 single-ended
		SD (3:0)	4 single-ended GPIO

Table 17 : XRM GPIO Groups

4.9.2.4 XRM I/F - High-speed Serial Links

Eight MGT links are routed between the Target FPGA and the XRM interface. Lanes (6:0) are routed through the Samtec QSE-DP connector, CN2. Lane (7) is routed through the Samtec QSH connector, CN1.

4.9.2.5 XRM IO Voltage Override

Each XRM is built with an I2C EEPROM that contains vital product information (VPD) such as part number, serial number, operating voltage, and product specific information. For designing custom XRMs, contact Alpha-Data for

details on duplicating this VPD data.

Alternatively, FORCE2V5_L can be driven low to select 1.8V for the front I/O voltage. Note that FORCE2V5_L is a signal name from a historical design, and the operating voltage will not be 2.5V but rather 1.8V if this mode is used.

4.9.3 GTX Links

The PL has 8 GTX links to the P5 connector and 8 GTX lanes to the P6 connector (full pinout information for these connectors are listed in Secondary XMC Connector, P5 and Secondary XMC Connector, P6.

The 8 lanes to the P6 connector can be switched to connect to the XRM CN2 connector instead of the P6 connector, using SW1-6 and SW1-7. (See Table 4)

The pin mappings are as follows:

Signal	FPGA + Pin	FPGA - Pin	Rear Connector + Pin	Rear Connector - Pin
P5_TX_0	N4	N3	P5.A1	P5.B1
P5_TX_1	P2	P1	P5.D1	P5.E1
P5_TX_2	R4	R3	P5.A3	P5.B3
P5_TX_3	T1	T1	P5.D3	P5.E3
P5_TX_4	V2	V1	P5.A5	P5.B5
P5_TX_5	W4	W3	P5.D5	P5.E5
P5_TX_6	Y1	Y2	P5.A7	P5.B7
P5_TX_7	AB2	AB1	P5.D7	P5.E7
-	-	-	-	-
P5_RX_0	P5	P6	P5.A11	P5.B11
P5_RX_1	T6	T5	P5.D11	P5.E11
P5_RX_2	U4	U3	P5.A13	P5.B13
P5_RX_3	V6	V5	P5.D13	P5.E13
P5_RX_4	AA4	AA3	P5.A15	P5.B15
P5_RX_5	Y6	Y5	P5.D15	P5.E15
P5_RX_6	AB6	AB5	P5.A17	P5.B17
P5_RX_7	AC4	AC3	P5.D17	P5.E17

Table 18 : PL RearMGT Mapping

Signal	FPGA + Pin	FPGA - Pin	Rear Connector + Pin	Rear Connector - Pin
P6_TX_0	AH2	AH1	P6.A1	P6.B1
P6_TX_1	AF2	AF1	P6.D1	P6.E1
P6_TX_2	AE4	AE3	P6.A3	P6.B3
P6_TX_3	AD2	AD1	P6.D3	P6.E3
P6_TX_4	AK10	AK9	P6.A5	P6.B5
P6_TX_5	AK6	AK5	P6.D5	P6.E5

Table 19 : PL RearMGT Mapping (continued on next page)

Signal	FPGA + Pin	FPGA - Pin	Rear Connector + Pin	Rear Connector - Pin
P6_TX_6	AJ4	AJ3	P6.A7	P6.B7
P6_TX_7	AK2	AK1	P6.D7	P6.E7
-	-	-	-	-
P6_RX_0	AH6	AH5	P6.A11	P6.B11
P6_RX_1	AG4	AG3	P6.D11	P6.E11
P6_RX_2	AF6	AF5	P6.A13	P6.B13
P6_RX_3	AD6	AD5	P6.D13	P6.E13
P6_RX_4	AH10	AH9	P6.A15	P6.B15
P6_RX_5	AJ8	AJ7	P6.D15	P6.E15
P6_RX_6	AG8	AG7	P6.A17	P6.B17
P6_RX_7	AE8	AE7	P6.D17	P6.E17

Table 19 : PL RearMGT Mapping

4.9.4 Rear GPIO Interface

38 single ended or 19 differential GPIO signals are available on the P6 connector. The pin mappings are as follows:

Signal	FPGA + Pin	FPGA - Pin	Rear Connector + Pin	Rear Connector - Pin
P6_X38s_0	AJ16	AK15	P5.C19	P5.C18
P5_X38s_1	AH18	AJ18	P5.F19	P5.F18
P5_X38s_2	AJ15	AK15	P5.C17	P5.C16
P5_X38s_3	AH17	AH16	P5.F17	P5.F16
P5_X38s_4	AJ14	AJ13	P5.C15	P5.C14
P5_X38s_5	AK13	AK12	P5.F15	P5.F14
P5_X38s_6	AH14	AH13	P5.C13	P5.C12
P5_X38s_7	AG12	AH12	P5.F13	P5.F12
P5_X38s_8	AE12	AF12	P5.C11	P5.C10
P5_X38s_9	AE13	AF13	P5.F11	P5.F10
P5_X38s_10	AC14	AC13	P5.C9	P5.C8
P5_X38s_11	AD14	AD13	P5.F9	P5.F8
P5_X38s_12	AA15	AA14	P5.C7	P5.C6
P5_X38s_13	AB12	AC12	P5.F7	P5.F6
P5_X38s_14	AE16	AE15	P5.C5	P5.C4
P5_X38s_15	AF15	AG15	P5.F5	P5.F4
P5_X38s_16	AE18	AE17	P5.C3	P5.C2
P5_X38s_17	AD16	AD15	P5.F3	P5.F2
P5_X38s_18	AF18	AF17	P5.C1	P5.F1

Table 20 : PL Rear GPIO Mapping

4.10 System Monitoring

The **7Z1** has the ability to monitor temperature and voltage to maintain a check on the operation of the board. The monitoring is implemented using an Atmel AVR microcontroller (uC).

The microcontroller continually measures all voltage rails and temperature sensors and transmits the results to the FPGA, where they are stored in block-ram.

The following voltage rails and temperatures are monitored by the microcontroller:

Monitor	*Purpose*
VPWR	Board Input Supply (either 5.0V or 12.0V)
12V0	12V Board Input Supply
5V0	5V Board Input Supply
3V3	Board Input Supply
2V5	FPGA IO Supply
AUX_IO_2V0	FPGA Aux IO Supply
1V8	FPGA Aux Supply, Flash Memory
MGT_AUX_1V8	FPGA MGT Aux Supply
1V5	DDR3 SDRAM, Target FPGA memory I/O
VIO	Variable XRM IO Supply
1V0	FPGA Core Supply (VccINT)
MGT_1V2	FPGA MGT Vtt Supply
MGT_1V0	FPGA MGT Vcc Supply
3V3_INT	Internal 3.3V Supply
Temp1	microcontroller internal temperature
Temp2	TMP422 internal temperature
Temp3	FPGA on-die temperature (measured in TMP422)

Table 21 : Voltage and Temperature Monitors (in microcontroller)

The SDK includes an example application ("monitor") that read the system monitor sensor values.

4.10.1 Automatic Temperature Monitoring

The system monitor checks that the board and FPGA are being operated within the specified limits. If the temperature is close to the limit, a "Warning Alarm" interrupt is set.

If a limit is exceeded, a "Critical Alarm" interrupt is set. After the Critical Alarm is set, there is a 5 second delay before the system monitor unconfigures the FPGA by asserting its "PROG" pin.

The purpose of this mechanism is to protect the card from damage due to over-temperature. It is possible that it will cause the user application and, possibly, the host computer to "hang".

The temperature limits are shown in Table Temperature Limits. Note that the Min and Max values include a 5°C margin to prevent measurement errors triggering a false alarm.

	Target FPGA				Board (uC and PCB)			
	Min	Lower Warning	Upper Warning	Max	Min	Lower Warning	Upper Warning	Max
Commercial	-5°C	+5°C	+80°C	+90°C	-5°C	+5°C	+65°C	+75°C
Extended	-5°C	+5°C	+95°C	+105°C	-5°C	+5°C	+80°C	+90°C
Industrial	-45°C	-35°C	+95°C	+105°C	-45°C	-35°C	+80°C	+90°C

Table 22 : Temperature Limits

4.10.2 System Monitor Status LEDs

LEDs D5 (Green) and D6 (Red) indicate the microcontroller status.

LEDs	*Status*
Flashing Green + Flashing Red (alternate)	Service Mode
Red	Missing application firmware or invalid firmware
Red + Green	Standby (Powered off)
Green	Running and no alarms
Flashing Green + Red	Attention - alarm active
Flashing Green + Flashing Red (together)	Attention - critical alarm active
Flashing Red	FPGA configuration cleared to protect board

Table 23 : System Monitor Status LEDs

Appendix A: Rear Connector Pinouts

Appendix A.1: Primary XMC Connector, P5

	A	B	C	D	E	F
1:	PET0p0	PET0n0	3.3V	PET0p1	PET0n1	VPWR(3)
2:	GND	GND	XMC_TRST#	GND	GND	MRSTI#
3:	PET0p2	PET0n2	3.3V	PET0p3	PET0n3	VPWR(3)
4:	GND	GND	XMC_TCK	GND	GND	MRSTO#
5:	PET0p4	PET0n4	3.3V	PET0p5	PET0n5	VPWR(3)
6:	GND	GND	XMC_TMS	GND	GND	+12V
7:	PET0p6	PET0n6	3.3V	PET0p7	PET0n7	VPWR(3)
8:	GND	GND	XMC_TDI	GND	GND	-12V
9:	-	-	-	-	-	VPWR(5)
10:	GND	GND	XMC_TDO	GND	GND	GA0
11:	PER0p0	PER0n0	MBIST#	PER0p1	PER0n1	VPWR(3)
12:	GND	GND	GA1	GND	GND	MPRESENT#
13:	PER0p2	PER0n2	3.3V AUX(2)	PER0p3	PER0n3	VPWR(3)
14:	GND	GND	GA2	GND	GND	MSDA
15:	PER0p4	PER0n4	-	PER0p5	PER0n5	VPWR(3)
16:	GND	GND	MVMRO	GND	GND	MSCL
17:	PER0p6	PER0n6	-	PER0p7	PER0n7	-
18:	GND	GND	-	GND	GND	-
19:	REFCLK+0	REFCLK-0	-	WAKE#	ROOT0#	-
Notes:	(1) PCIe Channel Lanes (7:0) are directly connected to the Target FPGA.					
	(2) 3.3V AUX is required.					
	(3) VPWR can be either +5V or +12V.					

Table 24 : XMC Connector P5

Appendix A.2: Secondary XMC Connector, P6

	A	B	C	D	E	F
1:	P6_TXp0	P6_TXn0	GPIO_18P	P6_TXp1	P6_TXn1	GPIO_18N
2:	GND	GND	GPIO_16N	GND	GND	GPIO_17N
3:	P6_TXp2	P6_TXn2	GPIO_16P	P6_TXp3	P6_TXn3	GPIO_17P
4:	GND	GND	GPIO_14N	GND	GND	GPIO_15N
5:	P6_TXp4	P6_TXn4	GPIO_14P	P6_TXp5	P6_TXn5	GPIO_15P
6:	GND	GND	GPIO_12N	GND	GND	GPIO_13N
7:	P6_TXp6	P6_TXn6	GPIO_12P	P6_TXp7	P6_TXn7	GPIO_13P
8:	GND	GND	GPIO_10N	GND	GND	GPIO_11N
9:	-	-	GPIO_10P	-	-	GPIO_11P
10:	GND	GND	GPIO_8N	GND	GND	GPIO_9N
11:	P6_RXp0	P6_RXn0	GPIO_8P	P6_RXp1	P6_RXn1	GPIO_9P
12:	GND	GND	GPIO_6N	GND	GND	GPIO_7N
13:	P6_RXp2	P6_RXn2	GPIO_6P	P6_RXp3	P6_RXn3	GPIO_7P
14:	GND	GND	GPIO_4N	GND	GND	GPIO_5N
15:	P6_RXp4	P6_RXn4	GPIO_4P	P6_RXp5	P6_RXn5	GPIO_5P
16:	GND	GND	GPIO_2N	GND	GND	GPIO_3N
17:	P6_RXp6	P6_RXn6	GPIO_2P	P6_RXp7	P6_RXn7	GPIO_3P
18:	GND	GND	GPIO_0N	GND	GND	GPIO_1N
19:	P6_RefClkP	P6_RefClkN	GPIO_0P	-	-	GPIO_1P
Notes:	(1) MGT Lanes are connected directly to the Target FPGA.					
	(2) GPIO signals are single-ended and 3.3V compatible.					

Table 25 : XMC Connector P6

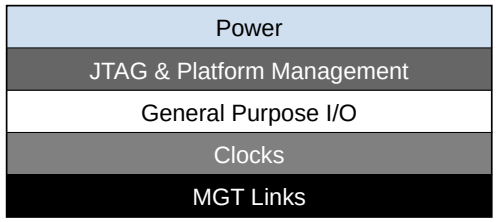
Appendix A.3: PMC Connector P4

Signal	Pin J14	Pin J14	Signal
ETH0_DA+	1	2	ETH0_DC+
ETH0_DA-	3	4	ETH0_DC-
GND	5	6	GND
ETH0_DB+	7	8	ETH0_DD+
ETH0_DB-	9	10	ETH0_DD-
GND	11	12	GND
ETH1_DA+	13	14	ETH1_DC+
ETH1_DA-	15	16	ETH1_DC-
GND	17	18	GND
ETH1_DB+	19	20	ETH1_DD+
ETH1_DB-	21	22	ETH1_DD-
GND	23	24	GND
USB1_D-	25	26	USB2_D-
USB1_D+	27	28	USB2_D+
USB1_VCC	29	30	USB2_VCC
	31	32	
	33	34	
	35	36	
	37	38	
	39	40	
	41	42	COM1_RXD
COM1_TXD	43	44	
COM2_TX-	45	46	COM2_RX-
COM2_TX+	47	48	COM2_RX+
	49	50	
	51	52	
	53	54	
	55	56	
	57	58	
	59	60	
	61	62	
	63	64	

Table 26 : PMC Connector P4

Appendix B: Front (XRM) Connector Pinouts

The XRM interface consists of two connectors: CN1 and CN2. CN1 is a 180-way Samtec QSH in 3 fields. It is for general-purpose signals, power and module control. CN2 is a 28-way Samtec QSE-DP for high-speed serial (MGT) links.



Appendix B.1: XRM Connector CN1, Field 1

Signal	FPGA	Samtec	Samtec	FPGA	Signal
DA_N0	V24	1	2	T27	DA_N1
DA_P0	U24	3	4	R27	DA_P1
DA_N2	P26	5	6	R28	DA_P3
DA_P2	P25	7	8	T28	DA_N3
DA_N4	R21	9	10	V29	DA_N5
DA_P4	P21	11	12	V28	DA_P5
DA_N6	P28	13	14	U29	DA_N7
DA_P6	N28	15	16	T29	DA_P7
DA_P8	R22	17	18	U25	DA_P9
DA_N8	R23	19	20	V26	DA_N9
DA_N10	N27	21	22	T25	DA_N11
DA_P10	N26	23	24	T24	DA_P11
DA_N12	P24	25	26	P30	DA_P13
DA_P12	P23	27	28	R30	DA_N13
DA_N14	P29	29	30	V27	DA_P15
DA_P14	N29	31	32	W28	DA_N15
DB_N0	T23	33	34	U30	DB_N1
DB_P0	T22	35	36	T30	DB_P1
SA_0	U21	37	38	R25	DA_CC_P16
3V3	-	39	40	R26	DA_CC_N16
3V3	-	41	42	-	FORCE2V5_L
3V3	-	43	44	-	2V5
5V0	-	45	46	-	VREF
5V0	-	47	48	-	VccIO
VBATT	-	49	50	-	VccIO
12V0	-	51	52	-	VccIO
12V0	-	53	54	-	M12V0
PRESENCE_L	-	55	56	-	TDI
TCK	-	57	58	-	TRST
TMS	-	59	60	-	TDO

Table 27 : XRM Connector CN1, Field 1

Appendix B.2: XRM Connector CN1, Field 2

Signal	FPGA	Samtec	Samtec	FPGA	Signal
DB_N2	W26	61	62	V22	DB_N3
DB_P2	W25	63	64	U22	DB_P3
DB_N4	W30	65	66	W24	DB_N5
DB_P4	W29	67	68	V23	DB_P5
DB_N6	AA28	69	70	AE26	DB_N7
DB_P6	AA27	71	72	AD25	DB_P7
DB_N8	AC27	73	74	AD30	DB_P9
DB_P8	AB27	75	76	AE30	DB_N9
DB_P10	Y28	77	78	AG27	DB_N11
DB_N10	AA29	79	80	AG26	DB_P11
DB_N12	Y27	81	82	AC26	DB_P13
DB_P12	Y26	83	84	AD26	DB_N13
DB_N14	AB30	85	86	AF25	DB_N15
DB_P14	AB29	87	88	AE25	DB_P15
DB_CC_P16	AE28	89	90	AA25	SB_1
DB_CC_N16	AF28	91	92	W23	SC_0
SA_1	V21	93	94	AA22	SC_1
SB_0	Y25	95	96	AA23	SD_0
DC_CC_P16	AC28	97	98	AA30	DC_N1
DC_CC_N16	AD28	99	100	Y30	DC_P1
DC_N0	AB26	101	102	AE22	DD_CC_P16
DC_P0	AB25	103	104	AF22	DD_CC_N16
SD_1	AC22	105	106	AC21	SD_3
SD_2	AC23	107	108	U27	GCLK_M2C_N
MGTCLK_M2C_P	AA8	109	110	U26	GCLK_M2C_P
MGTCLK_M2C_N	AA7	111	112	-	SDA
XRM_PECL_CLK_N	AH21	113	114	-	SCL
XRM_PECL_CLK_P	AG21	115	116	-	ALERT_N
MGT_C2M_P7	AK2	117	118	AE8	MGT_M2C_P7
MGT_C2M_N7	AK1	119	120	AE7	MGT_M2C_N7

Table 28 : XRM Connector CN1, Field 2

Appendix B.3: XRM Connector CN1, Field 3

Signal	FPGA	Samtec	Samtec	FPGA	Signal
DC_P2	AJ30	121	122	AC29	DC_P3
DC_N2	AK30	123	124	AD29	DC_N3
DC_N4	AF27	125	126	AF30	DC_P5
DC_P4	AE27	127	128	AG30	DC_N5
DC_P6	AK22	129	130	AF29	DC_P7
DC_N6	AK23	131	132	AG29	DC_N7
DC_N8	AK25	133	134	AH29	DC_N9
DC_P8	AJ25	135	136	AH28	DC_P9
DC_P10	AJ21	137	138	AJ24	DC_N11
DC_N10	AK21	139	140	AJ23	DC_P11
DC_P12	AJ28	141	142	AK28	DC_N13
DC_N12	AJ29	143	144	AK27	DC_P13
DC_N14	AH27	145	146	AG24	DD_P1
DC_P14	AH26	147	148	AG25	DD_N1
DD_P0	AG22	149	150	AK26	DC_N15
DD_N0	AH22	151	152	AJ26	DC_P15
DD_P2	AH23	153	154	AG19	DD_N3
DD_N2	AH24	155	156	AF19	DD_P3
DD_N4	AE21	157	158	AB24	DD_N5
DD_P4	AD21	159	160	AA24	DD_P5
DD_P6	AF23	161	162	AE23	DD_N7
DD_N6	AF24	163	164	AD23	DD_P7
DD_N8	AJ19	165	166	Y21	DD_N9
DD_P8	AH19	167	168	W21	DD_P9
DD_N10	AK20	169	170	AB22	DD_N11
DD_P10	AJ20	171	172	AB21	DD_P11
DD_N12	AG20	173	174	Y23	DD_N13
DD_P12	AF20	175	176	Y22	DD_P13
DD_N14	AK18	177	178	AD24	DD_N15
DD_P14	AK17	179	180	AC24	DD_P15

Table 29 : XRM Connector CN1, Field 3

Appendix B.4: XRM Connector CN2

Signal	FPGA	Samtec	Samtec	FPGA	Signal
MGT_C2M_P0	AH2	1	2	AH6	MGT_M2C_P0
MGT_C2M_N0	AH1	3	4	AH5	MGT_M2C_N0
MGT_C2M_P1	AF2	5	6	AG4	MGT_M2C_P1
MGT_C2M_N1	AF1	7	8	AG3	MGT_M2C_N1
MGT_C2M_P4	AK10	9	10	AH10	MGT_M2C_P4
MGT_C2M_N4	AK9	11	12	AH9	MGT_M2C_N4
MGT_C2M_P5	AK6	13	14	AJ8	MGT_M2C_P5
MGT_C2M_N5	AK5	15	16	AJ7	MGT_M2C_N5
MGT_C2M_P2	AE4	17	18	AF6	MGT_M2C_P2
MGT_C2M_N2	AE3	19	20	AF5	MGT_M2C_N2
MGT_C2M_P3	AD2	21	22	AD6	MGT_M2C_P3
MGT_C2M_N3	AD1	23	24	AD5	MGT_M2C_N3
MGT_C2M_P6	AJ4	25	26	AG8	MGT_M2C_P6
MGT_C2M_N6	AJ3	27	28	AG7	MGT_M2C_N6

Table 30 : XRM Connector CN2

Appendix C: XMC Breakout FPGA Pinout

The pinout below applies when using the ADM-XRC-7Z1 with the ADC-XMC-BREAKOUT. This table only shows pins that are connected to the FPGA, for the pinout of other interfaces (e.g. Ethernet, USB ...etc, see the ADM-XRC-7Z1 reference design).

XMC Breakout Pin	XMC Pin	FPGA Pin	Function
COM2 TX	P4 47	AB14	RS232
COM2 RX	P4 48	AB15	RS232
GPIO1	P6 C19	AJ16	GPIO
GPIO2	P6 C18	AK16	GPIO
GPIO3	P6 F19	AH18	GPIO
GPIO4	P6 F18	AJ18	GPIO
GPIO5	P6 C17	AJ15	GPIO
GPIO6	P6 C16	AK15	GPIO
GPIO7	P6 F17	AH17	GPIO
GPIO8	P6 F16	AH16	GPIO
GPIO9	P6 C15	AJ14	GPIO
GPIO10	P6 C14	AJ13	GPIO
GPIO11	P6 F15	AK13	GPIO
GPIO12	P6 F14	AK12	GPIO
GPIO13	P6 A19	AD10	MGT109 Clk P
GPIO14	P6 B19	AD9	MGT109 Clk N
SATA0_TX_P0	P6 A1	AH2	MGT TX
SATA0_TX_N0	P6 B1	AH1	MGT TX
SATA0_RX_P0	P6 A11	AH6	MGT RX
SATA0_RX_N0	P6 B11	AH5	MGT RX
SATA1_TX_P1	P6 D1	AF2	MGT TX
SATA1_TX_N1	P6 E1	AF1	MGT TX
SATA1_RX_P1	P6 D11	AG4	MGT RX
SATA1_RX_N1	P6 E11	AG3	MGT RX

Table 31 : XMC Connector P5

Revision History

Date	Revision	Nature of Change
03/07/13	1.0	Initial Release
04/10/13	1.1	Minor Updates
26/03/14	2.0	Updated for rev2 board, Clarified key features, Figure 1: corrected QSPI size, Table 5: corrected SW2-5 and SW2-6 descriptions to match rev2 PCB, 4.2.1.2: MBIST is not used, 4.2.1.4: Added description of External Reset Inhibit switch, 4.6.4: Corrected description of PROGCLK connection, Appendix A.2: removed P6 lanes 8 and 9
07/04/14	2.1	Section 4.1.2: Added figure showing LED locations
10/04/14	2.2	Appendix B: Added XRM pinout
11/04/14	2.3	Section 4.8.5: Correction to USB description
16/12/15	2.4	Table 22: Removed unused signal on p4
06/18/18	2.5	Updated missing information in certain sections.
14/02/22	2.6	Added XMC Breakout pinout to appendix.

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