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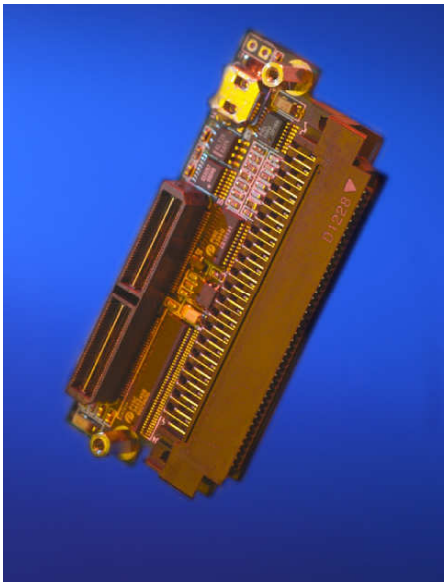
XRM-FPDP

Front Panel Data Port I/O Module

User Manual

Version 1.0

ALPHA DATA



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1. Introduction

XRM I/O modules allow for re-configurable connectivity solutions using specific connectors and I/O standards. This modular approach allows for specific interfaces to be employed on common FPGA platforms.

The XRM-FPDP is a front panel adapter module designed for use with Alpha Data's FPGA based XRC boards. It can function as a receiver or transmitter of FPDP data. The Front Panel Data Port (FPDP) bus is intended to provide data transfer between two or more boards at up to 160MB/s with the lowest possible latency. The FPDP bus is a 32-bit parallel synchronous bus wired by means of an 80-conductor ribbon cable.

1.1. Standards

ANSI/VITA 17-1998 (R2004)

2. Installation

The XRM-FPDP is designed to plug into the front panel connector (SAMTEC QSH series) of an Alpha Data FPGA card. The retaining screws should be tightened to secure the XRM-FPDP.

Note: This operation should not be performed while the host PMC or PCI card is powered up.

2.1. Handling instructions

Observe ESD precautions when handling the modules to prevent damage to components by electrostatic discharge. Avoid flexing the board.

2.2. Board Jumper Settings

The XRM-FPDP uses a 3.3V signalling voltage with the FPGA board. The proper setting must be made on the XRC host board for the front I/O voltage; typically done via a switch or jumper on the XRC board.

3. Module Description

The XRM-FPDP IO module provides connection to Front Panel Data Port interfaces. It uses the standard 80 way KEL 8831E-080-170L or RN P50E-080-P1-SR1-TG connector with Non Inverted FPDP pin assignments described in VITA17.

3.1. FPDP Interface

The XRM-FPDP utilizes bi-directional bus switches for all electrical connections to the J2 FPDP connector. This provides 5V signalling level tolerance and translates the signalling voltage to 3.3V for the FPGA connections.

3.2. J2 FPDP Pin Descriptions

FPDP Pin	Function	J1 Samtec Pin	XRM Bus Name	FPDP Pin	Function	J1 Samtec Pin	XRM Bus Name
1	GND	-	-	**2**	Strob	38	CLK0
3	GND	-	-	**4**	GND	-	-
5	GND	-	-	**6**	GND	-	-
7	Nrdy	77	IO_50P_1	**8**	GND	-	-
9	Dir	73	IO_72N_1	**10**	GND	-	-
11	Reserved	-	-	**12**	GND	-	-
13	Suspend	74	IO_71P_1	**14**	GND	-	-
15	GND	-	-	**16**	GND	-	-
17	PIO2	63	IO_73P_1	**18**	GND	-	-
19	PIO1	64	IO_68P_1	**20**	GND	-	-
21	Reserved	-	-	**22**	GND	-	-
23	Resreved	-	-	**24**	GND	-	-
25	Pstrobe +ve	89 (in) or 91(out)	*	**26**	GND	-	-
27	Pstrobe -ve	89 (in) or 91(out)	*	**28**	GND	-	-
29	Sync	61	IO_73N_1	**30**	GND	-	-
31	Dvalid	62	IO_68N_1	**32**	GND	-	-
33	D31	37	IO_51P_1	**34**	D30	36	IO_26P_1
35	GND	-	-	**36**	D29	35	IO_49P_1
37	D28	34	IO_26N_1	**38**	GND	-	-
39	D27	33	IO_49N_1	**40**	D26	32	IO_20N_1
41	GND	-	-	**42**	D25	31	IO_22P_1
43	D24	30	IO_20P_1	**44**	GND	-	-
45	D23	29	IO_22N_1	**46**	D22	28	IO_29N_1
47	GND	-	-	**48**	D21	27	IO_28P_1
49	D20	26	IO_29P_1	**50**	GND	-	-
51	D19	25	IO_28N_1	**52**	D18	24	IO_2P_1
53	GND	-	-	**54**	D17	23	IO_25P_1
55	D16	22	IO_2N_1	**56**	GND	-	-
57	D15	21	IO_25N_1	**58**	D14	20	IO_23N_1
59	GND	-	-	**60**	D13	19	IO_3N_1
61	D12	18	IO_23P_1	**62**	GND	-	-
63	D11	17	IO_3P_1	**64**	D10	16	IO_54P_1
65	GND	-	-	**66**	D09	15	IO_5P_1
67	D08	14	IO_54N_1	**68**	GND	-	-
69	D07	13	IO_5N_1	**70**	D06	12	IO_52P_1
71	GND	-	-	**72**	D05	11	IO_6P_1
73	D04	10	IO_52N_1	**74**	GND	-	-
75	D03	9	IO_6N_1	**76**	D02	8	IO_30N_1
77	GND	-	-	**78**	D01	7	IO_19P_1
79	D00	6	IO_30P_1	**80**	GND	-	-

* Note: the Pstrobe +/- differential PECL signal connects to a driver/receiver on the XRM module. This is connected to the Samtec connector on pin 89 as a clock input to the FPGA or on pin 91 as a clock output from the FPGA. (see control signals in section 3.4.3)

3.3. FPDP Signal Descriptions

SIGNAL	NAME	COMMENTS
D<31:00>	Data Bus	32-bit data bus driven by FPDP/TM Interfaces.
DIR*	Data Direction	The FPDP/TM asserts DIR* low.
DVALID*	Data Valid	When asserted, DVALID* indicates that the data bus has valid data. This signal is generated by the FPDP/TM.
STROB	Data Strobe	STROB is a free running clock supplied by the FPDP/TM. FPDP/R and FPDP/RM interfaces should sample the data with the rising edge of STROB when DVALID* is asserted.
NRDY*	Not Ready	NRDY* should be asserted by FPDP/R or FPDP/RM interfaces, when they are not ready to receive data. The

		FPDP/TM should sample this signal until the FPDP/R or FPDP/RM brings it high, at which time the transfer should commence. Since NRDY* is asynchronous to STROB, the FPDP/TM should double-synchronize to it before sampling its state; this avoids metastability problems.
PIO1, PIO2	Programmable I/O	The PIO signals are programmable I/O lines. They may be configured as inputs or outputs.
PSTROBE	+PECL Data Strobe	This signal along with PSTROBE* may be generated by the FPDP/TM as an optional differential ±PECL data strobe. PSTROBE is the positive version of the differential clock and has the same polarity as STROB. For high data rate applications, the differential ±PECL data strobe should be used instead of STROB.
PSTROBE*	-PECL Data Strobe	This signal is the negative version of the differential PECL data strobe.
Reserved		No connection should be made to reserved signals.
SUSPEND*	Suspend Data	SUSPEND* should be generated by FPDP/R or FPDP/RM interfaces to inform the data source of a pending buffer overflow condition. The FPDP/TM may delay for no more than 16 cycles in total before suspending the transfer by negating DVALID*. Since SUSPEND* is asynchronous to STROB, the FPDP/TM should double-synchronize to it before sampling its state; this avoids metastability problems.
SYNC*	Sync Pulse	The FPDP/TM must provide a Sync pulse to FPDP/R and FPDP/RM interfaces to synchronize data transfers when transmitting Single Frame data, Fixed Size Repeating Frame data or Dynamic Size Repeating Frame data. FPDP/R and FPDP/RM interfaces should wait for the Sync pulse before accepting data. FPDP/R and FPDP/RM interfaces should start to accept data on the first Data Valid period following the Sync pulse.

3.4. XRM Control signals

There are 6 signals provided from the FPGA to the XRM-FPDP to control the operation of the interface. This allows the module to be configured as a transmitter or receiver. The control signal allocations from the FPGA are shown below:

Signal	Description	H/W Default	TX Operation	RX Operation	J1 Samtec Pin	XRM Bus Name
Control<0>	0:- Enable FPDP Control line termination 1:- Disable FPDP Control line termination	Pull-Up	0	0	67	IO_67P_1
Control<1>	0 :- Receiver terminations 1:- Transmitter termination	Pull-Up	1	0	68	IO_76P_1
Control<2>	0 :- enable FPDP Control lines 1 :- Isolate FPDP Control lines	Pull-Up	0	0	65	IO_67N_1
Control<3>	0 :- enable FPDP Data lines 1 :- Isolate FPDP Datal lines	Pull-Up	0	0	66	IO_76N_1
Control<4>	0 :- enable FPDP PECL strobe 1 :- Disable FPDP PECL strobe	Pull-Up	0	0	69	IO_70N_1
Control<5>	0 :- enable receive FPDP PECL strobe 1 :- enable transmit FPDP PECL strobe	Pull-Up	1	0	70	IO_53N_1

3.4.1. Control of FPDP Signal Termination

Control<1> selects the group of signals for termination depending on if the XRM-FPDP is the transmitter or receiver. When it is the receiver, the signals Dir and Strob are inputs and should be terminated. When it is the transmitter, the signals Nrdy and Suspend are inputs and should be terminated. Control<0>

enables the termination of the selected group, and connects each signal to a 220 ohm pull-up and 330 ohm pull-down per the VITA17 specification.

3.4.2. Enabling FPDP Data / Control Busses

Control<2> and Control<3> enable the FPDP control lines and data lines respectively. When disabled, the corresponding FPDP signals are isolated from the J2 connector.

3.4.3. Control of PECL Strobe

The XRM-FPDP has a differential PECL driver/receiver to provide the FPDP Pstrobe signals for higher data rate applications. This differential strobe connection is enabled by control<4>. When control<5> is '1' The PECL driver is sourced from a single-ended FPGA signal, and driven as differential PECL to the FPDP connector. When control<5> is '0' the differential PECL receiver converts the FPDP inputs to a singled ended signal to the FPGA clock input. When the Pstrobe receive option is selected, the appropriate termination is provided by the XRM module.

3.5. Encryption Battery

The XRM-FPDP provides a battery as a backup power source for the XRC FPGA board encryption key. This is connected to VBATT of the target FPGA via the J1 Samtec connector. For more information see the relevant Xilinx user guide on using encrypted bitstreams.

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