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ALPHA DATA

XRM-IO146 User Manual

Revision: V2.1

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1 Introduction



Figure 1 : XRM-IO146



Figure 2 : XRM-IO146-ROCKET

The XRM-IO146 provides 146 I/O signals on a front panel MICTOR connector with a wide range of options to support GPIO requirements. Signals are driven / received by the FPGA for total user programmability and can be used single ended (i.e. LVTTL) or in pairs (i.e. LVDS). Micro-coax cable assemblies for this adapter can support signals up to 2GHz (also available from Alpha Data). For positive locking cable retention, an optional cable clamp assembly is available.

Each pair of I/O signals is routed as shown below using optional fit resistors. The default manufacturing option is Rs=0R and Rt not fitted, so that the signals pass straight through to an FPGA. Other options are available by contacting Alpha-Data and requesting a custom part ordering code. Alpha Data can also provide further information to rework the termination resistors at customer sites if IPC-A-610 specialists are available. Rs can be used to provide series dampening for point to point applications, or current limiting, but for LVDS is typically 0R0. Rt can be used for LVDS inputs to provide the termination voltage from the line current, or parallel termination; although Xilinx FPGAs from Virtex-4 onward have this termination available internally.

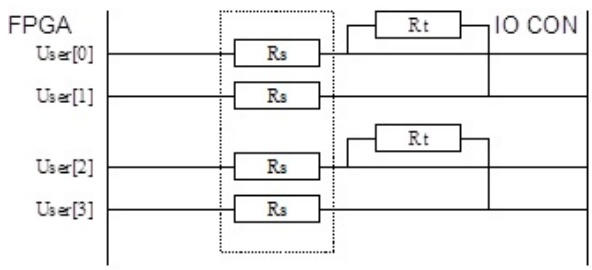


Figure 3 : XRM-IO146 Terminaion Options

Each single ended signal is routed via a series resistor. These are 33R0 by default, but can be customized by Alpha Data or at customer sites.

1.1 Specifications

The XRM-IO146 provides multiple channels of bidirectional I/O capability with complete programmability from the FPGA.

- Standard XRM format module (Alpha Data standard)
- Compatible with all Alpha Data boards featuring an XRM site
- 64 differential (LVDS, LVPECL, etc.) pairs + 4 clock capable pairs (LVDS, LVPECL, etc.) + 10 single ended (LVTTL, LVCMOS, etc.)
- All signals can be used single ended (up to 146 LVTTL, LVCMOS, etc.)
- XRM VCCIO selectable from the FPGA board at 1.2V to 3.3V (depending on limits of FPGA family)
- Battery holders to provide power for FPGA encryption key memory
- Option for 5V power output - rated to provide up to 300mA (protected by a resettable fuse)
- Option for 7x RocketIO lanes (7x Tx/Rx pairs) in lieu of 13 LVDS pairs and 2 - 5V output pins
- Option for positive locking cable clamp assembly

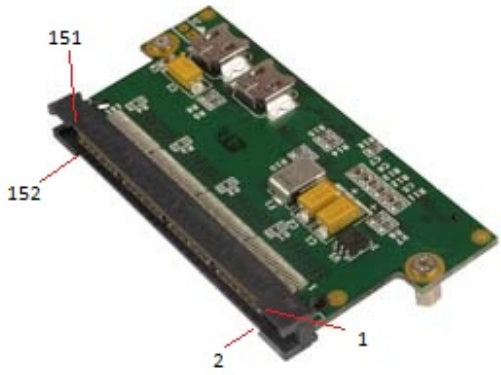


Figure 4 : XRM-IO146 Pin Diagram

2 Installation

2.1 Fitting

The XRM-IO146 is designed to plug in to the front panel connector (SAMTEC QSH series) on Alpha Data cards with an XRM site. Note that Virtex-6 and newer boards key this connector 180deg from Virtex-5 and earlier boards. For Virtex-6 and up, the XRM2 version is required and can't be interchanged with the XRM version for Virtex-5 and earlier boards. The retaining screws should be tightened to secure the XRM-IO146.

Note:
This operation should not be performed while the card is powered up.

2.2 Handling instructions

Observe precautions for preventing damage to components by electrostatic discharge. Personnel handling the board should take ESD precautions.

Note:
Avoid flexing the board.

2.3 Voltage Settings

Note:
This board will pass signals directly to the FPGA unless termination options are specified; users should ensure that the VIO setting on the FPGA card is set to suit the appropriate signaling level to ensure no damage can occur. Also ensure that the signals applied to this module are within the limits of the FPGA IOBs.

2.4 Battery Installation

The XRM-IO146 has 2 battery holders for supplying the VBATT power supply to maintain the encryption key memory within the Xilinx FPGA. If the encryption feature of the FPGA isn't used, then no batteries need to be installed. Use 1.5V SR60 coin cell batteries, 6.8mm, silver oxide such as Duracell D364 (not included by Alpha Data). When replacing the batteries, ensure one is always installed while replacing the other and the VBATT supply will continuously keep the encryption key backed up. Refer to the Xilinx configuration user guide for further information.

3 XRM-IO146 Interface Connector

The XRM-IO146 signal interface is a MICTOR 152-way receptacle connector, AMP/TYCO part number 5767044-4 (or equivalent).

Suggested mating part is AMP/TYCO 1-5767007-1 152 pin Mictor Plug (or similar).

Cable assemblies are available from Alpha Data or directly from Micro Interconnects (www.microinterconnects.com). Alpha Data can provide standard cable assemblies for 152M to 152M (50cm), 152M to 4 x 38M (50cm), or custom cabling solutions as requested.

4 XRM-IO146 Interface - Pinout Tables

The front panel MICTOR connector is broken up into 4 banks, which can be used for a single function or split up as required for an application (see coloring of banks in diagrams below). Cabling can be used to break off each bank to it's own connector, connected to another 152-pin MICTOR, or customized for a specific application. The following table shows the MICTOR connector pins, connection to the Samtec XRM connector and signal description. See the Alpha Data SDK for the UCF files to map each pin to the FPGA pad, or contact Alpha Data for further support.

- The first letter in the signal name (d or s) represents differential or single ended routing. RocketIO signals begin with (gtp).
- The second letter (a,b,c,d) represent the bank of the MICTOR connector. RocketIO signals specify the direction relative to the FPGA (tx or rx).
- Each pair is represented by _p / _n indicating polarity and a pair number.
- Clock capable signals (cc in name) can be used for differential clocks, single ended clocks, or data. Additional clock capable signals may be available depending on the main FPGA board allocation.
- Data signals can be used for differential pairs or single ended signals.

Options	Signal	Samtec	Mictor		Samtec	Signal	Options
	da_p<0>	3	1	2	6	da_p<3>	
	da_n<0>	1	3	4	8	da_n<3>	
	da_p<2>	7	5	6	4	da_p<1>	
	da_n<2>	5	7	8	2	da_n<1>	
	da_p<4>	11	9	10	12	da_p<5>	
	da_n<4>	9	11	12	10	da_n<5>	
	da_p<6>	15	13	14	16	da_p<7>	
	da_n<6>	13	15	16	14	da_n<7>	
DCI VRN	da_p<8>	17	17	18	18	da_p<9>	
DCI VRP	da_n<8>	19	19	20	20	da_n<9>	
	da_p<10>	23	21	22	24	da_p<11>	
	da_n<10>	21	23	24	22	da_n<11>	
	da_p<12>	27	25	26	26	da_p<13>	
	da_n<12>	25	27	28	28	da_n<13>	
	da_p<14>	31	29	30	30	da_p<15>	
	da_n<14>	29	31	32	32	da_n<15>	
	sa<0>	37	33	34	38	da_cc_p	
	sa<1>	93	35	36	40	da_cc_n	
+5V Fused	N/C		37	38	90	sa<2>	
	db_p<0>	35	39	40	36	db_p<1>	
	db_n<0>	33	41	42	34	db_n<1>	
	db_p<2>	63	43	44	64	db_p<3>	
	db_n<2>	61	45	46	62	db_n<3>	
	db_p<4>	67	47	48	68	db_p<5>	
	db_n<4>	65	49	50	66	db_n<5>	
	db_p<6>	71	51	52	72	db_p<7>	
	db_n<6>	69	53	54	70	db_n<7>	
	db_p<8>	75	55	56	74	db_p<9>	
	db_n<8>	73	57	58	76	db_n<9>	
	db_p<10>	77	59	60	80	db_p<11>	
	db_n<10>	79	61	62	78	db_n<11>	
	db_p<12>	83	63	64	82	db_p<13>	
	db_n<12>	81	65	66	84	db_n<13>	
	db_p<14>	87	67	68	88	db_p<15>	
	db_n<14>	85	69	70	86	db_n<15>	
	sb<0>	105	71	72	89	db_cc_p	
	sb<1>	107	73	74	91	db_cc_n	
+5V Fused	N/C		75	76	95	sb<2>	
	dc_p<0>	103	77	78	100	dc_p<1>	
	dc_n<0>	101	79	80	98	dc_n<1>	
	dc_p<2>	121	81	82	122	dc_p<3>	
	dc_n<2>	123	83	84	124	dc_n<3>	
	dc_p<4>	127	85	86	126	dc_p<5>	
	dc_n<4>	125	87	88	128	dc_n<5>	
	dc_p<6>	129	89	90	130	dc_p<7>	
	dc_n<6>	131	91	92	132	dc_n<7>	
	dc_p<8>	135	93	94	136	dc_p<9>	
	dc_n<8>	133	95	96	134	dc_n<9>	
	dc_p<10>	137	97	98	140	dc_p<11>	
	dc_n<10>	139	99	100	138	dc_n<11>	
	dc_p<12>	141	101	102	144	dc_p<13>	
	dc_n<12>	143	103	104	142	dc_n<13>	
	dc_p<14>	147	105	106	152	dc_p<15>	
	dc_n<14>	145	107	108	150	dc_n<15>	
	sc<0>	92	109	110	97	dc_cc_p	
	sc<1>	94	111	112	99	dc_cc_n	
+5V Fused	N/C		113	114		N/C	+5V Fused
	dd_p<0>	149	115	116	146	dd_p<1>	
	dd_n<0>	151	117	118	148	dd_n<1>	
DCI VRN	dd_p<2>	153	119	120	156	dd_p<3>	
DCI VRP	dd_n<2>	155	121	122	154	dd_n<3>	
	dd_p<4>	159	123	124	160	dd_p<5>	
	dd_n<4>	157	125	126	158	dd_n<5>	
	dd_p<6>	161	127	128	164	dd_p<7>	
	dd_n<6>	163	129	130	162	dd_n<7>	
	dd_p<8>	167	131	132	168	dd_p<9>	
	dd_n<8>	165	133	134	166	dd_n<9>	
	dd_p<10>	171	135	136	172	dd_p<11>	
	dd_n<10>	169	137	138	170	dd_n<11>	
	dd_p<12>	175	139	140	176	dd_p<13>	
	dd_n<12>	173	141	142	174	dd_n<13>	
	dd_p<14>	179	143	144	180	dd_p<15>	
	dd_n<14>	177	145	146	178	dd_n<15>	
	sd<0>	96	147	148	102	dd_cc_p	
	sd<1>	106	149	150	104	dd_cc_n	
+5V Fused	N/C		151	152		N/C	+5V Fused

Figure 5 : XRM-IO146 / XRM2-IO146 Pinout

Options	Signal	Samtec	Mictor		Samtec	Signal	Options
	da_p<0>	3	1	2	6	da_p<3>	
	da_n<0>	1	3	4	8	da_n<3>	
	da_p<2>	7	5	6	4	da_p<1>	
	da_n<2>	5	7	8	2	da_n<1>	
	da_p<4>	11	9	10	12	da_p<5>	
	da_n<4>	9	11	12	10	da_n<5>	
	da_p<6>	15	13	14	16	da_p<7>	
	da_n<6>	13	15	16	14	da_n<7>	
	da_p<8>	67	17	18	18	da_p<9>	
	da_n<8>	65	19	20	20	da_n<9>	
	da_p<10>	23	21	22	24	da_p<11>	
	da_n<10>	21	23	24	22	da_n<11>	
	da_p<12>	27	25	26	26	da_p<13>	
	da_n<12>	25	27	28	28	da_n<13>	
	da_p<14>	31	29	30	30	da_p<15>	
	da_n<14>	29	31	32	32	da_n<15>	
	da_p<16>	149	33	34	38	da_cc_p	
	da_n<16>	151	35	36	40	da_cc_n	
+5V Fused	N/C		37	38	37	sa<2>	
	db_p<0>	35	39	40	36	db_p<1>	
	db_n<0>	33	41	42	34	db_n<1>	
	db_p<2>	63	43	44	64	db_p<3>	
	db_n<2>	61	45	46	62	db_n<3>	
	db_p<4>	110	47	48	68	db_p<5>	
	db_n<4>	112	49	50	66	db_n<5>	
	db_p<6>	71	51	52	72	db_p<7>	
	db_n<6>	69	53	54	70	db_n<7>	
	db_p<8>	75	55	56	74	db_p<9>	
	db_n<8>	73	57	58	76	db_n<9>	
	db_p<10>	77	59	60	80	db_p<11>	
	db_n<10>	79	61	62	78	db_n<11>	
	db_p<12>	83	63	64	82	db_p<13>	
	db_n<12>	81	65	66	84	db_n<13>	
	db_p<14>	87	67	68	88	db_p<15>	
	db_n<14>	85	69	70	86	db_n<15>	
	db_p<16>	146	71	72	89	db_cc_p	
	db_n<16>	148	73	74	91	db_cc_n	
+5V Fused	N/C		75	76	154	sb<2>	
	dc_p<0>	103	77	78	100	dc_p<1>	
	dc_n<0>	101	79	80	98	dc_n<1>	
	dc_p<2>	121	81	82	122	dc_p<3>	
	dc_n<2>	123	83	84	124	dc_n<3>	
	dc_p<4>	127	85	86	126	dc_p<5>	
	dc_n<4>	125	87	88	128	dc_n<5>	
	dc_p<6>	129	89	90	130	dc_p<7>	
	dc_n<6>	131	91	92	132	dc_n<7>	
	dc_p<8>	135	93	94	136	dc_p<9>	
	dc_n<8>	133	95	96	134	dc_n<9>	
	dc_p<10>	137	97	98	140	dc_p<11>	
	dc_n<10>	139	99	100	138	dc_n<11>	
	dc_p<12>	141	101	102	144	dc_p<13>	
	dc_n<12>	143	103	104	142	dc_n<13>	
	dc_p<14>	147	105	106	152	dc_p<15>	
	dc_n<14>	145	107	108	150	dc_n<15>	
	dc_p<16>	95	109	110	97	dc_cc_p	
	dc_n<16>	93	111	112	99	dc_cc_n	
+5V Fused	N/C		113	114		N/C	+5V Fused
	gtp_rx_p<6>	CN2-26	115	116	CN2-25	gtp_tx_p<6>	
	gtp_rx_n<6>	CN2-28	117	118	CN2-27	gtp_tx_n<6>	
	gtp_rx_p<3>	CN2-22	119	120	CN2-21	gtp_tx_p<3>	
	gtp_rx_n<3>	CN2-24	121	122	CN2-23	gtp_tx_n<3>	
	sd<0>	92	123	124	96	sd<2>	
	sd<1>	90	125	126	94	sd<3>	
	gtp_rx_p<2>	CN2-18	127	128	CN2-17	gtp_tx_p<2>	
	gtp_rx_n<2>	CN2-20	129	130	CN2-19	gtp_tx_n<2>	
	gtp_rx_p<5>	CN2-14	131	132	CN2-13	gtp_tx_p<5>	
	gtp_rx_n<5>	CN2-16	133	134	CN2-15	gtp_tx_n<5>	
	gtp_rx_p<4>	CN2-10	135	136	CN2-9	gtp_tx_p<4>	
	gtp_rx_n<4>	CN2-12	137	138	CN2-11	gtp_tx_n<4>	
	gtp_rx_p<1>	CN2-6	139	140	CN2-5	gtp_tx_p<1>	
	gtp_rx_n<1>	CN2-8	141	142	CN2-7	gtp_tx_n<1>	
	gtp_rx_p<0>	CN2-2	143	144	CN2-1	gtp_tx_p<0>	
	gtp_rx_n<0>	CN2-4	145	146	CN2-3	gtp_tx_n<0>	
	sd<4>	108	147	148	102	sd<7>	
	sd<5>	106	149	150	104	sd<8>	
	sd<6>	107	151	152	105	sd<9>	

Figure 6 : XRM-IO146-ROCKET / XRM2-IO146-ROCKET Pinout

5 Positive Locking / Cable Clamp Assembly

The XRM-IO146 uses a MICTOR connector with a minimum retention force of 4.75lbs. For applications requiring positive locking on this connector or further strain relief, an optional locking assembly is available. This clamp interfaces with the housing on the cable assembly to lock it in place, and also provides strain relief to the cable itself by clamping it with protective material.

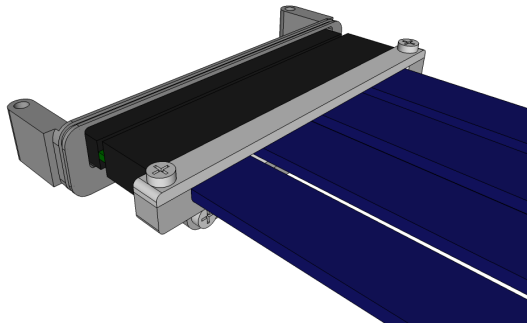


Figure 7 : MET-BEZEL-IO146-LOCK Top View

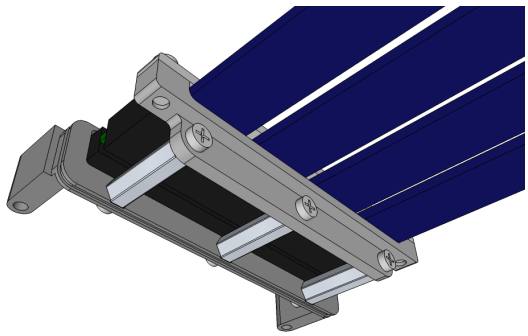


Figure 8 : MET-BEZEL-IO146-LOCK Bottom View

6 Product Codes

The following table describes the standard product codes and some of the available build options. Contact Alpha Data for further options, customizations, conformal coating, etc.

Product Code	Description
XRM-IO146	Standard module for Virtex-5 and earlier Alpha Data boards
XRM**2**-IO146	Standard module for Virtex-6 and later Alpha Data boards
XRM-IO146**A**	Standard module for ADM-XRC-4 board only
XRM-IO146**-G**	DCI enabled option for Virtex-4 and earlier
XRM(2)-IO146**-ROCKET**	High Speed Serial Lanes Option
XRM(2)-IO146**-LOCK**	Includes cable retention / positive locking assembly
XRM(2)-IO146**-ROCKET-LOCK**	HSS and includes cable retention / positive locking assembly
XRM(2)-IO146**-[code]**	Other build options as assigned by Alpha Data
Product Code	Accessory Description
XRM-IO146-LOOPBACK	Test adapter to loop back signals (not compatible with -ROCKET)
CAB-MICTOR-152	Cable assembly - 152M to 152M, 50cm
CAB-MICTOR-152M-4X38	Cable assembly - 152M split out to 4 x 38M, 50cm
MET-BEZEL-IO146-LOCK	Spare cable retention / positive locking assembly
Note: please also indicate the requirement to have the XRM-IO146 source 5V through the MICTOR Connector.	

Table 1 : Ordering Options

Revision History

Date	Revision	Nature of Change
2008	1.0	Initial Release
Nov 2012	2.0	Converted to XML, included XRM2 options, updated Mictor cable source, added cable retention option, added ROCKET option, created new pinout tables
Feb 2014	2.1	Clarrified +5V limits on the XRM-IO146 connector

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