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PMC-1553
MIL-STD-1553
PMC Module

REFERENCE MANUAL
718-13-000-4000

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AUGUST 1999

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GENERAL DESCRIPTION

INTRODUCTION

The PMC-1553 module provides Bus Controller (BC), Remote Terminal (RT) and Bus Monitor (BM) dual-redundant operations on the MIL-STD-1553 bus. The PMC form factor provide easy installation.

- UTMC Summit RISC based processor unit
- 64K x 16 bit dual ported SRAM
- Supports Bus Controller, Remote Terminal and Bus Monitor mode
- RT address and operational modes are program or jumper selectable
- 1553 bus long or short stub jumper option

FUNCTIONAL DESCRIPTION

A functional block diagram of the PMC module is depicted below in Figure 1. The PMC-1553 is designed around the SUMMIT that is used to manage the 1553 BUS.

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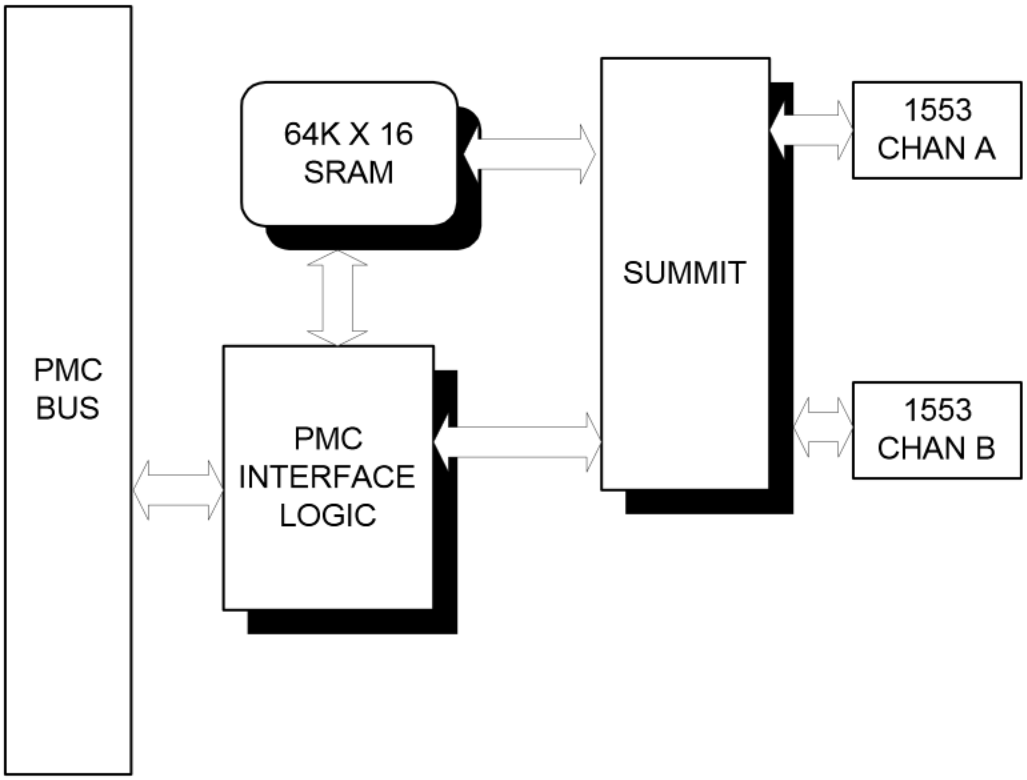


Figure 1

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REFERENCE MATERIALS LIST

The reader should refer to the “SUMMIT” 1996 product handbook, from UTMC, that provides detailed descriptions about the SUMMIT registers.

UTMC
1575 Garden of the Gods Road
Colorado Springs, Colorado
80907-3486 USA

Marketing Department :
719-594-8166 or 800-722-1575

Technical Information :
719-594-8252

Literature Requests :
800-645-UTMC

WWW Home Page :
http://www.utmc.com

The reader should refer to the PCI Local Bus Specification for a detailed explanation of the PCI bus architecture and timing requirements. This specification is available from the following source:

PCI Special Interest Group
PO Box 14070
Portland, OR 97214
Tel: (800) 433-5177
Tel: (503) 797-4207
Fax: (503) 234-6762

The reader is also referred to the S5933 PCI Controller data book:
AMCC Applied Micro Circuits Corporation
6195 Lusk Boulevard
San Diego, CA 92121-2793
Tel: (800) 755-2622

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HOST (PCI) SIDE

PCI CONFIGURATION REGISTERS

The card presents the following configuration values to the PCI system, based on the values stored in the NVRAM device read by the AMCC PCI interface chip.

Register	Value (Meaning)
Vendor ID	0x13c5 (ALPHI Technology)
Device ID	0x0306 (PMC-1553)
Revision ID	0x00
Class Code	0xff0000 (Device does not fit into defined class codes)
Interrupt Line	0xff
Interrupt Pin	A
Multifunction Device	No
Build In Self Test	No
Latency Timer	0x00
Minimum Grant	0x00
Maximum Latency	0x00
Expansion ROM Size	None

Table 0.1: PMC Configuration Registers

MEMORY AND REGISTER MAP SUMMARY

The addresses for the following registers and memory locations are based upon the assignment from the host processor. The PMC-1553 uses 3 of the 5 AMCC mapped base address registers. These base address registers are written by the PCI configurator after scanning the AMCC configuration space. The AMCC is normally programmed at the factory to request the following resources:

64 bytes of memory space for the AMCC PMC Operation Registers.
128 bytes for the SUMMIT registers and local STATUS Registers.
128 Kbytes of space for the Dual Ported SRAM

Base address registers 2 and 4 are not used and are disabled at the factory.
The following table specifies address offsets relative to the AMCC base address registers. For example, the AMCC PMC registers occupy 64 bytes of contiguous space relative to Base address 0. If the PMC configuration programs Base address 0 with the value $6000, then the AMCC registers would occupy memory locations 6000 to 603F.

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BASE ADDR	FROM	TO	DESCRIPTION	TYPE
0	00000000h	0000003Fh	AMCC PMC Operation Registers	MEM
1	00000000h	0000007Fh	SUMMIT IO Space	MEM
3	00000000h	0001FFFFh	SUMMIT DUAL PORTED SRAM	MEM

Table 2

NOTE: The AMCC has been programmed to request memory above 1 Mbyte.

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PMC OPERATION REGISTERS

The host processor communicates with the PMC-1553 module via the AMCC pass-through interface. After the base address registers have been programmed by the PMC configurator, PMC bus cycles are "passed through" to the local bus. Therefore, the PMC Operation Registers are not normally used by applications software. Only IMB4 Byte 3, MBEF, and INTCSR are useful to the PMC-1553 module. IMB4 is written by the PMC-1553 hardware when the SUMMIT generates an interrupt. The PMC Operation Register Offsets are shown below:

Offset	Register Name
00h	OMB1 Outgoing Mailbox Register 1
04h	OMB2 Outgoing Mailbox Register 2
08h	OMB3 Outgoing Mailbox Register 3
0Ch	OMB4 Outgoing Mailbox Register 4
10h	IMB1 Incoming Mailbox Register 1
14h	IMB2 Incoming Mailbox Register 2
18h	IMB3 Incoming Mailbox Register 3
1Ch	IMB4 Incoming Mailbox Register 4
20h	FIFO Register Port (bi-directional)
24h	MWAR Master Write Address Register
28h	MWTC Master Write Transfer Counter
2Ch	MRAR Master Read Address Register
30h	MRTC Master Read Transfer Counter
34h	MBEF Mailbox Empty/Full Status
38h	INTCSR Interrupt Control/Status Register
3Ch	MCSR Bus Master Control/Status Register

Table 3

For more information about these registers refer to the AMCC PMC controller manual.

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INTERNAL ORGANIZATION

The PMC-1553 facilitates host access to the :

- SUMMIT Registers
- Dual Port SRAM
- Status register

SUMMIT REGISTERS

REMOTE TERMINAL REGISTERS

Register Number	Name	Register Offset
0	Control Register	$00
1	Operational Status Register	$02
2	Current Command Register	$04
3	Interrupt Mask Register	$06
4	Pending Interrupt Register	$08
5	Interrupt Log List Pointer Register	$0A
6	BIT Word Register	$0C
7	Time-Tag Register	$0E
8	Remote Terminal Descriptor Pointer Register	$10
9	Status Word Bits Register	$12
10-15	Not Applicable	$14-$1E
16-31	Illegalization Registers	$20- $3E

Table 4

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BUS CONTROLLER REGISTERS

Register Number	Name	Register Offset
0	Control Register	$00
1	Operational Status Register	$02
2	Current Command Block Register	$04
3	Interrupt Mask Register	$06
4	Pending Interrupt Register	$08
5	Interrupt Log List Pointer Register	$0A
6	BIT Word Register	$0C
7	Minor-Frame Timer	$0E
8	Command Block Pointer Register	$10
9	Not Applicable	$12
10	BC Command Block Initialization Count Register	$14
11-31	Not Applicable	$16- $3E

Table 5

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MONITOR TERMINAL REGISTERS

Register Number	Name	Register Offset
0	Control Register	$00
1	Operational Status Register	$02
2	Current Command Block Register	$04
3	Interrupt Mask Register	$06
4	Pending Interrupt Register	$08
5	Interrupt Log List Pointer Register	$0A
6	BIT Word Register	$0C
7	Time-Tag Register	$0E
8-10	Not Applicable	$10-$14
11	Initial Monitor Command Block Pointer Register	$16
12	Initial Monitor Data Pointer Register	$18
13	Monitor Block Counter Register	$1A
14	Monitor Filter Register	$1C
15	Monitor Filter Register	$1E
16-31	Not Applicable	$20- $3E

Table 6

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SHARED MEMORY SRAM

The PMC-1553 has a 64K x 16-bit Shared Memory. The base address of the SRAM is provided by the PMC host controller. A local Flash E^2prom defines the resources needed by the PMC-1553 module. SRAM access are only in 16-bit mode. Arbitration between the Summit and the PMC Bus is made by the local hardware. Summit access to the SRAM takes priority over any pending host access. Therefore, the host access will be held off until the Summit access completes.

PMC SUMMIT RESOURCE REQUIREMENTS

SHARED MEMORY SPACE

NAME	OFFSET	DATA	R/W	COMMENTS
MEM SPACE	$0 - $1FFFF	D00-D15	R/W	Shared / Static RAM 64K x 16-bit (128Kbytes)

SUMMIT REGISTER SPACE

NAME	OFFSET	DATA	R/W	COMMENTS
SUMMIT REGISTERS	$00-$3F	D00-D15	R/W	SUMMIT Registers
PMC STATUS	$42-$43	D00-D15	R	Status Register Only D00-D07 is valid

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STATUS REGISTER

The STATUS register is used to determine the status of PMC-1553 jumper settings. The Status Register provides the following status bits:

Bit	Name	Function
0	MSEL0	Summit mode of Operation
1	MSEL1	
2	LOCK	Status of the Lock input Pin
3	READY	Status of the Ready Output Pin
4-7	NOT USED	

Table 7 Status register

SUMMIT MODE OF OPERATION

Mode select 0, in conjunction with Mode select 1, determines the Summit mode of operation. The table below describes these modes.

MSEL1	MSEL0	Mode Of Operation
0	0	Bus controller = SBC
0	1	Remote Terminal = SRT
1	0	Monitor Terminal = SMT
1	1	SMT/SRT

Table 8

LOCK

This read only bit reflects the inverted state of the LOCK input pin. The LOCK pin is latched on the rising edge of MRST. If the mode of operation must change, the user must perform a MRST.

READY

This read only bit reflects the inverted state of the output pin READY and is cleared on reset. This signal indicates the Summit has completed initialization or BIT, and regular execution may begin.

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LOCAL INTERRUPT SOURCES

The SUMMIT has two (2) interrupt lines. These interrupts are Ored to the INTREQ0 pin on the PMC bus. The Summit will provided the Interrupt Vector Register contents to the PMC bus on D00-D07 during an interrupt acknowledge cycle.

The source of each interrupt is listed below:

INTERRUPT name	Description
MSG_INT	Message interrupt.This pin is active for three clock cycles upon the occurrence of interrupt events which are enabled.
YF_INT	You failed Interrupt. This pin is active for three clock cycles upon the occurrence of interrupt events which are enabled.

Table 9

BYTE-SWAP ENABLE

The PMC-1553 has the ability to perform hardware byte-swapping. The jumper TTJ1 determines the behavior of the byte-swapping hardware. When TTJ1 is OPEN, no swapping occurs (Little-Endian). When TTJ1 is SHORTED, swapping occurs (Big-Endian). This feature allows the PMC-1553 memory and registers to appear correctly to Big-Endian Processors such as the PowerPC.

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JUMPER LOCATION DIAGRAM

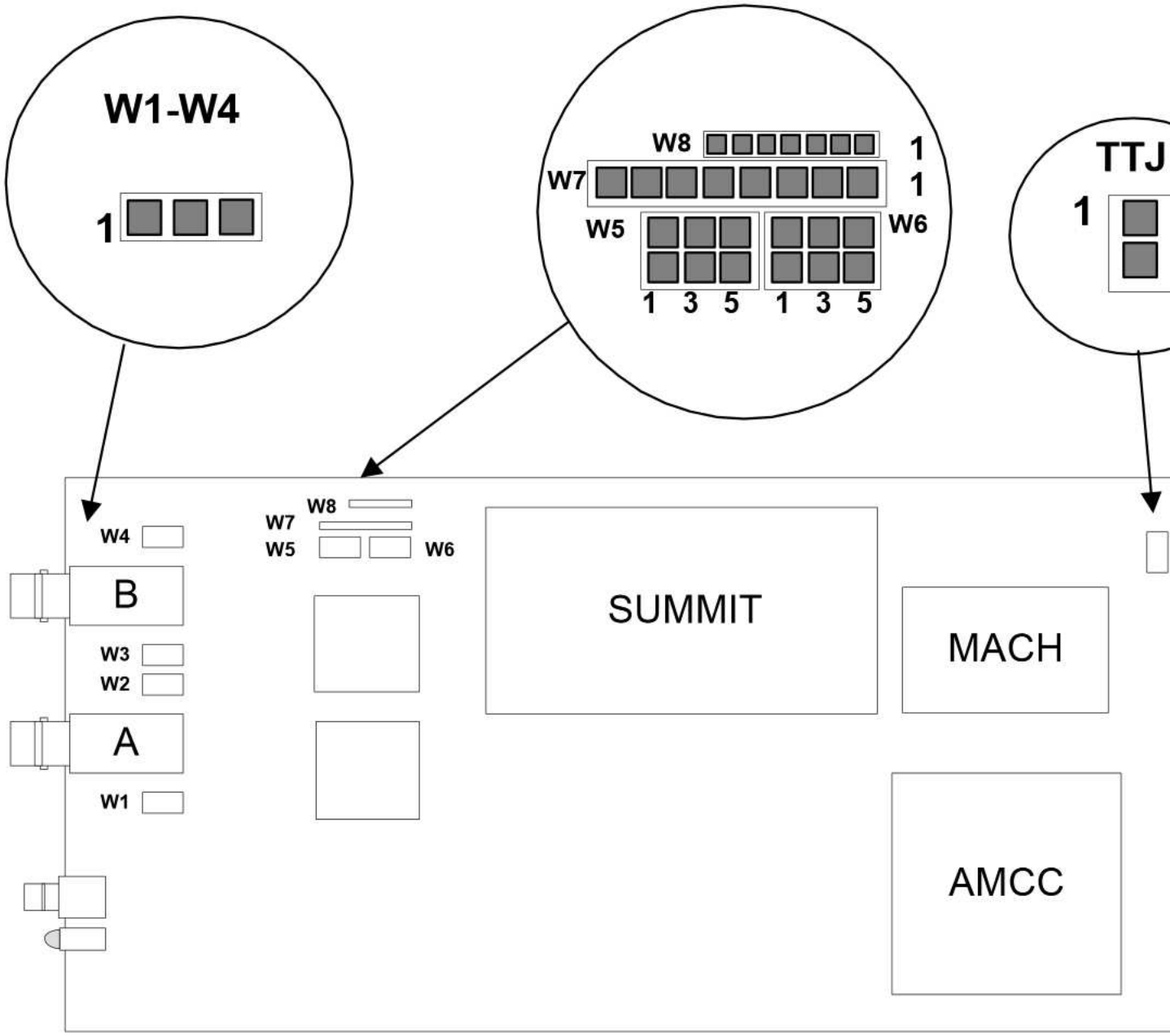


Figure 2

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JUMPER	FACTORY SETTING	DESCRIPTION
W1	1-2	Long Stub/Short Stub Output channel A - (Short Stub)
W2	2-3	Long Stub/Short Stub Output channel A + (Short Stub)
W3	2-3	Long Stub/Short Stub Output channel B + (Short Stub)
W4	1-2	Long Stub/Short Stub Output channel B - (Short Stub)
W5	None	Remote terminal address RTA3-RTPT
W6	None	Remote terminal address RTA0-RTA2
W7	None	Mode of Operation of the SUMMIT
W8	None	Summit JTAG test
TTJ1	None	Byte-Swap Enable
P4	None	MACH 445 programming plug

Table 10

W7 Mode of Operation Jumper Selection

Signal	Jumper set	Description
A/B* STD	1-2	Military standard Mil_STD_1553A or Mil_STD_1553B
LOCK	3-4	This Pin when set active prevent Sotware change to both the RT address,A/B* STD and Mode select
MSEL1	5-6	See Mode of Operation Table above
MSEL0	7-8	See Mode of Operation Table above

Table 11

W6 RT Address Selection

Signal	Jumper set	Description
RTA2	1-2	RT Address BIT 2
RTA1	3-4	RT Address BIT 1
RTA0	5-6	RT Address BIT 0

Table 12

W5 RT Address Selection

Signal	Jumper set	Description
RTPT	1-2	RT Address Parity
RTA4	3-4	RT Address BIT 4
RTA3	5-6	RT Address BIT 3

Table 13

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TTJ1 Byte-Swap Enable

Jumper set	Description
1-2	Open=Little-Endian(PCI Default), Shorted=Big-Endian

Table 14

Addendum

The following addendum is a special configuration developed for an end user please disregard if it doesn't pertain to your configuration.

Board part # PMC-1553 –O
This particular board was designed to output a 1hz clock from the front panel BNC connector when an onboard register is written to, then generate an interrupt every 1 second the 1hz clock is active.

To start the 1hz clock there must be an access to the summit registers region at the address $40, once you have made a read of $40 write the value $1 this will start the 1hz clock.

Once the 1hz clock starts outputting on the BNC connector every 1 second later the board will generate an interrupt.

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