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ATC-CIO32

Counter/Timer and Parallel I/O Unit

REFERENCE MANUAL

773-10-000-4000

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1. INTRODUCTION

The ATC-CIO32 module from ALPHI TECHNOLOGY is design around the Z8536 CIO Counter/Timer and Parallel I/O .

The two(2) on board Z8536 provide up to :

- four (4) I/O ports (8 bits each)
- two special ports (4bit each)
- six counters/Timers(16 bits each).

The ATC-CIO32 meets the single-wide Industry Pack standard according to the INDUSTRY PACK VITA 4 Specifications. An on-board non-volatile EEPROM maintains ATC-CIO32 indentification codes and provides additional user space.

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2. FEATURES

- Single-size INDUSTRY PACK module.
- Four general purpose I/O ports (non buffered)
- Two 4 bit special Purpose Port
- Up to six timers 16 bit that can be linked
- Multipe possibilities of interrupt source
- EEPROM on board (2 K bytes)
- 5 V only power supply
- Optional Extended temperature grade (-40°C to + 85°C)

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3. DESCRIPTION

The ATC-CIO32 is populated with two Zilog Counter/Timer and parallel I/O Z8536

Each devices provides :

- Two 8bit ports with each bit that can be programmed as Input ot Output.
- Three 16 bit Counter/ Timers that can be linked toghther.
- The flexibility of each timer is enhanced by the provision of up to four lines per Counter/Timer
- A third port (4 bit) provide possibilities of Handshake lines for Port A and B.

Specific patterns can be reconized using Port A and B with interrupt generation capabilities. In addition a 2K bytes EEPROM is available on board for user use.The First 64 bytes are pre-programmed by ALPHI to provide an identification information concerning the module in accordance of the VITA 4.0 specifications.

Note :

This document represents Port A, B and C of the Z8536 # 1 to be Port A,B,E at the level of the 50 Pin connector and Port A, B, C of the Z8536 # 2 to be Port C, D, F at the level of the 50 Pin connector.

3.1.1 GENERAL PURPOSE PORTS A AND B

Port A and B are identical,except that port B can be specified to provide external acces to Counter /Timers # 1and # 2.

Either port can be programmed to be :

- handshake driven port
- double buffered port (input,output,or bidirectional)
- a control type port with each bit direction controlled individualy.

Pattern reconition can be made by each port with interrupt generation when matched pattern occurs.

Each port has 12 registers to control all these capabilities.

3.1.2 PORT C

Port C function depens upon port A and port B utilization. Port C can be used :

- handshake lines
- I/O needs
- External access for the Counter/Timer # 3

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3.1.3 COUNTER/TIMERS

Each Z8536 has three identical counter timers that can eventually be linked toguether. Each Counter/Timer has up to four lines to enhance and control their functionality

They can be used as :

- Counter input
- Gate input
- Trigger input
- Counter/Timer output

Output can be :

- a pulse
- one-shot
- square wave
-

Port B lines are used as follow.

Function	C/T1	C/T2	C/T3
Counter / Timer output	PB4	PB0	PC0
Counter input	PB4	PB0	PC0
Trigger input	PB4	PB0	PC0
Gate input	PB4	PB0	PC0

Table 1 Port B special I/O pin utilisation

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4. BLOCK DIAGRAM

There are three basic section to the ATC-CI032

- The INDUSTRY PACK bus interface.
- The Z8536 controllers
- The 2 kByte of non-volatile memory.

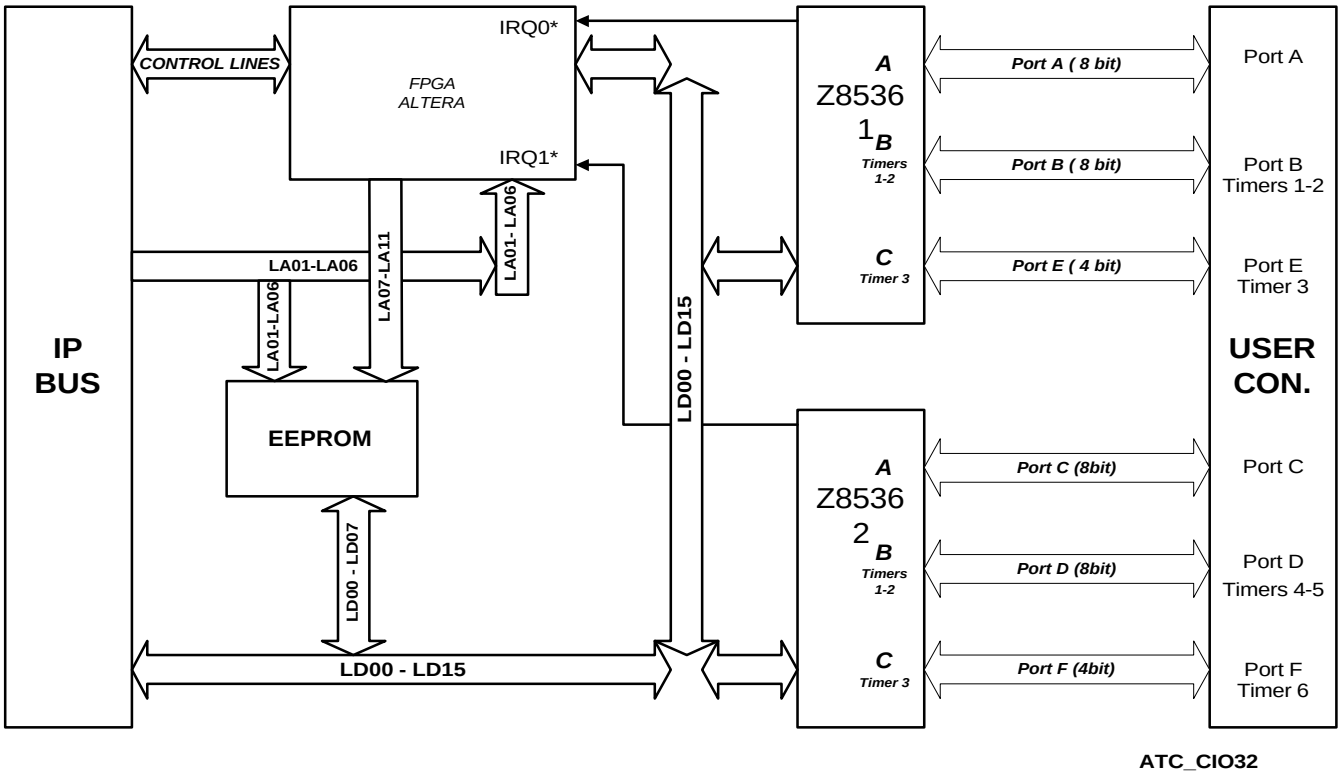


Figure 1ATC-CIO32 Block Diagram

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5. ATC-CIO32 SPACES

The following paragraph describe the different spaces used by the ATC-CIO32

- **ID** space INDUSTRY PACK identification codes
- **I/O** space CIO controllers registers access
- **INT** space Interrupt acknowledge
- **Memory** space User space

The base address of these spaces depends on the specific INDUSTRY PACK carrier used.

5.1.1 ID SPACE

The identification space is defined as follows:

	Description	value
$01	Ascii "I"	$49
$03	Ascii "P"	$50
$05	Ascii "A"	$41
$07	Ascii "C"	$43
$09	Manufacturer identification	$11
$0B	Module type	
$0D	Revision module	
$0F	Reserved $00	
$11	Software Driver #	low byte
$13	Software Driver #	high byte
$15	Number of bytes used in ID space	$0C
$17	CRC	
$19-3F	User available	

Correct reading of the first four bytes that contain the ASCII text "IPAC" can be used to identifie the presence of an Industries Pack module.

Location $09 provide the Manufacturer identities (ALPHI TECHNOLOGY INDUSTRY PACKs $11).

The next two location identifies the module type and revision.

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A 8-bit CHECKSUM (CRC) provide data integrity of the valid ID code set by the manufacturer.

The next bytes $ 19 to $ 3F are free for user data storage.

5.1.2 I/O SPACE

The two Z8536 controller registers are mapped within the I/O space. Sixteen (16) consecutive address are used (8-bit data path).

I/O space addr.	Register	Description
	Z8536 (1) controller	
$1	PEDR	Port E Data Register
$3	PBDR	Port B Data Register
$5	PADR	Port A Data Register
$7	PCIO1	Pointer #1 Register
	Z8536 (2) controller	
$9	PFDR	Port F Data Register
$B	PDDR	Port D Data Register
$D	PCDR	Port C Data Register
$F	PCIO2	Pointer #2 Register

Table 2 Direct access registers

5.1.3 INT SPACE

The ATC-CIO32 module use the two (2) Interrupts available to the IPbus.

Upon receiving an interrupt ,for example INTREQ1, the host can read the Interrupt vector from the interrupter,in this case from Z8536 # 2, by accessing the IP module whithin the host INT space lbase address + $02.

The IP module is making the difference between a response to INTREQ0 and INTREQ1 by decoding the address LA01.

5.1.4 MEMORY SPACE

A 2k on-board EEPROM is used to store the data for the ID space.

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Only 32 bytes are used.

The left-over space (2Kbytes- 32 bytes) can be accessed by the user in the memory space to store parameters.

5.1.5 WAIT STATE CYCLES

The table below shows the wait states generated by the module when accessed.

Space	Wait state Read	Wait state Write
I/O	2	2
Identification	2	2
Interrupt ack.	6	N/A

Table 3 Wait state

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6. Z6536 REGISTERS ACCESS AND PROGRAMMING

Z8536 CIO data registers use only two address A0 and A1. All the internal registers access use a two step sequence.

1. first write the address of the target register (6 bit) to the pointer register Pointer #1 (Z8536 #1) or Pointer #2 (Z8536 #2),
2. then read or write to the selected data register defined above.

6.1.1 RESET

The CIO32 is resetted by an hardware reset (IPRST = " 0 ") or software reset (writting into Master Interrupt Control Register with D0 = " 1 " .)

6.1.2 INITIALISATION

Initialisation will then begin by writting into Master Interrupt Control Register with D0 = " 0 " ;

Now we are in state 0 . Read cycle will return always with D0 = " 1 " if precedent operation is not performed .

Write to the pointer address register than read or write the pointed register

Read register can be made continuously without writting to the pointer again

Avoid to stay in state 1 because many internal operations are suspended .

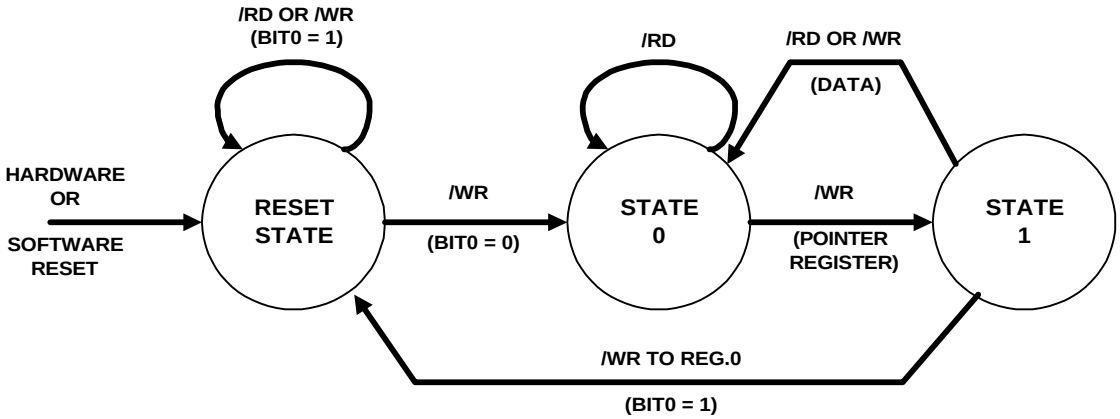


Figure 2State machine operation

6.1.3 DATA PORT REGISTER

Data Port A , B , C , D , E , F can be accessed directely at I/O base address as shown on table 1 . Internal state machine provide an automatic delay of 500 nS between /RD or /WR access .

6.1.4 INTERRUPT SOURCE AND TIMING

Interrupt source are :

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- Pattern recognition using bit mode
- ACKIN using handshake mode
- Counter/Timers

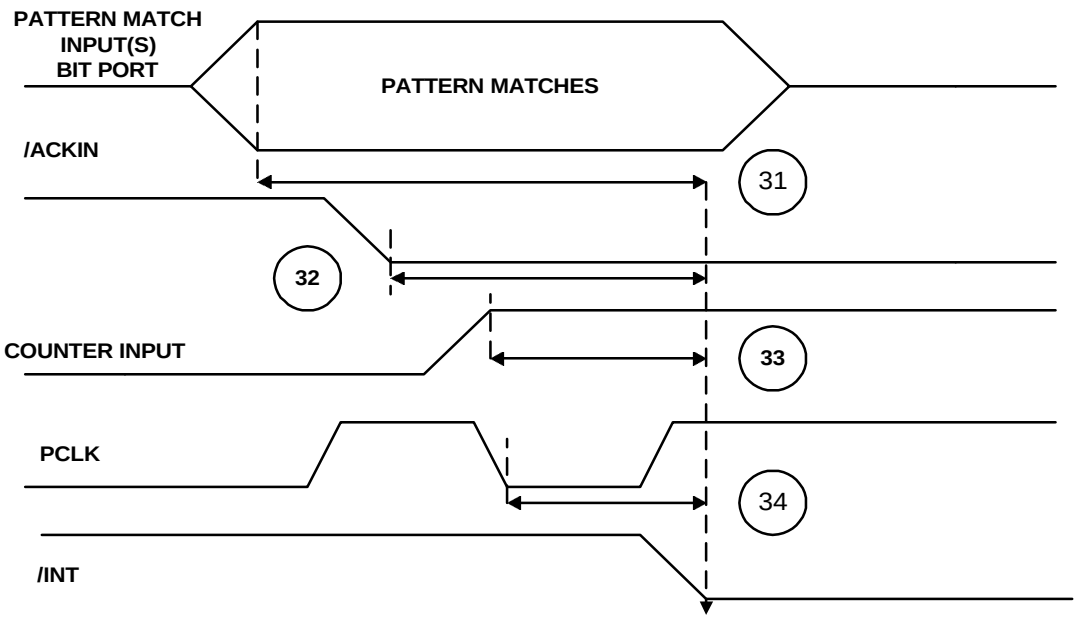


Figure 3Interrupt timing

Timing	Min	Max	Unit
31 TdPM(INT)			ns
32 TdACK(INT)			µs
33 TdCI(INT)			µs
34 TdPC(INT)			µs

Table 4Interrupt timing

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7. Z8536 INTERNAL MAPPING

Z8536	R/W	Description
$00	R/W	Master interrupt control register
$01	R/W	Master configuration control register
$02	R/W	Port A Interrupt vector register
$03	R/W	Port B Interrupt vector register
$04	R/W	Counter/Timer vector register
$05	R/W	Port C data path register
$06	R/W	Port C data direction register
$07	R/W	Port C special I/O control register

Table 5 Main control Registers

Z8536	R/W	Description
$08	R/W*	Port A command and Status register
$09	R/W*	Port B Command and Status
$0A	R/W*	Counter/Timer 1's Command andStatus
$0B	R/W*	Counter/Timer 2's Command and Status
$0C	R/W*	Counter/Timer 3's Command and Status
$0D	R/W	Port A data (can be accessed directely)
$0E	R/W	Port B data (can be accessed directely)
$0F	R/W	Port C data (can be accessed directely)

Table 6 Most often accessed registers

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Z836	R/W	Description
$20	R/W	Port A mode specification
$21	R/W	Port A handshake specification
$22	R/W	Port A data pathg polarity
$23	R/W	Port A data direction
$24	R/W	Port A special I/O control
$25	R/W	Port A pattern polarity
$26	R/W	Port A pattern transition
$27	R/W	Port A pattern mask

Table 7Port A Specification Registers

Z8536	R/W	Description
$28	R/W	Port B mode specification
$29	R/W	Port B handshake specification
$2A	R/W	Port B data pathg polarity
$2B	R/W	Port B data direction
$2C	R/W	Port B special I/O contro
$2D	R/W	Port B pattern polarity
$2E	R/W	Port B pattern transition
$2F	R/W	Port B pattern mask

Table 8Port B Specification Registers

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Z8536	R/W	Description
$10	R	Counter/Timer 1 current count MSB
$11	R	Counter/Timer 1 current count LSB
$12	R	Counter/Timer 2 current count MSB
$13	R	Counter/Timer 2 current count LSB
$14	R	Counter/Timer 3 current count MSB
$15	R	Counter/Timer 3 current count LSB
$16	R/W	Counter/Timer 1 current count MSB
$17	R/W	Counter/Timer 1 current count LSB
$18	R/W	Counter/Timer 2 current count MSB
$19	R/W	Counter/Timer 2 current count LSB
$1A	R/W	Counter/Timer 3 current count MSB
$1B	R/W	Counter/Timer 3 current count LSB
$1C	R/W	Counter/Timer 1 Mode Specification
$1D	R/W	Counter/Timer 2 Mode Specification
$1E	R/W	Counter/Timer 3 Mode Specification
$1F	R	Current vector

Table 9Counter/Timer Related Registers

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8. CONNECTOR

All the 4 I/O ports signals are available on the 50 pin connector with also the 2 special 4 bit from port E and F.Ground(GND) and +5V are also provided. The latter is protected by a Fuse.

PIN	SIGNAL	PIN	SIGNAL
1	GND	26	GND
2	Port A0	27	Port A1
3	Port A2	28	Port A3
4	Port E0	29	Port E1
5	Port A4	30	Port A5
6	Port A6	31	Port A7
7	+5V	32	+5V
8	Port B0	33	Port B1
9	Port B2	34	Port B3
10	Port E2	35	Port E3
11	Port B4	36	Port B5
12	Port B6	37	Port B7
13	GND	38	GND
14	Port C0	39	Port C1
15	Port C2	40	Port C3
16	Port F0	41	Port F1
17	Port C4	42	Port C5
18	Port C6	43	Port C7
19	+5V	44	+5V
20	Port D0	45	Port D1
21	Port D2	46	Port D3
22	Port F2	47	Port F3
23	Port D4	48	Port D5
24	Port D6	49	Port D7
25	GND	50	GND

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Table 10 50 pin connector

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