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# ATC-DA816

## 8 channel 16 bit 10uS DA
## Industry Pack Module

## REFERENCE MANUAL

783-10-000-4000
Version 1.1
Jan 2001

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# 1. GENERAL DESCRIPTION

## 1.1 INTRODUCTION

The **ATC_DA816A** is an high performance DIGITAL TO ANALOG module. The **ATC_DA816A** digitize 8 channels with 16 bits of resolution at a maximum conversion rate of 10 µS.

The primary features of the **ATC_DA816A** are as follows:

- Eight 16 bit 10 µS D/A converters.
- Individual buffer for each output.

## 1.2 FUNCTIONAL DESCRIPTION

A functional block diagram of the **ATC_DA816A** is presented below in Figure 1-1.

The **ATC_DA816A** operates as a slave that is managed by the host processor on the IP bus.

The **ATC_DA816A** is supported by ALPHI Technology under *Windows NT* by a **Board Support Package** which is supplied with the card. Other documentation supplied with the card will describe this support in full detail.

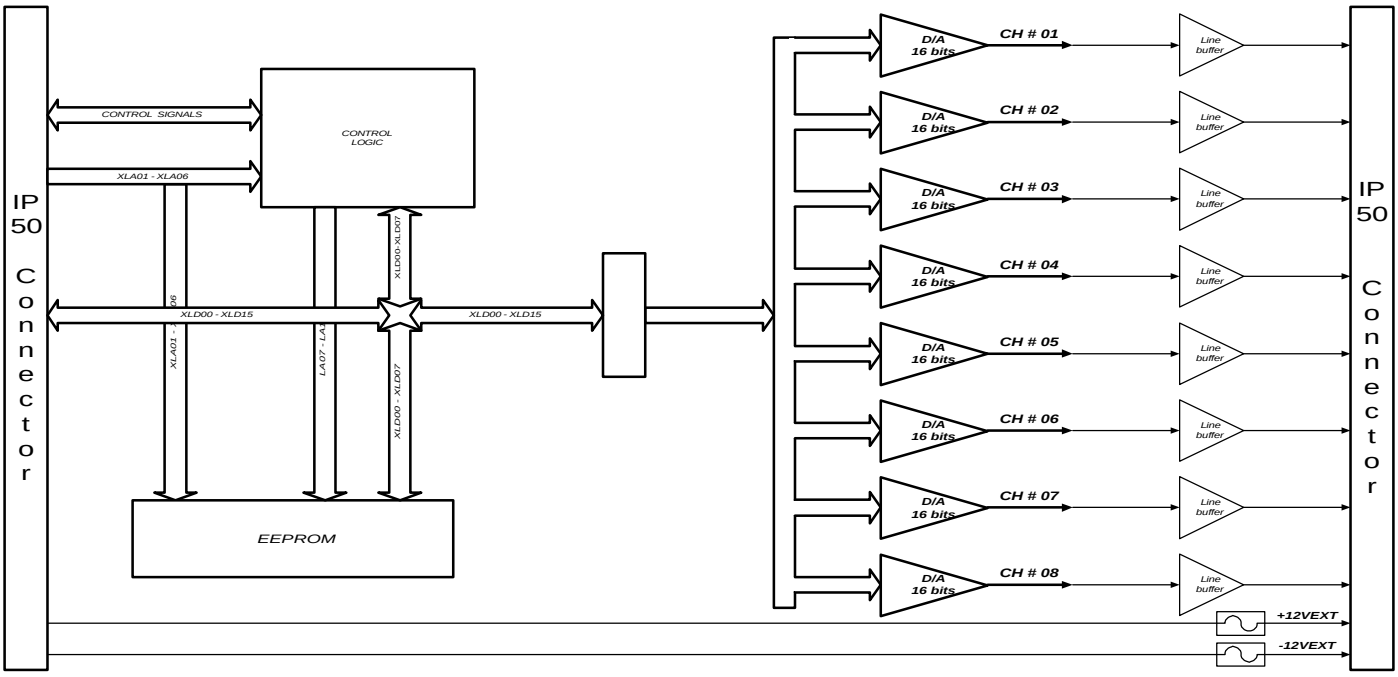



***Figure 1.1: Block Diagram***



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## 2. INTERNAL ORGANIZATION

The **ATC_DA816A** card is divided into different sections. Each section and its relationship to other sections will be discussed. The **ATC_DA816A** sections are:

- IP interface
- Analog Output

### 2.1 IP INTERFACE

#### 2.1.1 IDSPACE

A EEPROM memory that occupies 2 Kbytes address space provide information about the module to the User. The lower address contains data related to the type of module, revision, etc...

The Upper space can be used to store some information. Only ODD address is valid. Each IP to conform to the IP Bus Specification has 32 byte of EEPROM that can be read by the local Host to identifies the IP module Manufacturer, type, revision, etc.

Left over memory (2K-32 byte) is available to the user to stored information related to the module offset  gain error for eventual software correction

| ID space address | Description | Value |
|---|---|---|
| $01 | ASCII “I” | $49 |
| $03 | ASCII “P” | $50 |
| $05 | ASCII “A” | $41 |
| $07 | ASCII “H” | $48 |
| $09 | Manufacturer identification | $11 |
| $0B | Module type | $0D |
| $0D | Revision module | $0B |
| $0F | Reserved | |
| $11 | Driver ID,low byte | |
| $13 | Driver ID,high byte | |
| $15 | Number of bytes used | $0A |
| $17 | CRC | |
| $19-$3F | User space | |

***Table 2-1 FLASH  byte content***



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Address $01-$07 identifies “IPAH”. Also this identifies the EEprom beginning.

### 2.1.2 IOSPACE

#### 2.1.2.1 LOCAL REGISTERS

The DAC0816A module use 8 DAC712 D/A converter from Burr-Brown

A double buffered interface is use to transfer incoming data to the output.

The First 8 address are used to pre-load data into the first stage of each D/A converter.

A write to the next address ($10 ) will transfer the data into the output register in a synchronous manner.

The Next 8 address are used to transfer directly data to the output.

Eight registers associated one to each channel are located into the I/O space



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| Offset | Register Name | |
|---|---|---|
| $00 | Ch # 1 | First register stage pre_load of D/A # 1 |
| $02 | Ch # 2 | First register stage pre_load of D/A # 2 |
| $04 | Ch # 3 | First register stage pre_load of D/A # 3 |
| $06 | Ch # 4 | First register stage pre_load of D/A # 4 |
| $08 | Ch # 5 | First register stage pre_load of D/A # 5 |
| $0A | Ch # 6 | First register stage pre_load of D/A # 6 |
| $0C | Ch # 7 | First register stage pre_load of D/A # 7 |
| $0E | Ch # 8 | First register stage pre_load of D/A # 8 |
| $11 | DAC_OUT | Analog Output update of all D/A"s |
| $19 | DAC_RST | D/A reset |
| $20 | Ch # 1 | Direct transfer of Data to Output D/A # 1 |
| $22 | Ch # 2 | Direct transfer of Data to Output D/A # 2 |
| $24 | Ch # 3 | Direct transfer of Data to Output D/A # 3 |
| $26 | Ch # 4 | Direct transfer of Data to Output D/A # 4 |
| $28 | Ch # 5 | Direct transfer of Data to Output D/A # 5 |
| $2A | Ch # 6 | Direct transfer of Data to Output D/A # 6 |
| $2C | Ch # 7 | Direct transfer of Data to Output D/A # 7 |
| $2E | Ch # 8 | Direct transfer of Data to Output D/A # 8 |

***Table 2.1: Registers***

### 2.1.3 INTSPACE

not used



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### 2.1.4 Memory space

The on board EEPROM provide a 2K space available for the user ( in reality 2k-32bytes)

## 2.2 ANALOG OUTPUT

The **ATC_DA816A** has eight analog output each with its own buffer.

The outputs are +/- 10 Volts.

| | |
|---|---|
| DAC712 Burr-Brown | |
| Input code | Binary Two'Complement |
| Linearity error | +/- 2 LSB |
| Differential Linearity Error | +/- 2 LSB |
| Bipolar Zero error | +/-20mV or +/- 1% of FSR |
| Settling time ( to 0.003% of FSR ) | |
| -20V Output Step | 10 μS |
| Output Slew rate 10V/uS | |
| OPA132 | |
| Input offset | +/- .5 mV typ. |
| Slew rate | 20V/uS |
| Voltage output : | |
| -RL = 10 KΩ | (V+)-1.2 min (V-)+0.5 min |
| -RL = 2 KΩ | (V+)-1.5 min (V-)+1.2 min |
| -RL = 600Ω | (V+)-2.5 min (V-)+1.9 min |
| High load capacitance | |
| Low noise | |



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## 3. OUTPUT CONNECTOR

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | | 26 | |
| 2 | | 27 | AGND |
| 3 | D/A # 1 | 28 | AGND |
| 4 | AGND | 29 | AGND |
| 5 | D/A # 2 | 30 | AGND |
| 6 | AGND | 31 | +12VEXT |
| 7 | | 32 | |
| 8 | +12VEXT | 33 | AGND |
| 9 | D/A # 3 | 34 | AGND |
| 10 | AGND | 35 | AGND |
| 11 | D/A # 4 | 36 | AGND |
| 12 | AGND | 37 | |
| 13 | | 38 | |
| 14 | | 39 | AGND |
| 15 | D/A # 5 | 40 | AGND |
| 16 | AGND | 41 | AGND |
| 17 | D/A # 6 | 42 | AGND |
| 18 | AGND | 43 | -12VEXT |
| 19 | | 44 | |
| 20 | -12VEXT | 45 | AGND |
| 21 | D/A # 7 | 46 | AGND |
| 22 | AGND | 47 | AGND |
| 23 | D/A # 8 | 48 | AGND |
| 24 | AGND | 49 | |
| 25 | | 50 | |



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