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ATC-OPTO_IN16

16 Channel Opto isolated INPUT

REFERENCE MANUAL

785-10-000-4000

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1. INTRODUCTION

The ATC-OPTO_IN16 module from ALPHI TECHNOLOGY is design around the Z8536 CIO Counter/Timer and Parallel I/O .

The one on board Z8536 provide up to :

- 2 Input ports (8 bits each)
- one special port (4bit each)

The ATC-OPTO_IN16 meets the single-wide Industry Pack standard according to the INDUSTRY PACK VITA 4 Specifications. An on-board non-volatile EEPROM maintains ATC-OPTO_IN16 indentification codes and provides additional user space.

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2. FEATURES

- Single-size INDUSTRY PACK module.
- Two Opto INPUT ports
- 4 bit special Port

- EEPROM on board (2 K bytes)
- 5 V only power supply
- Optional Extended temperature grade (-40°C to + 85°C)

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3. DESCRIPTION

The ATC-OPTO_IN16 is populated with one Zilog Counter/Timer and parallel I/O Z8536

Each devices provides :

- Two 8bit ports with each bit that can be programmed as Input ot Output.
- Three 16 bit Counter/ Timers that can be linked toghther.
- The flexibility of each timer is enhanced by the provision of up to four lines per Counter/Timer
- A third port (4 bit) provide possibilities of Handshake lines for Port A and B.

Specific patterns can be reconized using Port A and B with interrupt generation capabilities. In addition a 2K bytes EEPROM is available on board for user use.The First 64 bytes are pre-programmed by ALPHI to provide an identification information concerning the module in accordance of the VITA 4.0 specifications.

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3.1.1 GENERAL PURPOSE PORTS A AND B

Port A and B are identical,except that port B can be specified to provide external acces to Counter /Timers # 1and # 2.

Either port can be programmed to be :

- handshake driven port
- double buffered port (input,output,or bidirectional)
- a control type port with each bit direction controlled individualy.

Pattern reconition can be made by each port with interrupt generation when matched pattern occurs.

Each port has 12 registers to control all these capabilities.

3.1.2 PORT C

Port C function depens upon port A and port B utilization. Port C can be used :

- handshake lines
- I/O needs
- External access for the Counter/Timer # 3

3.1.3 COUNTER/TIMERS

Each Z8536 has three identical counter timers that can eventually be linked toguether. Each Counter/Timer has up to four lines to enhance and control their functionality

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They can be used as :

- Counter input
- Gate input
- Trigger input
- Counter/Timer output

Output can be :

- a pulse
- one-shot
- square wave

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4. ATC-OPTO_IN16 SPACES

The following paragraph describe the different spaces used by the ATC-OPTO_IN16

- **ID** space INDUSTRY PACK identification codes
- **I/O** space CIO controllers registers access
- **INT** space Interrupt acknowledge
- **Memory** space User space

The base address of these spaces depends on the specific INDUSTRY PACK carrier used.

4.1.1 ID SPACE

The identification space is defined as follows:

	Description	value
$01	Ascii "I"	$49
$03	Ascii "P"	$50
$05	Ascii "A"	$41
$07	Ascii "C"	$43
$09	Manufacturer identification	$11
$0B	Module type	$0E
$0D	Revision module	$0A
$0F	Reserved $00	
$11	Software Driver #	low byte
$13	Software Driver #	high byte
$15	Number of bytes used in ID space	$0A
$17	CRC	
$19-3F	User available	

Correct reading of the first four bytes that contain the ASCII text "IPAC" can be used to identifie the presence of an Industries Pack module.

Location $09 provide the Manufacturer identities (ALPHI TECHNOLOGY INDUSTRY PACKs $11).

The next two location identifies the module type and revision.

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A 8-bit CHECKSUM (CRC) provide data integrity of the valid ID code set by the manufacturer.

The next bytes $ 19 to $ 3F are free for user data storage.

4.1.2 I/O SPACE

The two Z8536 controller registers are mapped within the I/O space. Sixteen (16) consecutive address are used (8-bit data path).

I/O space addr.	Register	Description
$1	PCDR	Port C Data Register
$3	PBDR	Port B Data Register
$5	PADR	Port A Data Register
$7	PR	Pointer Register

Table 1 Direct access registers

4.1.3 WAIT STATE CYCLES

The table below shows the wait states generated by the module when accessed.

Space	Wait state Read	Wait state Write
I/O	2	2
Identification	2	2
Interrupt ack.	4	N/A

Table 2 Wait state

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5. Z6536 REGISTERS ACCESS AND PROGRAMMING

Z8536 CIO data registers use only two address A0 and A1. All the internal registers access use a two step sequence.

1. first write the address of the target register (6 bit) to the pointer register .
2. then read or write to the selected data register defined above.

5.1.1 RESET

The CIO32 is resetted by an hardware reset (IPRST = " 0 ") or software reset (writting into Master Interrupt Control Register with D0 = " 1 " .)

5.1.2 INITIALISATION

Initialisation will then begin by writting into Master Interrupt Control Register with D0 = " 0 " ;

Now we are in state 0 . Read cycle will return always with D0 = " 1 " if precedent operation is not performed .

Write to the pointer address register than read or write the pointed register

Read register can be made continuously without writting to the pointer again

Avoid to stay in state 1 because many internal operations are suspended .

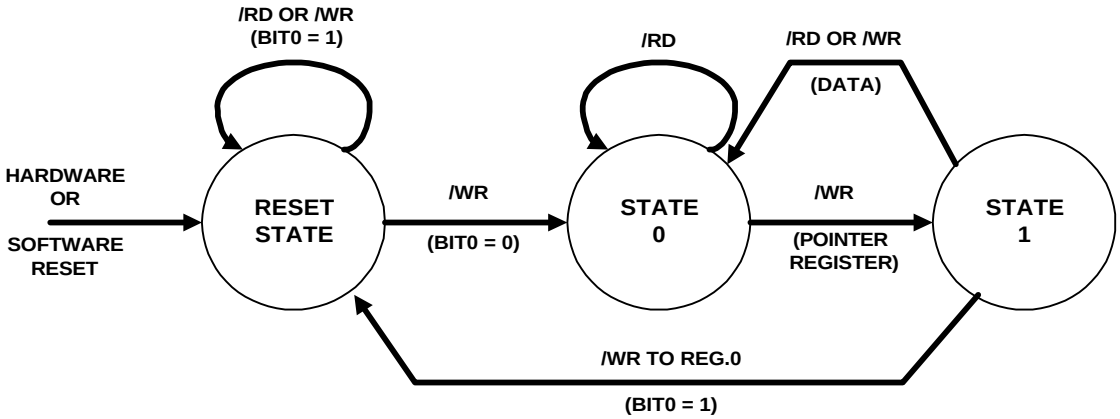


Figure 1State machine operation

5.1.3 DATA PORT REGISTER

Data Port A , B , C can be accessed directely at I/O base address as shown on table 1 . Internal state machine provide an automatic delay of 500 nS between /RD or /WR access .

5.1.4 INTERRUPT SOURCE AND TIMING

Interrupt source are :

- Pattern recognition using bit mode

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- ACKIN using handshake mode
- Counter/Timers

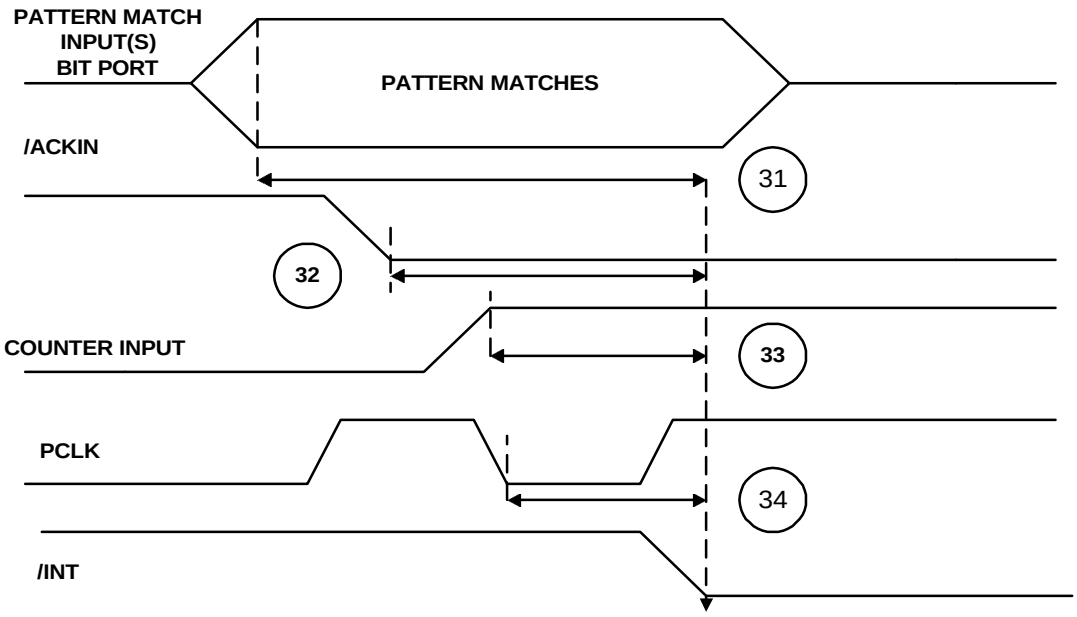


Figure 2Interrupt timing

Timing	Min	Max	Unit
31 TdPM(INT)			ns
32 TdACK(INT)			µs
33 TdCI(INT)			µs
34 TdPC(INT)			µs

Table 3Interrupt timing

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6. Z8536 INTERNAL MAPPING

Z8536	R/W	Description
$00	R/W	Master interrupt control register
$01	R/W	Master configuration control register
$02	R/W	Port A Interrupt vector register
$03	R/W	Port B Interrupt vector register
$04	R/W	Counter/Timer vector register
$05	R/W	Port C data path register
$06	R/W	Port C data direction register
$07	R/W	Port C special I/O control register

Table 4 Main control Registers

Z8536	R/W	Description
$08	R/W*	Port A command and Status register
$09	R/W*	Port B Command and Status
$0A	R/W*	Counter/Timer 1's Command andStatus
$0B	R/W*	Counter/Timer 2's Command and Status
$0C	R/W*	Counter/Timer 3's Command and Status
$0D	R/W	Port A data (can be accessed directely)
$0E	R/W	Port B data (can be accessed directely)
$0F	R/W	Port C data (can be accessed directely)

Table 5 Most often accessed registers

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Z836	R/W	Description
$20	R/W	Port A mode specification
$21	R/W	Port A handshake specification
$22	R/W	Port A data pathg polarity
$23	R/W	Port A data direction
$24	R/W	Port A special I/O control
$25	R/W	Port A pattern polarity
$26	R/W	Port A pattern transition
$27	R/W	Port A pattern mask

Table 6Port A Specification Registers

Z8536	R/W	Description
$28	R/W	Port B mode specification
$29	R/W	Port B handshake specification
$2A	R/W	Port B data pathg polarity
$2B	R/W	Port B data direction
$2C	R/W	Port B special I/O contro
$2D	R/W	Port B pattern polarity
$2E	R/W	Port B pattern transition
$2F	R/W	Port B pattern mask

Table 7Port B Specification Registers

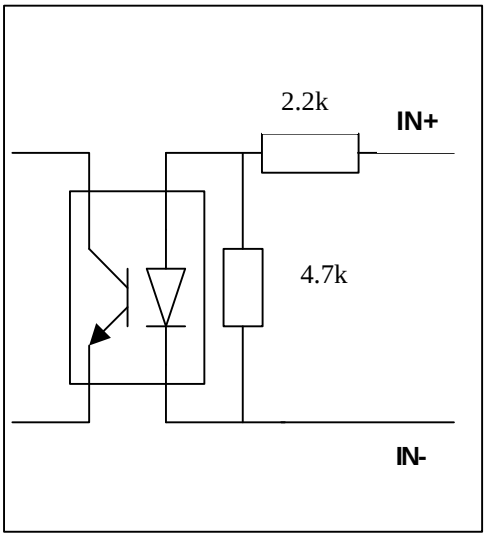
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Z8536	R/W	Description
$10	R	Counter/Timer 1 current count MSB
$11	R	Counter/Timer 1 current count LSB
$12	R	Counter/Timer 2 current count MSB
$13	R	Counter/Timer 2 current count LSB
$14	R	Counter/Timer 3 current count MSB
$15	R	Counter/Timer 3 current count LSB
$16	R/W	Counter/Timer 1 current count MSB
$17	R/W	Counter/Timer 1 current count LSB
$18	R/W	Counter/Timer 2 current count MSB
$19	R/W	Counter/Timer 2 current count LSB
$1A	R/W	Counter/Timer 3 current count MSB
$1B	R/W	Counter/Timer 3 current count LSB
$1C	R/W	Counter/Timer 1 Mode Specification
$1D	R/W	Counter/Timer 2 Mode Specification
$1E	R/W	Counter/Timer 3 Mode Specification
$1F	R	Current vector

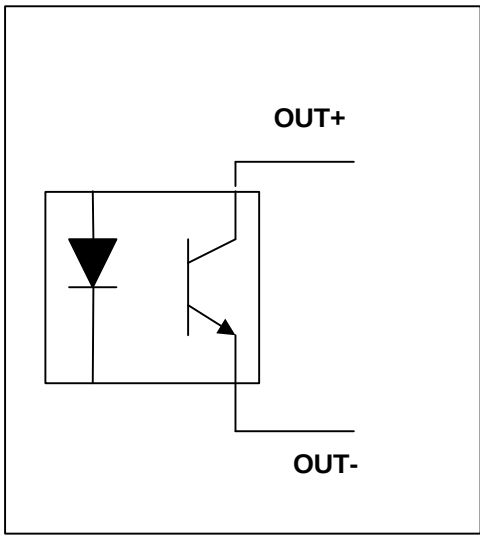
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7. INTPUT CIRCUIT

All port A , B and 2 bits on port C (PC1 and PC3) are connect to a intput opto circuit .



Two bit on port C (PC0 and PC3) are connect in input opto circuit.



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8. CONNECTOR

PIN	SIGNAL	PIN	SIGNAL
1	OUT17+	26	OUT17-
2	IN01+	27	IN01-
3	IN02+	28	IN02-
4	OUT20+	29	OUT20-
5	IN03+	30	IN03-
6	IN04+	31	IN04-
7	STROB1+	32	STROB1-
8	IN05+	33	IN05-
9	IN06+	34	IN06-
10	STROB2+	35	STROB2-
11	IN07+	36	IN07-
12	IN08+	37	IN08-
13	NC	38	NC
14	IN09+	39	IN09-
15	IN10+	40	IN10-
16	NC	41	NC
17	IN11+	42	IN11-
18	IN12+	43	IN12-
19	NC	44	NC
20	IN13+	45	IN13-
21	IN14+	46	IN14-
22	NC	47	NC
23	IN15+	48	IN15-
24	IN16+	49	IN16-
25	NC	50	NC

Table 8 50 pin connector

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