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# CPCI-OUT48

## 48 Channels of Optically Isolated Digital Outputs for 3U *CPCI*™ Systems

## REFERENCE MANUAL

742-11-000-4000
Version 1.1
June 1998

**ALPHI TECHNOLOGY CORPORATION**

**6202 S. Maple Avenue #120**
**Tempe, AZ 85283 USA**
**Tel: (480) 838-2428**
**Fax: (480) 838-4477**

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# 1. GENERAL DESCRIPTION

## 1.1 INTRODUCTION

The **CPCI-OUT48** is a CPCI expansion card in a 3U form factor. The **CPCI-OUT48** allows:

- 48 optically isolated digital outputs writable by the CPCI HOST computer
- Direct memory mapped access to the registers
- Front panel I/O connectors for all outputs
- High current / voltage outputs for control applications
- Optional high speed optocouplers for communication applications

## 1.2 FUNCTIONAL DESCRIPTION

A functional block diagram of the **CPCI-OUT48** is presented below in Figure 1-1.

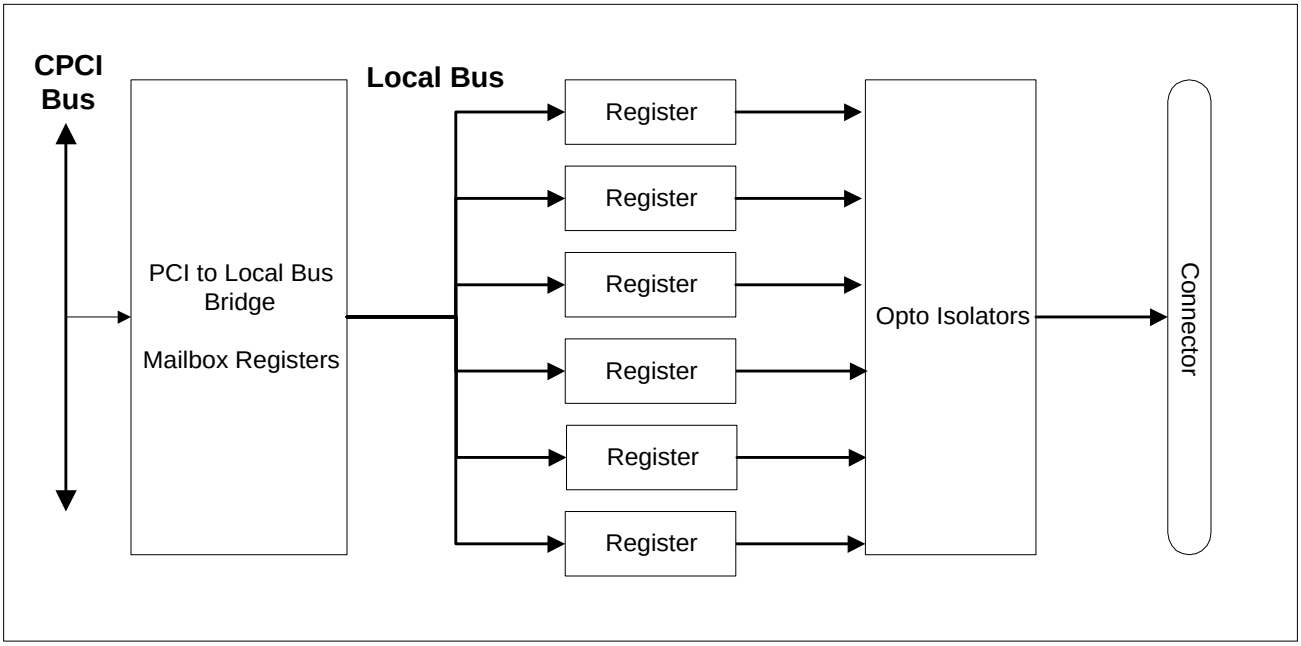



***Figure 1.1: Block Diagram***

The jumper and the connector placement is depicted in Figure 1-2.



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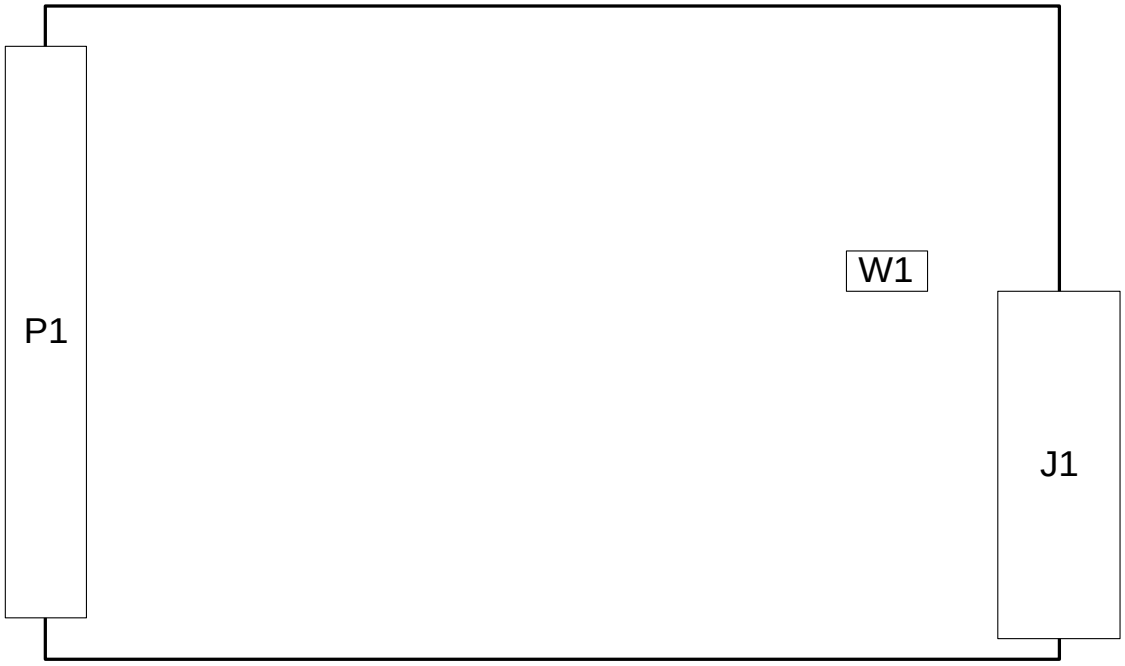



***Figure 1.2: Jumper and Connector Locations***

The **CPCI-OUT48** operates as a slave that is managed by the host processor on the CPCI bus.

The **CPCI-OUT48** is supported by ALPHI Technology under *Windows NT* by a **Board Support Package** which is supplied with the card. Other documentation supplied with the card will describe this support in full detail.

This is provided in a manner consistent across ALPHI Technology platforms.

### 1.3 Hardware Options

There are two hardware options available. Option –1 is for control applications and is the default configuration. Option –2 is for high speed digital signals.

| Parameter | Option -1 | Option -2 |
|---|---|---|
| $t_{on}$ | 1 mS | 5 μS |
| $t_{off}$ | 50 μS | 5 μS |
| $i_{max}$ | 140 mA | 5 mA |
| $r_{on}$ | < 15 Ω | 50 Ω |
| $V_{max}$ | 100 V peak AC / DC | 50 VDC |

***Table 1.1: Hardware Options***



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## 1.4 REFERENCE MATERIALS LIST

The reader should refer to the PCI Local Bus Specification for a detailed explanation of the PCI bus architecture and timing requirements. This specification is available from the following source:

**PCI Special Interest Group**
**PO Box 14070**
**Portland, OR 97214**
**Tel: (800) 433-5177**
**Tel: (503) 797-4207**
**Fax: (503) 234-6762**

The reader is also referred to the S5933 PCI Controller data book:

**AMCC Applied Micro Circuits Corporation**
**6195 Lusk Boulevard**
**San Diego, CA 92121-2793**
**Tel: (800) 755-2622**
**http://www.amcc.com**

WindowsNT and Windows95 Programming Tools:

**BlueWater Systems**
**144 Railroad Ave. Suite #217**
**Edmonds, WA 98020**
**Tel: (206) 771-3610**
**Fax: (206) 771-2742**
**E-Mail: info@bluewatersystems.com**
**Web: http://www.bluewatersystems.com**



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# 2. HOST (CPCI) SIDE

## 2.1 PCI CONFIGURATION REGISTERS

The card presents the following configuration values to the CPCI system, based on the values stored in the NVRAM device read by the AMCC PCI interface chip.

| Register | Value (Meaning) |
|---|---|
| Vendor ID | 0x13c5 (ALPHI Technology) |
| Device ID | 0x0107 (CPCI-OUT48) |
| Revision ID | 0x00 |
| Class Code | 0xff0000 (Device does not fit into defined class codes) |
| Interrupt Line | 0xff |
| Interrupt Pin | A |
| Multifunction Device | No |
| Build In Self Test | No |
| Latency Timer | 0x00 |
| Minimum Grant | 0x00 |
| Maximum Latency | 0x00 |
| Expansion ROM Size | None |

***Table 2.1: CPCI Configuration Registers***

## 2.2 PCI BASE ADDRESS REGISTERS

The card requests base address regions from the CPCI system after RESET, based on the values stored in the NVRAM device read by the AMCC PCI interface chip.

The decode addresses of these regions are assigned by the host processor. The **CPCI-OUT48** uses 2 of the 5 AMCC mapped base address registers. The AMCC is normally programmed at the factory to request the following resources from the CPCI BIOS:

| BAR | From | To | Description | Type |
|---|---|---|---|---|
| 0 | 0x00000000 | 0x0000003F | AMCC PCI Operation Registers | MEM |
| 1 | 0x00000000 | 0x000000FF | Host Control Region | MEM |

***Table 2.2: Base Addresses and Use***

***NOTE: The AMCC has been programmed to request memory above 1 Mbytes.***



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## 2.3 CPCI OPERATION REGISTERS

The host processor communicates with the **CPCI-OUT48** module via the AMCC pass-through interface. After the base address registers have been programmed by the CPCI configurator, incoming CPCI I/O or Memory cycles are translated into either accesses to the AMCC chip or passed through to the output registers as described in the next section. The PCI Operation Registers of the AMCC 5933 chip are depicted below:

| Offset | Register Name |
|---|---|
| 0x00 | OMB1 Outgoing Mailbox Register 1 |
| 0x04 | OMB2 Outgoing Mailbox Register 2 |
| 0x08 | OMB3 Outgoing Mailbox Register 3 |
| 0x0C | OMB4 Outgoing Mailbox Register 4 |
| 0x10 | IMB1 Incoming Mailbox Register 1 |
| 0x14 | IMB2 Incoming Mailbox Register 2 |
| 0x18 | IMB3 Incoming Mailbox Register 3 |
| 0x1C | IMB4 Incoming Mailbox Register 4 |
| 0x20 | FIFO Register Port (bi-directional) |
| 0x24 | MWAR Master Write Address Register |
| 0x28 | MWTC Master Write Transfer Counter |
| 0x2C | MRAR Master Read Address Register |
| 0x30 | MRTC Master Read Transfer Counter |
| 0x34 | MBEF Mailbox Empty/Full Status |
| 0x38 | INTCSR Interrupt Control/Status Register |
| 0x3C | MCSR Bus Master Control/Status Register |

***Table 2.2: AMCC Registers (HOST)***

For more information about these registers refer to the AMCC PCI controller manual.

## 2.4 Host Control Region

Accesses to the following offsets from BAR1 will allow for communication with the card. There are six byte registers which directly drive the output opto-isolators.

| Offset | Register Name |
|---|---|
| 0x00 | Output Register 0 |
| 0x01 | Output Register 1 |
| 0x02 | Output Register 2 |
| 0x03 | Output Register 3 |
| 0x04 | Output Register 4 |
| 0x05 | Output Register 5 |
| 0x08 | LED Register |

***Table 2.3: Host Control Region***



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### 2.4.1 Output Registers (Write Only)

| BIT 07 | BIT 06 | BIT 05 | BIT 04 | BIT 03 | BIT 02 | BIT 01 | BIT 00 |
|---|---|---|---|---|---|---|---|
| OUT8 | OUT7 | OUT6 | OUT5 | OUT4 | OUT3 | OUT2 | OUT1 |
| OUT16 | OUT15 | OUT14 | OUT13 | OUT12 | OUT11 | OUT10 | OUT9 |
| OUT24 | OUT23 | OUT22 | OUT21 | OUT20 | OUT19 | OUT18 | OUT17 |
| OUT32 | OUT31 | OUT30 | OUT29 | OUT28 | OUT27 | OUT26 | OUT25 |
| OUT40 | OUT39 | OUT38 | OUT37 | OUT36 | OUT35 | OUT34 | OUT33 |
| OUT48 | OUT47 | OUT46 | OUT45 | OUT44 | OUT43 | OUT42 | OUT41 |

***OUTxx Output Bit***

If a bit is a 1, then the associated output transistor of the opto-isolator is turned on.

If a bit is 0, then the output transistor is turned off.

For example, if the emitter is tied to ground, and the collector is connected to +5 Volts through a bias resistor, then the output is low when the bit is a 1, and high when the bit is zero.

Alternatively, if the load is switched directly by the transistor of the opto-isolator, then the load is powered when the bit is a 1 and not powered when the bit is 0.

### 2.4.2 LED Register (Write Only)

When bit 0 is toggled from a 0 to a 1, the LED on the front panel is illuminated for a brief interval.

## 2.5 RESET SIGNALS

The **CPCI-OUT48** is reset when the CPCI bus is reset, when the reset bit of the AMCC 5933 issues a reset, and when jumper W1 is shorted.

After a RESET, all 6 registers are cleared to 0, thereby turning off all the opto-isolators.

## 3. HARDWARE EQUIVALENT

Figure 3.1 displays the output circuit for the –2 option. Polarity is not important for the –1 option, and the –1 option will switch AC loads as well as DC loads.



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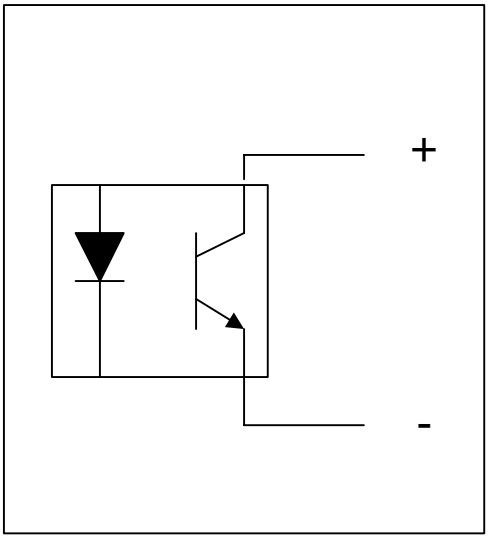



***Figure 3.1: Output Circuit***

## 4. JUMPER DESCRIPTION

A RESET is asserted by shorting jumper W1.

## 5. LED INDICATORS

There are two LED indicators visible at the CPCI card bracket. They are marked with a legend on the bracket, and they are labeled on the PCB as L1 and L2 where L1 is at the top of the card. The LEDs have the following meanings:

| LED | LEGEND | Meaning |
|---|---|---|
| L1 | WR | HOST is writing to an output register. |
| L2 | SW | HOST has written to register LED. |

***Table 5.1 LED Descriptions***



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# 6. CONNECTIONS

## 6.1 DIGITAL OUTPUT CONNECTOR (P1)

A 100 pin subminiature D shelled connector is used to route all the digital output signals off the card. ALPHI Technology can supply transition modules and cable assemblies to meet any special requirements. Contact the factory for additional information.

Connectors are manufactured by AMP and the style is LIMIT.05 Series 3.

| Use | Model |
|---|---|
| On PC Board | 787082-9 |
| Suggested Plug | 749111-8 |

***Table 6.1: I/O Connector Model Numbers***

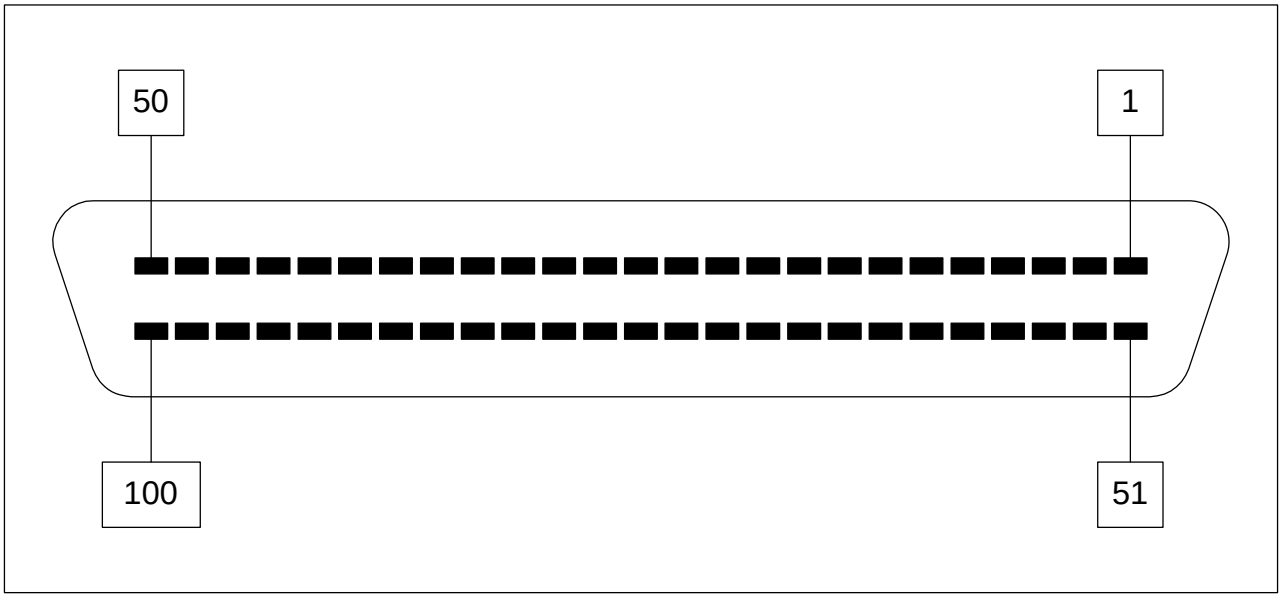



***Figure 6.1: Digital Output Connector***



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| Pin | Connection | Pin | Connection |
|---|---|---|---|
| 1 | +5V Fused | 51 | +5V Fused |
| 2 | Ground | 52 | Ground |
| 3 | OUT47+ | 53 | OUT48+ |
| 4 | OUT47- | 54 | OUT48- |
| 5 | OUT45+ | 55 | OUT46+ |
| 6 | OUT45- | 56 | OUT46- |
| 7 | OUT43+ | 57 | OUT44+ |
| 8 | OUT43- | 58 | OUT44- |
| 9 | OUT41+ | 59 | OUT42+ |
| 10 | OUT41- | 60 | OUT42- |
| 11 | OUT39+ | 61 | OUT40+ |
| 12 | OUT39- | 62 | OUT40- |
| 13 | OUT37+ | 63 | OUT38+ |
| 14 | OUT37- | 64 | OUT38- |
| 15 | OUT35+ | 65 | OUT36+ |
| 16 | OUT35- | 66 | OUT36- |
| 17 | OUT33+ | 67 | OUT34+ |
| 18 | OUT33- | 68 | OUT34- |
| 19 | OUT31+ | 69 | OUT32+ |
| 20 | OUT31- | 70 | OUT32- |
| 21 | OUT29+ | 71 | OUT30+ |
| 22 | OUT29- | 72 | OUT30- |
| 23 | OUT27+ | 73 | OUT28+ |
| 24 | OUT27- | 74 | OUT28- |
| 25 | OUT25+ | 75 | OUT26+ |
| 26 | OUT25- | 76 | OUT26- |
| 27 | OUT23+ | 77 | OUT24+ |
| 28 | OUT23- | 78 | OUT24- |
| 29 | OUT21+ | 79 | OUT22+ |
| 30 | OUT21- | 80 | OUT22- |
| 31 | OUT19+ | 81 | OUT20+ |
| 32 | OUT19- | 82 | OUT20- |
| 33 | OUT17+ | 83 | OUT18+ |
| 34 | OUT17- | 84 | OUT18- |
| 35 | OUT15+ | 85 | OUT16+ |
| 36 | OUT15- | 86 | OUT16- |
| 37 | OUT13+ | 87 | OUT14+ |
| 38 | OUT13- | 88 | OUT14- |
| 39 | OUT11+ | 89 | OUT12+ |
| 40 | OUT11- | 90 | OUT12- |
| 41 | OUT9+ | 91 | OUT10+ |
| 42 | OUT9- | 92 | OUT10- |
| 43 | OUT7+ | 93 | OUT8+ |
| 44 | OUT7- | 94 | OUT8- |
| 45 | OUT5+ | 95 | OUT6+ |
| 46 | OUT5- | 96 | OUT6- |
| 47 | OUT3+ | 97 | OUT4+ |
| 48 | OUT3- | 98 | OUT4- |
| 49 | OUT1+ | 99 | OUT2+ |
| 50 | OUT1- | 100 | OUT2- |

***Table 6.2: Digital Output Connector***



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### 6.2 32 BIT CPCI BUS (J1)

This connector plugs into the backplane and provides the standard CPCI signals for all CPCI systems.

### 6.3 FACTORY USE (P2)

This connector is used at the factory for programming the FPGA.



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