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CPCI-4SIP

Slave Quad IndustryPack® Carrier for 6U *CompactPCI*™ systems

REFERENCE MANUAL

784-12-000-4000
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TABLE OF CONTENTS

1. GENERAL DESCRIPTION _____ 1

1.1 INTRODUCTION _____ 1

1.2 FUNCTIONAL DESCRIPTION _____ 1

1.3 REFERENCE MATERIALS LIST _____ 4

2. HOST (CPCI) SIDE _____ 5

2.1 PCI CONFIGURATION REGISTERS _____ 5

2.2 PCI BASE ADDRESS REGISTERS _____ 5

2.3 PCI IP STATUS REGISTER _____ 6

2.4 CPCI OPERATION REGISTERS _____ 7

2.5 IP ID AND I/O REGION _____ 8

2.6 IP MEMORY REGION _____ 8

3. IP DETAILS _____ 8

3.1 IP MODULE ID SPACE _____ 9

3.2 IP MODULE IO SPACE _____ 9

3.3 IP MODULE MEMORY SPACE _____ 9

3.4 IP MODULE INTERRUPT SPACE _____ 10

4. RESET SIGNALS _____ 10

5. JUMPER DESCRIPTIONS _____ 10

6. LED INDICATORS _____ 11

7. CONNECTIONS _____ 11

7.1 IP I/O CONNECTORS (P1, P2, P4, P5) _____ 11

7.2 REAR I/O JUMPER BLOCK _____ 12

7.3 32 BIT CPCI BUS (P1) _____ 17

7.3 IPSTROPE (P3) _____ 17

Table 2.1: CPCI Configuration Registers _____ 5

Table 5.1 Jumper Descriptions _____ 10

Table 6.1 LED Descriptions _____ 11

Table 7.1: I/O Connector Model Numbers _____ 11

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1. GENERAL DESCRIPTION

1.1 INTRODUCTION

The CPCI-4SIP is a 3U format CompactPCI (CPCI) bus IP carrier. The **CPCI-4SIP** provides mechanical support and the electrical interfaces for four single width IP modules, or two double width IP module. Multiple **CPCI-4SIP** boards may be installed in a single system. The primary features of the **CPCI-4SIP** are as follows:

- Support for up to four IP modules
- 8 MHz or 32 MHz IP operation via jumper selection
- Direct I/O or Memory mapped access from CPCI bus via AMCC 5933 PCI Chip
- Supports double-wide form factor Industry Pack®
- Full interrupt support of host
- Front panel I/O connectors for all IP's

1.2 FUNCTIONAL DESCRIPTION

A functional block diagram of the **CPCI-4SIP** is presented below in Figure 1-1. The jumper placement and the connector placement are depicted in Figure 1-2. The **CPCI-4SIP** operates as a slave that is managed by the host processor on the CPCI bus. Each pair of IP modules share a common clock that can be jumpered for 8 or 32 MHz operation.

The **CPCI-4SIP** is supported by ALPHI Technology under *Windows NT* by a **Board Support Package, which** is supplied with the card. Other documentation supplied with the card will describe this support in full detail.

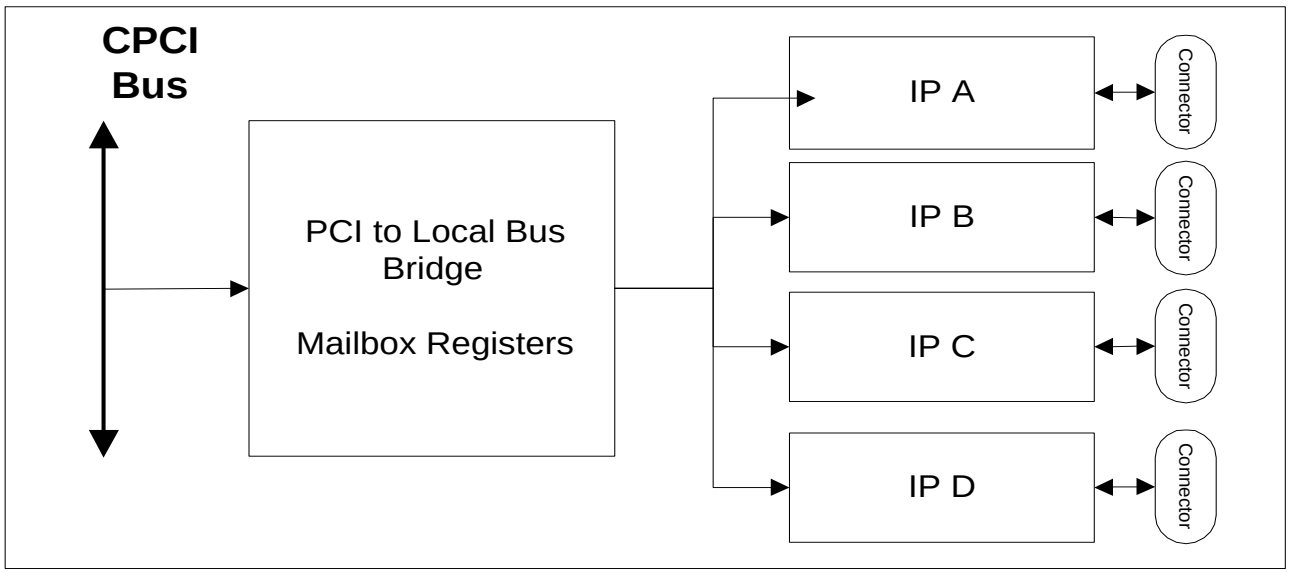


Figure 1.1: Block Diagram

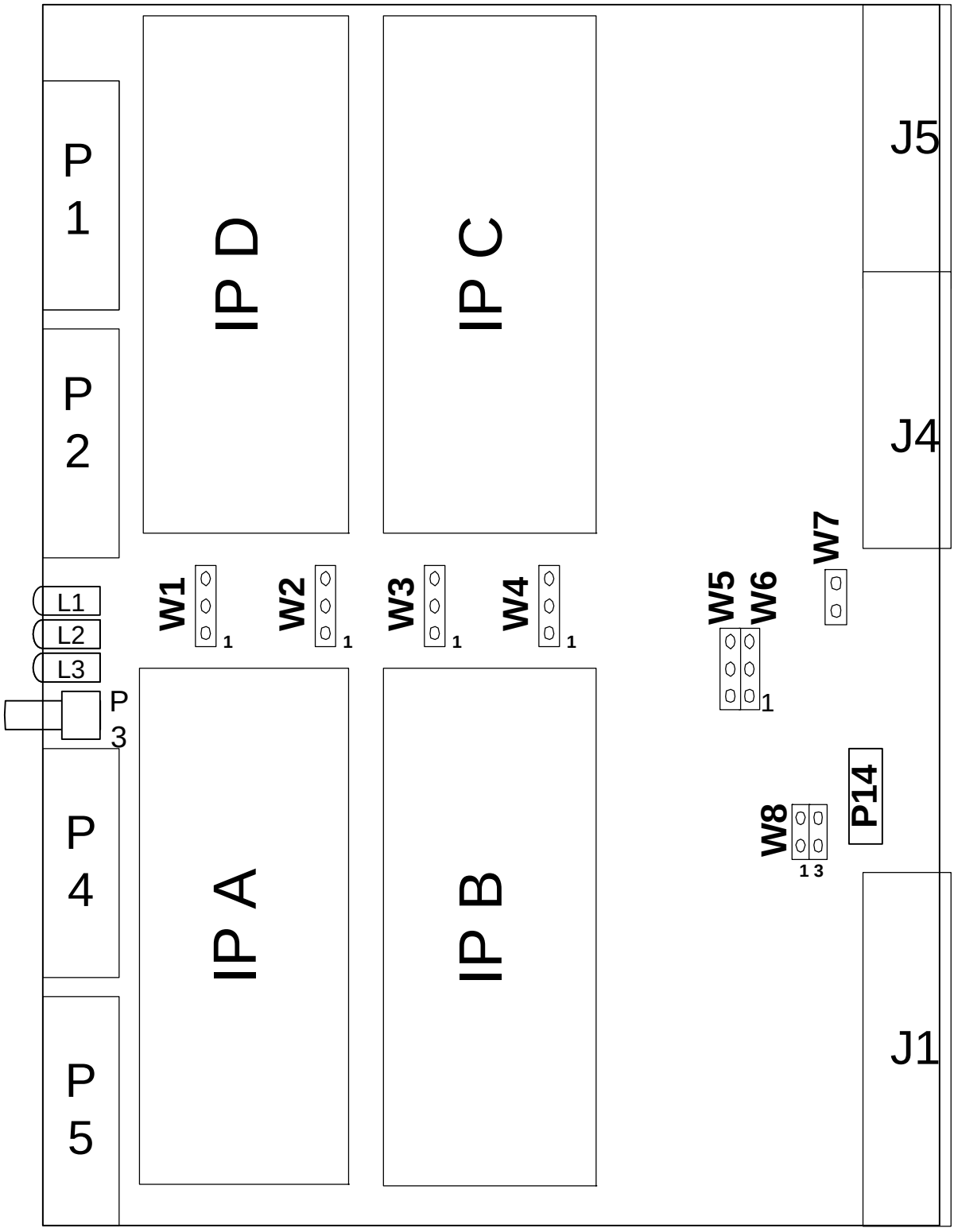
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Figure 1.2: Jumper and Connector Locations

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1.3 REFERENCE MATERIALS LIST

The reader should refer to the PCI Local Bus Specification for a detailed explanation of the PCI bus architecture and timing requirements. This specification is available from the following source:

PCI Special Interest Group
PO Box 14070
Portland, OR 97214
Tel: (800) 433-5177
Tel: (503) 797-4207
Fax: (503) 234-6762

The reader is also referred to the S5933 PCI Controller data book:

AMCC Applied Micro Circuits Corporation
6195 Lusk Boulevard
San Diego, CA 92121-2793
Tel: (800) 755-2622
http://www.amcc.com

WindowsNT and Windows95 Programming Tools:

BlueWater Systems
144 Railroad Ave. Suite #217
Edmonds, WA 98020
Tel: (206) 771-3610
Fax: (206) 771-2742
E-Mail: info@bluewatersystems.com
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2. HOST (CPCI) SIDE

2.1 PCI CONFIGURATION REGISTERS

The card presents the following configuration values to the CPCI system, based on the values stored in the NVRAM device read by the AMCC PCI interface chip.

Register	Value (Meaning)
Vendor ID	0x13c5 (ALPHI Technology)
Device ID	0x0202 (CPCI-4SIP)
Revision ID	0x00
Class Code	0xff0000 (Device does not fit into defined class codes)
Interrupt Line	0xff
Interrupt Pin	A
Multifunction Device	No
Build In Self Test	No
Latency Timer	0x00
Minimum Grant	0x00
Maximum Latency	0x00
Expansion ROM Size	None

Table 2.1: CPCI Configuration Registers

2.2 PCI BASE ADDRESS REGISTERS

The card requests base address regions from the CPCI system after RESET, based on the values stored in the NVRAM device read by the AMCC PCI interface chip.

The decode addresses of these regions are assigned by the host processor. The **CPCI-4SIP** uses 3 of the 4 AMCC mapped base address registers. The AMCC is normally programmed at the factory to request the following resource from the CPCI BIOS:

BAR	From	To	Description	Type
0	0x00000000	0x00000003F	AMCC PCI Operation Registers	MEM
1	0x00000000	0x000007FF	IP ID and IO Region	MEM
3	0x00000000	0x01FFFFFF	IP Memory Region	MEM
4	0x00000000	0x01FFFFFF	IP Memory Region	MEM

Table 2.2: Base Address and Use

NOTE: The AMCC has been programmed to request memory above 1 Mbytes.

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2.3 PCI IP STATUS REGISTER

This register is available to give status of DMA requests and Interrupt requests of each of the four IP locations. To access these registers make a read at base address of IP-A and add C0. With no IP's installed you should see $FFFF. The following Table 2.3 will read results.

Bit	Register Name
Bit 0	INTREQA0
Bit 1	INTREQA1
Bit 2	INTREQB0
Bit 3	INTREQB1
Bit 4	INTREQC0
Bit 5	INTREQC1
Bit 6	INTREQD0
Bit 7	INTREQD1
Bit 8	DMARQA0
Bit 9	DMARQA1
Bit 10	DMARQB0
Bit 11	DMARQB1
Bit 12	DMARQC0
Bit 13	DMARQC1
Bit 14	DMARQD0
Bit 15	DMARQD1

Table 2.3: PCI IP STATUS REGISTER

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2.4 CPCI OPERATION REGISTERS

The host processor communicates with the **CPCI-4SIP** card via the AMCC pass-through interface. After the base address register has been programmed by the CPCI configurator, incoming CPCI I/O or Memory cycles are used to access the registers of the AMCC chip. The PCI Operation Registers of the AMCC 5933 chip are depicted below:

Offset	Register Name
0x00	OMB1 Outgoing Mailbox Register 1
0x04	OMB2 Outgoing Mailbox Register 2
0x08	OMB3 Outgoing Mailbox Register 3
0x0C	OMB4 Outgoing Mailbox Register 4
0x10	IMB1 Incoming Mailbox Register 1
0x14	IMB2 Incoming Mailbox Register 2
0x18	IMB3 Incoming Mailbox Register 3
0x1C	IMB4 Incoming Mailbox Register 4
0x20	FIFO Register Port (bi-directional)
0x24	MWAR Master Write Address Register
0x28	MWTC Master Write Transfer Counter
0x2C	MRAR Master Read Address Register
0x30	MRTC Master Read Transfer Counter
0x34	MBEF Mailbox Empty/Full Status
0x38	INTCSR Interrupt Control/Status Register
0x3C	MCSR Bus Master Control/Status Register

Table 2.4: AMCC Registers (HOST)

For more information about these registers refer to the AMCC PCI controller manual.

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2.5 IP ID AND I/O REGION

16 bit accesses to the following offsets from BAR1 will allow for communication with the four IPs. Unspecified addresses are reserved. Note that the **CPCI-4SIP** only supports 16-bit access to the I/O regions, but it does support 32-bit access to memory regions.

FROM	TO	R/W	REGION
0x00	0x3F	R/W	IP_A ID Space
0x80	0x81	R	IP_A Interrupt Vector 0
0x82	0x83	R	IP_A Interrupt Vector 1
0x100	0x17F	R/W	IP_A I/O Space
0x200	0x23F	R/W	IP_B ID Space
0x280	0x281	R	IP_B Interrupt Vector 0
0x282	0x283	R	IP_B Interrupt Vector 1
0x300	0x37F	R/W	IP_B I/O Space
0x400	0x43F	R/W	IP_C ID Space
0x480	0x481	R/W	IP_C Interrupt Vector 0
0x482	0x483	R/W	IP_C Interrupt Vector 1
0x500	0x57F	R/W	IP_C I/O Space
0x600	0x63F	R/W	IP_D ID Space
0x680	0x681	R/W	IP_D Interrupt Vector 0
0x682	0x683	R/W	IP_D Interrupt Vector 1
0x700	0x77F	R/W	IP_D I/O Space

Table 2.5: IP ID and I/O Regions

2.6 IP MEMORY REGION

16 bit and 32 bit accesses to the following offsets from BAR2 & BAR3 will allow for communication with the four IPs. If the jumper is set for 32-bit access, then all four IPs are strobed.

AMCC	FROM	TO	R/W	REGION
BAR3	0x000000	0x7FFFFF	R/W	IP_A Memory Space
BAR3	0x800000	0xFFFFFF	R/W	IP_B Memory Space
BAR4	0x000000	0x7FFFFF	R/W	IP_C Memory Space
BAR4	0x800000	0xFFFFFF	R/W	IP_D Memory Space

Table 2.6: IP Memory Regions

3. IP DETAILS

Please consult the IP User's Manual for details about accessing the particular IP used.

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3.1 IP MODULE ID SPACE

Each IP must support identification PROM. The CPCI-4SIP decodes 64 bytes of ID space for each IP module. The ID PROM contains information about each the IP, which is defined in the Industry Pack Specification. The four IP ID's spaces can be accessed at fixed offsets from Base Address 1, as indicated in Table 2.5. The information required for the most common IP PROM format is shown below:

OFFSET	DESCRIPTION	VALUE
0x00	ASCII "I"	0x49
0x02	ASCII "P"	0x50
0x04	ASCII "A"	0x41
0x06	ASCII "C"	0x43
0x08	Manufacturer ID	
0x0A	Model No	
0x0C	Revision	
0x0E	Reserved	0x00
0x10	Driver ID, Low Byte	
0x12	Driver ID, High Byte	
0x14	Number of bytes used	0x0C
0x16	CRC	
OFFSET	**DESCRIPTION**	**VALUE**
0x18-0x3F	User Space	

Table 3.1: Typical ID Space Layout

3.2 IP MODULE IO SPACE

The CPCI-4SIP decodes 128 bytes of IO space for each IP module. The four IP I/O spaces can be accessed at fixed offsets from Base Address 1, as indicated in Table 2.5.

3.3 IP MODULE MEMORY SPACE

The CPCI-4SIP decodes 8 Mbytes of MEM space for each IP module. The four IP MEM spaces can be accessed at fixed offsets from Base Address 2 and Base Address 3, indicated in Table 2.6.

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3.4 IP MODULE INTERRUPT SPACE

The CPCI-4SIP routes the interrupts from all IP modules to the INTA# signal on the CompactPCI bus. The CPCI-4SIP decodes 2 16-bit words of INT space for each IP module to supply an optional interrupt vector. The four IP INT spaces can be accessed at fixed offsets from Base Address 1, as indicated in Table 2.5. IMB4 in the AMCC 5933 PCI Interface chip is written by the CPCI-4SIP hardware when one or more IP modules are asserting an interrupt. If incoming Mailbox 4 Byte 3 interrupts have been enabled, then the CPCI-4SIP will assert INTA#. Some IP modules may require that the host processor perform a read to INT space to clear pending interrupts. The PCI Operation Registers MBEF and INTCSR can be used to manage IP interrupts. See the Board Support Package for examples of how to support HOST interrupts.

4. RESET SIGNALS

The **CPCI-4SIP** can be reset from two different sources:

- At power on or when the PCI RESET is asserted, the watchdog timer will hold the IP reset lines low for 200 ms.
- The AMCC has a bit called SYSRST that the HOST can toggle to reset the IP's. Software should hold the RESET asserted for 200 mS to meet the IP specifications.

5. JUMPER DESCRIPTIONS

JUMPER	FACTORY SETTING	DESCRIPTION
W1	None	IP_A IPSTROBE 1 & 2 Strobe In - 2 & 3 Strobe Out
W2	None	IP_B IPSTROBE 1 & 2 Strobe In - 2 & 3 Strobe Out
W3	None	IP_C IPSTROBE 1 & 2 Strobe In - 2 & 3 Strobe Out
W4	None	IP_D IPSTROBE 1 & 2 Strobe In - 2 & 3 Strobe Out
W5	2 & 3	IPCLK- AB (8Mhz Factory) 1 & 2 (32 MHz)
W6	2 & 3	IPCLK-CD (8Mhz Factory) 1 & 2 (32 MHz)
W7	None	PCI RESET
W8	1 & 2 – 3 & 4	Disable 32BIT Access. (16BIT ACCESS Factory)

Table 5.1 Jumper Descriptions

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6. LED INDICATORS

There are Six LED indicators visible at the CPCI card bracket. They are marked with a legend on the bracket, and they are labeled on the PCB as L1 – L3 where L1 is at the top of the card.

The LED's have the following meanings:

LED	LEGEND	Meaning
L1	Lower Upper	PCI Accessing IP- D PCI Accessing IP- C
L2	Lower Upper	PCI HOST Reading From IP. PCI HOST Wrinting To IP.
L3	Lower Upper	PCI Accessing IP- B PCI Accessing IP- A

Table 6.1 LED Descriptions

7. CONNECTIONS

7.1 IP I/O CONNECTORS (P1, P2, P4, P5)

Connector	I/O for
P11 & P13	IP_A
P12 & P14	IP_B
P9 & P10	IP_C
P7 & P8	IP_D

50 pin subminiature D shelled connectors are used to route all the IP I/O signals off the card. ALPHI Technology can supply transition modules and cable assemblies to meet any special requirements. Contact the factory for additional information.

Connectors are manufactured by AMP and the style is CHAMP.

Use	Model
On PC Board	787096-1
Suggested Plug	787131-1
Suggested Shell	787133-2

Table 7.1: I/O Connector Model Numbers

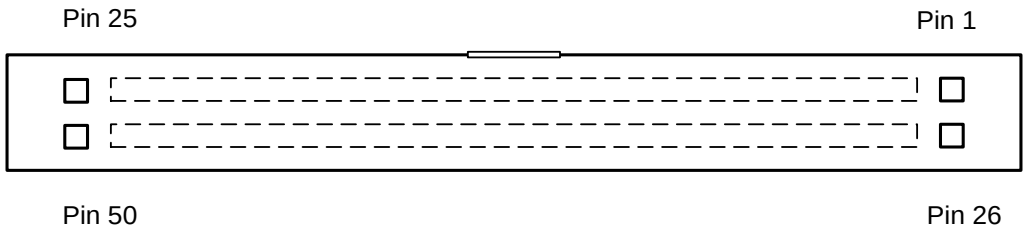


Figure 7.1: IP I/O CONNECTORS

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The I/O signals for the four IP's are directly routed off the card through the front panel.

7.2 REAR I/O JUMPER BLOCK

This jumper block is used to route IP, I/O to the rear panel.

IP I/O Line	Header and Pin	Header and Pin	Backplane and Pin
IP_A:1	H20:19	H20:20	J4:11
IP_A:2	H19:19	H19:20	J4:36
IP_A:3	H18:19	H18:20	J4:61
IP_A:4	H17:19	H17:20	J4:86
IP_A:5	H16:19	H16:20	J4:111
IP_A:6	H20:17	H20:18	J4:10
IP_A:7	H19:17	H19:18	J4:35
IP_A:8	H18:17	H18:18	J4:60
IP_A:9	H17:17	H17:18	J4:85
IP_A:10	H16:17	H16:18	J4:110
IP_A:11	H20:15	H20:16	J4:9
IP_A:12	H19:15	H19:16	J4:34
IP_A:13	H18:15	H18:16	J4:59
IP_A:14	H17:15	H17:16	J4:84
IP_A:15	H16:15	H16:16	J4:109
IP_A:16	H20:13	H20:14	J4:8
IP_A:17	H19:13	H19:14	J4:33
IP_A:18	H18:13	H18:14	J4:58
IP_A:19	H17:13	H17:14	J4:83
IP_A:20	H16:13	H16:14	J4:108
IP_A:21	H20:11	H20:12	J4:7
IP_A:22	H19:11	H19:12	J4:32
IP_A:23	H18:11	H18:12	J4:57
IP_A:24	H17:11	H17:12	J4:82
IP_A:25	H16:11	H16:12	J4:107
IP_A:26	H20:9	H20:10	J4:6
IP_A:27	H19:9	H19:10	J4:31
IP_A:28	H18:9	H18:10	J4:56
IP_A:29	H17:9	H17:10	J4:81
IP_A:30	H16:9	H16:10	J4:106
IP_A:31	H20:7	H20:8	J4:5
IP_A:32	H19:7	H19:8	J4:30
IP_A:33	H18:7	H18:8	J4:55
IP_A:34	H17:7	H17:8	J4:80
IP_A:35	H16:7	H16:8	J4:105
IP_A:36	H20:5	H20:6	J4:4
IP_A:37	H19:5	H19:6	J4:29
IP_A:38	H18:5	H18:6	J4:54
IP_A:39	H17:5	H17:6	J4:79
IP_A:40	H16:5	H16:6	J4:104
IP_A:41	H20:3	H20:4	J4:3
IP_A:42	H19:3	H19:4	J4:28
IP_A:43	H18:3	H18:4	J4:53
IP_A:44	H17:3	H17:4	J4:78
IP_A:45	H16:3	H16:4	J4:103
IP_A:46	H20:1	H20:2	J4:2
IP_A:47	H19:1	H19:2	J4:27
IP_A:48	H18:1	H18:2	J4:52
IP_A:49	H17:1	H17:2	J4:77

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IP_A:50	H16:1	H16:2	J4:102

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IP I/O Line	Header and Pin	Header and Pin	Backplane and Pin
IP_B:1	H15:19	H15:20	J4:25
IP_B:2	H14:19	H14:20	J4:50
IP_B:3	H13:19	H13:20	J4:75
IP_B:4	H12:19	H12:20	J4:100
IP_B:5	H11:19	H11:20	J4:125
IP_B:6	H15:17	H15:18	J4:24
IP_B:7	H14:17	H14:18	J4:49
IP_B:8	H13:17	H13:18	J4:74
IP_B:9	H12:17	H12:18	J4:99
IP_B:10	H11:17	H11:18	J4:124
IP_B:11	H15:15	H15:16	J4:23
IP_B:12	H14:15	H14:16	J4:48
IP_B:13	H13:15	H13:16	J4:73
IP_B:14	H12:15	H12:16	J4:98
IP_B:15	H11:15	H11:16	J4:123
IP_B:16	H15:13	H15:14	J4:22
IP_B:17	H14:13	H14:14	J4:47
IP_B:18	H13:13	H13:14	J4:72
IP_B:19	H12:13	H12:14	J4:97
IP_B:20	H11:13	H11:14	J4:122
IP_B:21	H15:11	H15:12	J4:21
IP_B:22	H14:11	H14:12	J4:46
IP_B:23	H13:11	H13:12	J4:71
IP_B:24	H12:11	H12:12	J4:96
IP_B:25	H11:11	H11:12	J4:121
IP_B:26	H15:9	H15:10	J4:20
IP_B:27	H14:9	H14:10	J4:45
IP_B:28	H13:9	H13:10	J4:70
IP_B:29	H12:9	H12:10	J4:95
IP_B:30	H11:9	H11:10	J4:120
IP_B:31	H15:7	H15:8	J4:19
IP_B:32	H14:7	H14:8	J4:44
IP_B:33	H13:7	H13:8	J4:69
IP_B:34	H12:7	H12:8	J4:94
IP_B:35	H11:7	H11:8	J4:119
IP_B:36	H15:5	H15:6	J4:18
IP_B:37	H14:5	H14:6	J4:43
IP_B:38	H13:5	H13:6	J4:68
IP_B:39	H12:5	H12:6	J4:93
IP_B:40	H11:5	H11:6	J4:118
IP_B:41	H15:3	H15:4	J4:17
IP_B:42	H14:3	H14:4	J4:42
IP_B:43	H13:3	H13:4	J4:67
IP_B:44	H12:3	H12:4	J4:92
IP_B:45	H11:3	H11:4	J4:117
IP_B:46	H15:1	H15:2	J4:16
IP_B:47	H14:1	H14:2	J4:41
IP_B:48	H13:1	H13:2	J4:66
IP_B:49	H12:1	H12:2	J4:91
IP_B:50	H11:1	H11:2	J4:116

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IP I/O Line	Header and Pin	Header and Pin	Backplane and Pin
IP_C:1	H10:19	H10:20	J5:11
IP_C:2	H9:19	H9:20	J5:33
IP_C:3	H8:19	H8:20	J5:55
IP_C:4	H7:19	H7:20	J5:77
IP_C:5	H6:19	H6:20	J5:99
IP_C:6	H10:17	H10:18	J5:10
IP_C:7	H9:17	H9:18	J5:32
IP_C:8	H8:17	H8:18	J5:54
IP_C:9	H7:17	H7:18	J5:76
IP_C:10	H6:17	H6:18	J5:98
IP_C:11	H10:15	H10:16	J5:9
IP_C:12	H9:15	H9:16	J5:31
IP_C:13	H8:15	H8:16	J5:53
IP_C:14	H7:15	H7:16	J5:75
IP_C:15	H6:15	H6:16	J5:97
IP_C:16	H10:13	H10:14	J5:8
IP_C:17	H9:13	H9:14	J5:30
IP_C:18	H8:13	H8:14	J5:52
IP_C:19	H7:13	H7:14	J5:74
IP_C:20	H6:13	H6:14	J5:96
IP_C:21	H10:11	H10:12	J5:7
IP_C:22	H9:11	H9:12	J5:29
IP_C:23	H8:11	H8:12	J5:51
IP_C:24	H7:11	H7:12	J5:73
IP_C:25	H6:11	H6:12	J5:95
IP_C:26	H10:9	H10:10	J5:6
IP_C:27	H9:9	H9:10	J5:28
IP_C:28	H8:9	H8:10	J5:50
IP_C:29	H7:9	H7:10	J5:72
IP_C:30	H6:9	H6:10	J5:94
IP_C:31	H10:7	H10:8	J5:5
IP_C:32	H9:7	H9:8	J5:27
IP_C:33	H8:7	H8:8	J5:49
IP_C:34	H7:7	H7:8	J5:71
IP_C:35	H6:7	H6:8	J5:93
IP_C:36	H10:5	H10:6	J5:4
IP_C:37	H9:5	H9:6	J5:26
IP_C:38	H8:5	H8:6	J5:48
IP_C:39	H7:5	H7:6	J5:70
IP_C:40	H6:5	H6:6	J5:92
IP_C:41	H10:3	H10:4	J5:3
IP_C:42	H9:3	H9:4	J5:25
IP_C:43	H8:3	H8:4	J5:47
IP_C:44	H7:3	H7:4	J5:69
IP_C:45	H6:3	H6:4	J5:91
IP_C:46	H10:1	H10:2	J5:2
IP_C:47	H9:1	H9:2	J5:24
IP_C:48	H8:1	H8:2	J5:46
IP_C:49	H7:1	H7:2	J5:68
IP_C:50	H6:1	H6:2	J5:90

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IP I/O Line	Header and Pin	Header and Pin	Backplane and Pin
IP_D:1	H5:19	H5:20	J5:22
IP_D:2	H4:19	H4:20	J5:44
IP_D:3	H3:19	H3:20	J5:66
IP_D:4	H2:19	H2:20	J5:88
IP_D:5	H1:19	H1:20	J5:110
IP_D:6	H5:17	H5:18	J5:21
IP_D:7	H4:17	H4:18	J5:43
IP_D:8	H3:17	H3:18	J5:65
IP_D:9	H2:17	H2:18	J5:87
IP_D:10	H1:17	H1:18	J5:109
IP_D:11	H5:15	H5:16	J5:20
IP_D:12	H4:15	H4:16	J5:42
IP_D:13	H3:15	H3:16	J5:64
IP_D:14	H2:15	H2:16	J5:86
IP_D:15	H1:15	H1:16	J5:108
IP_D:16	H5:13	H5:14	J5:19
IP_D:17	H4:13	H4:14	J5:41
IP_D:18	H3:13	H3:14	J5:63
IP_D:19	H2:13	H2:14	J5:85
IP_D:20	H1:13	H1:14	J5:107
IP_D:21	H5:11	H5:12	J5:18
IP_D:22	H4:11	H4:12	J5:40
IP_D:23	H3:11	H3:12	J5:62
IP_D:24	H2:11	H2:12	J5:84
IP_D:25	H1:11	H1:12	J5:106
IP_D:26	H5:9	H5:10	J5:17
IP_D:27	H4:9	H4:10	J5:39
IP_D:28	H3:9	H3:10	J5:61
IP_D:29	H2:9	H2:10	J5:83
IP_D:30	H1:9	H1:10	J5:105
IP_D:31	H5:7	H5:8	J5:16
IP_D:32	H4:7	H4:8	J5:38
IP_D:33	H3:7	H3:8	J5:60
IP_D:34	H2:7	H2:8	J5:82
IP_D:35	H1:7	H1:8	J5:104
IP_D:36	H5:5	H5:6	J5:15
IP_D:37	H4:5	H4:6	J5:37
IP_D:38	H3:5	H3:6	J5:59
IP_D:39	H2:5	H2:6	J5:81
IP_D:40	H1:5	H1:6	J5:103
IP_D:41	H5:3	H5:4	J5:14
IP_D:42	H4:3	H4:4	J5:36
IP_D:43	H3:3	H3:4	J5:58
IP_D:44	H2:3	H2:4	J5:80
IP_D:45	H1:3	H1:4	J5:102
IP_D:46	H5:1	H5:2	J5:13
IP_D:47	H4:1	H4:2	J5:35
IP_D:48	H3:1	H3:2	J5:57
IP_D:49	H2:1	H2:2	J5:79
IP_D:50	H1:1	H1:2	J5:101

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7.3 32 BIT CPCI BUS (P1)

This connector plugs into the backplane and provides the standard CPCI signals for all CPCI systems.

7.4 IPSTROPE (P3)

If the IP used support Strobe, the External Trigger P3 can be used to trigger each IP

Separately, or select individual IP trigger using the W1 – W4 jumpers.

Each IP can Receive or Sent Trigger.

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