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PMC-1553B-PLX

MIL-STD-1553
SuMMIT™
PMC Module

REFERENCE MANUAL

Revision 1.8
June 2012

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UPDATES HISTORY:

REV 1.0	**RELEASE**		**MARCH, 2007**
REV 1.1	**MEMORY MAP**	**PAGE 5,6**	**AUGUST, 2007**
REV 1.2	**UPDATE JUMPER SETTING**	**PAGE 12**	**SEPTEMBER, 2007**
REV 1.3	**CORRECT PINOUT**	**PAGE 17**	**SEPTEMBER, 2007**
REV 1.4	**SRAM SPACE CORRECTION**	**PAGE 10**	**SEPTEMBER, 2007**
REV 1.5	**CORRECT TABLE 9,14**	**PAGE 13**	**SEPTEMBER, 2007**
REV 1.6	**CORRECT TABLE 2**	**PAGE 5**	**MARCH, 2008**
REV 1.7	**ADD REGISTER $46**	**PAGE 9**	**APRIL, 2011**
REV 1.8	**CORRECT REAR I/O PINS,**	**PAGE 16**	**JUNE, 2012**

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1 GENERAL DESCRIPTION

2 INTRODUCTION

The PMC-1553B-PLX module provides Bus Controller (BC), Remote Terminal (RT) and Bus Monitor (BM) dual-redundant operations on the MIL-STD-1553 bus. The PMC form-factor provides easy installation.

The ***PMC-1553B-PLX*** is installed with the following resources:

- One or 2 UTMC SuMMIT™ 1553 based processor unit
- One Channel Dual Redundant or 2 Channels Dual Redundant
- 64K x 16 bit dual ported SRAM
- Bus Controller, Remote Terminal and Bus Monitor mode
- RT address and operational modes are program or jumper selectable
- 1553 bus long or short stub jumper option with onboard transformers
- PMC VIO 5V/3.3V signaling

2.1 FUNCTIONAL DESCRIPTION

A functional block diagram of the PMC module is depicted below in Figure 1.
The PMC-1553B-PLX is designed around the UTMC SuMMIT™ CHIP, that can performs the 1553 bus operations without interaction with the host CPU once the UT1553B SuMMIT™ has been programmed.

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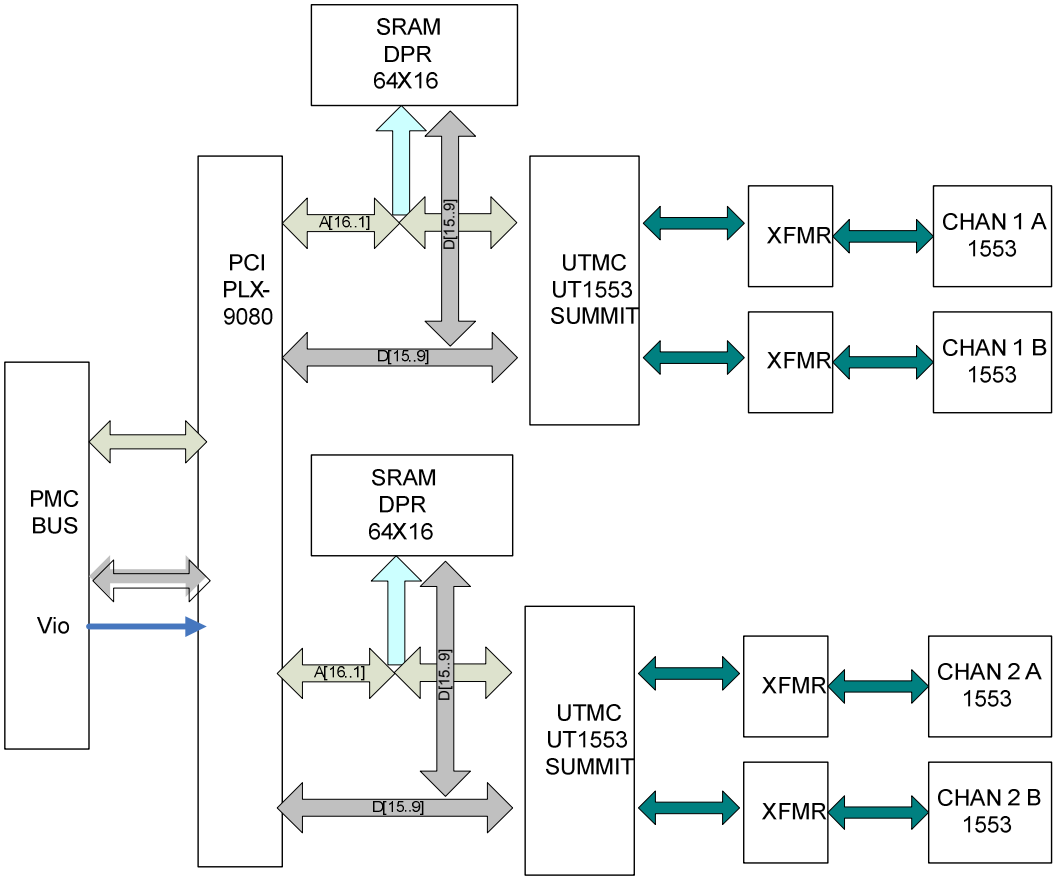


Figure 1: PMC-1553B-PLX Block Diagram with 2 Channels option

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2.2 REFERENCE MATERIALS LIST

The reader should refer to the UTMC Webb site for the complete BCRTM registers.

Manual and Data Sheet:
http://www.utmc.com/ProductPages/AE_SuMMIT2.cfm

WWW Home Page:
http://www.utmc.com/

Technical Questions - Please Contact info-ams@aeroflex.com

The reader should refer to the PMC Local Bus Specification for a detailed explanation of the PMC bus architecture and timing requirements. This specification is available from the following source:

PMC Special Interest Group
PO Box 14070
Portland, OR 97214
Tel: (800) 433-5177
Tel: (503) 797-4207
Fax: (503) 234-6762

The reader is also referred to the PLX-9080 PMC Controller data book:

PLX TECHNOLOGY
6195 Lusk Boulevard
San Diego, CA 92121-2793
Tel: (800) 755-2622

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3 HOST (PMC) SIDE

3.1 Interface to HOST (PMC)

All PMC devices contain a set of registers in Configuration Space to allow determining the manufacturer and model of the device, determining the resources necessary for the correct operation of the device, and other configuration information. Configuration space is decoded on a per slot / device basis via a mechanism described in the PMC specification.

All PMC devices can be relocated in physical memory by means of several Base Address Registers. These registers contain the high address bits, which must be matched for any access to the card to be successful. Part of the protocol of programming the Base Address Registers allows for the transfer of information regarding the size of the regions. The actual Base Address Registers are located in Configuration Space.

Normally, configuring the card is performed by the system controller and some form of firmware or BIOS. Unfortunately, determining Base Addresses and other configuration information in Configuration Space is operating system dependent. One of the primary functions of the device driver under Windows NT is to map these resources to the user application. The card is actually accessed through the decoded base address registers.

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3.2 PMC Configuration Space

PMC Address: *CONFIG:0x00 – 0x3C*
Mode of Access: *Read/Write*
Reset By *PMC Hardware Reset*

The card has the following registers available to PMC Configuration Space. They are implemented in the PLX chip. The registers are also accessible from the DSP Local bus.

Offset Into PMC CFG	31 – 24	23 – 16	15 – 8	7 – 0
0x00	Device ID		Vendor ID	
0x04	Status		Command	
0x08	Class Code			Revision ID
0x0C	BIST	Header Type	PMC Latency Timer	Cache Line Size
0x10	PMC Base Address 0 (Memory Access to PLX Registers)			
0x14	PMC Base Address 1 (I/O Access to PLX Registers)			
0x18	PMC Base Address 2 (Memory Access to DSP SRAM and card registers)			
0x1C	PMC Base Address 3 (Not Used for this card)			
0x20	Unused PMC Base Address 4			
0x24	Unused PMC Base Address 5			
0x28	Cardbus CIS Pointer (Not Supported)			
0x2C	Subsystem ID		Subsystem Vendor ID	
0x30	PMC Base Address for Expansion ROM			
0x34	Reserved			
0x38	Reserved			
0x3C	Max Latency	Min Grant	Interrupt Pin	Interrupt Line
0x80	RT Jumper status- READ ONLY			
0x82	Int. Status- READ ONLY			

Table 1 PMC Configuration Space

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The card presents the following initial configuration values to the PMC system, based on the values stored in the NVRAM device read by the PLX PMC9080 interface chip.

Register	Value (Meaning)
Vendor ID	0x13C5 (ALPHI Technology)
Device ID	0x0314 (PMC-1553B-PLX-1) Single Channel 0x0315 (PMC-1553B-PLX-2) Dual Channel
Revision ID	0x00
Class Code	0xff0000 (Device does not fit into defined class codes)
Interrupt Line	0xff
Interrupt Pin	A
Multifunction Device	No
Build In Self Test	No
Latency Timer	0
Minimum Grant	0
Maximum Latency	0
Base Address 0 Size	256 Bytes Allocated
Base Address 1 Size	256 Bytes Allocated
Base Address 2 Size	128 Bytes Allocated Single Channel PMC-1553B-PLX-1 256 Bytes Allocated Dual Channel PMC-1553B-PLX-2
Base Address 3 Size	128 Kbytes Allocated Single Channel PMC-1553B-PLX-1 256 Kbytes Allocated Dual Channel PMC-1553B-PLX-2
Expansion ROM Size	None

Table 2 PMC-1553B-PLX Configuration Register Default Values

3.3 PMC Base Address Regions

HOST Address	WIDTH USED	Description	TYPE
BAR0	64 bytes 0x00– 0x3f	PLX Operation Registers	MEM
BAR1	256 bytes	NOT USED	I/O
BAR2	512 bytes 0x00– 0x1ff	Ch 1-2 SuMMIT™ I/O Space 16 bit wide	MEM
BAR3	256 Kbytes 0x00– 0x3ffff	Ch 1-2 SuMMIT™ DUAL PORTED SRAM 16 bit wide	MEM

Table 3 PMC-1553B-PLX

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4 INTERNAL ORGANIZATION

The ***PMC-1553B-PLX*** allows host access to the:

- SuMMIT™ Registers
- Dual Port SRAM
- Status register

4.1 SuMMIT™ Registers

4.1.1 Local status register #0: $40-$42

The local register is used to determine the status of ***PMC-1553B-PLX*** jumper settings. The Status Register provides the following status bits:

7	6	5	4	3	2	1	0
READYB#	GND	MSEL1 Ch2	MSEL0 Ch2	READYA#	GND	MSEL1 Ch1	MSEL0 Ch1

Mode select 0, in conjunction with Mode select 1, determines the SuMMIT™ mode of operation. The table below describes these modes.

MSEL1	MSEL0	Mode Of Operation
0	0	Bus controller = SBC
0	1	Remote Terminal = SRT
1	0	Monitor Terminal = SMT
1	1	SMT/SRT

Table 4 MODE OF OPERATION

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4.1.2 Local status register #1: $44

This register is used to determine the status of the ***PMC-1553B-PLX*** jumper settings for board Jumpers. The Status Register provides the following status bits where Bit 0-7 gives the status for Ch1 and Bit 8-15 status Ch2

J9, 10 RT Jumper Status Register $44

15	14	13	12	11	10	9	8
Ch2LOCK	Ch2ABSTB	Ch2RTPT	Ch2RTA4	Ch2RTA3	Ch2RTA2	Ch2RTA1	Ch2RTA0

7	6	5	4	3	2	1	0
Ch1LOCK	Ch1ABSTB	Ch1RTPT	Ch1RTA4	Ch1RTA3	Ch1RTA2	Ch1RTA1	Ch1RTA0

Bit	Name	Function
0	Ch1RTA0	RT Address Bit 0 Ch 1
1	Ch1RTA1	RT Address Bit 1Ch 1
2	Ch1RTA2	RT Address Bit 2 Ch 1
3	Ch1RTA3	RT Address Bit 3 Ch 1
4	Ch1RTA4	RT Address Bit 4 Ch 1
5	Ch1RTPT	RT Address Parity
6	Ch1ABSTB	SuMMIT™ 1553A or 1553B Select
7	LOCK1	Status of the Lock input Pin
8	Ch2RTA0	RT Address Bit 0 Ch 2
9	Ch2RTA1	RT Address Bit 1Ch 2
10	Ch2RTA2	RT Address Bit 2 Ch 2
11	Ch2RTA3	RT Address Bit 3 Ch 2
12	Ch2RTA4	RT Address Bit 4 Ch 2
13	Ch2RTPT	RT Address Parity
14	Ch2ABSTB	SuMMIT™ 1553A or 1553B Select
15	LOCK2	Status of the Lock input Pin

Table 5 Bit Description

LOCK

This read only bit reflects the inverted state of the LOCK input pin. The LOCK pin is latched on the rising edge of MRST. If the mode of operation must change, the user must perform a MRST.

4.1.3 Interrupt Local status register: $46

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This local register is used to determine which Summit interrupted on IntA.
The Status Register provides the following status bits:

7	6	5	4	3	2	1	0
-	-	-	-	Ch2 **MSG**	Ch2 **YF**	Ch1 **MSG**	Ch1 **YF**

Each SuMMIT™ has two (2) interrupt lines. MSG and YF
These interrupts requests are connected to an 'or' structure, the output of the 'or' is latched and sent to the PLX9080's **LINTI#** pin.

When an interrupt is received, this Local register will allow the user to find out which Summit has Interrupted the bus without checking each Summit separate to determine which channel to serve.

Because the SuMMIT™ is only sending a pulse, the interrupt are memorized by a latch to maintain the LINTI pin low for the PLX9080.

The Host needs to toggle bit #16 of the PLX Configuration register (0x6c) to remove the interrupt.

This bit corresponds to the PLX USERO output.

The bit #16 is high upon reset and needs to be pulsed low to remove the latched LINTI# signal.

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4.1.4 SuMMIT™ REGISTER SPACE

NAME	OFFSET	DATA	R/W	COMMENTS
SuMMIT™ REGISTERS 1	$00-$3F	D00-D15	R/W	SuMMIT™ Registers
Local REGISTERS	$40-$7F	D00-D15	R	Status Registers
SuMMIT™ REGISTERS 2	$80-$FF	D00-D15	R/W	SuMMIT™ Registers

4.1.5 REMOTE TERMINAL REGISTERS

Register Number	Name	Register Offset
0	Control Register	$00
1	Operational Status Register	$02
2	Current Command Register	$04
3	Interrupt Mask Register	$06
4	Pending Interrupt Register	$08
5	Interrupt Log List Pointer Register	$0A
6	BIT Word Register	$0C
7	Time-Tag Register	$0E
8	Remote Terminal Descriptor Pointer Register	$10
9	Status Word Bits Register	$12
10-15	Not Applicable	$14-$1E
16-31	Illegalization Registers	$20- $3E

Table 6 REMOTE TERMINAL REGISTERS

4.1.6 BUS CONTROLLER REGISTERS

Register Number	Name	Register Offset
0	Control Register	$00
1	Operational Status Register	$02
2	Current Command Block Register	$04
3	Interrupt Mask Register	$06
4	Pending Interrupt Register	$08
5	Interrupt Log List Pointer Register	$0A
6	BIT Word Register	$0C

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7	Minor-Frame Timer	$0E
8	Command Block Pointer Register	$10
9	Not Applicable	$12
10	BC Command Block Initialization Count Register	$14
11-31	Not Applicable	$16- $3E

Table 7 BUS CONTROLLER REGISTERS

4.1.7 MONITOR TERMINAL REGISTERS

Register Number	Name	Register Offset
0	Control Register	$00
1	Operational Status Register	$02
2	Current Command Block Register	$04
3	Interrupt Mask Register	$06
4	Pending Interrupt Register	$08
5	Interrupt Log List Pointer Register	$0A
6	BIT Word Register	$0C
7	Time-Tag Register	$0E
8-10	Not Applicable	$10-$14
11	Initial Monitor Command Block Pointer Register	$16
12	Initial Monitor Data Pointer Register	$18
13	Monitor Block Counter Register	$1A
14	Monitor Filter Register	$1C
15	Monitor Filter Register	$1E
16-31	Not Applicable	$20- $3E

Table 8 MONITOR TERMINAL REGISTERS

4.2 Shared Static RAM

NAME	OFFSET	DATA	R/W	COMMENTS
MEM SPACE1	$0 - $1FFFF	D00-D15	R/W	Shared / Static RAM 64K x 16-bit (128Kbytes)
MEM SPACE2	$20000 - $3FFFF	D00-D15	R/W	Shared / Static RAM 64K x 16-bit (128Kbytes)

The ***PMC-1553B-PLX*** has a 64K x 16-bit Shared Memory for each channel. The base address of the SRAM is provided by the PMC host controller. A local Flash E^2prom defines the resources needed by the PMC-1553 module. SRAM accesses are only made in 16-bit mode. The on-board logic does the arbitration between the SuMMIT™ and the PMC. SuMMIT™ access to the SRAM takes priority over any pending host access. Therefore, the host access will be held off until the SuMMIT™ access completes.

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5 Board layout

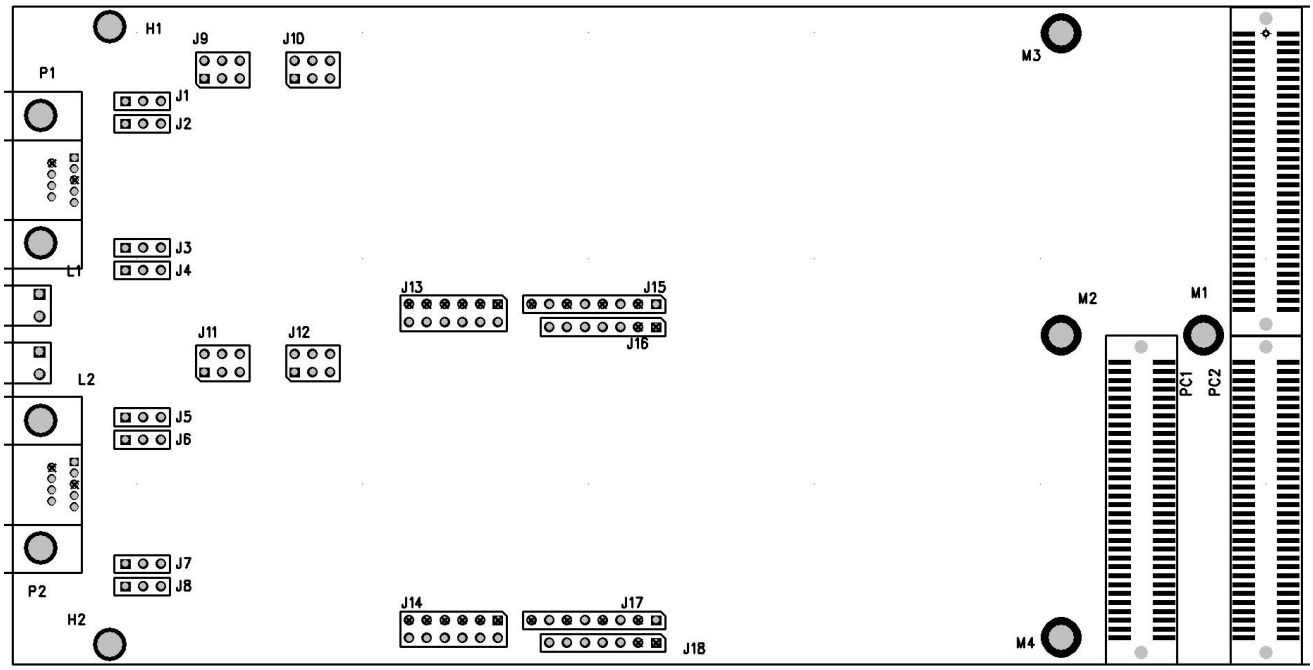


Figure 2: JUMPER LOCATION DIAGRAM

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6 Jumper Description

Channel 1 Configuration:

JUMPER	FACTORY SETTING	DESCRIPTION
J4	2-3	Long Stub/Short Stub Output channel 1A - (Short Stub)
J3	1-2	Long Stub/Short Stub Output channel 1A + (Short Stub)
J2	2-3	Long Stub/Short Stub Output channel 1B - (Short Stub)
J1	1-2	Long Stub/Short Stub Output channel 1B + (Short Stub)
J13	None	1553 bus RT address and parity selection
J15	None	Mode Select (1553A,NO LOCK,BC)
J10	None	Route to Rear I/O Ch 1A
J9	None	Route to Rear I/O Ch 1B

Table 9: Channel #1 Jumper Configuration

Signal	Jumper set	Description
A/B* STD	1-2	Military standard Mil_STD_1553A or Mil_STD_1553B
LOCK	3-4	This Pin when set active prevent Software change to both the RT address, A/B* STD and Mode select
MSEL1	5-6	See Mode of Operation Table above
MSEL0	7-8	See Mode of Operation Table above

Table 10: J15 Mode of Operation Jumper Selection

Signal	Jumper set	Description
RTPT	1-2	RT Address Parity
RTA4	3-4	RT Address Bit 4
RTA3	5-6	RT Address Bit 3
RTA2	7-8	RT Address Bit 2
RTA1	9-10	RT Address Bit 1
RTA0	11-12	RT Address Bit 0

Table 11: J13 RT address and parity selection

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Signal	Jumper set	Description
Ch 1A+	1-2	Routing Ch 1A+ to rear I/O pin 63
Ch 1A-	3-4	Routing Ch 1A- to rear I/O pin 61
GND Ch1A	5-6	Routing Ground Ch A to rear I/O Pin 59

Table 12: J10 Routing Connection

Signal	Jumper set	Description
Ch 1B+	1-2	Routing Ch 1B+ to rear I/O pin 57
Ch 1B-	3-4	Routing Ch 1B- to rear I/O pin 55
GND Ch1B	5-6	Routing Ground Ch B to rear I/O Pin 53

Table 13: J9 Routing Connection

Channel 2 Configuration:

JUMPER	FACTORY SETTING	DESCRIPTION
J8	2-3	Long Stub/Short Stub Output channel 2A - (Short Stub)
J7	1-2	Long Stub/Short Stub Output channel 2A + (Short Stub)
J5	2-3	Long Stub/Short Stub Output channel 2B - (Short Stub)
J6	1-2	Long Stub/Short Stub Output channel 2B + (Short Stub)
J14	None	Ch 2 1553 bus RT address and parity selection
J17	None	Ch 2 Mode Select (1553A,NO LOCK,BC)
J12	None	Route to Rear I/O Ch 2A
J11	None	Route to Rear I/O Ch 2B

Table 14: Channel #2 Jumper Configuration

Signal	Jumper set	Description
A/B* STD	1-2	Military standard Mil_STD_1553A or Mil_STD_1553B
LOCK	3-4	This Pin when set active prevent Software change to both the RT address, A/B* STD and Mode select
MSEL1	5-6	See Mode of Operation Table above
MSEL0	7-8	See Mode of Operation Table above

Table 15: J17 Mode of Operation Jumper Selection

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Signal	Jumper set	Description
RTPT	1-2	RT Address Parity
RTA4	3-4	RT Address Bit 4
RTA3	5-6	RT Address Bit 3
RTA2	7-8	RT Address Bit 2
RTA1	9-10	RT Address Bit 1
RTA0	11-12	RT Address Bit 0

Table 16: J14 RT address and parity selection

Signal	Jumper set	Description
Ch 2A+	1-2	Routing Ch 2A+ to rear I/O pin 49
Ch 2A-	3-4	Routing Ch 2A- to rear I/O pin 47
GND Ch2A	5-6	Routing Ground Ch A to rear I/O Pin 45

Table 17: J12 Routing Connection

Signal	Jumper set	Description
Ch 2B+	1-2	Routing Ch 2B+ to rear I/O pin 43
Ch 2B-	3-4	Routing Ch 2B- to rear I/O pin 41
GND Ch2B	5-6	Routing Ground Ch B to rear I/O Pin 39

Table 18: J11 Routing Connection

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7 Rear I/O Connections

Pin	Signal	Pin	Description
1	NC	2	NC
3	NC	4	NC
5	NC	6	NC
7	NC	8	NC
9	NC	10	NC
11	NC	12	NC
13	NC	14	NC
15	NC	16	NC
17	NC	18	NC
19	NC	20	NC
21	NC	22	NC
23	NC	24	NC
25	NC	26	NC
27	NC	28	NC
29	NC	30	NC
31	NC	32	NC
33	TAG_CLKB_IN	34	1MHZ CLK_B_OUT
35	GND	36	GND
37	TAG_CLKA_IN	38	1MHZ CLK_A_OUT
39	GND CH 2B	40	NC
41	CH 2 B-	42	NC
43	CH 2 B+	44	NC
45	GND CH 2A	46	NC
47	CH 2 A-	48	NC
49	CH 2 A+	50	NC
51	NC	52	NC
53	GND CH 1B	54	NC
55	CH 1 B-	56	NC
57	CH 1 B+	58	NC
59	GND CH 1A	60	NC
61	CH 1 A-	62	NC
63	CH 1 A+	64	NC

Table 19: PC4 I/O Connector

NC: No Connect
Ch1 A/B +/- : Channel 1 A and B on 1553 +/-
Ch2 A/B +/- : Channel 2 A and B on 1553 +/-
TAG_CLKx_IN: External Input for Tag Clock Ch 1 and Ch2
1MHZ CLK_A_OUT : Output 1 MHZ Clock

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8 Front Panel I/O Connections

2 Micro-DSub are used for the front panel access for Ch 1 and 2

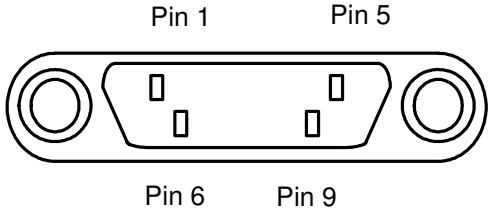


Table 20: 9 Pin I/O Connector

Pin	Signal
1	CH 1 B+
2	CH 1 B -
3	GND CH 1B
4	CH 1 A+
5	CH 1 A -
6	GND CH 1A
7	GND
8	TAG_CLKA_IN
9	1MHZ CLK_A_OUT

Table 21: Front Panel I/O Connector Ch1

Pin	Signal
1	CH 2 B+
2	CH 2 B -
3	GND CH 2B
4	CH 2 A+
5	CH 1 A -
6	GND CH 2A
7	GND
8	TAG_CLKB_IN
9	1MHZ CLK_B_OUT

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Table 22: Front Panel I/O Connector Ch2

Connectors are manufactured by ITT Cannon.

Use	Model
On PC Board	MDSM-9PE-C10
Suggested Plug	MDSM-9SC-Z11-VS1
Contact	MDS-S-TS

CONNECTION HARDWARE FOR 1553 BUS

The following hardware is available from Alphi Technology.

ALPHI Technology stocks the above connectors and other cabling options.
We can also build complete cable assemblies to meet your requirements.

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Summary

- Engineering Kits
- Micro Dsub To Triax
- External CLK Input
- External CLK output
- 78 ohm Terminators
- T connectors
- Vita compliant

MIL-1553 ENGINEERING KITS: CABLES, T'S AND TERMINATORS



COMPLETE 1553 ENGINEERING KIT

Ordering Information

Part Number : **EngKit-1553-Micro**
1 Cable, 2 T's, 2 Terminators
Option : 1 Cable only

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